查询DCR760N70供应商

DCR760N85

Phase Control Thyristor
Preliminary Information

DS5856-1.0 MAY 2005 (LN23972)

FEATURES

- Double Side Cooling
- High Surge Capability

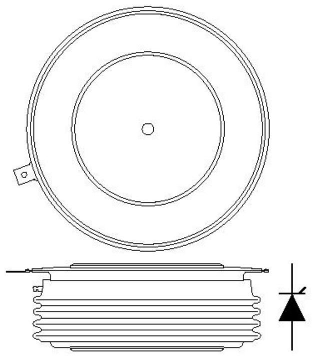
APPLICATIONS

- Medium Voltage Soft Starts
- High Voltage Power Supplies
- Static Switches

KEY PARAMETERS

V_{DRM}	**8500V**
$I_{T(AV)}$	**760A**
I_{TSM}	**12800A**
dV/dt*	**1500V/µs**
dI/dt	**200A/µs**

*** Higher dV/dt selections available**



Outline type code: N

(See Package Details for further information)

Fig. 1 Package outline

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR760N85 DCR760N80 DCR760N75 DCR760N70	8500 8000 7500 7000	T_{vj} = -40° C to 125° C, I_{DRM} = I_{RRM} = 200mA, V_{DRM}, V_{RRM} t_p = 10ms, V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR760N85

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS

T_{case} = 60° C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	760	A
$I_{T(RMS)}$	RMS value	-	1190	A
I_T	Continuous (direct) on-state current	-	1150	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125° C	12.8	kA
I^2t	I^2t for fusing	$V_R = 0$	0.82	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.0202	° C/W
		Single side cooled	Anode DC	-	0.0379	° C/W
			Cathode DC	-	0.0451	° C/W
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 23 kN	Double side	-	0.004	° C/W
		(with mounting compound)	Single side	-	0.008	° C/W
T_{vj}	Virtual junction temperature	On-state (conducting)		-	135	° C
		Reverse (blocking)		-	125	° C
T_{stg}	Storage temperature range			-55	125	° C
F_m	Clamping force			20.0	25.0	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125° C		-	200	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125° C, gate open		-	1500	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$ Gate source 30V, 10Ω, t_r < 0.5µs, T_j = 125° C	Repetitive 50Hz	-	100	A/µs
			Non-repetitive	-	200	A/µs
$V_{T(TO)}$	Threshold voltage – Low level	100A to 500A at T_{case} = 125° C		-	1.081	V
	Threshold voltage – High level	500A to 3000A at T_{case} = 125° C		-	1.243	V
r_T	On-state slope resistance – Low level	100A to 500A at T_{case} = 125° C		-	1.694	mΩ
	On-state slope resistance – High level	500A to 3000A at T_{case} = 125° C		-	1.342	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω t_r = 0.5µs, T_j = 25° C		TBD	TBD	µs
t_q	Turn-off time	T_j = 125° C, V_R = 200V, dI/dt = 1A/µs, dV_{DR}/dt = 20V/µs linear		1000	1600	µs
Q_S	Stored charge	I_T = 2000A, T_j = 125° C, dI/dt – 1A/µs, V_{Rpeak} = 60% V_{drm}, V_R = 40% V_{drm}		3400	5600	µC
I_L	Latching current	T_j = 25° C, V_D = 5V		TBD	TBD	mA
I_H	Holding current	T_j = 25° C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		TBD	TBD	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25° C	1.5	V
V_{GD}	Gate non-trigger voltage	At V_{DRM}, T_{case} = 125° C	TBD	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25° C	250	mA
I_{GD}	Gate non-trigger current	V_{DRM} = 5V, T_{case} = 25° C	TBD	mA

CURVES

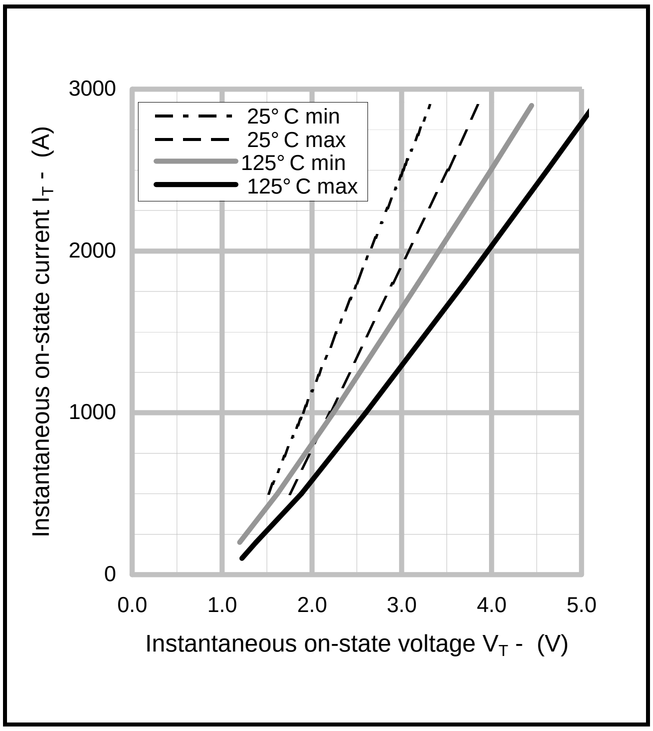


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$V_{TM} = A + B\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 0.882859
B = 0.020109
C = 0.001177
D = 0.012682

these values are valid for T_j = 125° C for I_T 100A to 3000A

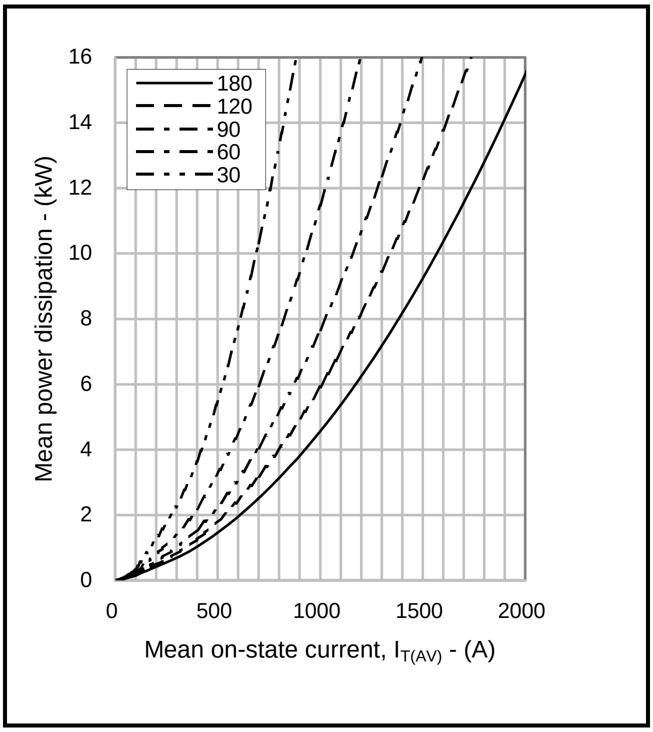


Fig.3 On-state power dissipation – sine wave

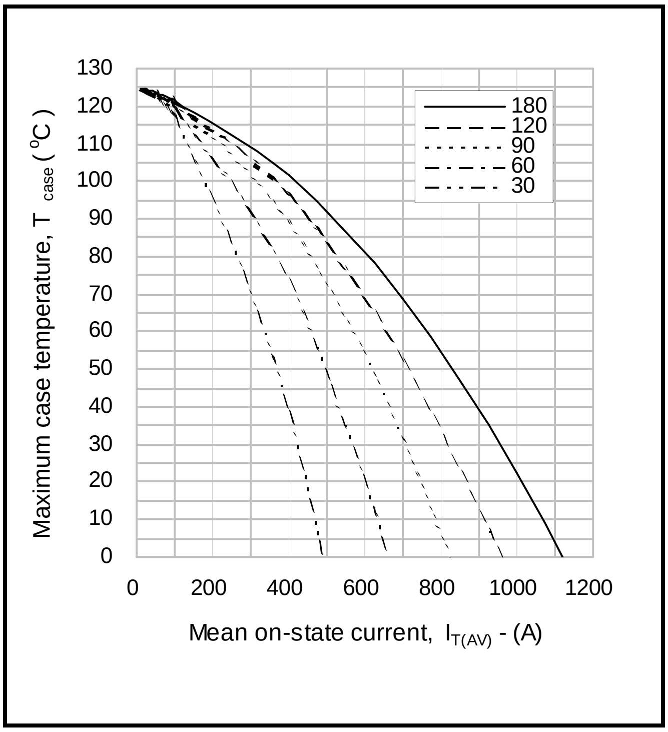


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

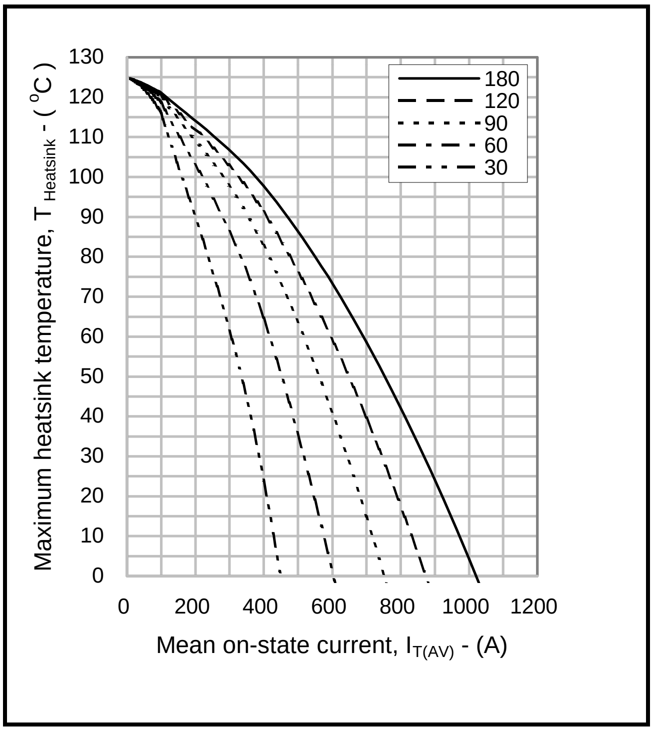


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

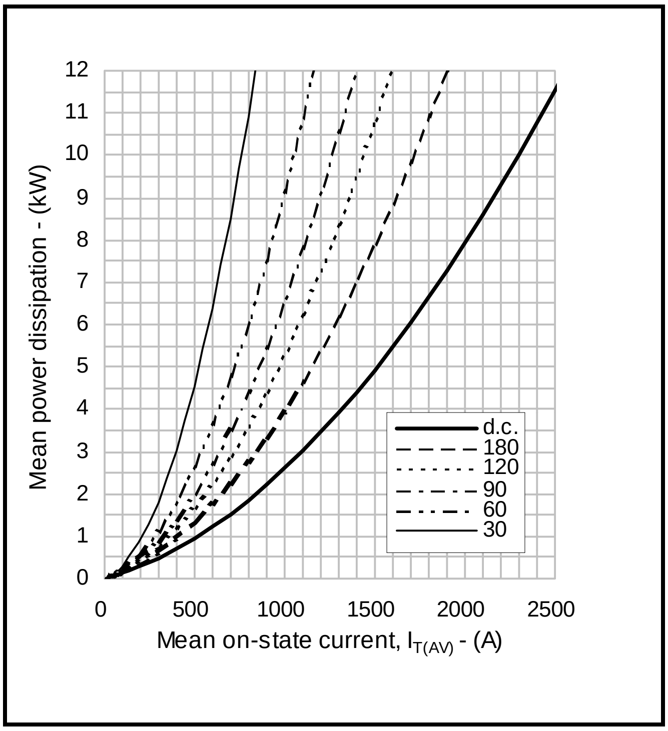


Fig.6 On-state power dissipation – rectangular wave

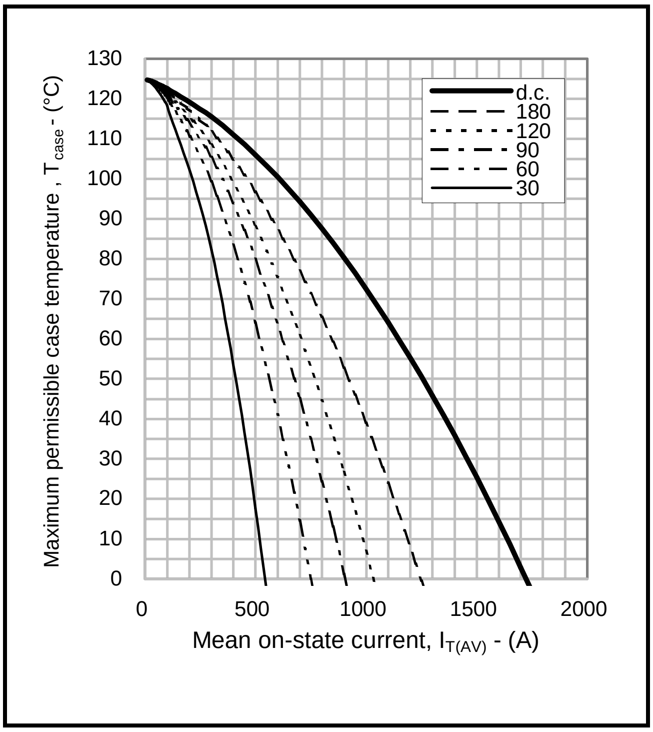


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

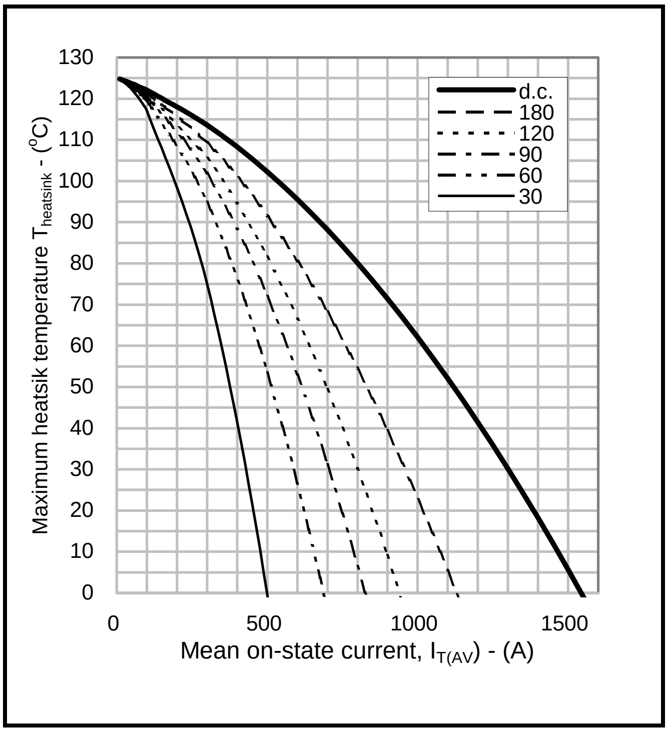
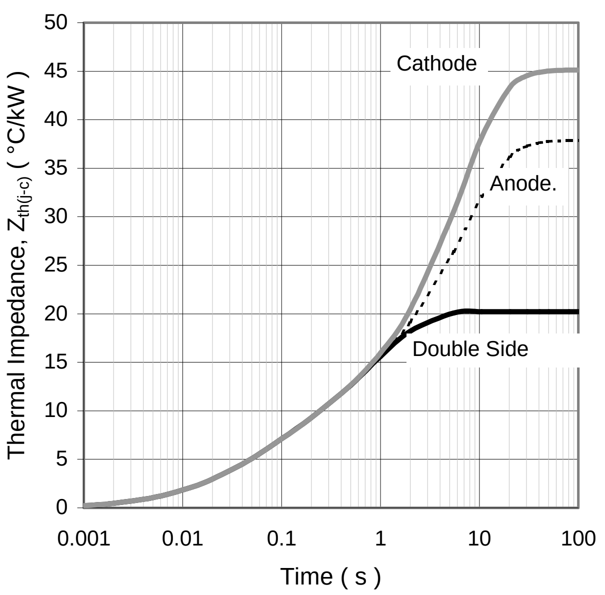


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R_i (° C/kW)	1.2849	4.988	5.5614	8.3856
	T_i (s)	0.009195	0.057825	0.43183	1.3814
Anode side cooled	R_i (° C/kW)	1.4937	5.1268	6.8498	24.2935
	T_i (s)	0.010286	0.064874	0.49207	7.2582
Cathode side cooled	R_i (° C/kW)	1.6042	5.285	5.0921	33.032
	T_i (s)	0.010861	0.069332	0.464312	6.671

$Z_{th} = \Sigma$ [R_i x (1-exp. (t/T_i))] **[1]**

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	2.25	1.53
120	2.60	2.19
90	2.98	2.55
60	3.32	2.94
30	3.59	3.37
15	3.71	3.60

Anode Side Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	2.23	1.52
120	2.57	2.16
90	2.94	2.52
60	3.27	2.90
30	3.53	3.32
15	3.65	3.53

Cathode Sided Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	2.22	1.52
120	2.56	2.15
90	2.92	2.51
60	3.25	2.88
30	3.50	3.29
15	3.62	3.51

Fig.9 Maximum (limit) transient thermal impedance – junction to case (° C/kW)

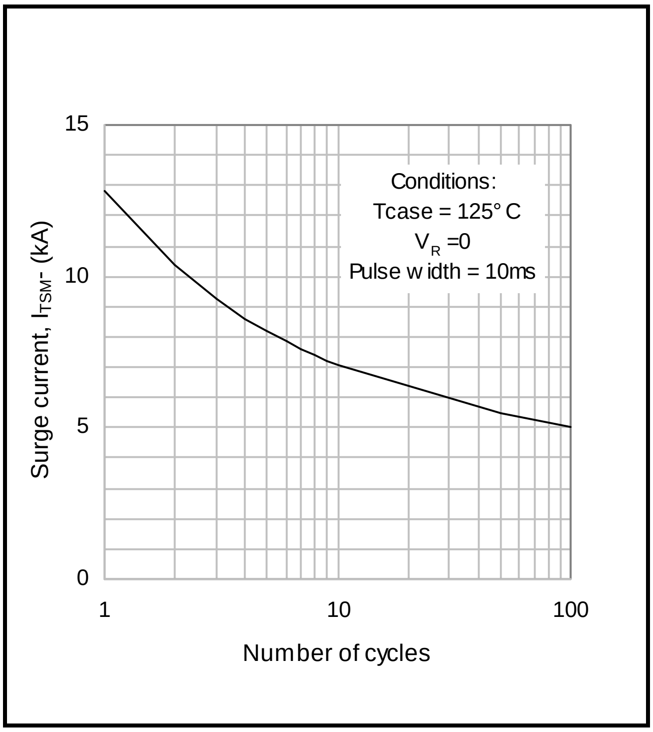


Fig.10 Multi-cycle surge current

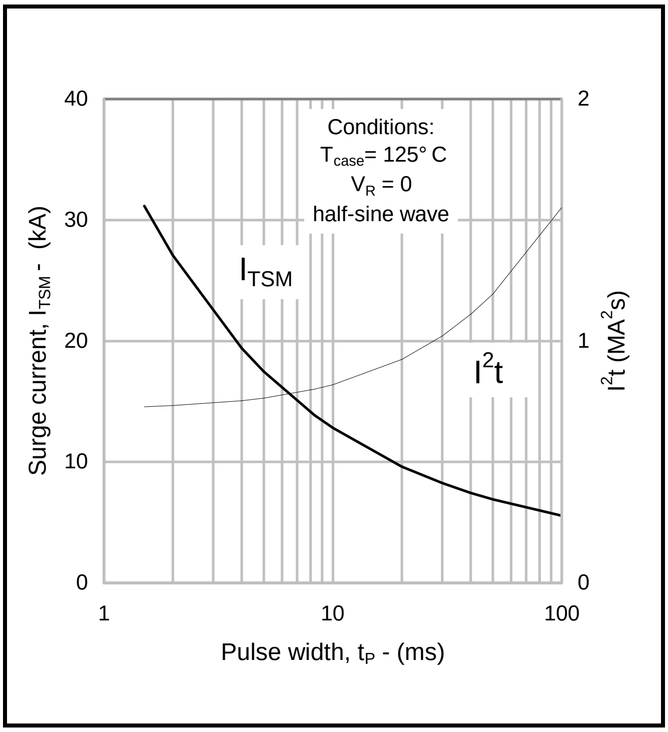
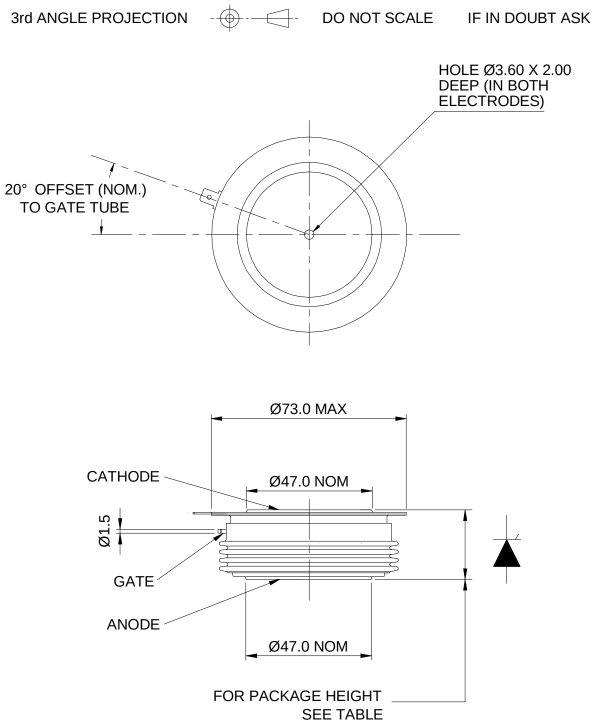


Fig.11 Single-cycle surge current

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise.
DO NOT SCALE.



Device	Maximum Thickness (mm)	Minimum Thickness (mm)
DCR1XXXN22	34.465	33.915
DCR1XXXN28	34.54	33.99
DCRXXXN42	34.77	34.22
DCRXXXN52	34.89	34.34
DCR890N65	35.15	34.6
DCR760N85	**35.51**	**34.96**

Lead length: 420mm
Lead terminal connector: M4 ring

Package outline type code: N

Fig.15 Package outline

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.

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