STRH40N6

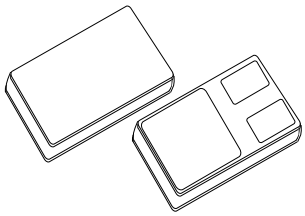
Rad-Hard P-channel 60 V, 30 A Power MOSFET

Datasheet — production data

Features

V_{BDSS}	I_D	$R_{DS(on)}$	Q_g
60 V	30 A	36 mOhm	43 nC

- Fast switching
- 100% avalanche tested
- Hermetic package
- 70 krad TID
- SEE radiation hardened



SMD.5

Applications

- Satellite
- High reliability

Description

This N-channel Power MOSFET is developed with STMicroelectronics unique STripFET™ process. It has specifically been designed to sustain high TID and provide immunity to heavy ion effects.

Figure 1. Internal schematic diagram

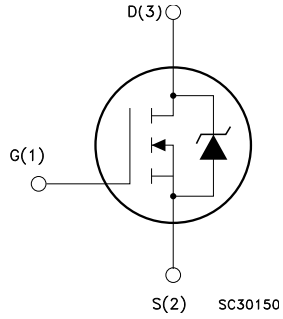


Table 1. Device summary

Part numbers	ESCC part number	Quality level	Package	Lead finish	Mass (g)	Temp. range	EPPL
STRH40N6S1	-	Engineering model	SMD.5	Gold	2	-55 to 150°C	-
STRH40N6SG	TBD	ESCC flight					Target

Note: Contact ST sales office for information about the specific conditions for tape and reel, product in die form and other packages.

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1 Electrical ratings

(T_C= 25 °C unless otherwise specified)

Table 2. Absolute maximum ratings (pre-irradiation)

Symbol	Parameter	Value	Unit
V_{DS}(1)	Drain-source voltage (V_{GS} = 0)	60	V
V_{GS}(2)	Gate-source voltage	±20	V
I_D (3)	Drain current (continuous) at T_C= 25°C	30	A
I_D (3)	Drain current (continuous) at T_C= 100°C	19	A
I_{DM} (4)	Drain current (pulsed)	120	A
P_{TOT} (5)	Total dissipation at T_C= 25°C	75	W
P_{TOT} (3)	Total dissipation at T_C= 25°C	66	W
dv/dt (6)	Peak diode recovery voltage slope	2.5	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. This rating is guaranteed @ $T_J \geq 25$ °C (see *Figure 10: Normalized BV_{DSS} vs temperature*).
2. This value is guaranteed over the full range of temperature.
3. Rated according to the Rthj-case + Rthc-s
4. Pulse width limited by safe operating area
5. Rated according to the Rthj-case
6. $I_{SD} \leq 40$ A, di/dt ≤ 1060 A/µs, V_{DD} = 80 %$V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case	1.67	°C/W
Rthc-s	Case-to-sink	0.21	°C/W
Rthj-amb(1)	Thermal resistance junction -amb	50	°C/W

1. When mounted on heat sink of 300 mm², t < 10 sec

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	15	A
E_{AS}(1)	Single pulse avalanche energy (starting Tj= 25°C, Id= 20 A, Vdd= 40 V)	354	mJ
E_{AS}	Single pulse avalanche energy (starting Tj= 110 °C, Id= 20 A, Vdd= 40 V)	105	

Table 4. Avalanche characteristics (continued)

Symbol	Parameter	Value	Unit
E_{AR}	Repetitive avalanche (Vdd = 50 V, I_{AR} = 17.5 A, f = 10 KHz, T_J = 25 °C, duty cycle = 50%)	20	mJ
	Repetitive avalanche (Vdd = 40 V, I_{AR} = 15 A, f = 100 KHz, T_J = 25 °C, duty cycle = 10%)	1.3	
	Repetitive avalanche (Vdd = 40 V, I_{AR} = 15 A, f = 100 KHz, T_J = 110 °C, duty cycle = 10%)	0.4	

1. Maximum rating value.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Pre-irradiation

Table 5. Pre-irradiation on/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	80% BV_{Dss}			10	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = 20 V V_{GS} = -20 V	 -100		100	nA
BV_{DSS}(1)	Drain-to-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	60			V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	2		4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 12 V I_D = 15 A		0.036	0.045	Ω

1. This rating is guaranteed @ $T_J \geq$ 25 °C (see *Figure 10: Normalized BV_{DSS} vs temperature*).

Table 6. Pre-irradiation dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss}(1) C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{GS} = 0, V_{DS} = 25 V, f=1MHz	1312 281 111	1640 351 139	1968 421 167	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-to-source charge Gate-to-drain (“Miller”) charge	V_{DD} = 30 V, I_D = 40 A, V_{GS}=12 V	35 9 12	43 11 15	52 13 18	nC nC nC
R_G(2)	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level=20 mV open drain	1.04	1.3	1.56	Ω

1. This value is guaranteed over the full range of temperature.
2. Not tested, guaranteed by process.

Table 7. Pre-irradiation switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 20 A, R_G = 4.7 Ω, V_{GS} = 12 V	13	17	21	ns
t_r	Rise time		26	59	92	ns
$t_{d(off)}$	Turn-off-delay time		18	33	48	ns
t_f	Fall time		7	11.5	16	ns

Table 8. Pre-irradiation source drain diode(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} I_{SDM} (2)	Source-drain current Source-drain current (pulsed)				30 120	A A
V_{SD} (3)	Forward on voltage	I_{SD} = 30 A, V_{GS} = 0		1.1		V
t_{rr}(4) Q_{rr}(4) I_{RRM}(4)	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 40 A, di/dt = 100 A/µs V_{DD}= 48 V, Tj = 25 °C	288	360 3.3 18.2	432	ns µC A
t_{rr}(4) Q_{rr}(4) I_{RRM}(4)	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 40 A, di/dt = 100 A/µs V_{DD}= 48 V, Tj = 150 °C	352	440 4.4 19.8	529	ns µC A

1. Refer to the *Figure 16: Source drain diode*.
2. Pulse width limited by safe operating area.
3. Pulsed: pulse duration = 300µs, duty cycle 1.5%
4. Not tested in production, guaranteed by process.

3 Radiation characteristics

The technology of the STMicroelectronics Rad-Hard Power MOSFETs is extremely resistant to radiative environments. Every manufacturing lot is tested for total ionizing dose (irradiation done according to the ESCC 22900 specification, window 1) using the TO-3 package. Both pre-irradiation and post-irradiation performances are tested and specified using the same circuitry and test conditions in order to provide a direct comparison.

(T_{amb}= 22 ± 3 °C unless otherwise specified).

Total dose radiation (TID) testing

One bias conditions using the TO-3 package:

– V_{GS} bias: + 15 V applied and V_{DS}= 0 V during irradiation

The following parameters are measured (see *Table 9*, *Table 10* and *Table 11*):

- before irradiation
- after irradiation
- after 24 hrs @ room temperature
- after 168 hrs @ 100 °C anneal

Table 9. Post-irradiation on/off states @ T_J= 25 °C, (Co60 γ rays 70 K Rad(Si))

Symbol	Parameter	Test conditions	Drift values Δ	Unit
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	80% BV_{Dss}	+20	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = 20 V V_{GS} = -20 V	1.5 -1.5	nA
BV_{DSS}	Drain-to-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	-20%	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	-60% / +20%	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V; I_D = 20 A	±10%	Ω

Table 10. Dynamic post-irradiation @ T_J= 25 °C, (Co60 γ rays 70 K Rad(Si))

Symbol	Parameter	Test conditions	Drift values Δ	Unit
Q_g	Total gate charge	I_G = 1 mA, V_{GS} = 12 V, V_{DS} = 30 V, I_{DS} = 20 A	-5% / +50%	nC
Q_{gs}	Gate-source charge		±35%	
Q_{gd}	Gate-drain charge		-5% / +110%	

Table 11. Source drain diode post-irradiation @ T_J= 25 °C, (Co60 γ rays 70 K Rad(Si))(1)

Symbol	Parameter	Test conditions	Drift values Δ.	Unit
V_{SD} (2)	Forward on voltage	I_{SD} = 40 A, V_{GS} = 0	±5%	V

1. Refer to *Figure 16*.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Single event effect, SOA

The technology of the STMicroelectronics Rad-Hard Power MOSFETs is extremely resistant to heavy ion environment for single event effect (irradiation per MIL-STD-750E, method 1080 bias circuit in *Figure 3: Single event effect, bias circuit*) SEB and SEGR tests have been performed with a fluence of 3e+5 ions/cm².

The accept/reject criteria are:

- SEB test: drain voltage checked, trigger level is set to V_{ds} = - 5 V. Stop condition: as soon as a SEB occurs or if the fluence reaches 3e+5 ions/cm².
- SEGR test: the gate current is monitored every 100 ms. A gate stress is performed before and after irradiation. Stop condition: as soon as the gate current reaches 100 nA (during irradiation or during PIGS test) or if the fluence reaches 3e+5 ions/cm².

The results are:

  – no SEB
  – SEGR test produces the following SOA (see *Table 12: Single event effect (SEE), safe operating area (SOA)* and *Figure 2: Single event effect, SOA*)

Table 12. Single event effect (SEE), safe operating area (SOA)

Ion	Let (Mev/(mg/cm²))	Energy (MeV)	Range (µm)	V_{DS} (V)				
				@V_{GS}=0	@V_{GS}= -2 V	@V_{GS}= -5 V	@V_{GS}= -10 V	@V_{GS}= -20 V
Kr	32	768	94	60	48	39	27	15

Figure 2. Single event effect, SOA

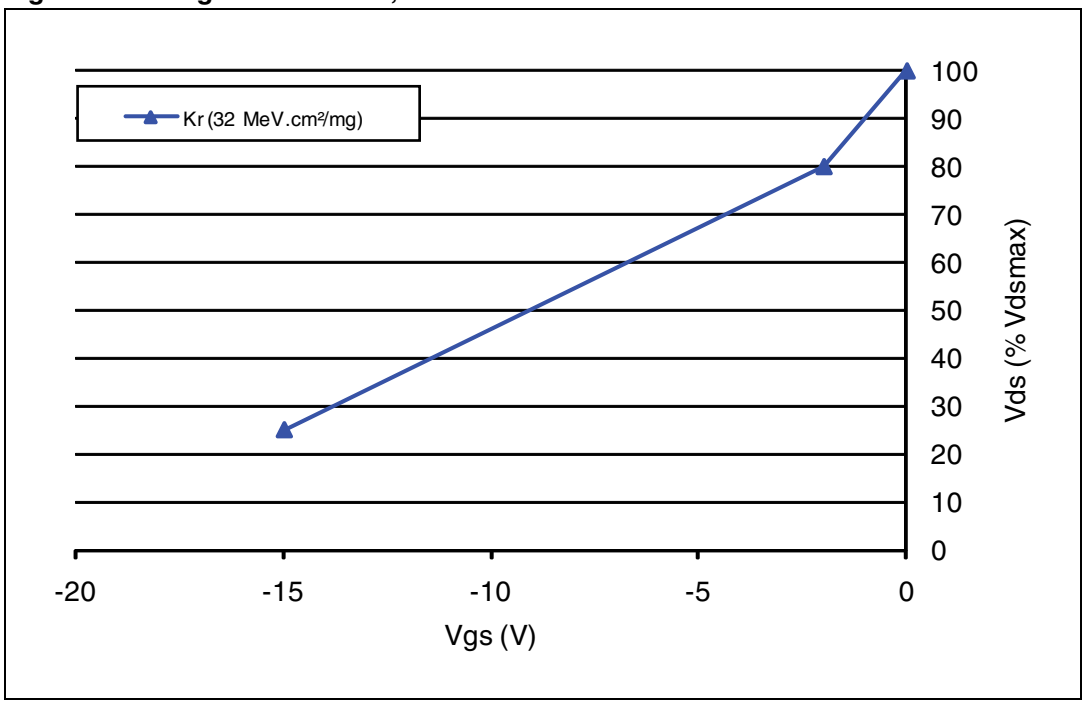
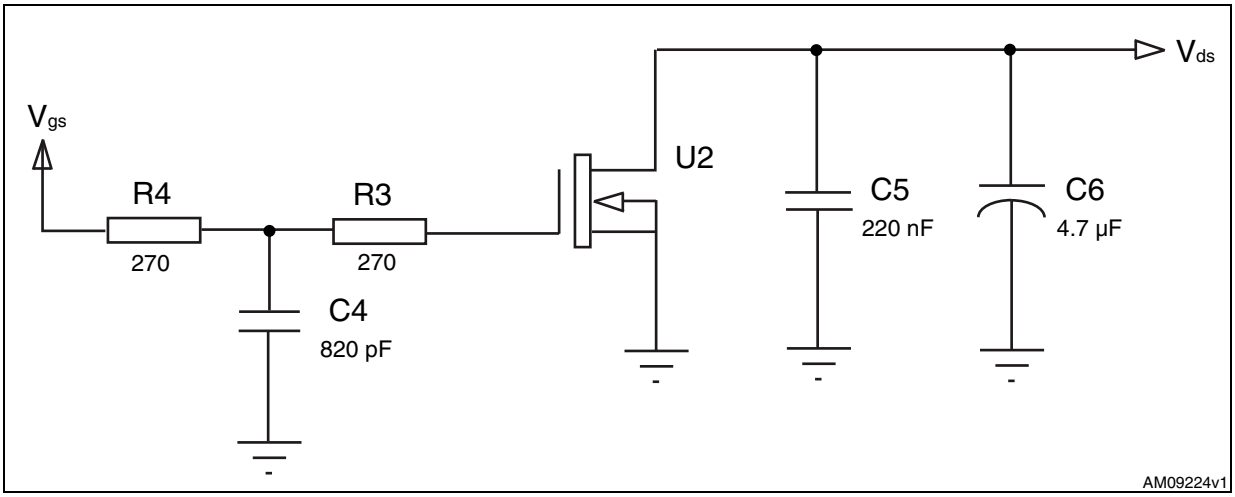


Figure 3. Single event effect, bias circuit(a)



a. Bias condition during radiation refer to *Table 12: Single event effect (SEE), safe operating area (SOA)* .

4 Electrical characteristics (curves)

Figure 4. Safe operating area

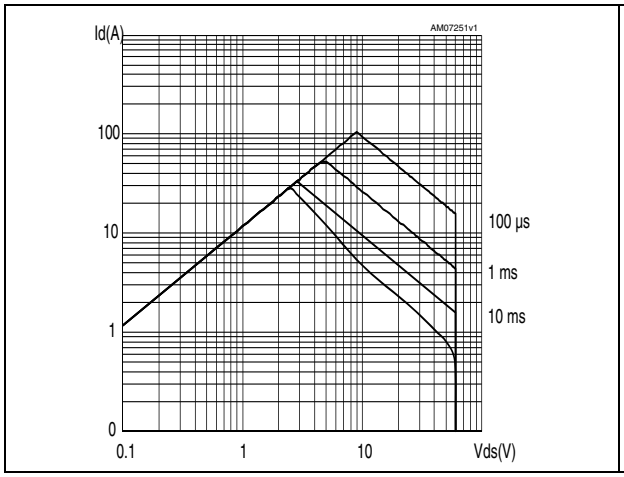


Figure 5. Thermal impedance

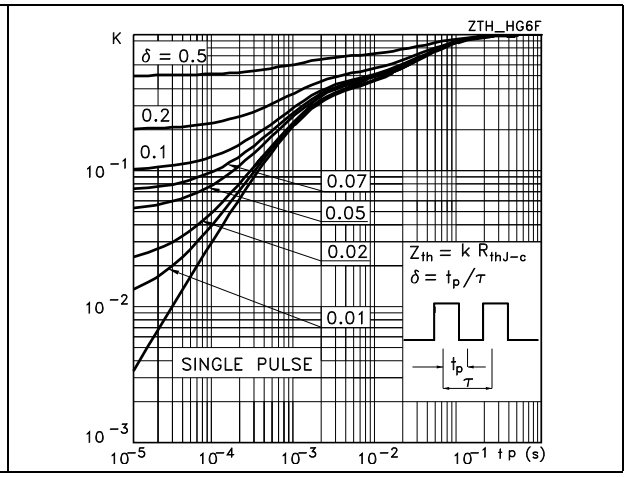


Figure 6. Output characteristics

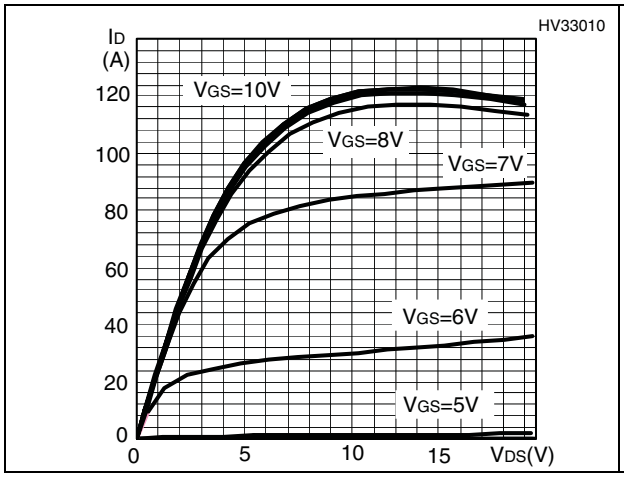


Figure 7. Transfer characteristics

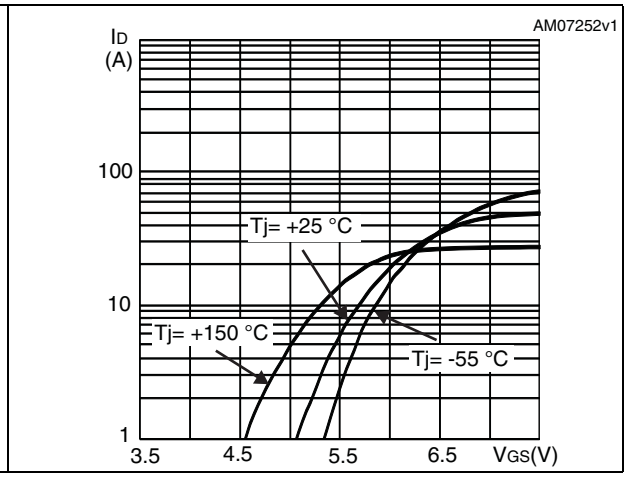


Figure 8. Gate charge vs gate-source voltage

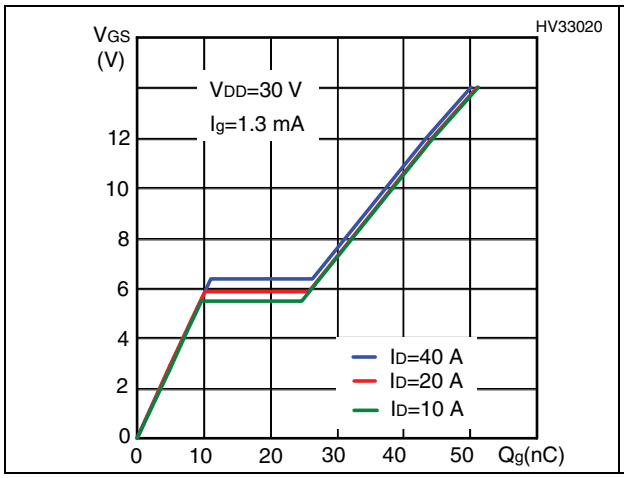


Figure 9. Capacitance variations

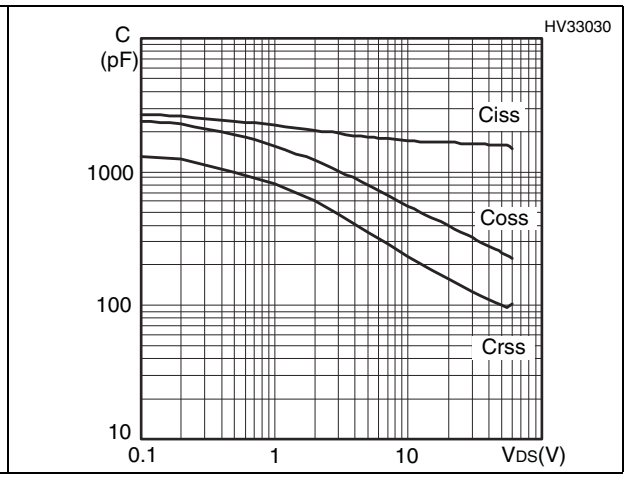


Figure 10. Normalized BV_{DSS} vs temperature

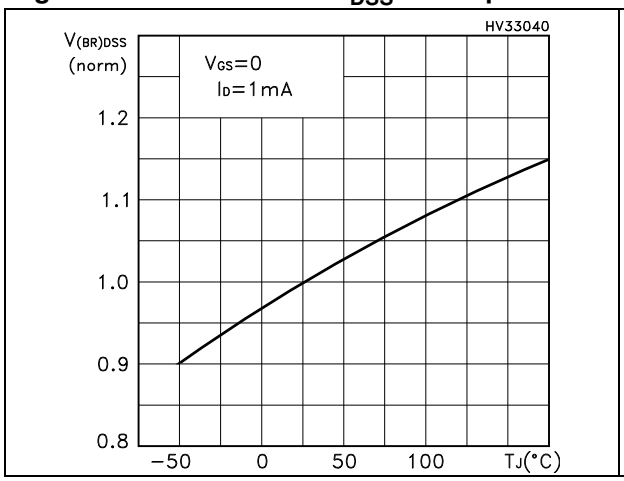


Figure 11. Static drain-source on resistance

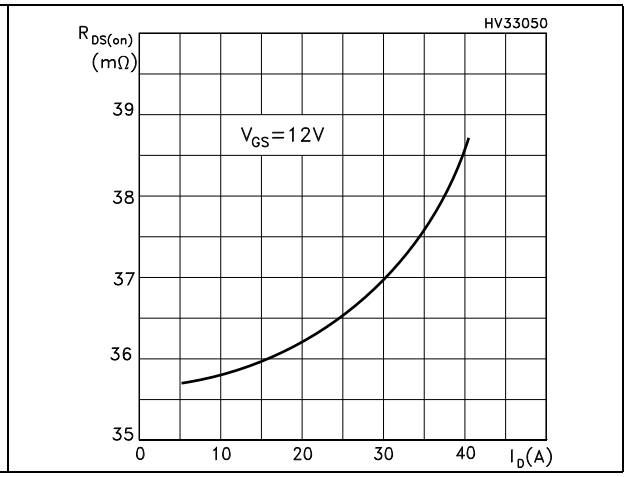


Figure 12. Normalized gate threshold voltage vs temperature

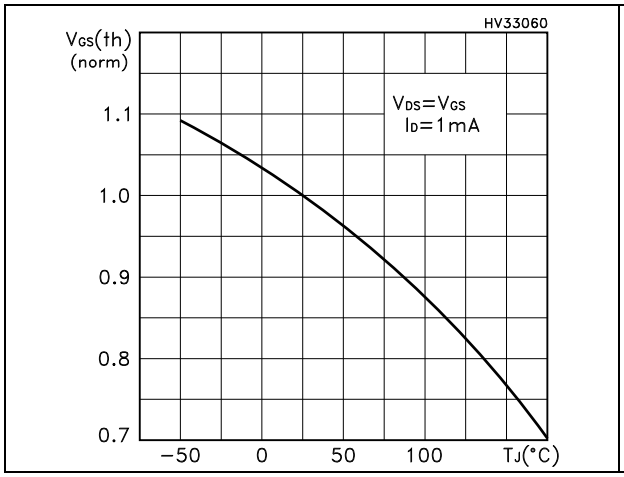


Figure 13. Normalized on resistance vs temperature

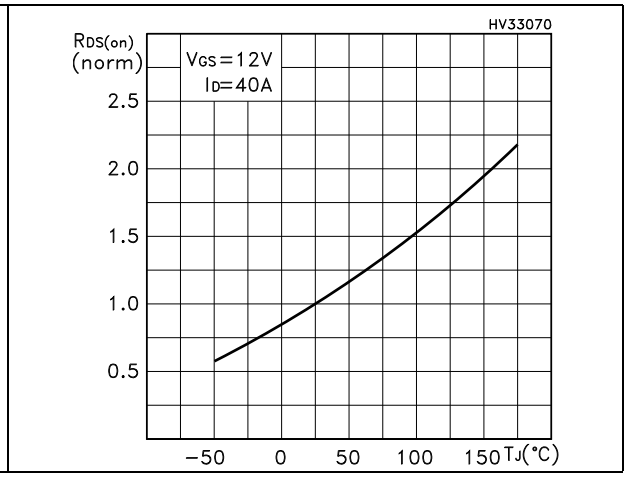
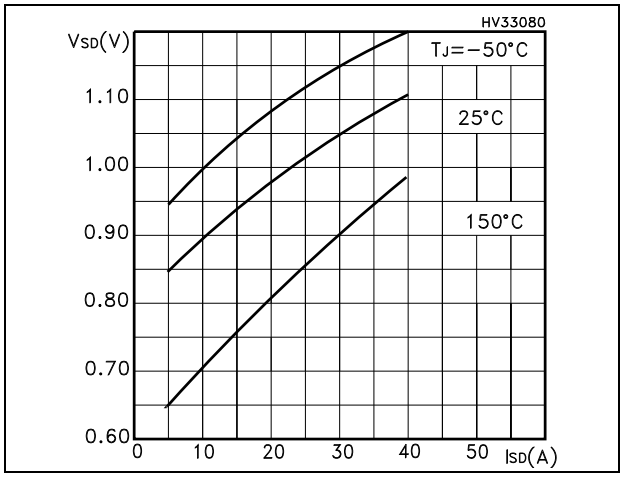
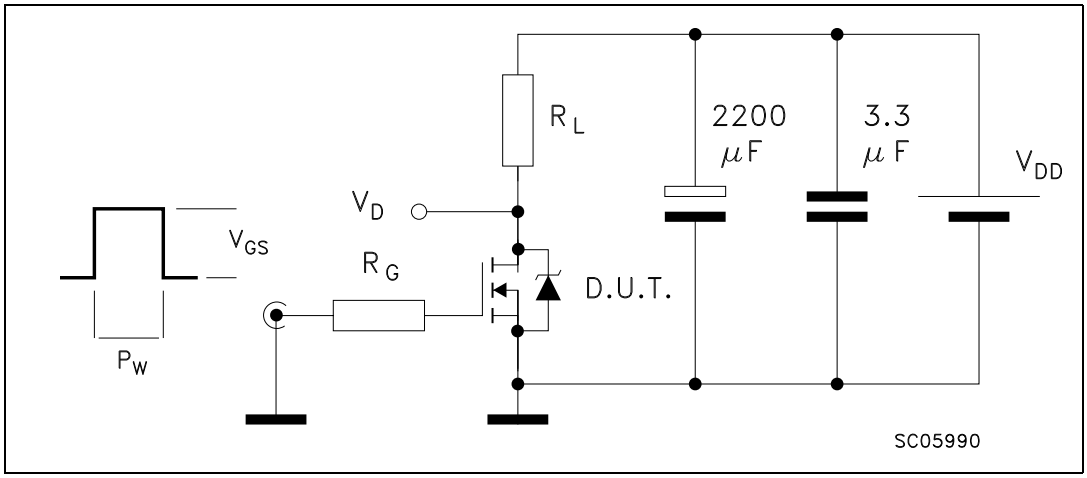


Figure 14. Source drain-diode forward characteristics



5 Test circuits

Figure 15. Switching times test circuit for resistive load (1)



1. Max driver V_{GS} slope = 1V/ns (no DUT)

Figure 16. Source drain diode

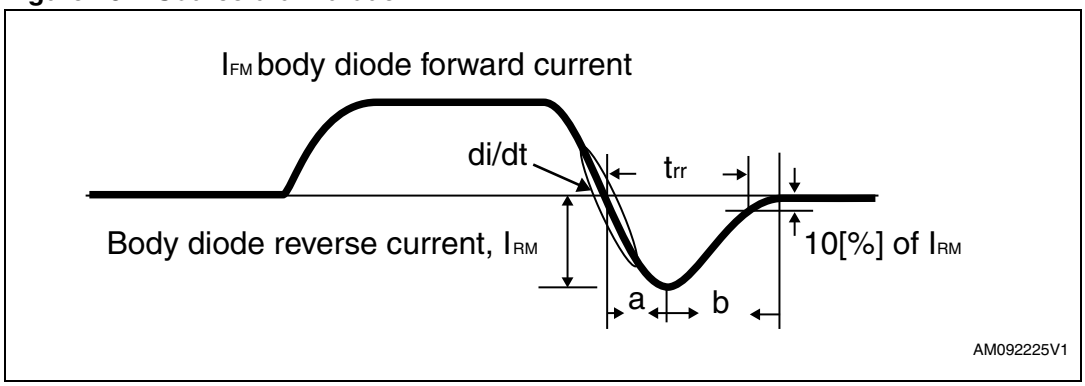
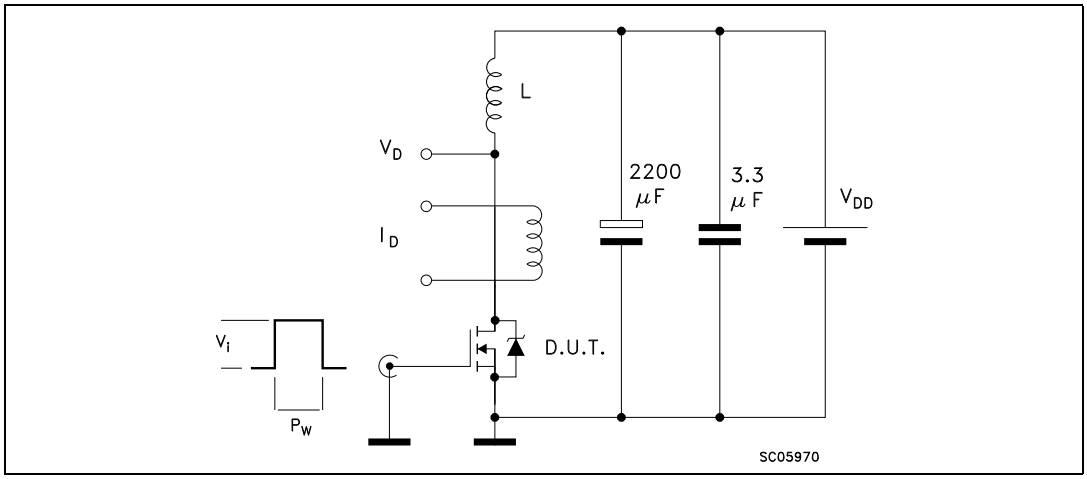


Figure 17. Unclamped inductive load test circuit (single pulse and repetitive)



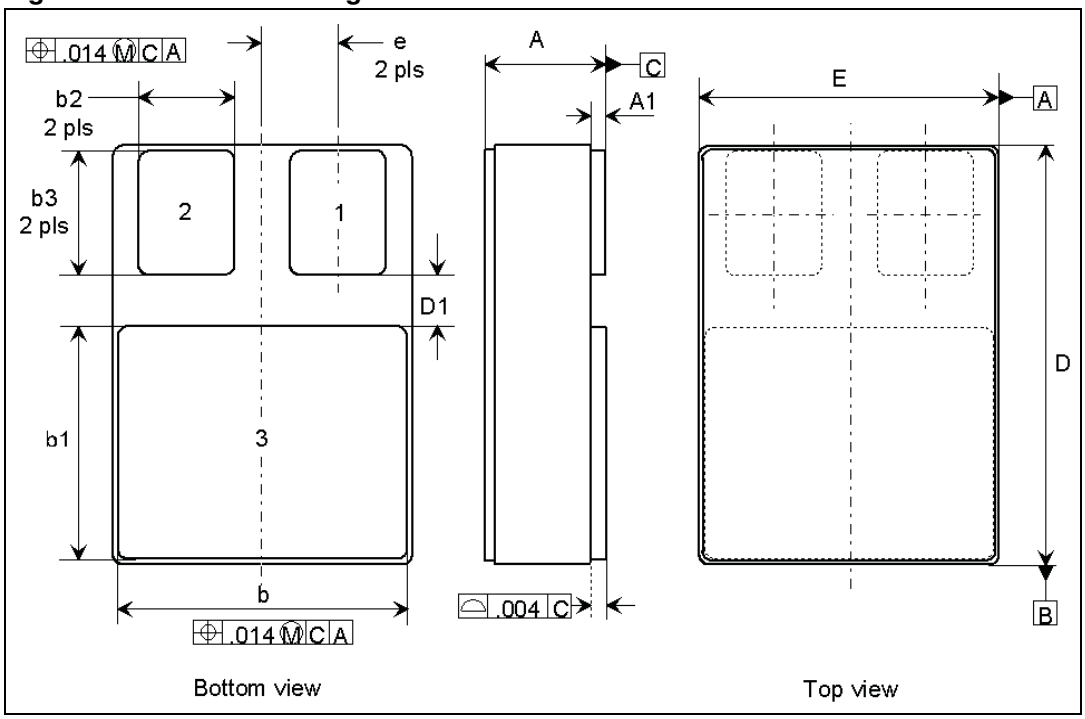
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 13. SMD.5 mechanical data

Dim.	mm			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.84	3.00	3.15	0.112	0.118	0.124
A1	0.25	0.38	0.51	0.010	0.015	0.020
b	7.13	7.26	7.39	0.281	0.286	0.291
b1	5.58	5.72	5.84	0.220	0.225	0.230
b2	2.28	2.41	2.54	0.090	0.095	0.100
b3	2.92	3.05	3.18	0.115	0.120	0.125
D	10.03	10.16	10.28	0.935	0.400	0.405
D1	0.76			0.030		0.685
E	7.39	7.52	7.64	0.291	0.296	0.301
e		1.91			0.075	

Figure 18. TSMD.5 drawing



7 Order codes

Table 14. Ordering information

Order codes	ESCC part number	Quality level	EPPL	Package	Lead finish	Marking	Packing
STRH40N6S1	-	Engineering model	-	SMD-0.5	Gold	STRH40N6FSY1 +BeO	Strip pack
STRH40N6SG	TBD	ESCC flight	Target			TBD	

Contact ST sales office for information about the specific conditions for tape and reel, product in die form and other packages.

8 Revision history

Table 15. Document revision history

Date	Revision	Changes
03-Jan-2011	1	First release.
25-Aug-2011	2	Updated order codes in *Table 1: Device summary* and *Table 14: Ordering information*. Minor text changes.
09-Nov-2011	3	Updated dynamic values on *Table 7: Pre-irradiation switching times*. Document status changed from preliminary data to datasheet.
28-Mar-2012	4	Updated title in cover page.

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