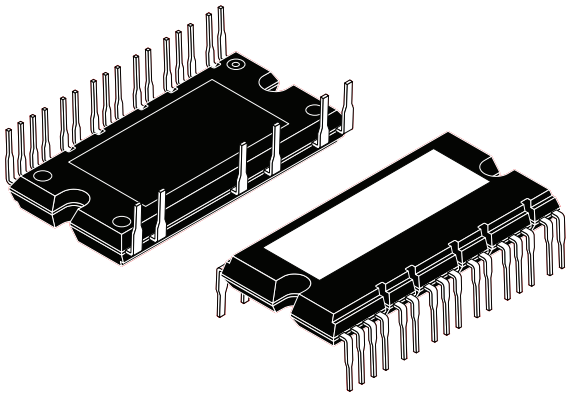
STGIPS35K60L1

SLLIMM™ (small low-loss intelligent molded module) IPM, single phase - 35 A, 600 V short-circuit rugged IGBT

Preliminary data

Features

- IPM 35 A, 600 V single phase IGBT including control ICs for gate driving and free-wheeling diodes
- Short-circuit rugged IGBTs
- $V_{CE(sat)}$ negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull down / pull up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Dead time and interlocking function
- Smart shutdown function
- Comparator for fault protection against over temperature and overcurrent
- DBC substrate leading to low thermal resistance
- Isolation rating of 2500 V_{rms}/min
- 4.7 kΩ NTC for temperature control
- UL recognition pending (in agreement to QQQX2.E81734 - Electrically-isolated semiconductor devices - component)



SDIP-22L

Description

This intelligent power module provides a compact, high performance AC motor drive for a simple and rugged design. It targets power inverters for air conditioners. It combines ST proprietary control ICs with the most advanced short-circuit rugged IGBT system technology. SLLIMM™ is a trademark of STMicroelectronics.

Applications

- Power inverters for compressors

Table 1. Device summary

Order code	Marking	Package	Packaging
STGIPS35K60L1	GIPS35K60L1	SDIP-22L	Tube

Contents

1 Internal schematic diagram and pin configuration

Figure 1. Internal schematic diagram

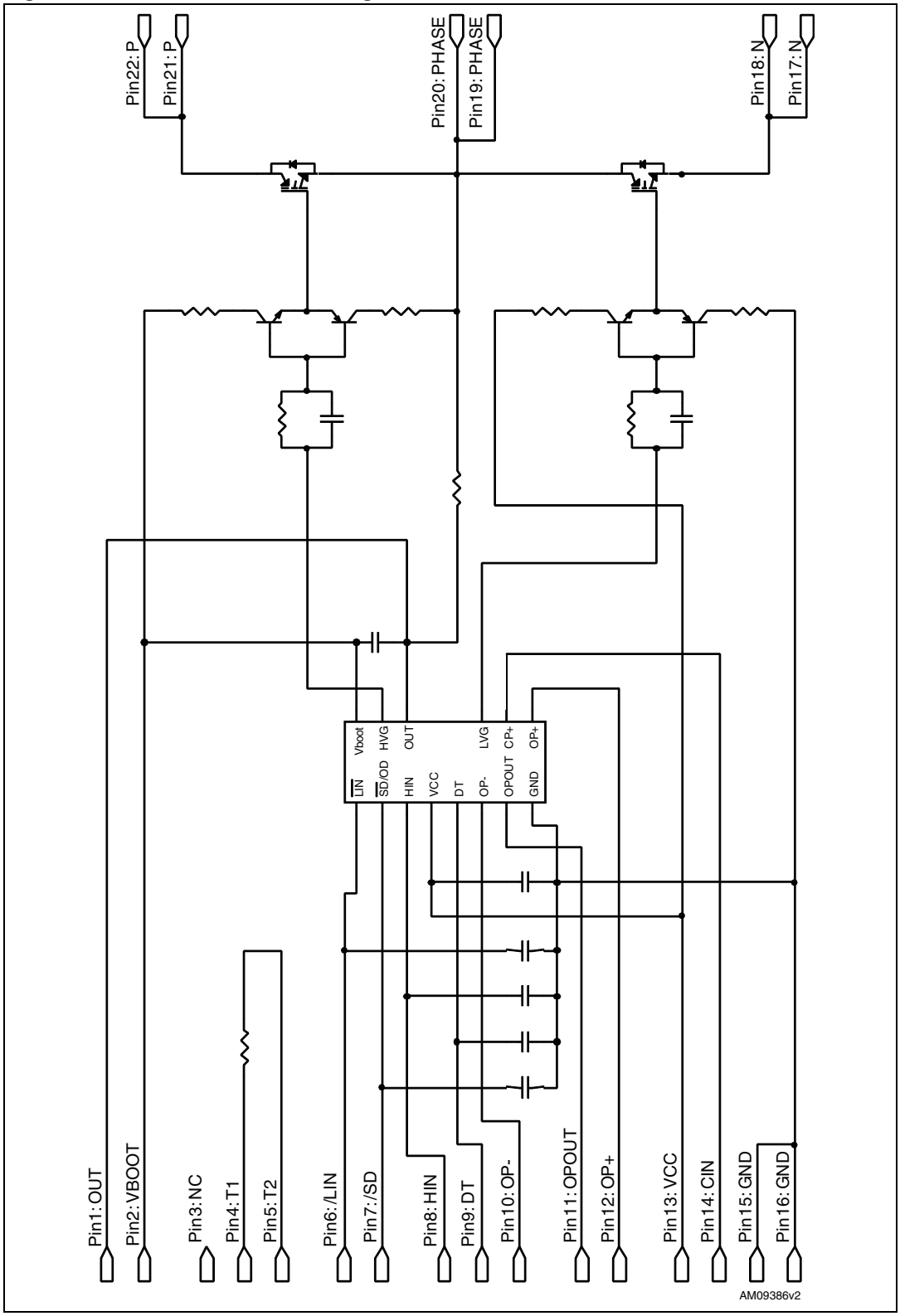
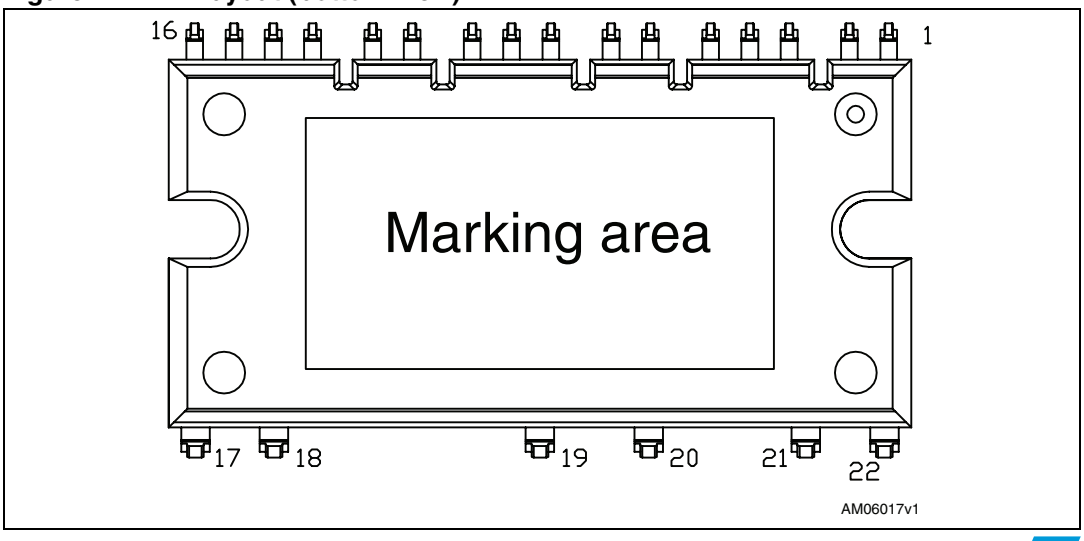


Table 2. Pin description

Pin	Symbol	Description
1	OUT_{PHASE}	PHASE reference output
2	V_{boot}	Bootstrap voltage
3	NC	Not connected
4	T_1	NTC thermistor terminal 1
5	T_2	NTC thermistor terminal 2
6	$\overline{LIN}$	Low side logic input
7	$\overline{SD}$/OD	Shutdown logic input (active low) / open drain (comparator output)
8	HIN	High side logic input
9	DT	Dead time setting
10	OP-	Op amp inverting input
11	OP_{OUT}	Op amp output
12	OP+	Op amp non inverting input
13	V_{CC}	Low voltage power supply
14	CIN	Comparator input
15	GND	Ground
16	GND	Ground
17	N	Negative DC input
18	N	Negative DC input
19	PHASE	Phase output
20	PHASE	Phase output
21	P	Positive DC input
22	P	Positive DC input

Figure 2. Pin layout (bottom view)



2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{CES}	Each IGBT collector emitter voltage (V_{IN} = 0)	600	V
$\pm I_C$ (1)	Each IGBT continuous collector current at T_C = 25°C	35	A
$\pm I_{CP}$ (2)	Each IGBT pulsed collector current	70	A
P_{TOT}	Each IGBT total dissipation at T_C = 25°C	100	W
t_{scw}	Short circuit withstand time, V_{CE} = 0.5 $V_{(BR)CES}$ T_J = 125 °C, V_{CC} = V_{boot}= 15 V, V_I= 1 "logic state"	5	µs

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

2. Pulse width limited by max junction temperature

Table 4. Control part

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage applied between OUT - GND	V_{boot} - 21 to V_{boot} + 0.3	V
V_{CC}	Low voltage power supply	-0.3 to +21	V
V_{CIN}	Comparator input voltage	-0.3 to V_{CC} +0.3	V
V_{boot}	Bootstrap voltage applied between V_{boot} - OUT	-0.3 to 620	V
V_{IN}	Logic input voltage applied between HIN, $\overline{LIN}$ and GND	-0.3 to 15	V
$V_{\overline{SD}/OD}$	Open-drain voltage	-0.3 to 15	V
dV_{OUT}/dt	Allowed output slew rate	50	V/ns

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 sec.)	2500	V
T_J (1)	Operating junction temperature for IGBT and diode	-40 to 150	°C
T_C	Module case operation temperature	-40 to 125	°C

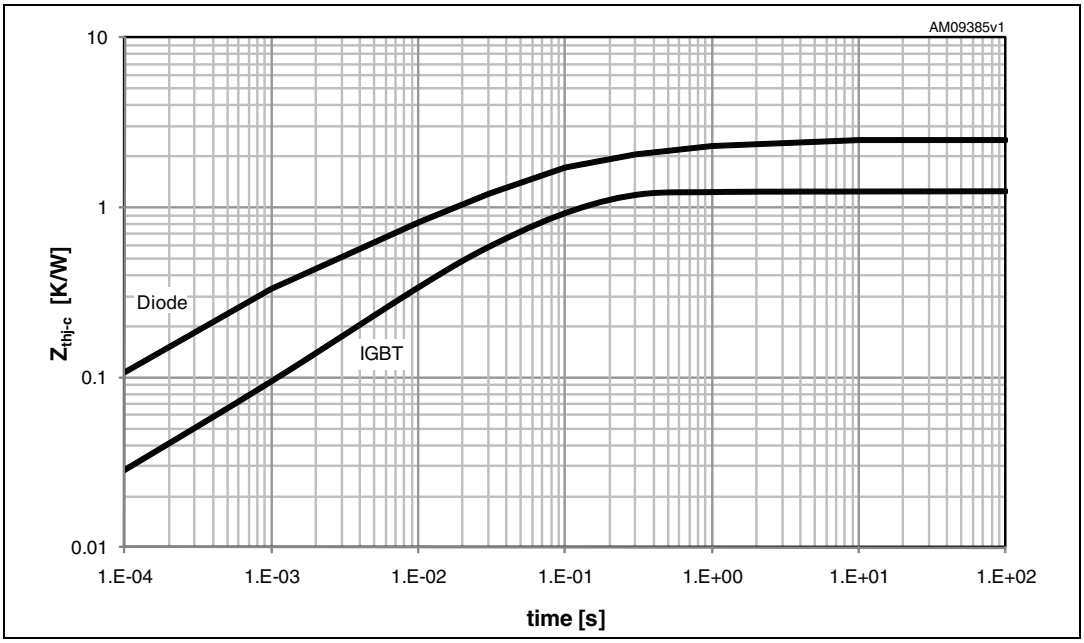
1. The maximum junction temperature rating of the power chips integrated within the SDIP module is 150°C (@$T_C \leq$ 100°C). To ensure safe operation of the SDIP module, the average junction temperature should be limited to $T_j(avg) \leq$ 125°C (@$T_C \leq$ 100°C).

2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case single IGBT	1.25	°C/W
	Thermal resistance junction-case single diode	2.5	°C/W

Figure 3. Transient thermal impedance IGBT/diode - inverter



3 Electrical characteristics

T_J = 25 °C unless otherwise specified.

Table 7. Inverter part

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{CC} = V_{boot} = 15 V, V_{IN} = 1 "logic state", I_C = 30 A	-	2.1	2.7	V
		V_{CC} = V_{boot} = 15 V, V_{IN} = 1 "logic state", I_C = 30 A, T_J = 125 °C	-	1.9		
I_{CES}	Collector-cut off current (V_{IN} (1)= 0 “logic state”)	V_{CE} = 600 V, V_{CC} = V_{Boot} = 15 V	-		500	µA
V_F	Diode forward voltage	V_{IN} = 0 "logic state", I_F = 30A	-		2.5	V
Switching on/off (inductive load) (1)						
t_{on}	Turn-on time	V_{DD} = 410 V, V_{CC} = V_{boot} = 15 V, V_{IN} = 1 "logic state" (see *Table 13*) I_C = 30 A (see *Figure 4* and *5*)	-	440	-	ns
$t_{c(on)}$	Crossover time (on)		-	87	-	
t_{off}	Turn-off time		-	280	-	
$t_{c(off)}$	Crossover time (off)		-	130	-	
t_{rr}	Reverse recovery time		-	60	-	
E_{on}	Turn-on switching losses		-	680	-	µJ
E_{off}	Turn-off switching losses		-	760	-	
$di/dt_{(on)}$	Rate of rise of on-state current	V_{DD} = 410 V, V_{CC} = V_{boot} = 15 V, V_{IN} = 1 "logic state" (see *Table 13*), I_C = 70 A (see *Figure 4* and *5*)	-	2000	-	A/µs
t_{on}	Turn-on time	V_{DD} = 410 V, V_{CC} = V_{boot} = 15 V, V_{IN} = 1 "logic state" (see *Table 13*) I_C = 30 A, T_J = 125 °C (see *Figure 4* and *5*)	-	550	-	ns
$t_{c(on)}$	Crossover time (on)		-	110	-	
t_{off}	Turn-off time		-	410	-	
$t_{c(off)}$	Crossover time (off)		-	200	-	
t_{rr}	Reverse recovery time		-	85	-	
E_{on}	Turn-on switching losses		-	1025	-	µJ
E_{off}	Turn-off switching losses		-	1400	-	
$di/dt_{(on)}$	Rate of rise of on-state current	V_{DD} = 410 V, V_{CC} = V_{boot} = 15 V, V_{IN} = 1 "logic state" (see *Table 13*) I_C = 70 A, T_J = 125 °C (see *Figure 4* and *5*)	-	1750	-	A/µs

1. t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition. Parameter values take into account a 20 nH stray inductance.

Figure 4. Switching time test circuit

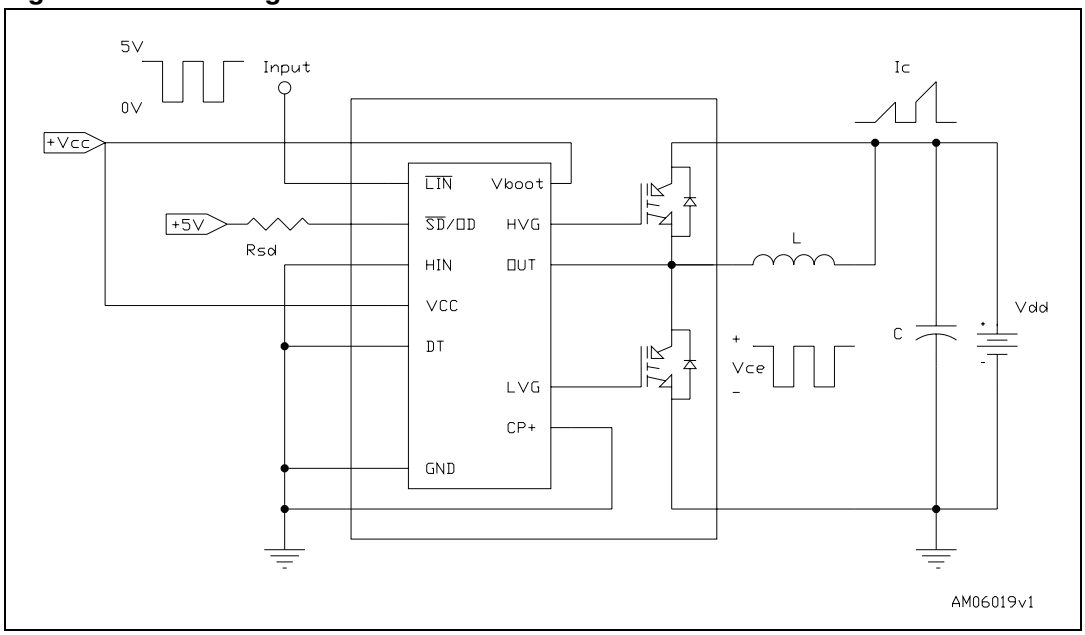
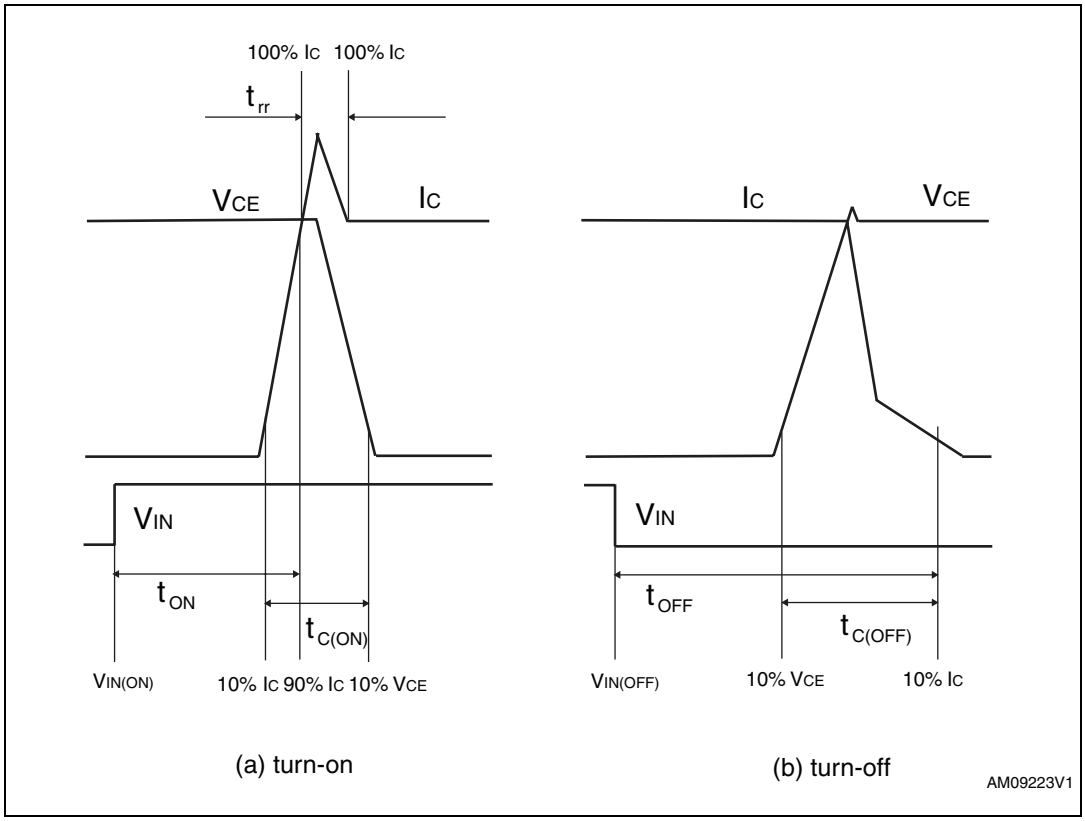


Figure 5. Switching time definition (1)



1. “Switching time definition" refers to HIN inputs (active high). For $\overline{LIN}$ inputs (active low), V_{IN} polarity must be inverted for turn-on and turn-off.

3.1 Control part

Table 8. Low voltage power supply (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.5	1.8	V
V_{CC_thON}	V_{CC} UV turn ON threshold		11.5	12	12.5	V
V_{CC_thOFF}	V_{CC} UV turn OFF threshold		10	10.5	11	V
I_{qccu}	Undervoltage quiescent supply current	V_{CC} = 10 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ = 5 V; HIN = 0, CIN = 0			200	µA
I_{qcc}	Quiescent current	V_{CC} = 15 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ = 5 V HIN = 0, CIN = 0			1	mA
V_{ref}	Internal reference voltage		0.5	0.54	0.58	V

Table 9. Bootstrapped voltage (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BS_hys}	V_{BS} UV hysteresis		1.2	1.5	1.8	V
V_{BS_thON}	V_{BS} UV turn ON threshold		10.6	11.5	12.4	V
V_{BS_thOFF}	V_{BS} UV turn OFF threshold		9.1	10	10.9	V
I_{QBSU}	Undervoltage V_{BS} quiescent current	V_{BS} = 10 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ and HIN = 5 V; CIN = 0		70	110	µA
I_{QBS}	V_{BS} quiescent current	V_{BS} = 15 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ and HIN = 5 V; CIN = 0		150	210	µA
$R_{DS(on)}$	Bootstrap driver on resistance	LVG ON		120		Ω

Table 10. Logic inputs (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage				0.8	V
V_{ih}	High logic level voltage		2.25			V
I_{HINh}	HIN logic “1” input bias current	HIN = 15 V	110	175	260	µA
I_{HINl}	HIN logic “0” input bias current	HIN = 0 V			1	µA
I_{LINl}	$\overline{LIN}$ logic “1” input bias current	$\overline{LIN}$ = 0 V	3	6	20	µA
I_{LINh}	$\overline{LIN}$ logic “0” input bias current	$\overline{LIN}$ = 15 V			1	µA
I_{SDh}	$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ = 15 V	10	40	100	µA
I_{SDl}	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 0 V			1	µA

Table 11. Op amp characteristics (V_{CC} = 15 V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	V_{ic} = 0 V, V_o = 7.5 V			6	mV
I_{io}	Input offset current	V_{ic} = 0 V, V_o = 7.5 V		4	40	nA
I_{ib}	Input bias current (1)			100	200	nA
V_{icm}	Input common mode voltage range		0			V
V_{OL}	Low level output voltage	R_L = 10 kΩ to V_{CC}		75	150	mV
V_{OH}	High level output voltage	R_L = 10 kΩ to GND	14	14.7		V
I_o	Output short circuit current	Source, V_{id} = +1; V_o = 0 V	16	30		mA
		Sink, V_{id} = -1; V_o = V_{CC}	50	80		mA
SR	Slew rate	V_i = 1 - 4 V; C_L = 100 pF; unity gain	2.5	3.8		V/µs
GBWP	Gain bandwidth product	V_o = 7.5 V	8	12		MHz
A_{vd}	Large signal voltage gain	R_L = 2 kΩ	70	85		dB
SVR	Supply voltage rejection ratio	vs. V_{CC}	60	75		dB
CMRR	Common mode rejection ratio		55	70		dB

1. The direction of input current is out of the IC.

Table 12. Sense comparator characteristics (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ib}	Input bias current	V_{CP+} = 1 V	-		1	µA
V_{ol}	Open-drain low-level output voltage	I_{od} = - 3 mA	-		0.5	V
t_{d_comp}	Comparator delay	$\overline{SD}$/OD pulled to 5 V through 100 kΩ resistor	-	90	130	ns
SR	Slew rate	C_L = 180 pF; R_{pu} = 5 kΩ	-	60		V/µsec
t_{sd}	Shutdown to high / low side driver propagation delay	V_{OUT} = 0, V_{boot} = V_{CC}, V_{IN} = 0 to 3.3 V	50	125	200	ns
t_{isd}	Comparator triggering to high / low side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CINi	50	200	250	

Table 13. Truth table

Condition	Logic input (V_I)			Output	
	$\overline{SD}$/OD	$\overline{LIN}$	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X	X	L	L
Interlocking half-bridge tri-state	H	L	H	L	L
0 ‘’logic state” half-bridge tri-state	H	H	L	L	L
1 “logic state” low side direct driving	H	L	L	H	L
1 “logic state” high side direct driving	H	H	H	L	H

Note: X: don’t care

3.1.1 NTC thermistor

Table 14. NTC thermistor

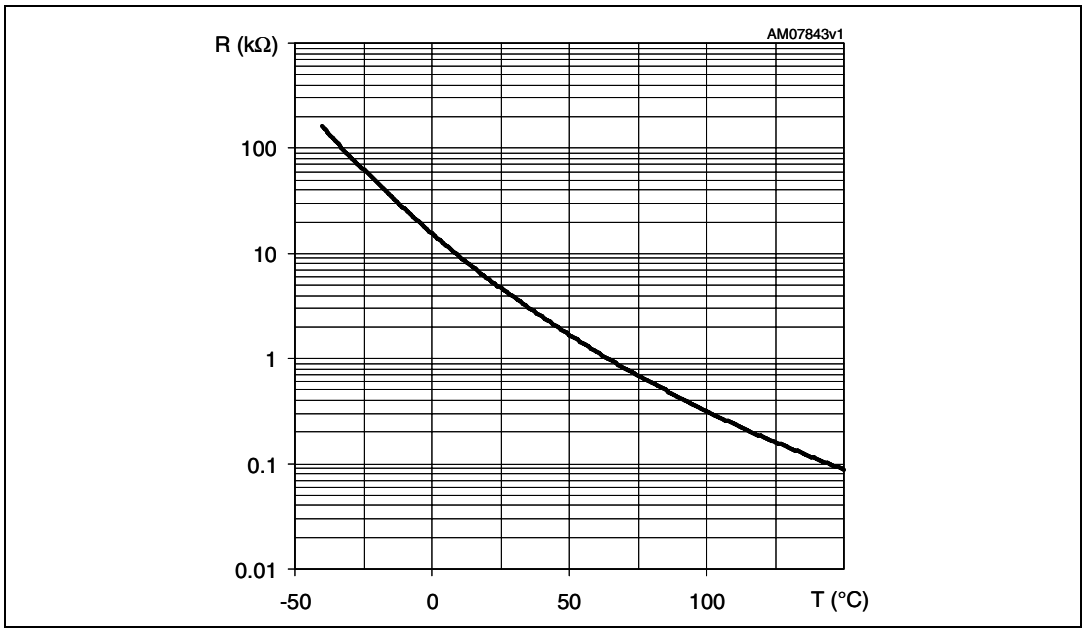
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
R_{25}	Resistance	T_C = 25°C		4.7		kΩ
R_{125}	Resistance	T_C = 125°C		160		Ω
B	B-constant	T_C = 25°C		3950		K
T	Operating temperature		-40		150	°C

Equation 1: resistance variation vs. temperature

$$R(T) = R_{25} \cdot e^{B\left(\frac{1}{T} - \frac{1}{298}\right)}$$

Where T are temperatures in Kelvins

Figure 6. NTC resistance vs. temperature



3.1.2 Dead time

Figure 7. Dead time and interlocking waveforms definitions

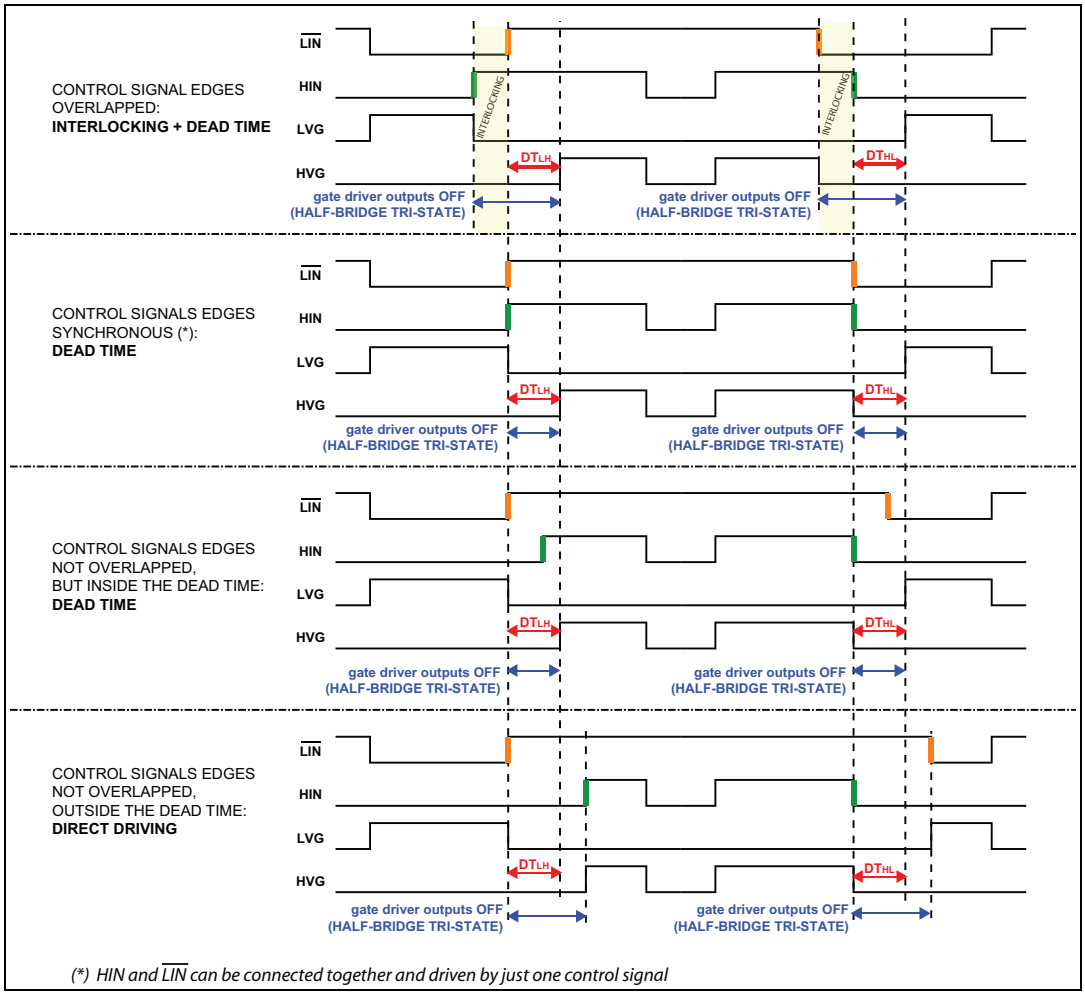
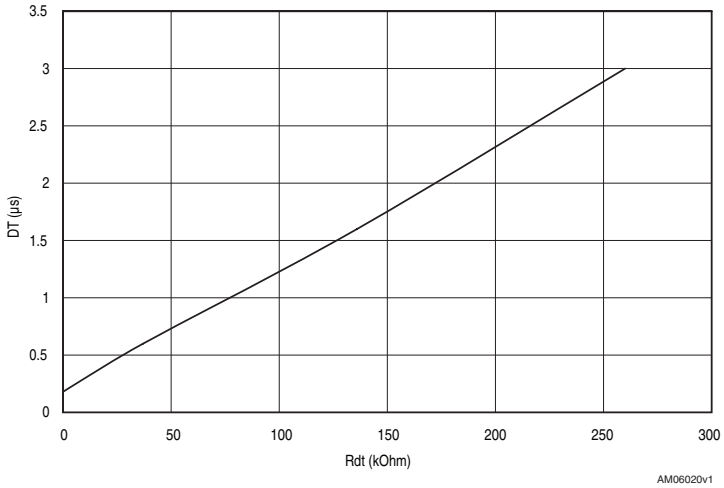


Figure 8. Typical dead time vs. DT resistor value



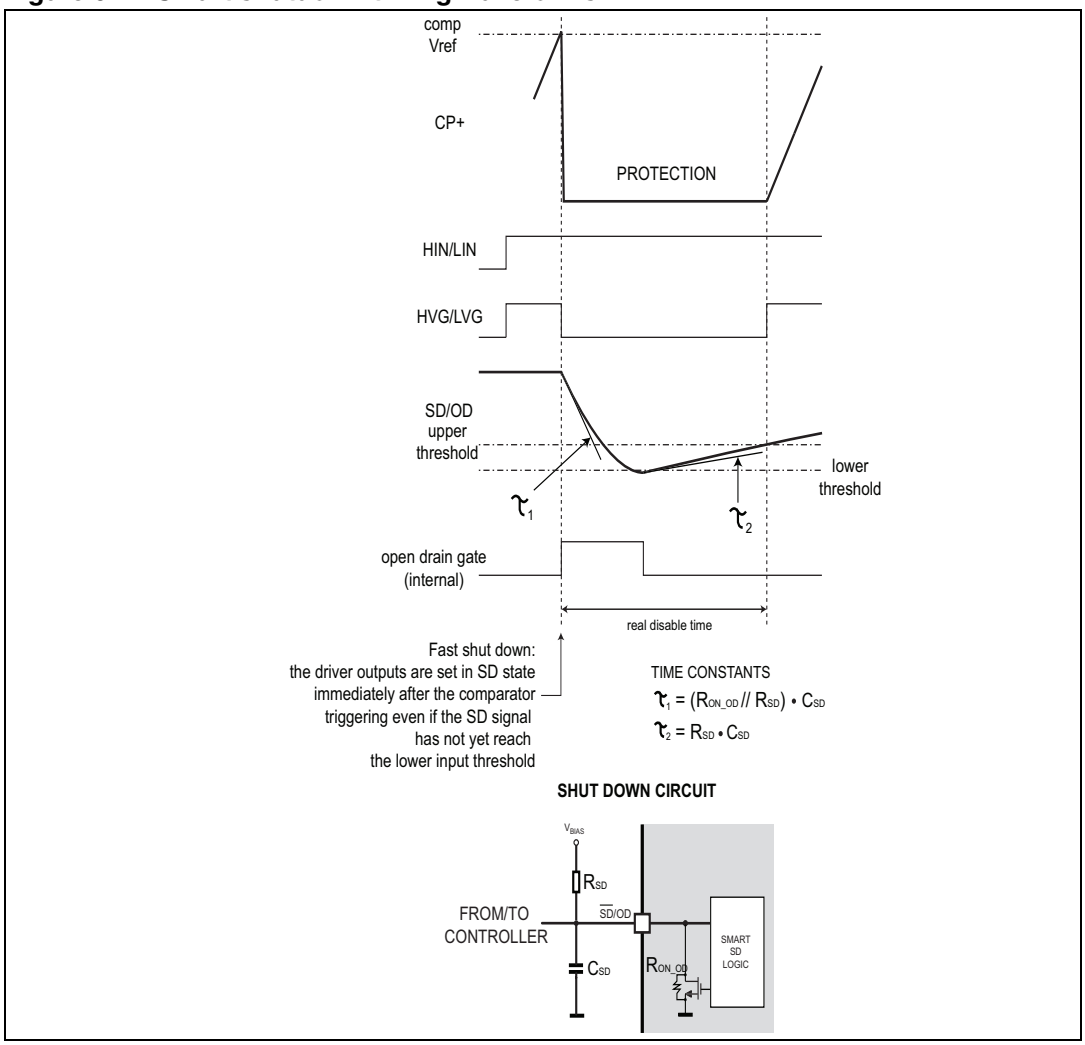
3.2 Recommendations

- Input signal HIN is active high logic. A 85 kΩ (typ.) pull down resistor is built-in for each high side input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.
- Input signal $\overline{\text{LIN}}$ is active low logic. A 720 kΩ (typ.) pull-up resistor, connected to an internal 5 V regulator through a diode, is built-in for each low side input.
- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The $\overline{\text{SD}}$/OD signal should be pulled up to 5 V / 3.3 V with an external resistor (see *Section 4: Smart shutdown function* for detailed info).
- When setting the maximum voltage to be applied between P-N, the internal stray inductance and the maximum di/dt should be considered. Due to both internal and layout stray inductances, the di/dt results in a voltage surges between the DC-link capacitor and the switches during commutations.
- Suggested control supply voltage (V_{CC}): from 13.5 V to 18 V
- Suggested high side bias voltage (V_{BS} between V_{BOOT} and PHASE): from 13 V to 18 V

4 Smart shutdown function

The STGIPS35K60L1 integrates a comparator for fault sensing purposes. The comparator non-inverting input (C_{IN}) can be connected to an external shunt resistor in order to implement a simple overcurrent protection function. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low-level leading the half-bridge in tri-state. In the common overcurrent protection architectures the comparator output is usually connected to the shutdown input through a RC network, in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Our smart shutdown architecture allows to immediately turn-off the output gate driver in case of overcurrent, the fault signal has a preferential path which directly switches off the outputs. The time delay between the fault and the outputs turn-off is no more dependent on the RC values of the external network connected to the shutdown pin. At the same time the internal logic turns on the open-drain output and holds it on until the shutdown voltage goes below the logic input lower threshold. Finally the smart shutdown function provides the possibility to increase the real disable time without increasing the constant time of the external RC network.

Figure 9. Smart shutdown timing waveforms



Pls refer to *Table 12* for internal propagation delay time details.

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

Table 15. SDIP-22L package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	43.90	44.40	44.90
A1	1.15	1.35	1.55
A2	1.40	1.60	1.80
A3	38.90	39.40	39.90
B	21.50	22.00	22.50
B1	11.25	11.85	12.45
B2	24.70	25.20	25.70
C	5.00	5.40	6.00
C1	6.50	7.00	7.50
C2	11.20	11.70	12.20
e	2.15	2.35	2.55
e1	3.40	3.60	3.80
e2	4.50	4.70	4.90
e3	15.70	15.90	16.10
e4	6.30	6.50	6.70
e5	9.20	9.40	9.60
D		33.20	
D1		5.60	
E		10.20	
E1		0.40	
F	0.85	1.00	1.15
F1	0.35	0.50	0.65
R	1.55	1.75	1.95
T	0.45	0.55	0.65
V	0°		6°

Figure 10. SDIP-22L package drawing (dimensions are in mm.)

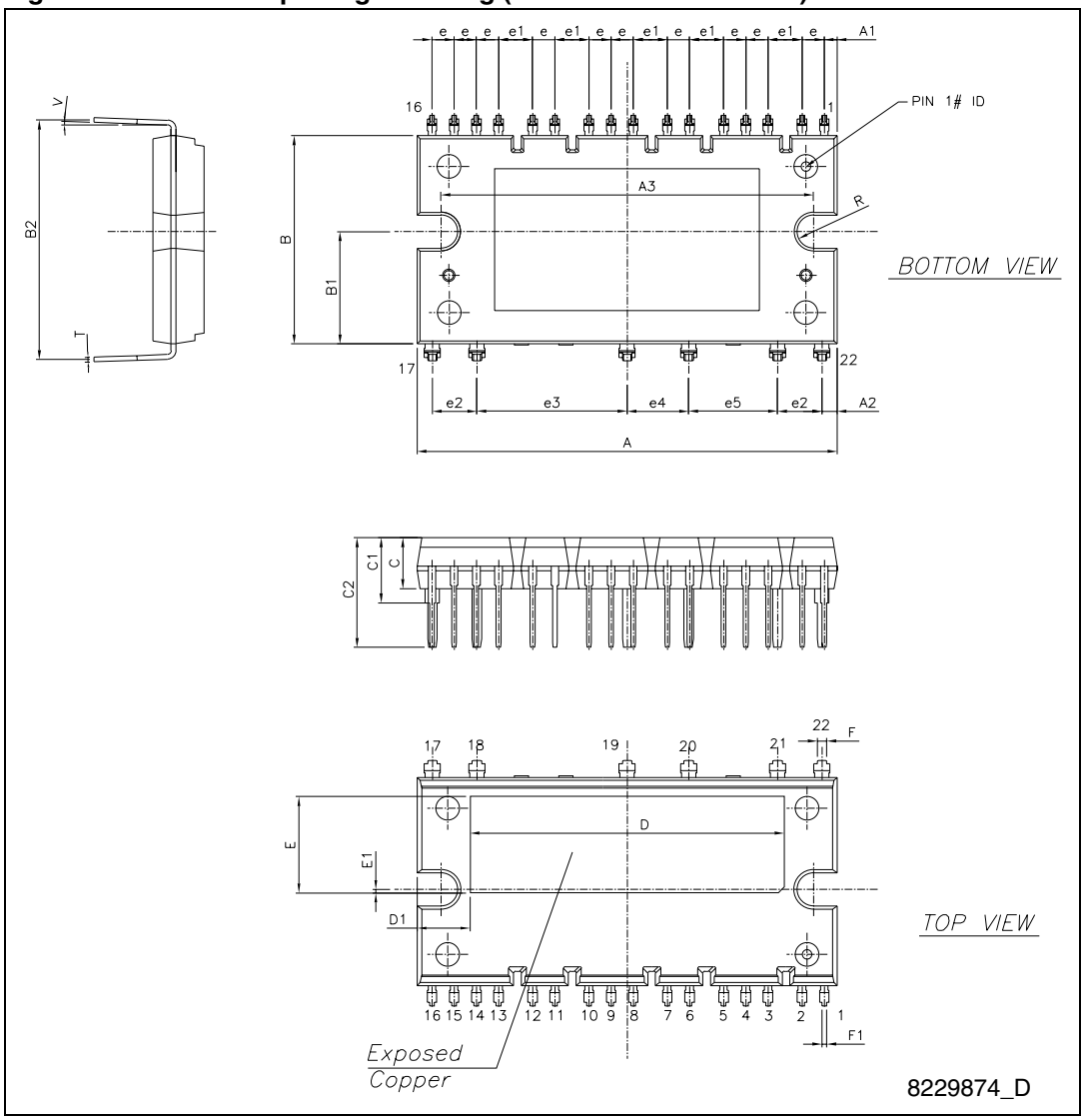


Figure 11. SDIP-22L shipping tube (dimensions are in mm.)

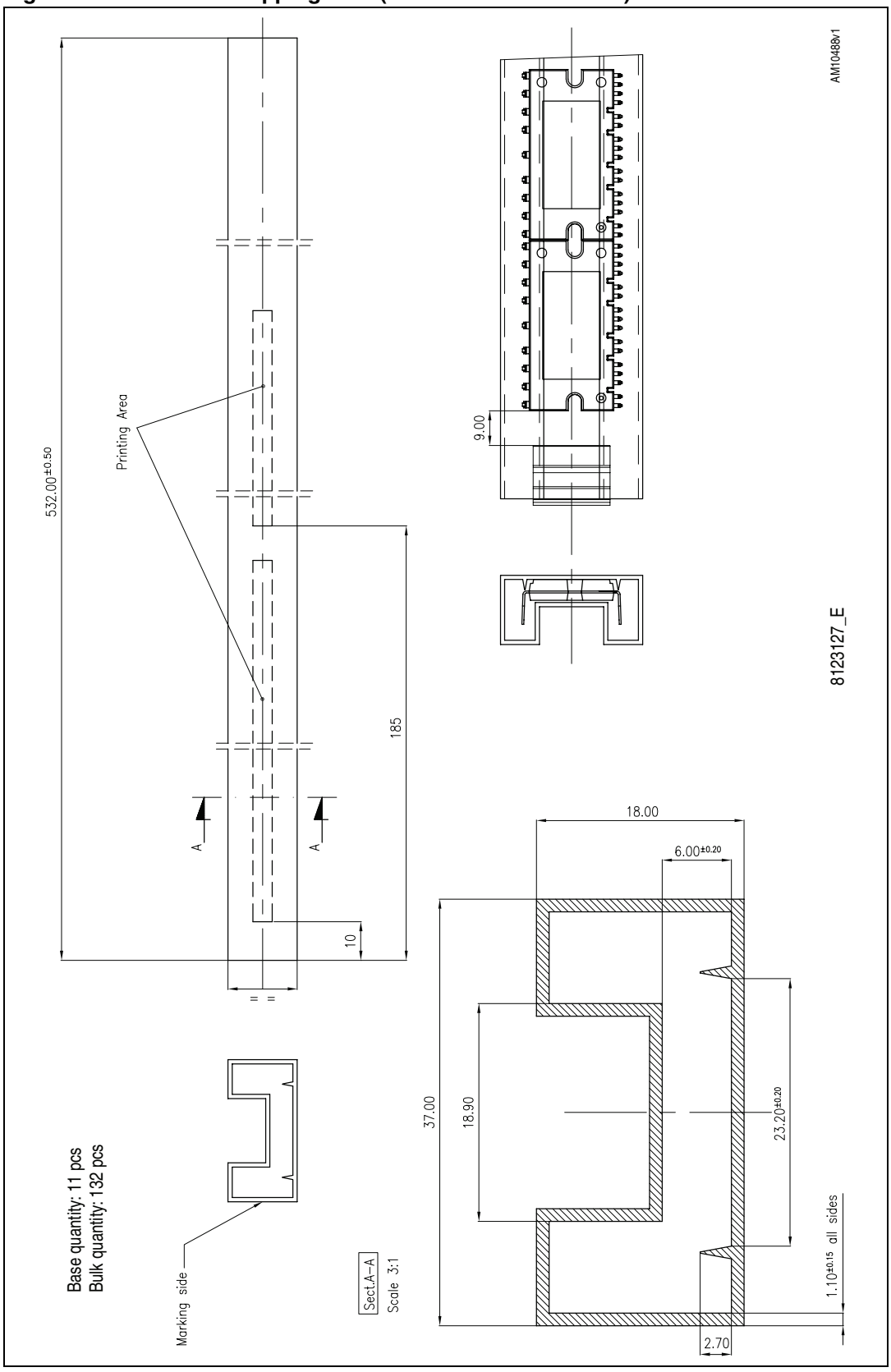
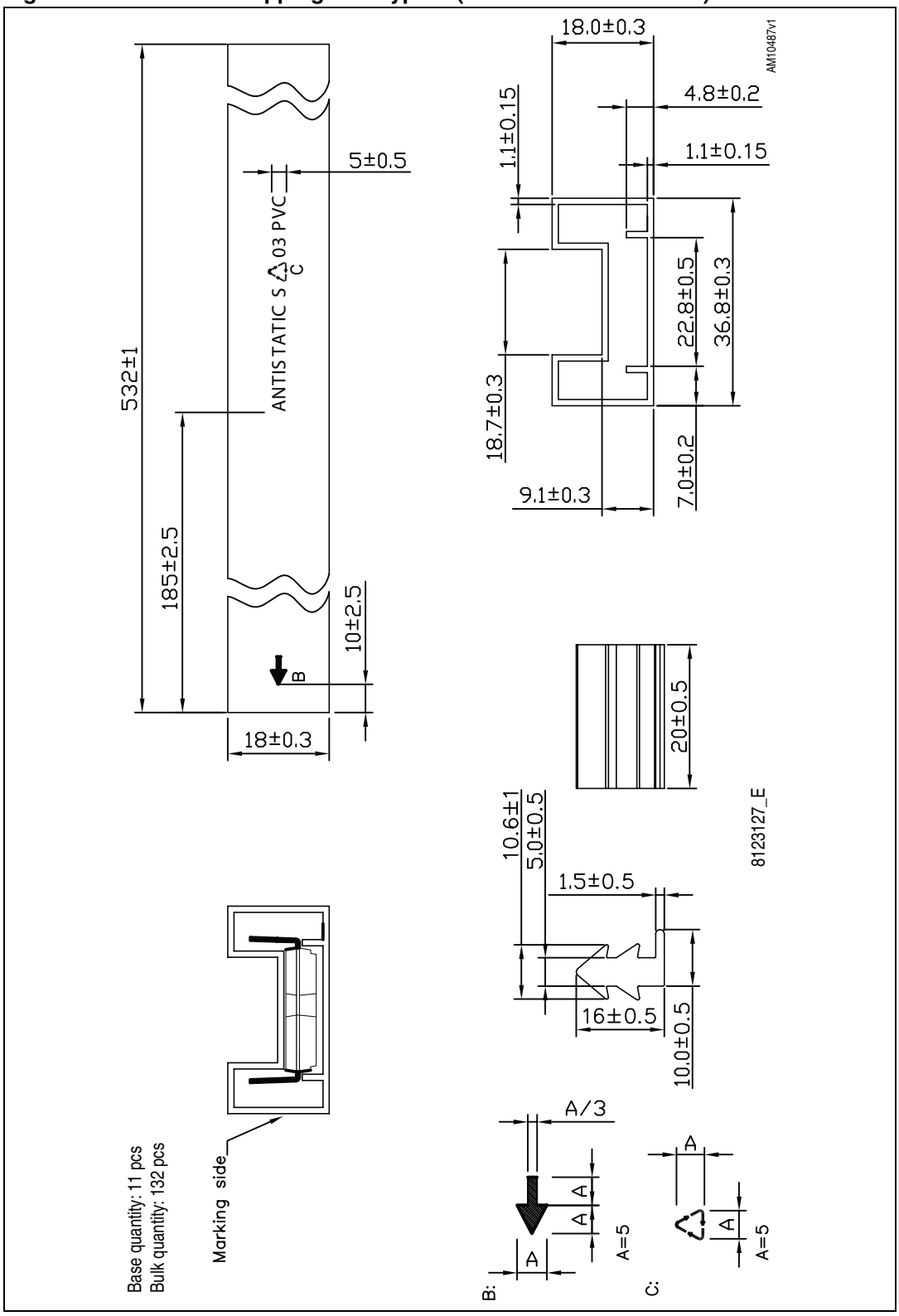


Figure 12. SDIP-22L shipping tube type B (dimensions are in mm.)



6 Revision history

Table 16. Document revision history

Date	Revision	Changes
15-Jun-2011	1	Initial release.
24-Jan-2012	2	Added: feature *UL recognition pending (in agreement to QQQX2.E81734 - Electrically-isolated semiconductor devices - component) on page 1* and *Figure 11 on page 18*. Updated: *Figure 10 on page 17*.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com