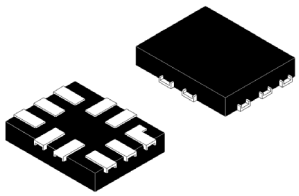
STG3682

Low voltage high bandwidth dual SPDT switch

Features

- Ultra low power dissipation:
  - I_{CC} = 0.2µA (Max.) at T_A = 85°C
- Low “ON” resistance:
  - R_{ON} = 4.6Ω (T_A = 25°C) at V_{CC} = 4.3V
  - R_{ON} = 5.8Ω (T_A = 25°C) at V_{CC} = 3.0V
- Wide operating voltage range:
  - V_{CC} (Opr) = 1.65V to 4.3V single supply
- 4.3V tolerant and 1.8V compatible threshold on digital control input at V_{CC} = 2.3V to 3.0V
- Typical bandwidth (-3dB) at 800MHz on all channels
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD performance exceeds JESD22
  - 2000-V Human body model (A114-A)
- USB (2.0) High speed (480Mbps) signal switching compliant



QFN10 (1.8mm x 1.4mm)

Description

The STG3682 is a high-speed CMOS low voltage dual analog S.P.D.T. (Single Pole Dual Throw) Switch or 2:1 Multiplexer /Demultiplexer Switch fabricated in silicon gate C^2MOS technology. It is designed to operate from 1.65V to 4.3V, making this device ideal for portable applications.

The nSEL inputs are provided to control the switch. The switch S1 is ON (they are connected to common Ports Dn) when the nSEL input is held high and OFF (high impedance state exists between the two ports) when SEL is held low; the switch S2 is ON (it is connected to common Port D) when the nSEL input is held low and OFF (high impedance state exists between the two ports) when nSEL is held high.

Additional key features are fast switching speed, Break Before Make Delay Time and Ultra Low Power Consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Order codes

Part number	Package	Packaging
STG3682QTR	QFN10 (1.8mm x 1.4mm)	Tape and reel

Contents

1 **Pin settings** 3
1.1 Pin connection 3
1.2 Pin description 3

2 **Device summary** 4

3 **Maximum rating** 5
3.1 Recommended operating conditions 5

4 **Electrical characteristics** 6

5 **Test circuits** 10

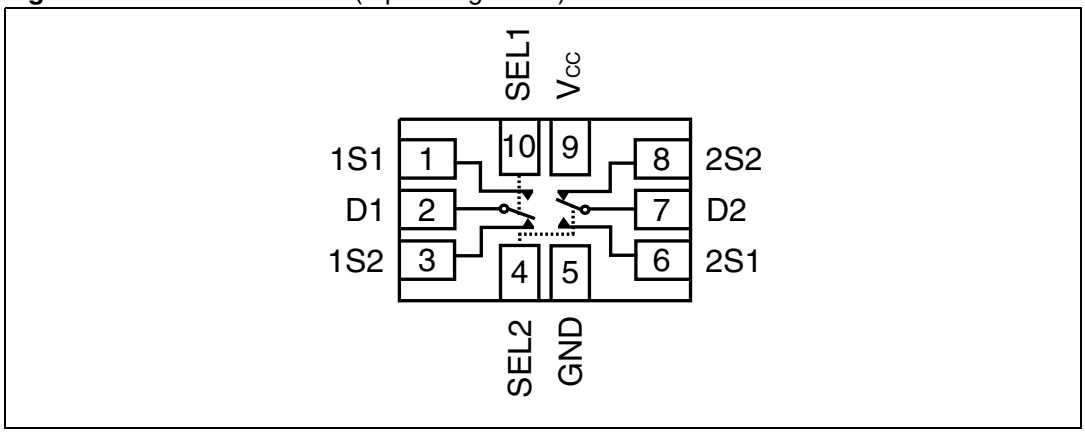
6 **Package mechanical data** 13

7 **Revision history** 18

1 Pin settings

1.1 Pin connection

Figure 1. Pin connection (top through view)



1.2 Pin description

Table 1. Pin description

Pin N°	Symbol	Name and function
1,3,6,8	1S1, 1S2, 2S1, 2S2	Independent channels
2,7	D1,D2	Common channels
10,4	SEL1,SEL2	Control
9	VCC	Possitive supply voltage
5	GND	Ground (0V)

Note: Exposed pad must be soldered to a floating plane. Do NOT connect to power or ground.

2 Device summary

Figure 2. Input equivalent circuit

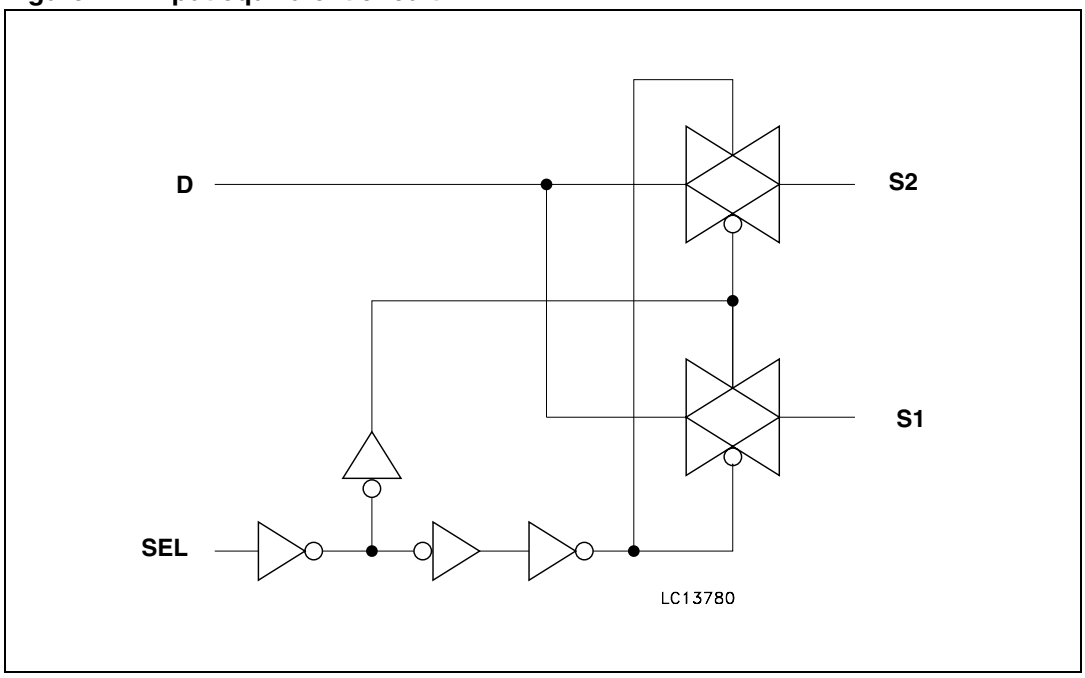


Table 2. Truth table

SEL	Switch S1	Switch S2
H	ON	OFF (1)
L	OFF (1)	ON

1. High Impedance

3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{SEL}<0V)	-50	mA
I_{IK}	DC input diode current (V_{SEL}<0V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±128	mA
I_{OP}	DC output current peak (pulse at 1ms, 10% duty cycle)	±300	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70°C (1)	1120	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec)	300	°C

1. Derate above 70ºC by 18.5mW/C

3.1 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage(1)		1.65 to 4.3	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.3	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_{CC} = 1.65V to 2.7V	0 to 20	ns/V
		V_{CC} = 3.0 to 4.3V	0 to 10	

1. Truth Table guaranteed: 1.2V to 4.3V

4 Electrical characteristics

Table 5. DC specifications

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
V_{IH}	High level input voltage	1.65 -1.95		$0.65V_{CC}$			$0.65V_{CC}$		V
		2.3-2.5		1.2			1.2		
		2.7-3.0		1.3			1.3		
		3.3-3.6		1.4			1.4		
		4.3		1.6			1.6		
V_{IL}	Low level input voltage	1.65-1.95				0.25			V
		2.3-2.5				0.25			
		2.7-3.0				0.25			
		3.3-3.6				0.30			
		4.3				0.40			
R_{PEAK}	Switch ON peak resistance	1.8	V_S = 0V to V_{CC} I_S = 8mA		12.0	16.0			Ω
		2.7			6.3	8.0			
		3.0			5.8	7.5			
		3.7			5.0	6.5			
		4.3			4.6	6.0			
R_{ON}	Switch On resistance	3.0	V_S = 3V I_S = 8mA		4.0	5.2			Ω
		3.0	V_S = 0.8V I_S = 8mA		5.0	6.5			
ΔR_{ON}	ON resistance match between channels (1)	1.8	V_S @ R_{ON} Max I_S = 8mA						Ω
		2.7							
		3.0			0.3				
		3.7							
		4.3							
R_{FLAT}	ON resistance flatness (2)	1.8	V_S = 0V to V_{CC} I_S = 8mA		6.6				Ω
		2.7			2.0				
		3.0			1.7				
		3.7			1.5				
		4.3			1.6				
I_{OFF}	OFF state leakage current (SN), (D)	4.3	V_S = 0.3 or 4V			±20		±100	nA

Table 5. DC specifications

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
I_{IN}	Input leakage current	0 to 4.3	V_{SEL} = 0 to 4.3V			±0.1		±1	µA
I_{CC}	Quiescent supply current	1.65 to 4.3	V_{SEL} = V_{CC} or GND			±0.1		±1.0	µA
I_{CCLV}	Quiescent supply current low voltage driving	4.3	$V_{1\text{-}2SEL}$, $V_{3\text{-}4SEL}$ = 1.65V		±37	±50		±100	µA
			$V_{1\text{-}2SEL}$, $V_{3\text{-}4SEL}$ = 1.80V		±33	±40		±50	
			$V_{1\text{-}2SEL}$, $V_{3\text{-}4SEL}$ = 2.60V		±11	±20		±30	

1. Note 1: ΔRon = max |mSN-nSNI, where m = 1..4 and n = 1..4, N = 1..2
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 6. AC electrical characteristics (C_L = 35pF, R_L = 50Ω, $t_r = t_f \leq$5ns)

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation delay	1.65-1.95			0.30				ns
		2.3-2.7			0.30				
		3.0-3.3			0.25				
		3.6-4.3			0.25				
t_{ON}	Turn-ON time	1.65-1.95	V_S = 0.8V		31				ns
		2.3-2.7	V_S = 1.5V		20	26		34	
		3.0-3.3			15	20		26	
		3.6-4.3			12	15		20	
t_{OFF}	Turn-OFF time	1.65-1.95	V_S = 0.8		22				ns
		2.3-2.7	V_S = 1.5V		14	18		23	
		3.0-3.3			11	14		18	
		3.6-4.3			10	13		17	
t_D	Break before make time delay	1.65-1.95	C_L = 35pF R_L = 50Ω V_S = 1.5V	1	7				ns
		2.3-2.7		1	5				
		3.0-3.3		1	4				
		3.6-4.3		1	3				
Q	Charge injection	1.65	C_L = 100pF V_{GEN} = 0V R_{GEN} = 0Ω		2.8				pC
		2.3			3.5				
		3.0			3.8				
		4.3			5.0				

Table 7. Analog switch characteristics (C_L = 5pF, R_L = 50Ω, T_A = 25°C)

Symbol	Parameter	Test Conditions		Value					Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
OIRR	OFF Isolation (1)	1.65 - 4.3	V_S = 1V_{RMS}, f = 1MHz Signal = 0 dBm		-79				dB
			V_S = 1V_{RMS}, f = 10MHz Signal = 0 dBm		-60				
Xtalk	Crosstalk	1.65 - 4.3	V_S = 1V_{RMS}, f = 1MHz Signal = 0 dBm		-78				dB
			V_S = 1V_{RMS}, f = 10MHz Signal = 0 dBm		-61				
BW	-3dB bandwidth	3.0 - 4.3	R_L = 50Ω Signal = 0dBm		800				MHz
D_G	Differential gain	3.0 - 4.3	RL = 150Ω		0.64				%
D_P	Differential phase	3.0 - 4.3	RL = 150Ω		0.1				deg
C_{IN}	Control pin input capacitance		V_{CC} = 0V		6.2				pF
C_{ON}	Sn Port capacitance when switch is enabled	3.3	f = 1MHz		22				
C_{OFF}	Sn Port capacitance when switch is disabled	3.3	f = 1MHz		21				

1. Off Isolation = 20Log10 (V_D/V_S), V_D = output. V_S = input to off switch.

Table 8. USB related AC electrical characteristics

Symbol	Parameter	Test conditions		Value					Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
$t_{SK(0)}$	Channel-to-channel skew	3.0 to 3.6	C_L=10pF		26				ps
$t_{SK(P)}$	Skew of opposite transition of the same output	3.0 to 3.6	C_L=10pF		60				ps
T_J	Total jitter	3.0 to 3.6	R_L = 50Ω, C_L= 10pF, t_R = t_F = 750ps at 480Mbps		130				ps

5 Test circuits

Figure 3. ON-Resistance

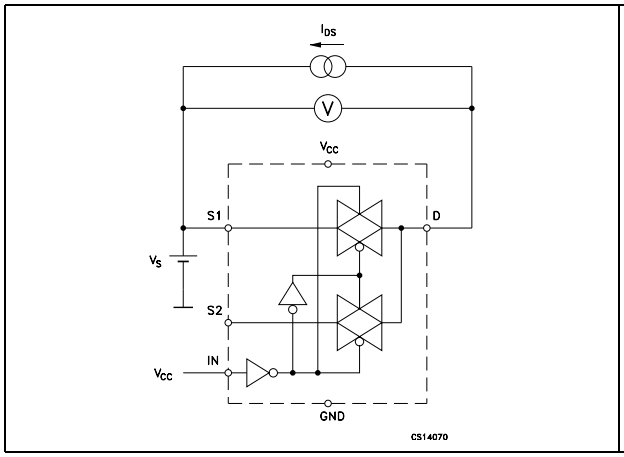


Figure 4. Bandwidth

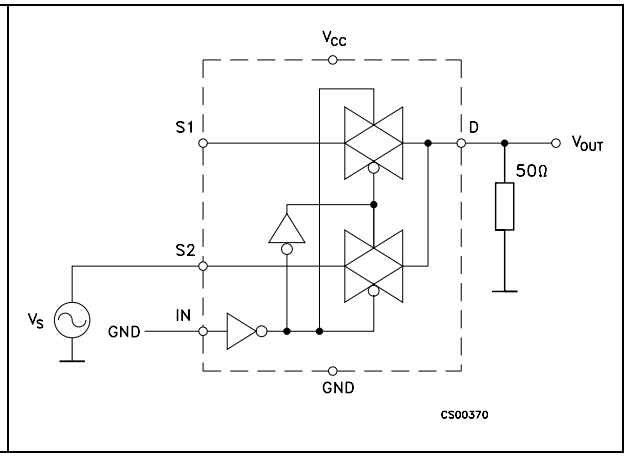


Figure 5. OFF Leakage

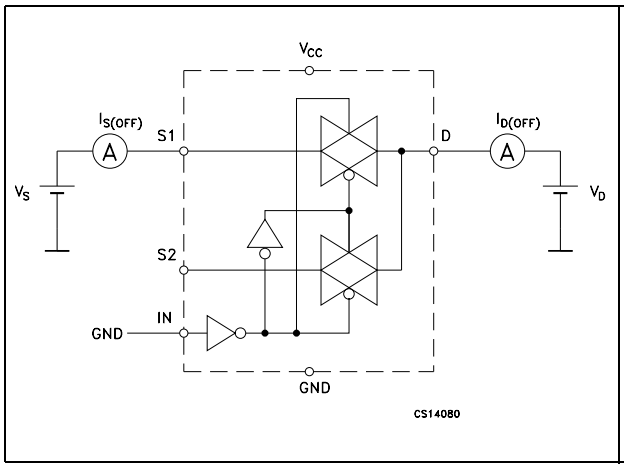


Figure 6. Channel to channel crosstalk

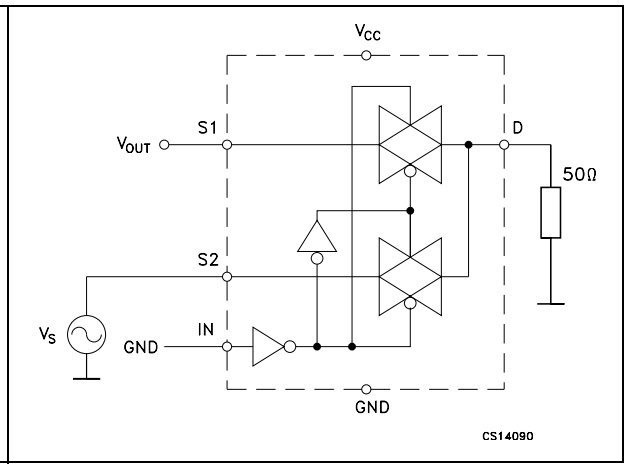


Figure 7. OFF Isolation

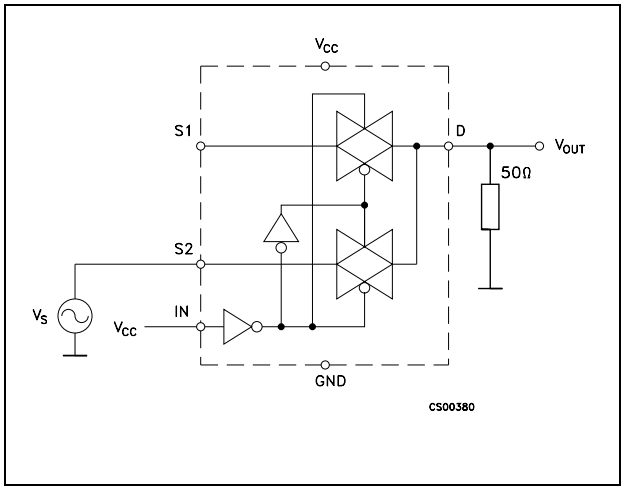
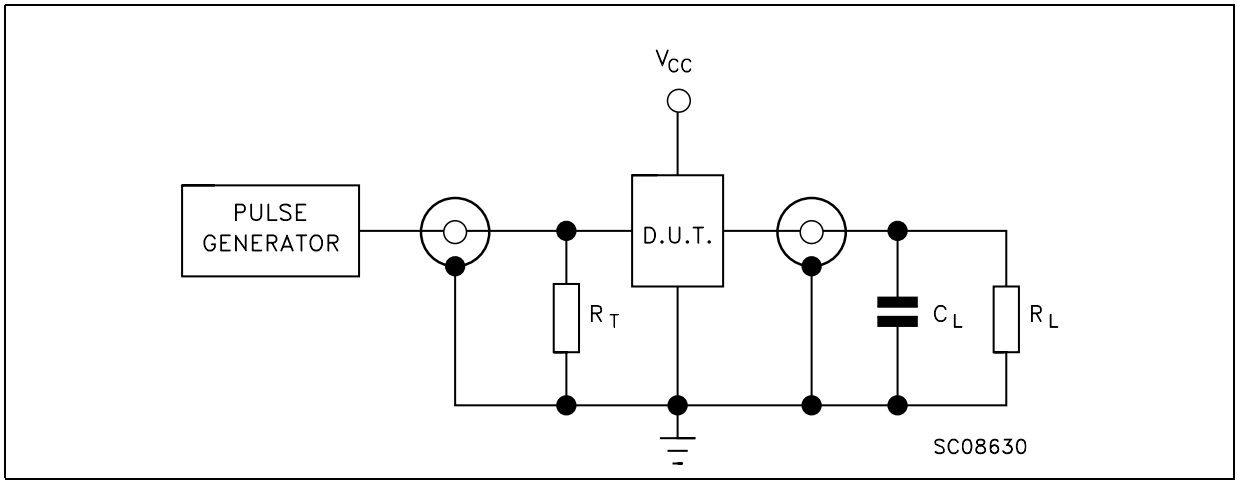


Figure 8. Test circuit



Note: 1 C_L = 5/35pF or equivalent: (includes jig capacitance)

2 R_L = 50Ω or equivalent

3 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 9. Break-before-make time delay

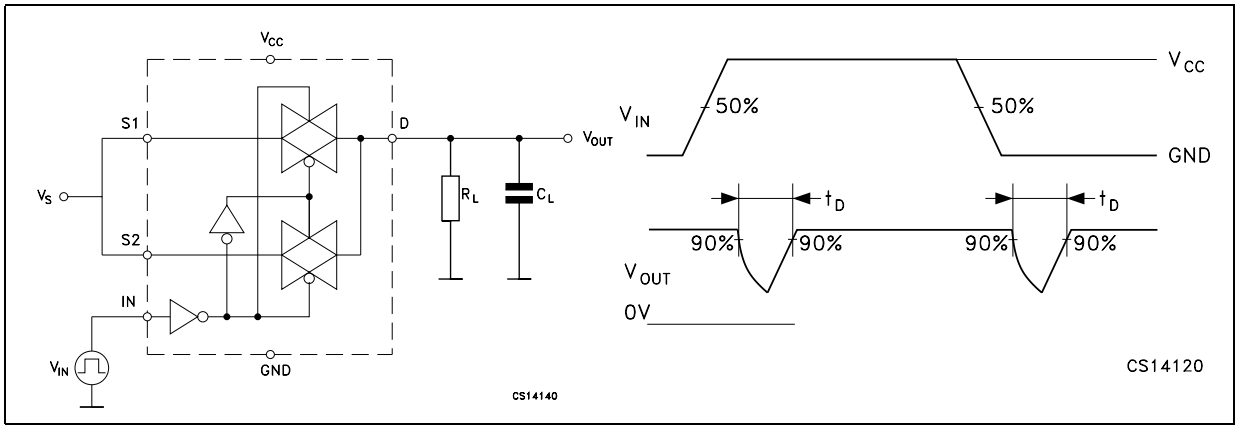


Figure 10. Switching time and charge injection
(V_{GEN} = 0V, R_{GEN} = 0Ω, R_L = 1MΩ, C_L = 100pF)

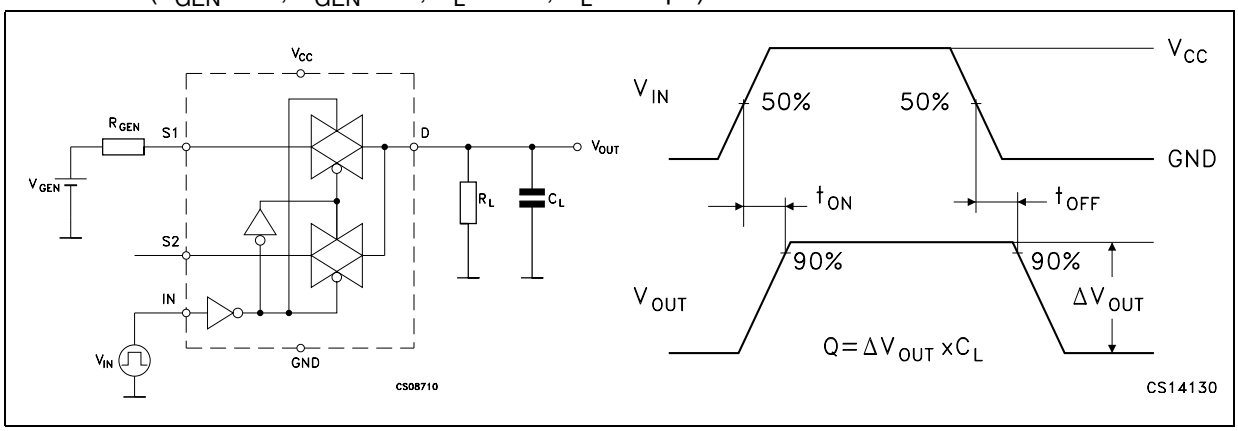
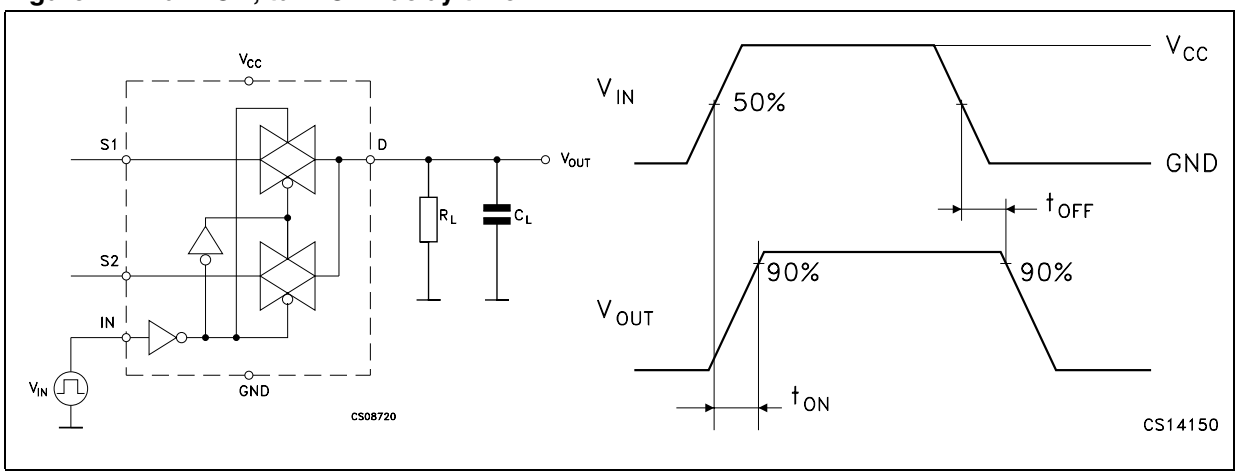


Figure 11. Turn ON, turn OFF delay time



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 9. QFN10L(1.8x1.4) Mechical data

ref.	mm			inch		
	Nom	Min	Max	Nom	Min	Max
A	0.50	0.45	0.55	0.020	0.017	0.021
A1	0.02	0	0.05	0.001	0	0.002
A3	0.127			0.005	0	0
b	0.20	0.15	0.25	0.007	0.006	0.010
D	1.80	1.70	1.90	0.070	0.066	0.074
E	1.40	1.30	1.50	0.055	0.051	0.059
e	0.40			0.015		
L	0.40	0.30	0.50	0.015	0.011	0.020

Figure 12. Package dimension

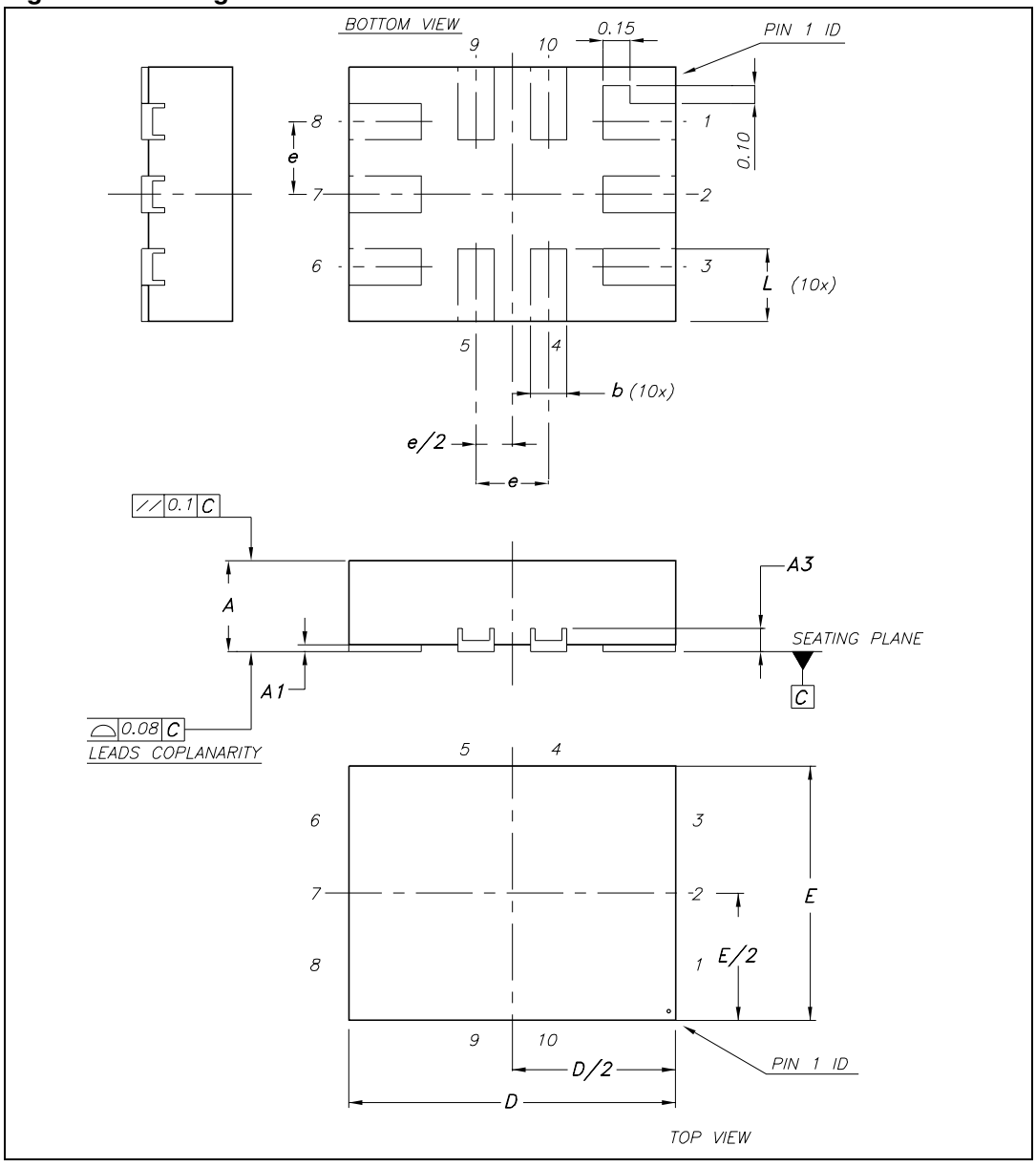


Figure 13. QFN10L(1.8x1.4) Foot print recommendation

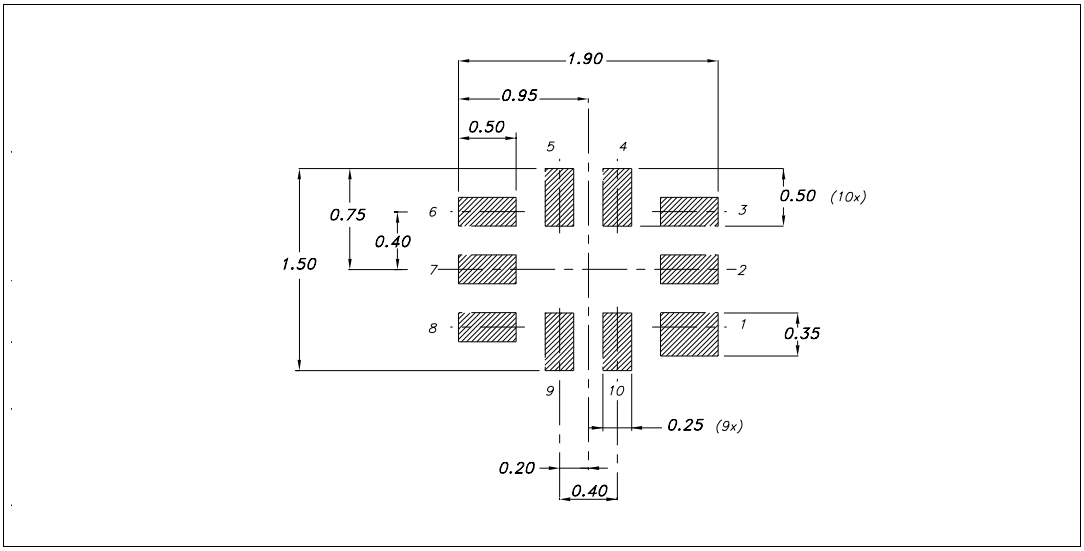


Figure 14. QFN10L(1.8x1.4) carrier type

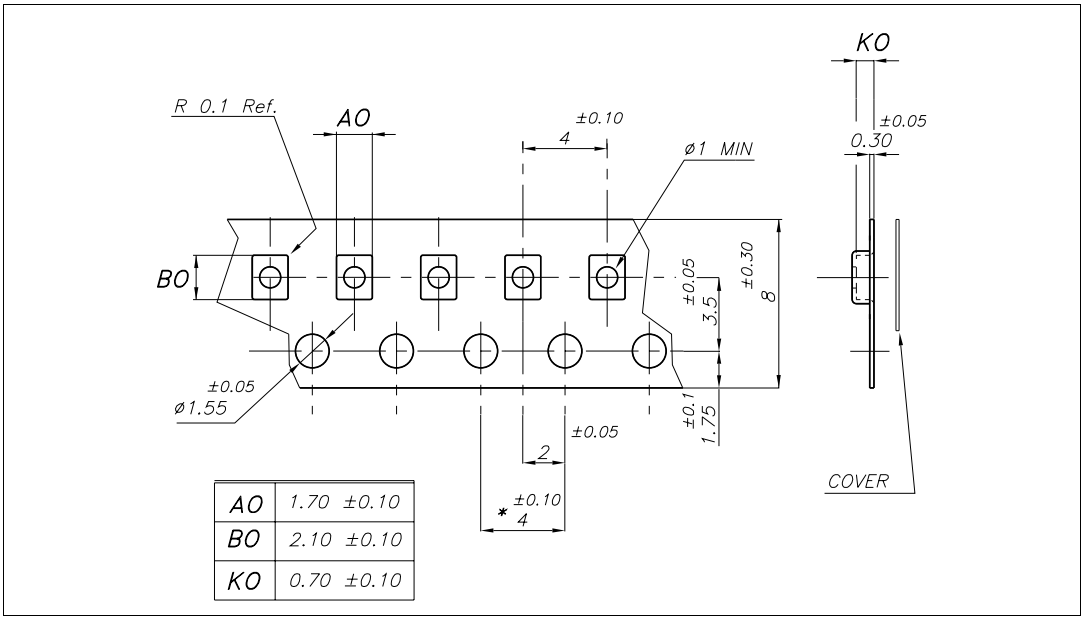


Figure 15. QFN10L(1.8x1.4) Reel information

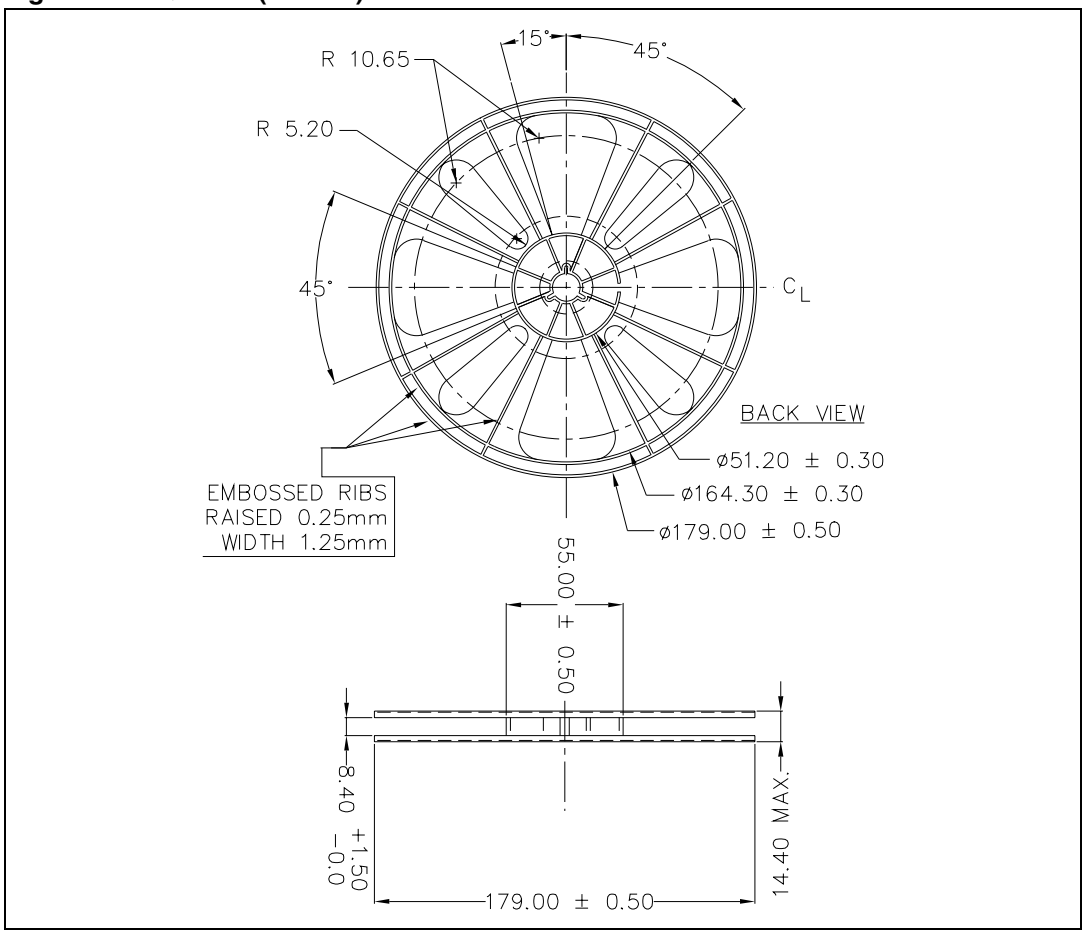
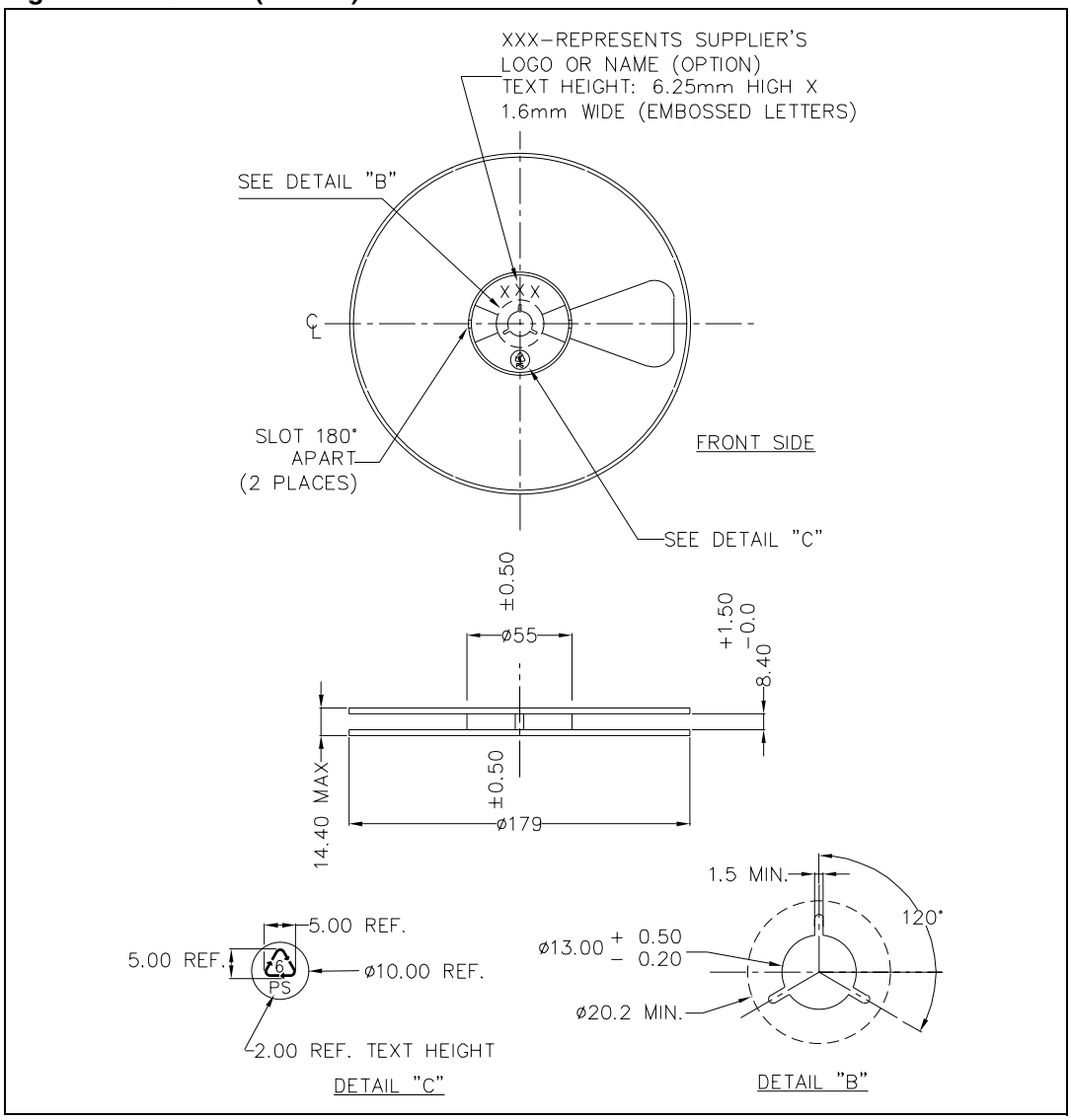


Figure 16. QFN10L(1.8x1.4) Reel information



7 Revision history

Table 10. Revision history

Date	Revision	Changes
04-Dec-2006	1	First release

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com