SGS-THOMSON MICROELECTRONICS

STG 1732, STG1764

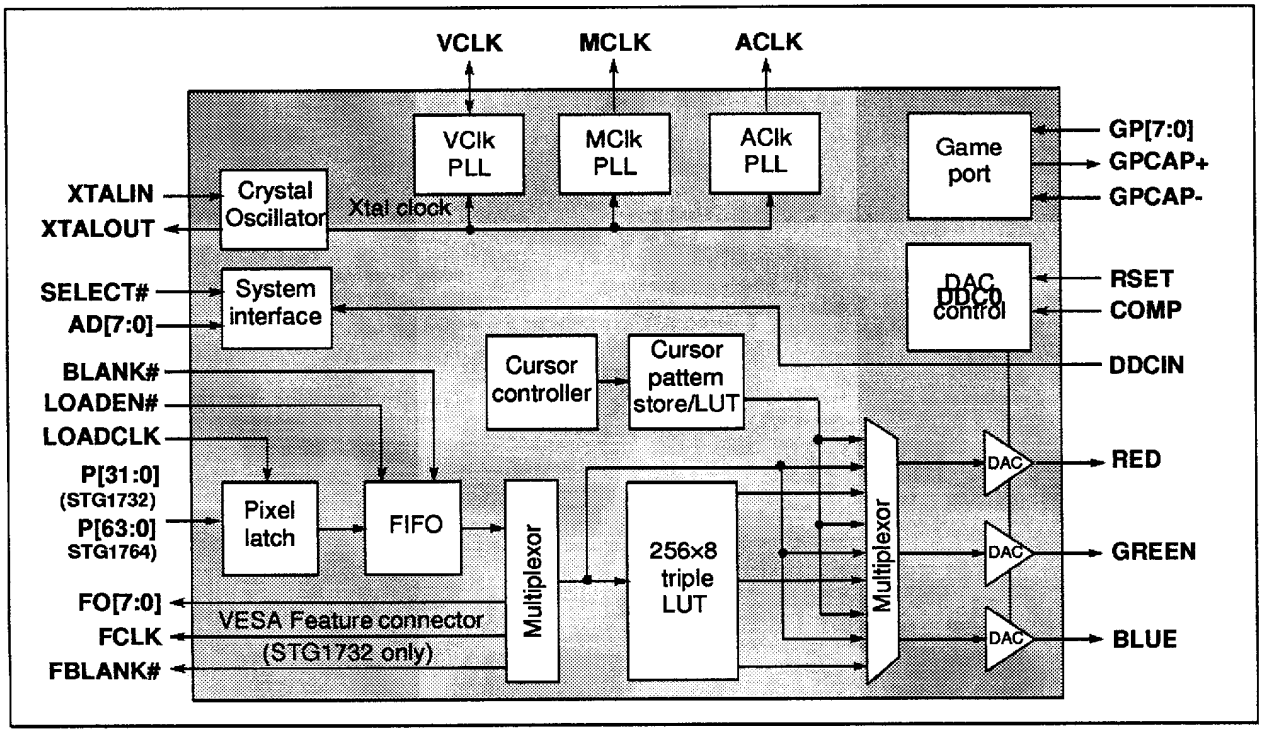
32/64-BIT MULTIMEDIA PALETTE-DACS

- Multiple Visuals Supported
  - 4 bit indexed planar
  - 8 bit indexed
  - 15 bit direct color (corrected through LUT)
  - 15 bit true color
  - 30 bit direct color (corrected through LUT)
  - 30 bit true color
- 32 x 32, 2-plane user definable hardware cursor
- 8-channel analog/digital Game Port interface
- Deep pixel input FIFO
- 3 programmable Phase Lock Loops (memory, video and audio)
- Single Crystal (12.096MHz)
- Triple 10-bit DACs
- VESA feature connector port (STG1732 only)
- Intelligent power management
- PixMix™ pixel mode switching on 15 and 30-bit visuals
- Software selectable 16, 32, or 64-bit input pixel port width (64-bit on STG1764 only)
- 8:1, 4:1, 2:1, or 1:1 multiplexed pixel port
- Video rates up to 170MHz

DESCRIPTION

The STG1732 and STG1764 are 32-bit and 64-bit pixel port Palette-DACs compatible with the architecture of the STG2000 Multimedia Accelerator. The STG1732 and STG1764 feature integrated clock synthesizers, game port and hardware cursor. For support of DRAM based graphics memory the pixel port implements a pixel FIFO buffer which may be burst filled directly from a DRAM bus.

BLOCK DIAGRAM



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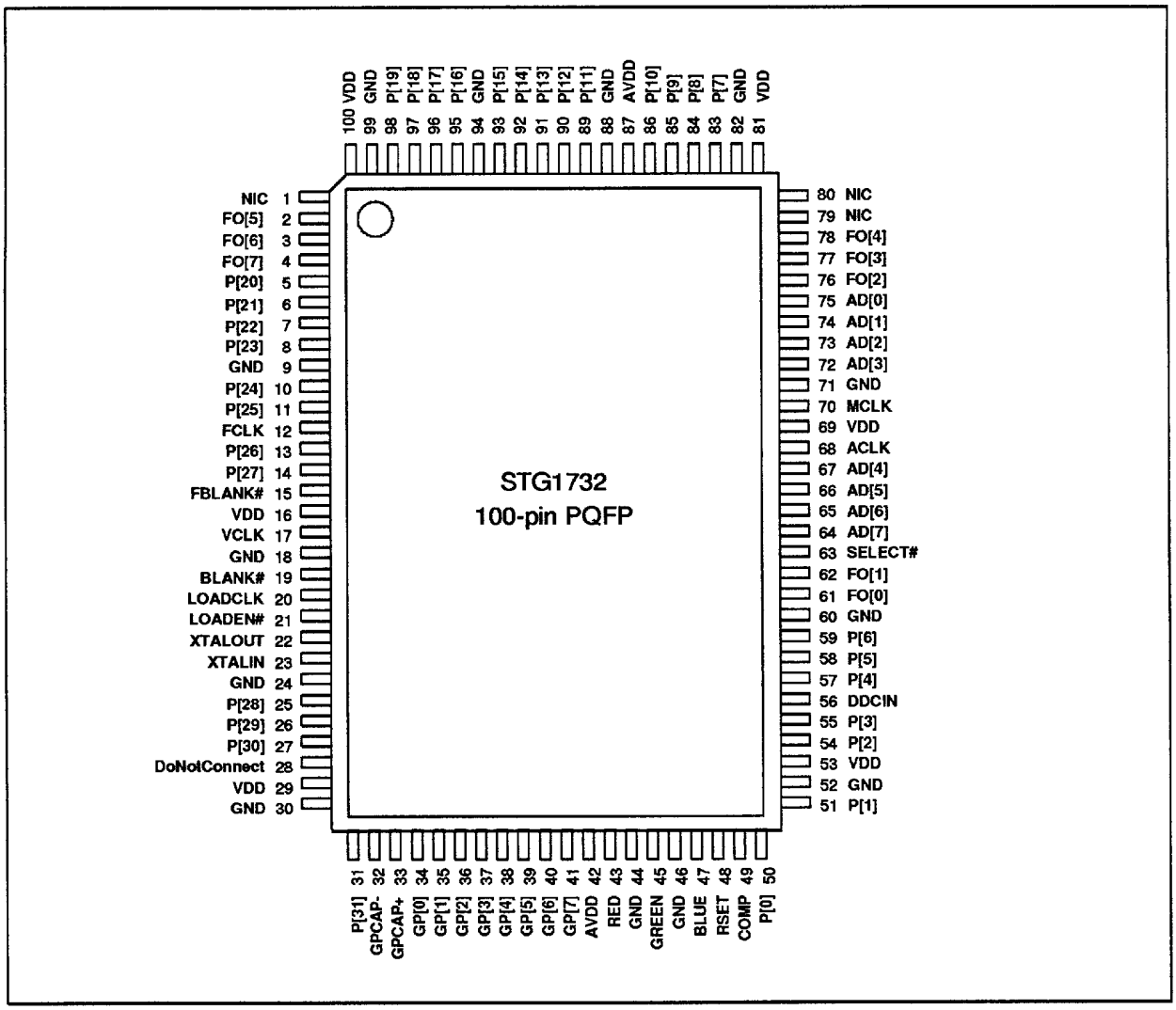
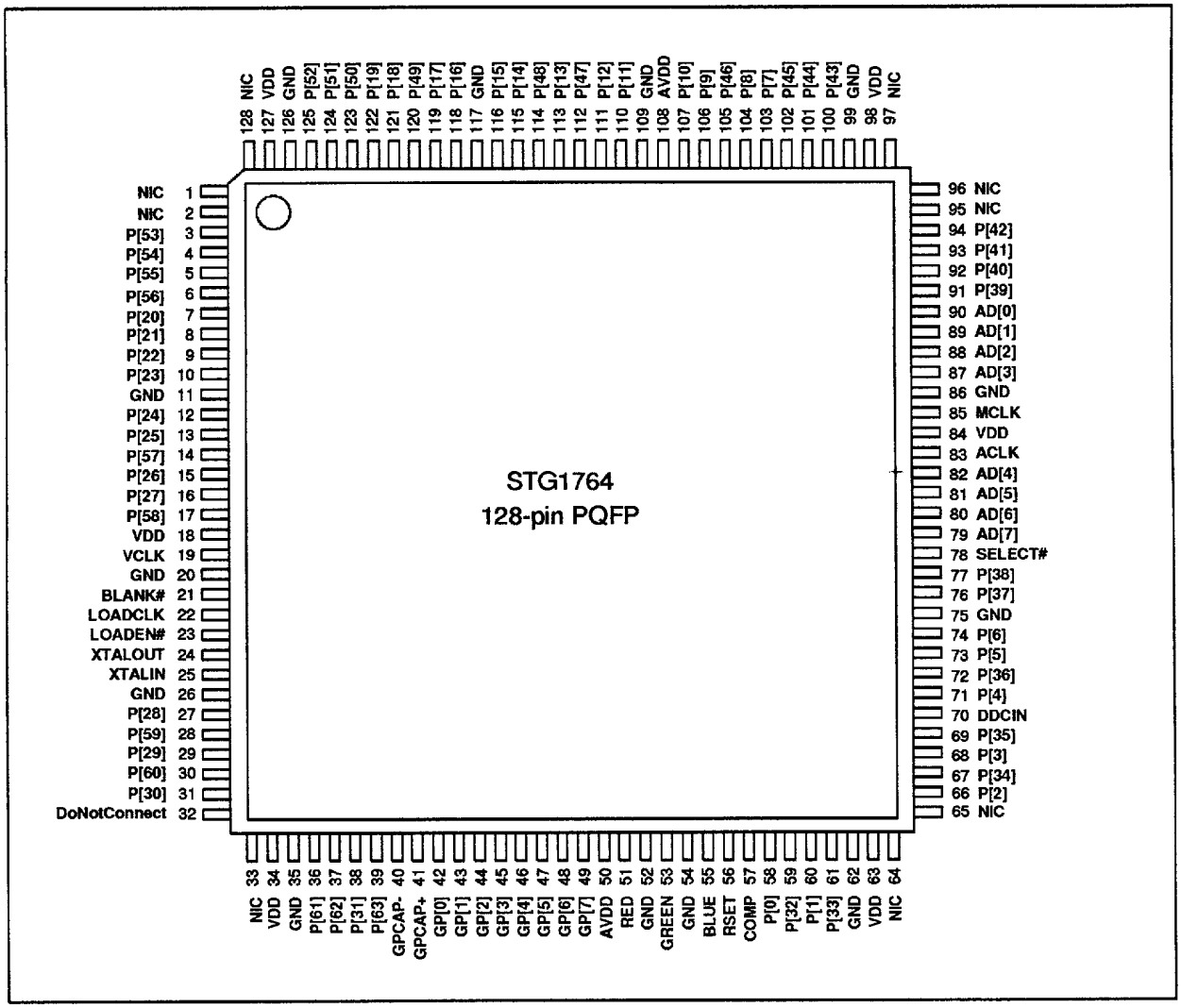
1 DEVICE PINOUTS

1.1 STG1732 PINOUT



1.2 STG1764 PINOUT



2 PIN DESCRIPTIONS

2.1 STG1732 PIXEL PORT

Signal	I/O	Description
P[31:0]	I	The pixel data word. The selected pixel mode determines how this data is interpreted.
LOADCLK	I	The rising edge of **LOADCLK** controls the sampling of pixel data on **P[31:0]** and **LOADEN#** in all modes.
LOADEN#	I	This signal qualifies the sampling of pixel data. When **LOADEN#** = 1, the data on **P[31:0]** on the rising edge of **LOADCLK** is ignored.
BLANK#	I	A '0' sampled on this pin on the rising edge of **VCLK** will, after the pipeline delay, turn the DAC outputs off. A special protocol on the **BLANK#** and **VCLK** pins enables VBLANK to reset various functions of the Palette-DAC at the start of frame flyback.

2.2 STG1764 PIXEL PORT

Signal	I/O	Description
P[63:0]	I	The pixel data word. The selected pixel mode determines how this data is interpreted.
LOADCLK	I	The rising edge of **LOADCLK** controls the sampling of pixel data on **P[63:0]** and **LOADEN#** in all modes.
LOADEN#	I	This signal qualifies the sampling of pixel data. When **LOADEN#** = 1, the data on **P[63:0]** on the rising edge of **LOADCLK** is ignored.
BLANK#	I	A '0' sampled on this pin on the rising edge of **VCLK** will, after the pipeline delay, turn the DAC outputs off. A special protocol on the **BLANK#** and **VCLK** pins enables the STG2000 Multimedia Accelerator to reset various functions of the Palette-DAC at the start of frame flyback.

2.3 VESA FEATURE CONNECTOR PORT (STG1732 ONLY)

Signal	I/O	Description
FO[7:0]	O	Feature connector pixel data outputs.
FCLK	O	The rising edge of **FCLK** validates the sampling of the **FBLANK#** signal and pixel data outputs on **FO[7:0]**.
FBLANK#	O	Feature connector blanking signal.

2.4 SYSTEM INTERFACE

Signal	I/O	Description
SELECT#	I	This signal when '0' enables write or read accesses to and from the system interface. The falling edge latches a 4-bit address from **AD[3:0]** and samples **AD[7]** to identify whether the current cycle is a write (**AD[7]** = 0) or a read operation (**AD[7]** = 1).
AD[7:0]	I/O	This 8-bit bus is used to present the address and write/read information on the falling edge of **SELECT#** and to transfer data to and from the internal registers under the control of **AD[7]**.

2.5 CLOCK SYNTHESIZERS

Signal	I/O	Description
MCLK	O	The Memory Clock synthesizer output. This signal connects to the STG2000 **MCLKx2** pin.
VCLK	I/O	The Video Clock synthesizer output. This signal is the video frequency at the DACs divided by 1, 2, 4, 8, or 16, depending on the selected mode. In systems containing multiple Palette-DACs, **VCLK** can be configured as an input, enabling slave devices to be synchronized to the master clock.
ACLK	O	The Audio Clock synthesizer output. This signal is used to provide the timing reference to the subsystem audio codec.
XTALIN	I	A 12.096MHz series resonant crystal is connected between these two points to provide the reference clock for the synthesizers, see Figure 11, page 19.
XTALOUT	O	

2.6 GAME PORT

Signal	I/O	Description
GP[7:0]	I	This 8-bit port interfaces with potentiometers up to 150KΩ and/or SPST switches, to support joysticks.
GPCAP+	-	An external capacitor is connected between **GPCAP-** and **GPCAP+** to contribute to an RC time constant, R being the variable joystick resistance. Example connections for an analog Game Port are given in Section 7.
GPCAP-	-	

2.7 DACS

Signal	I/O	Description
RED, GREEN, BLUE	O	The DAC outputs. These are designed to drive a doubly terminated 75Ω load.
COMP	-	External compensation capacitor for the DACs. This pin should be connected to AVDD via the compensation capacitor, see Figure 11, page 19.
RSET	-	A precision resistor placed between this pin and GND sets the full-scale DAC current, see Figure 11, page 19.

2.8 VESA DISPLAY DATA CHANNEL PORT

Signal	I/O	Description
DDCIN	I	This bit is provided to allow a bitstream monitor ID to be sampled on successive VSync pulses to the display monitor, see Section 5, page 13.

2.9 POWER SUPPLY

Signal	I/O	Description
AVDD	P	Analog power supply for the DACs and PLL.
VDD	P	Digital power supply.
GND	P	Common GND rail for all circuitry.
NIC	-	No internal connection; it is recommended these pins are tied to GND.

3 SYSTEM INTERFACE

The STG1732 and STG1764 system interface comprises the **SELECT#** signal and an 8-bit multiplexed address and data bus, **AD[7:0]**.

SELECT# connects to pin **CS_DAC#** and **AD[7:0]** connect directly to pins **MDB[15:8]** of the STG2000 Multimedia Accelerator. The system interface pins are described in Section 2.4, page 5.

The register interface of the STG1732 and STG1764 is based on the standard SGS-THOMSON Palette-DAC interface. Four direct access registers are supported.

3.1 SYSTEM INTERFACE REGISTERS

Tables showing register contents include a column indicating if register fields are readable **(R)** *or writable* **(W)** *and the initial power-on or soft reset value of the field* **(I)**. *'-' indicates not readable / writable,* X *indicates not reset.*

Table 1. STG1732 and STG1764 registers

Address (AD[3:0])	Register function
0000	Write Palette Address Register
0001	Color Data Register
0010	Pixel Mask Register[1]
0011	Read Palette Address Register
0100-0111	Reserved

NOTE

1 The Pixel Mask Register has a power-on and soft reset value of 0xFF

Writing to the Palette

Table 2. Write Palette Address Register 0x0

Bits	Function	R W I
7:0	Current Write Address	R W X

Table 3. Color Data Register 0x1

Bits	Function	R W I
7:0	R, G or B color value	R W X

To update the palette the required palette address is first written to the Write Palette Address Register. The R, G and B color values are then written in succession to the Color Data Register following which the Write Palette Address Register is automatically incremented.

Reading from the Palette

Table 4. Read Palette Address Register 0x3

Bits	Function	R W I
7:0	Current Read Address	R[1] W X

NOTE

1 In VGA modes the STG2000 replaces these bits with a pair of bits indicating the last Palette Address Register written to. In non-VGA modes the current read address can be read from the STG1732 or STG1764.

To read from the palette the required palette address is first written to the Read Palette Address Register. The R, G and B color values are then read in succession from the Color Data Register following which the Read Palette Address Register is automatically incremented.

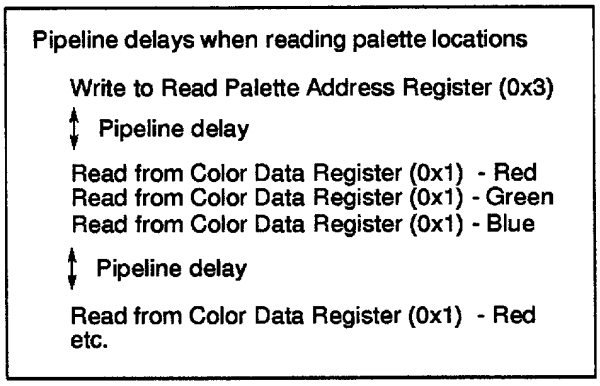
Pixel Mask Register (0x2)

This register provides a bitwise AND function of the Palette Address (8-bit indexed pixels only).

Pipelined registers

The registers used in accessing palette (LUT) locations are affected by read cycle pipeline delays. The position of these delays in a read sequence is shown in Figure 1.

Figure 1. Occurrence of pipeline delays



3.2 SYSTEM INTERFACE TIMING SPECIFICATION

Accesses to the pipelined RAMs - including the 256 location LUT must adhere to the cycle times tCP and tRP as specified below.

Figure 2. System interface read/write cycle

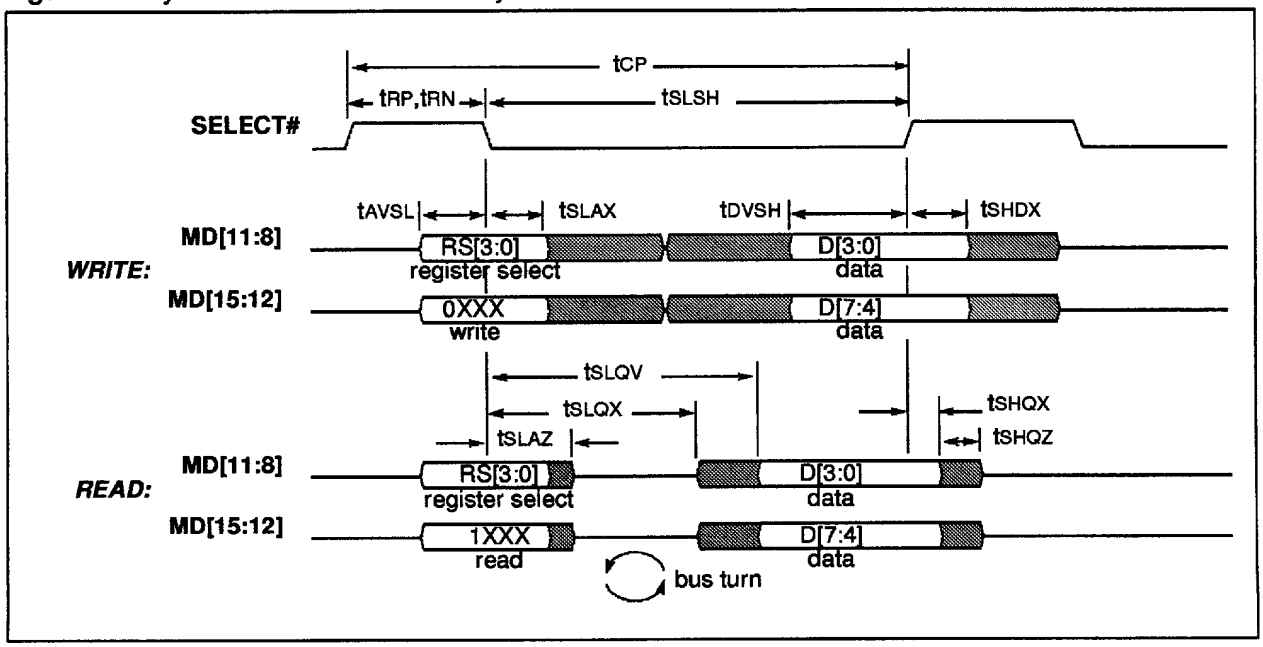


Table 5. System interface timing parameters

Symbol	Parameter	Min.	Max.	Unit	Notes
tCP	**SELECT#** pipeline cycle time	2xTDCLK+10		ns	Write cycle, 1
tRP	**SELECT#** pipeline recovery time	6xTDCLK		ns	Read cycle, 1, 2
tRN	**SELECT#** non-pipeline recovery time	30		ns	
tSLSH	**SELECT#** pulse time	50		ns	
tAVSL	Address setup time	8		ns	
tSLAX	Address hold time	0		ns	
tDVSH	Write data setup time	8		ns	Write cycle
tSHDX	Write data hold time	0		ns	Write cycle
tSLAZ	Address tri-state time		10	ns	Read cycle
tSLQX	Output turn-on delay	10		ns	Read cycle, 3
tSLQV	Read access time		40	ns	Read cycle, 4
tSHQX	Read data hold time	5		ns	Read cycle, 3
tSHQZ	Output turn-off delay		20	ns	Read cycle

NOTES

1 DCLK is the pixel dot clock period (undivided VCLK)

2 Access recovery times are specified as the time before a particular access, because the worst case access (reading a RED palette color value) can occur after either reading a BLUE palette color value or after writing to the Address Register (read mode). The occurrence of pipeline delays when reading palette locations is described on page 7.

3 Output load on **AD[7:0]** = 25pF

4 Output load on **AD[7:0]** = 80pF

4 PIXEL PORT

4.1 VISUALS (BITS PER PIXEL MODES) SUPPORTED

The following descriptions apply to 16 and 32-bit pixel ports. For a 64-bit port, data on pins **P[31:0]** is interpreted as described below for a 32-bit port. Data on pins **P[63:32]** is identical in format and displayed sequentially to that on **P[31:0]**.

4-bit indexed (VGA planar) visual

In the 4-bit indexed planar visual each 32-bit word contains four pixel planes. Each plane contains one bit of each of eight indexed color pixels (p0 to p7 in display order). The least significant bit of each pixel is contained in plane 0, the most significant bit in plane 3. This visual is not supported at pixel rates above 135MHz.

Use of pixel input pins (32-bit port)																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
plane 3								plane 2								plane 1								plane 0							
p0	p1	p2	p3	p4	p5	p6	p7	p0	p1	p2	p3	p4	p5	p6	p7	p0	p1	p2	p3	p4	p5	p6	p7	p0	p1	p2	p3	p4	p5	p6	p7

For a 16-bit pixel port a 32-bit word is accumulated over two cycles as shown below.

Use of pixel input pins (16-bit port, 2nd cycle)																Use of pixel input pins (16-bit port, 1st cycle)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
plane 3								plane 2								plane 1								plane 0							
p0	p1	p2	p3	p4	p5	p6	p7	p0	p1	p2	p3	p4	p5	p6	p7	p0	p1	p2	p3	p4	p5	p6	p7	p0	p1	p2	p3	p4	p5	p6	p7

8-bit indexed visual

In the 8-bit indexed visual each 32-bit word contains four 8-bit indexed color pixels, each comprising bits b[7:0] as shown below. For a 16-bit port, pixels 0 and 1 are sampled on the 1st cycle and pixels 2 and 3 on the 2nd cycle of the port.

Use of pixel input pins (32-bit port)																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
pixel 3								pixel 2								pixel 1								pixel 0							
b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0

16-bit visual

In 16-bit visuals, when PixMix mode is enabled, the PixMix bit (bit 15 of each pixel) selects whether pixel data bypasses the LUT, to feed the DACs directly, or indirectly, through the LUT, to allow pseudo color indexing or gamma correction to be applied. If PixMix mode is not enabled then the bypass mode will always be selected, and the LUT powered down. The LUT must therefore be reprogrammed if PixMix is re-enabled.

For a 16-bit port a single pixel is sampled for each cycle, for a 32-bit port two pixels are sampled for each cycle as shown below. This table indicates the effect of the PixMix bit when PixMix mode is enabled.

Indexed or direct color mode	Use of pixel input pins (32-bit port)																													
	Pixel 1																Pixel 0													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Direct	0	Red gamma							Green gamma					Blue gamma			0	Red gamma						Green gamma				Blue gamma			
X	1	Red bypass							Green bypass					Blue bypass			1	Red bypass						Green bypass				Blue bypass			
Indexed	0	X	X	X	X	X	X	X	Indexed color								0	X	X	X	X	X	X	X	Indexed color						

32-bit visual

In 32-bit visuals, when PixMix mode is enabled, the PixMix bit (bit 31 of each pixel) selects whether pixel data bypasses the LUT, to feed the DACs directly, or indirectly, through the LUT, to allow pseudo color indexing or gamma correction to be applied. If PixMix mode is not enabled then the bypass mode will always be selected, and the LUT powered down. The LUT must therefore be reprogrammed if PixMix is re-enabled.

For a 16-bit port bits [15:0] of each pixel are sampled on the first cycle and bits [31:16] on the second cycle of the port. This table indicates the effect of the PixMix bit when PixMix mode is enabled.

Indexed or direct color mode	Use of pixel input pins (32-bit port)																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Direct	0	X	Red gamma								X	X	Green gamma								X	X	Blue gamma							X	X
X	1	X	Red bypass										Green bypass										Blue bypass								
Indexed	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Indexed color						

Pixel mapping to the LUT and DACs

In the 16-bit visual, with gamma correction selected, each 5-bit color value is expanded to an 8-bit LUT address as shown below:

Color value [4:0]	4	3	2	1	0	4	3	2
LUT input [7:0]	7	6	5	4	3	2	1	0

In indexed color and gamma corrected visuals, the LUT outputs an 8-bit color value mapping to the 10-bit DAC input as shown below:

Color value [7:0]	7	6	5	4	3	2	1	0	7	6
DAC input [9:0]	9	8	7	6	5	4	3	2	1	0

In the direct (LUT bypass) modes each 5-bit color value maps to the 10-bit DAC as shown below:

Color value [4:0]	4	3	2	1	0	4	3	2	1	0
DAC input [9:0]	9	8	7	6	5	4	3	2	1	0

Support for visuals at different pixel rates

Visual (bpp)	Pixel rate (MHz)			
	50	100	135	170*
4	✓	✓	✓	
8	✓	✓	✓	•
16	✓	✓	•	•
32	✓	•		

NOTES

✓ = Supported by STG1732 and STG1764

• = Supported by STG1764

* STG1764-170, preliminary only

4.2 PIXEL PORT TIMING SPECIFICATION

Figure 3. Pixel port timing diagram

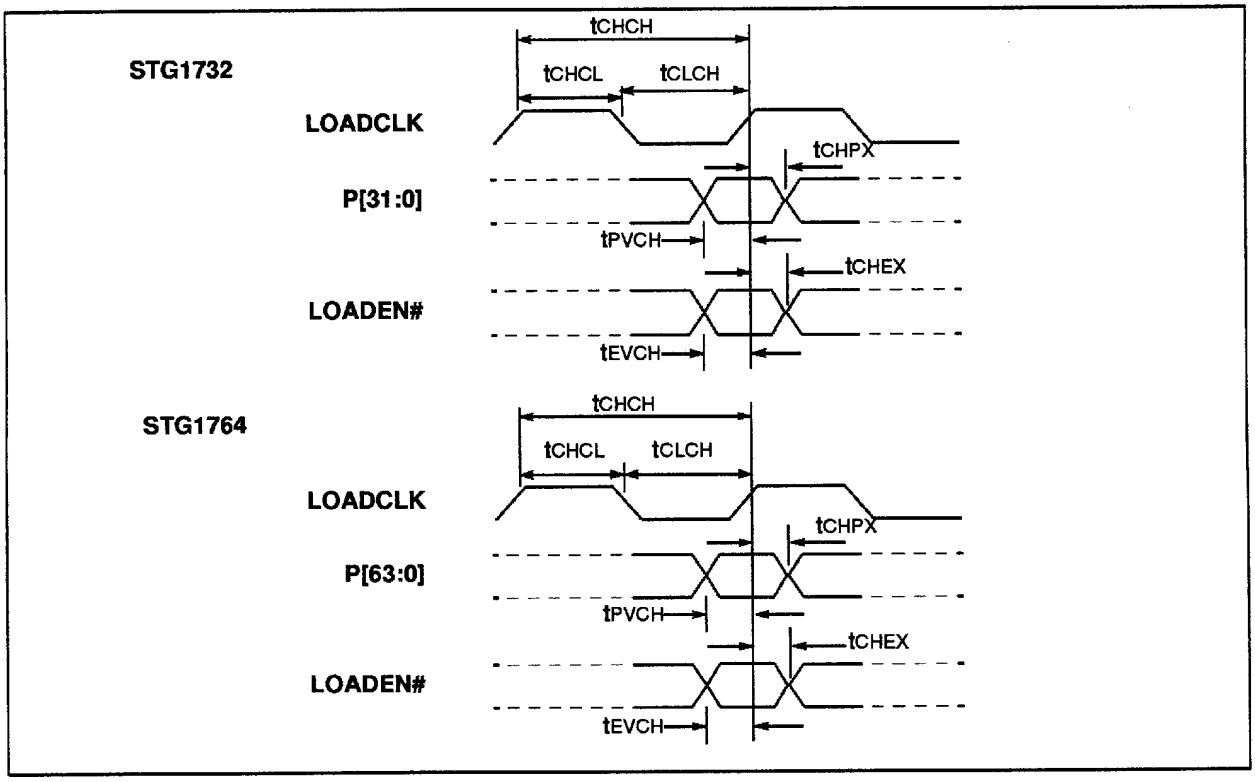


Table 6. Pixel port timing parameters

Symbol	Parameter	Min.	Max.	Units	Notes
tCHCH	**LOADCLK** period	20.0		ns	
tCLCH	**LOADCLK** low time	6.0		ns	
tCHCL	**LOADCLK** high time	5.0		ns	
tPVCH	Pixel data set-up time	3.0		ns	
tCHPX	Pixel data hold time	1.0		ns	
tEVCH	**LOADEN#** set-up time	3.0		ns	
tCHEX	**LOADEN#** hold time	1.0		ns	

VBLANK detection

The start of frame flyback (VBLANK) is detected through a special protocol on the **BLANK#** pin. This protocol, shown in Figure 4, comprises the sequence 010, sampled on the **BLANK#** pin on successive rising edges of VCLK.

When VBLANK is detected the internal FIFO pointers and cursor position are reset. These actions can also be triggered through the VBLANK Control Register in extended register space.

Figure 4. VBLANK detection protocol

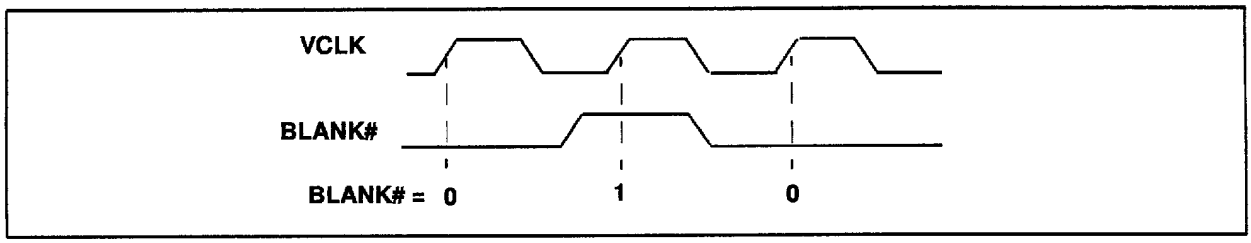


Figure 5. VBLANK detection timing diagram

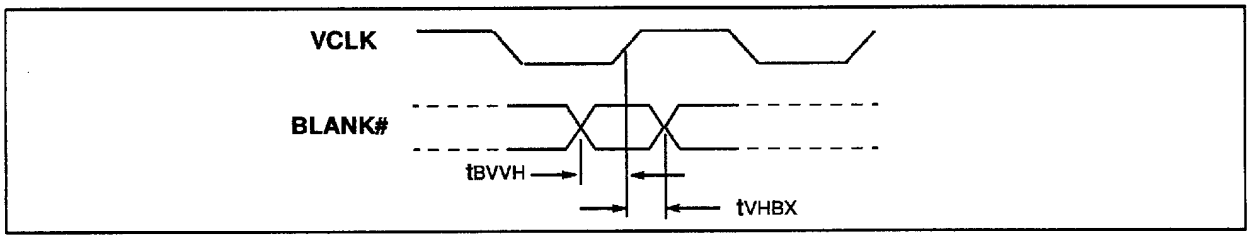


Table 7. VBlank detection timing parameters

Symbol	Parameter	Min.	Max.	Units	Notes
tBVVH	**BLANK#** set-up time	2.0		ns	
tVHBX	**BLANK#** hold time	2.0		ns	

4.3 PIXEL FIFO

The FIFO provides buffering of pixel data latched in on **LOADCLK**, ready to be read out into the pixel pipeline under control of **BLANK#**. The internal core word width of the FIFO is 128 bits and therefore pixels are accumulated until 128 bits have been latched (2x64bits, 4x32 bits, or 8x16-bit pixel port load cycles) and then written into the core. The FIFO write is pipelined, so that to be able to read (display) all the required pixels from the FIFO, some extra 'dummy' **LOADCLK** cycles must be performed, after building the last complete 128-bit word, to flush the required data to be written into the core. A different number of extra **LOADCLK** cycles is required for each pixel port width mode, as shown in Table 8.

Table 8. Extra LOADCLK cycles required by the pixel FIFO

Pixel port width	16	32	64
Extra **LOADCLK** cycles required	5	3	2

Reading data from the FIFO is controlled by **BLANK#** and occurs in 32-bit words. This places a limitation on the resolution of the line length that **BLANK#** can control. If the VCLK is configured to be a divided ratio of the pixel dot clock then the resolution is further reduced by a factor of the divide ratio. Table 9 shows the number of pixels of which the displayed line length must be a multiple of for each of the visuals, for a VCLK divide ratio of 1.

Table 9. Permitted line length multiples

Visual (width)	4	8	16	32
Number of pixels that the line length must be a multiple of	8	4	2	1

5 SAMPLING OF DDCIN

Figure 6. **DDCIN** timing diagram

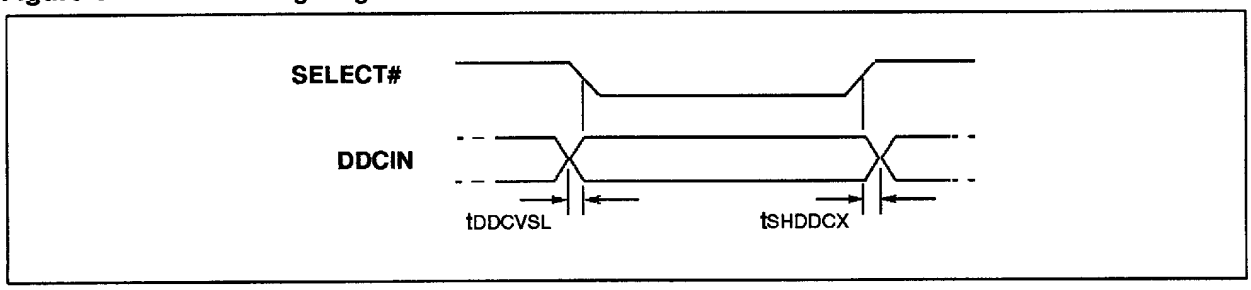


Table 10. DDCIN timing parameters

Symbol	Parameter	Min.	Max.	Units	Notes
tDDCVSL	**DDCIN** setup time	0		ns	
tSHDDCX	**DDCIN** hold time	0		ns	

6 VESA FEATURE CONNECTOR PORT (STG1732 ONLY)

Figure 7. VESA Feature connector port timing diagram

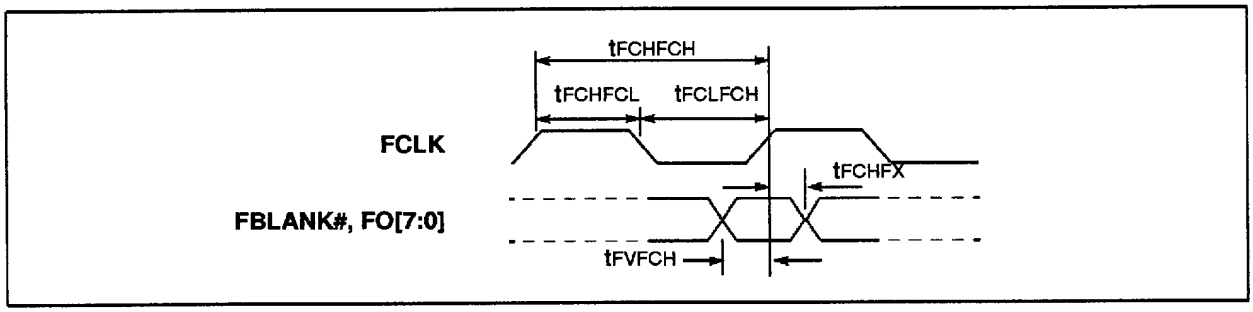


Table 11. VESA Feature connector port timing parameters

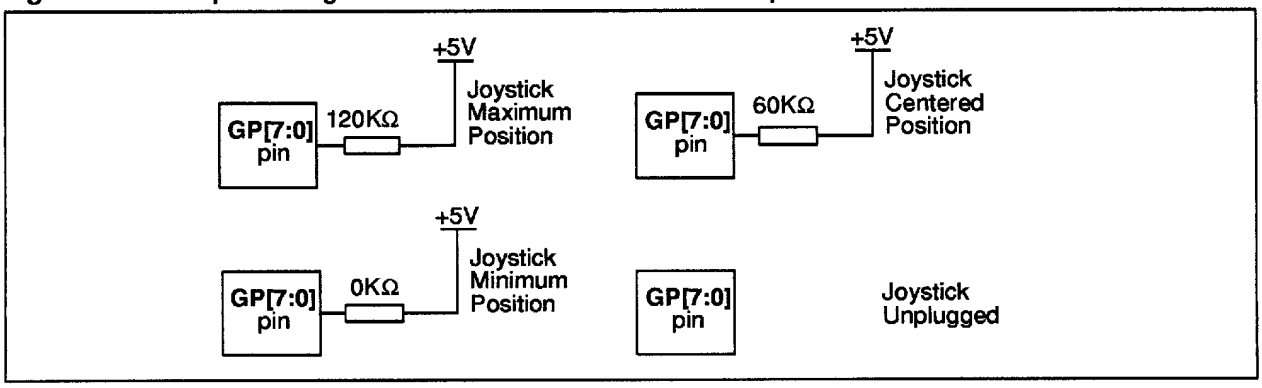
Symbol	Parameter	Min.	Max.	Units	Notes
tFCHFCH	**FCLK** period	35.0		ns	
tFCLFCH	**FCLK** low time	14.0		ns	
tFCHFCL	**FCLK** high time	14.0		ns	
tFVFCH	Pixel data set-up time	10.0		ns	
tFCHFX	Pixel data hold time	2.0		ns	

7 GAME PORT

The Game Port supports a high level of flexibility and accuracy when interfacing to external devices such as joysticks, throttle, pedals and/or switches. An external peripheral connected to any of the eight channels is capable of being measured as either an analog or digital device.

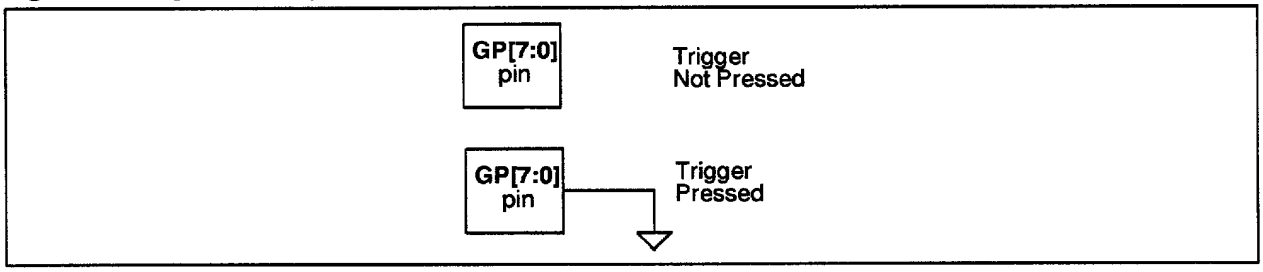
When a channel is an analog input, its pin is connected to the variable part of a joystick, throttle or pedals which are connected to VDD through a potentiometer (see Section 8.3). As the position changes, the potentiometer varies between its maximum resistance and zero ohms. An external capacitor connected between **GPCAP+** and **GPCAP-** is charged to VDD through the potentiometer. The varying resistance contributes to a variation in the RC time constant of the circuit.

Figure 8. Example analog Game Port conditions for a 120KΩ potentiometer



When a channel is a digital input, its pin is connected to a SPST switch to ground. If the trigger is not pressed the pin will be left floating. If the trigger is pressed the pin will be shorted to ground.

Figure 9. Digital Game port conditions



The 'Joystick Unplugged' and the 'Trigger Not Pressed' conditions are the same. When in this state the pin will be considered a digital input, since it is definitely known that a potentiometer is not connected, even though it is not known if a digital peripheral is attached.

The game port is accessible through two mechanisms known as the Real Mode Game Port or the High-Precision Game Port.

7.1 REAL MODE GAME PORT

The STG1732 and STG1764 Real Mode Game Port emulates and provides compatibility with the existing IBM Game Port standard. In this case the Palette-DAC Real Mode Game Port Register is mapped into I/O location 0x201 by the STG2000. This register allows existing DOS game applications to run with the STG2000 Multimedia Accelerator without modification. Details of the Real Mode Game Port Register are given in the STG2000 Datasheet [2].

7.2 HIGH-PRECISION GAME PORT

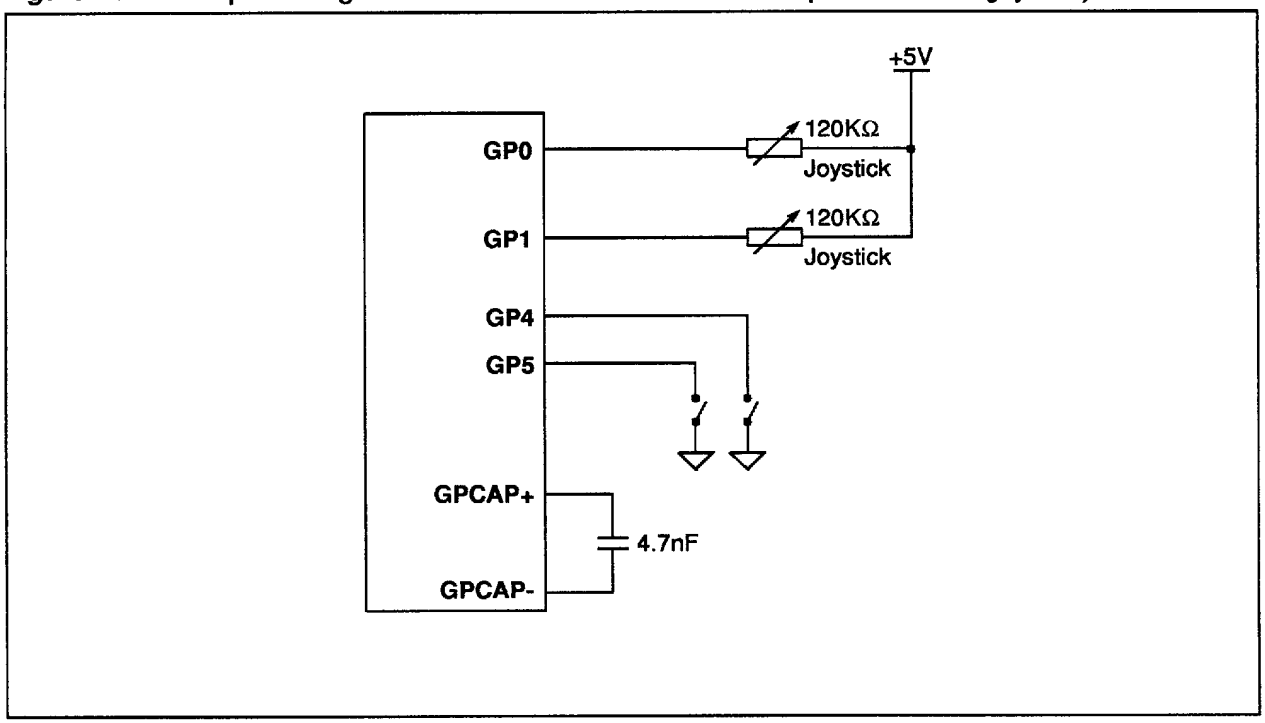
The High-Precision Game Port is accessed through the STG2000 programming interface (see [3] for details). It releases from the CPU the task of timing and polling the analog channels of the Real Mode Game Port. The capture logic in the Game Port continually updates all channels (up to 8 analog registers) with

new values. Additional flexibility is provided by allowing any of the 8 channels to be used for analog or digital measurement. The Game Port detects which channels are analog and which are digital and reports this to the application. The relevant values for each channel can then be read.

When the Game Port is capturing the analog input from a selected **GP[7:0]** pin, the crystal clock is used as a timing reference (see Section 8.3, page 17).

7.3 ANALOG GAME PORT CONNECTIONS

Figure 10. Example analog Game Port connections for a 120KΩ potentiometer (joystick)



8 ELECTRICAL SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Min.	Max.	Units	Notes
VDD/AVDD	DC supply voltage		7.0	V	
	Voltage on input and output pins	GND-1.0	VDD+0.5	V	
TS	Storage temperature (ambient)	-55	125	°C	
TA	Temperature under bias	0	85	°C	
PDmax	Power dissipation		2.5	W	
	Analog output current (per output)		45	mA	
	DC digital output current (per output)		25	mA	

NOTES

1 Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2 For thermal management information on the STG1732 and STG1764 refer to [6].

8.2 DAC CHARACTERISTICS

Parameter	Min.	Typ.	Max.	Units	Notes
Resolution		10		bits	
DAC operating frequency			135	MHz	1
DAC operating frequency			170	MHz	2
White relative to Black current	16.74	17.62	18.50	mA	3
DAC to DAC matching		±1	±2.5	%	3,5
Integral linearity		±0.5	±1.5	LSB_8	3,4,9
Differential linearity		±0.25	±1	LSB_8	3,4,9
DAC output voltage			1.2	V	3
DAC output impedance		20		kΩ	
Risetime (black to white level)		1	3	ns	3,6,7
Settling time (black to white)			7.4	ns	1,3,6,8
Settling time (black to white)			5.9	ns	2,3,6,8
Glitch energy		50	100	pVs	3,6
Comparator trip voltage	280	335	420	mV	
Comparator settling time			100	µs	
Internal Vref voltage		1.235		V	
Internal Vref voltage accuracy		±3	±5	%	

NOTES

1 STG1732-135 and STG 1764-135
2 STG1764-170, preliminary only
3 VREF = 1.235V, RSET = 147Ω
4 LSB_8 = 1 LSB of 8-bit resolution DAC
5 About the midpoint of the distribution of the three DACs
6 37.5ohm, 30pF load
7 10% to 90%
8 Settling to within 2% of full scale deflection
9 Monotonicity guaranteed

8.3 GAMEPORT CHARACTERISTICS

Symbol	Parameter	Min	Typ.	Max	Units	Notes
RPT_GP	Analog capture repeatability	8	10		bits	1, 2, 3
VT_GP	Analog comparator switching threshold	0.4VDD	0.5VDD	0.6VDD	V	
IIL_GP	**GP[7:0]** input leakage current			±100	µA	
IPULLUP_GP	**GP[7:0]** digital mode pullup current	0.15		5	mA	
VIH_GP	**GP[7:0]** digital mode VIH	0.8VDD			V	
VIL_GP	**GP[7:0]** digital mode VIL			0.2VDD	V	
ICHARGE_ GPCAP	**GPCAP+/GPCAP-** capacitor charge current	0.5		5	mA	
IDISCHARGE_ GPCAP	**GPCAP+/GPCAP-** capacitor discharge current	0.2		2	mA	

NOTES

1 Each analog channel returns 16 bits, which may be read by software, of which 13-bits are updated by the Game Port capture logic.

2 Crystal clock frequency = 12.096MHz (each channel captured once per frame at 90Hz).

3 **GPCAP+/GPCAP-** capacitor = 4.7nF

8.4 FREQUENCY SYNTHESIS CHARACTERISTICS

Parameter	Min	Typ.	Max	Units	Notes
XTALIN crystal frequency range	4		20	MHz	
Internal VCO frequency	64		135	MHz	1
Internal VCO frequency	64		170	MHz	2
VCLK output frequency			50	MHz	3
MCLK output frequency			100	MHz	3
ACLK output frequency			25	MHz	3
Synthesizer lock time			500	µs	
VCLK, MCLK, ACLK rise time			4	ns	3
VCLK, MCLK, ACLK fall time			4	ns	3
VCLK, MCLK, ACLK mark space ratio		50		%	

NOTES

1 STG1732-135 and STG1764-135

2 STG1764-170, preliminary only

3 C_{load}=15pF

8.5 VCLK INPUT CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
tVHVH	**VCLK** input frequency	20			ns	1
tVLVH	**VCLK** low time	7			ns	
tVHVL	**VCLK** high time	5			ns	

NOTE

1 **VCLK** assigned as an input

8.6 PIPELINE DELAYS

Parameter	Typ.	Notes
Pipeline delay (4bpp, 8bpp)	(3×VCLK periods) + (16×Pixel clock periods)+7ns	1
Pipeline delay (16bpp, 32bpp)	(3×VCLK periods) + (15×Pixel clock periods)+7ns	1

NOTE

1 Measured from the rising edge of VCLK (with **BLANK#** sampled high) to the occurrence of the related pixel data on the DACs.

8.7 DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
IDD	Average power supply current (135MHz)		270	340	mA	1
IDD	Average power supply current (170MHz)		310	390	mA	2
IDDP	Average power supply current (palette RAM powered down, 135MHz)		220		mA	1
IDDP	Average power supply current (palette RAM powered down, 170MHz)		260		mA	2
IDDS	Average power supply current (sleep mode)		60		mA	3
IIN	Digital input current			±100	µA	
IOZ	Off state digital output current			±50	µA	
VOH	Output logic 1 level	2.4			V	4
VOL	Output logic 0 level			0.4	V	4

NOTES

1 Typ. and max. figures both measured at 135MHz, with differences due to VDD, pixel mode and part to part variations.
2 Typ. and max. figures both measured at 170MHz, with differences due to VDD, pixel mode and part to part variations. (STG1764-170, preliminary only)
3 Typ. figure measured at 35MHz, with differences due to VDD, pixel mode and part to part variations.
4 I_{load}=5mA

8.8 OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
VDD	Positive supply voltage	4.75	5.0	5.25	V	1
VIH	Input logic 1 voltage	2.2		VDD+0.5	V	
VIL	Input logic 0 voltage	-0.5		0.8	V	
TA	Ambient operating temperature		25	70	°C	

NOTE

1 These voltage ranges apply equally for AVDD and VDD.

9 ANALOG INTERFACE

Figure 11. Recommended circuit

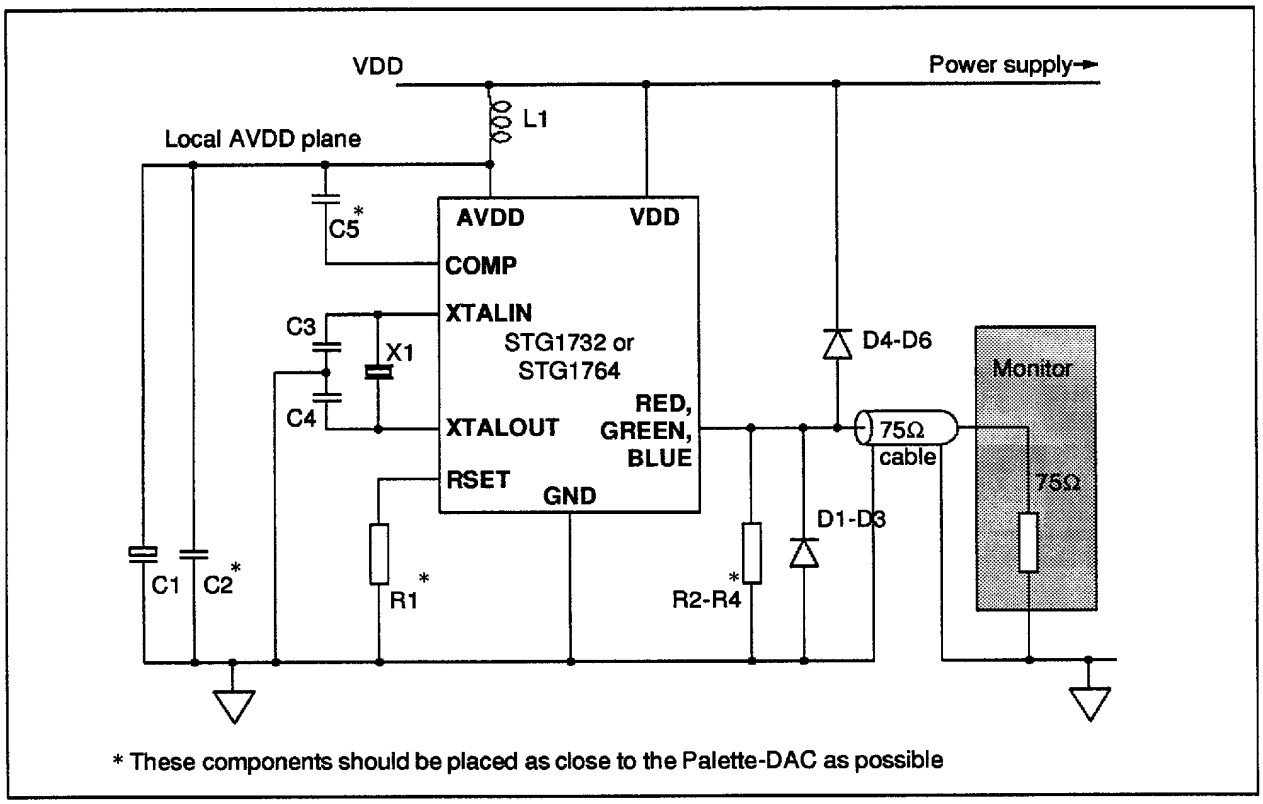


Table 12. Table of parts for recommended circuit (Figure 11)

Part number	Value	Description
C1	22µF	tantulum capacitor
C2	100nF	surface mount capacitor
C3-C4	22pF	surface mount capacitor
C5	10nF	surface mount capacitor
R1	147Ω	1% resistor
R2-R4	75Ω	1% resistor
D1-D6	1N4148	protection diodes
L1	1µH	inductor
X1	12.096MHz	series resonant crystal

10 PACKAGE DIMENSIONS

Table 13. STG1732 100-pin Plastic Quad Flat Pack dimensions

REF. (see Figure 12)	CONTROL DIMENSIONS - mm			ALTERNATIVE DIMENSIONS - inches			NOTES
	MIN	NOM	MAX	MIN	NOM	MAX	
A	-	-	3.400	-	-	0.134	
A1	0.100	-	-	0.004	-	-	
A2	2.540	2.800	3.050	0.096	0.110	0.120	
B	0.220	-	0.380	0.009	-	0.015	
C	0.130	-	0.230	0.005	-	0.009	
D	22.950	-	24.150	0.904	-	0.951	
D1	19.900	20.000	20.100	0.783	0.787	0.791	
D3	-	18.850	-	-	0.742	-	REF
E	16.950	-	18.150	0.667	-	0.715	
E1	13.900	14.000	14.100	0.547	0.551	0.555	
E3	-	12.350	-	-	0.486	-	REF
e	-	0.650	-	-	0.026	-	BSC
G	-	-	0.100	-	-	0.004	
θ	0°	-	7°	0°	-	7°	
L	0.650	0.800	0.950	0.026	0.031	0.037	
Zd	-	0.580	-	-	0.023	-	REF
Ze	-	0.830	-	-	0.033	-	REF

NOTES

1 Lead finish to be 85 Sn/15 Pb solder plate.

2 Maximum lead displacement from the notional center line will be no greater than ± 0.125 mm.

Figure 12. STG1732 100-pin Plastic Quad Flat Pack dimension reference

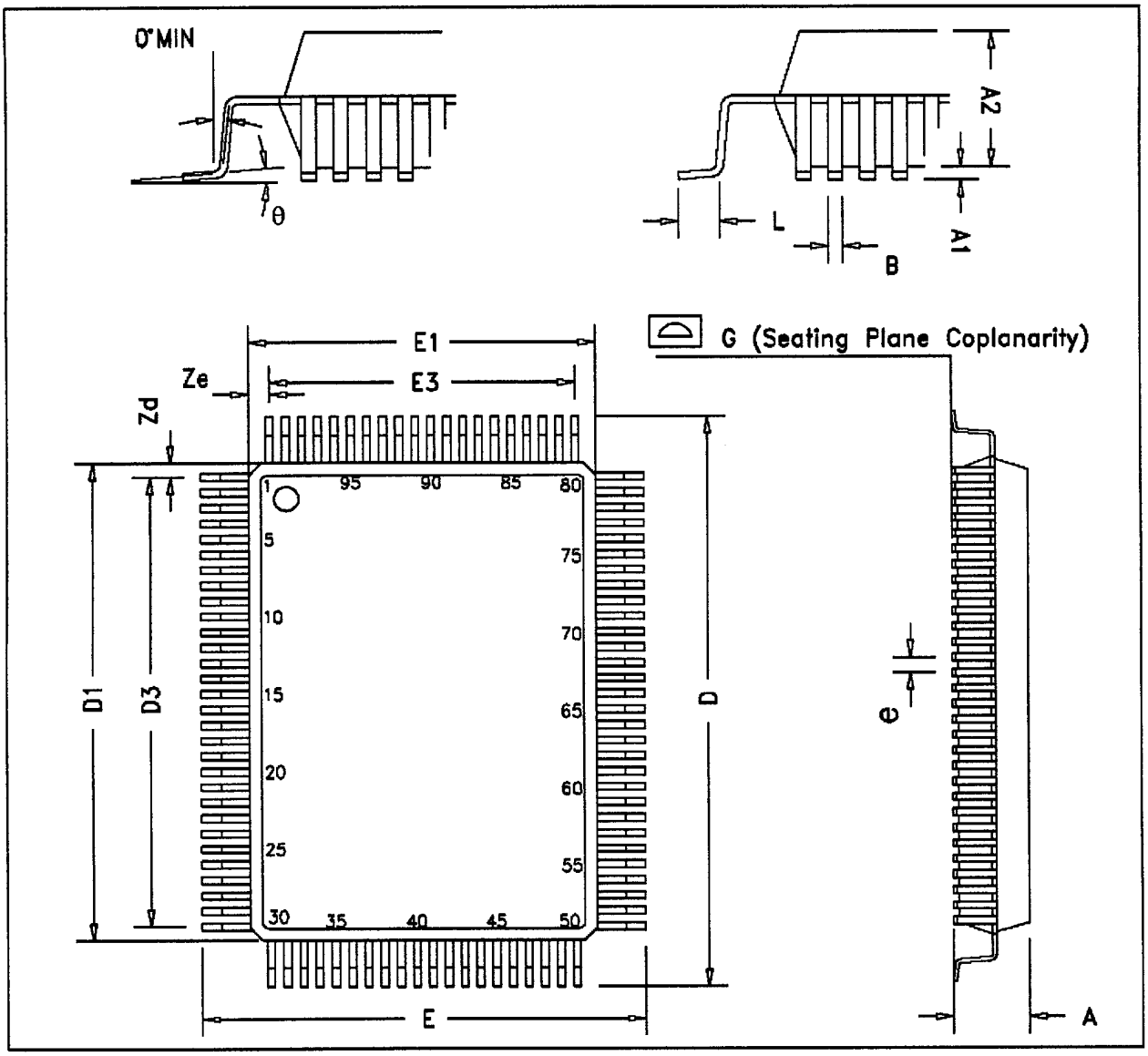


Table 14. STG1764 128-pin Plastic Quad Flat Pack dimensions

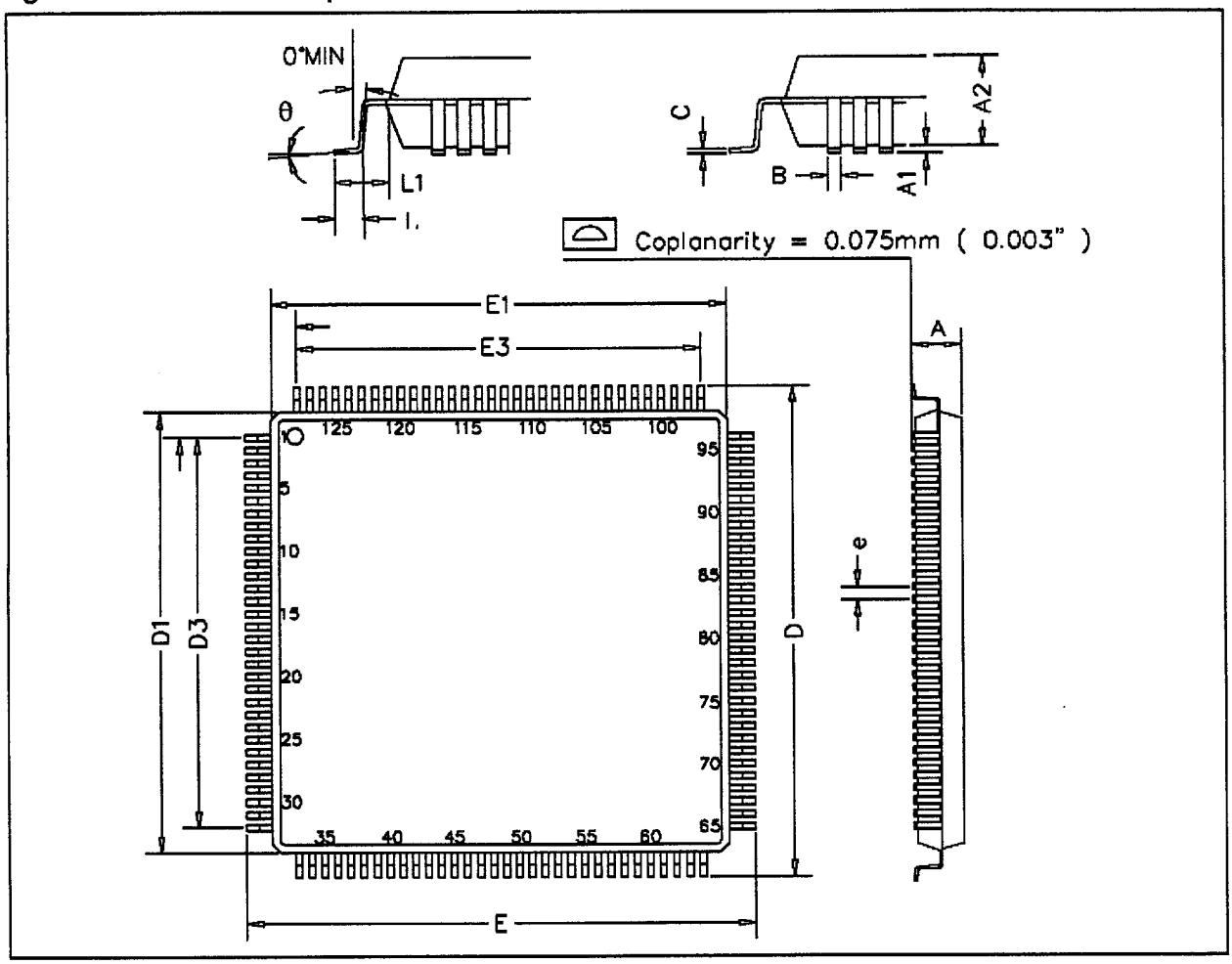
REF. (see Figure 13)	CONTROL DIMENSIONS - mm			ALTERNATIVE DIMENSIONS - inches			NOTES
	MIN	NOM	MAX	MIN	NOM	MAX	
A	-	-	4.07	-	-	0.160	
A1	0.25	-	-	0.010	-	-	
A2	3.17	3.42	3.67	0.125	o.135	0.144	
B	0.30	-	0.45	0.012	-	0.018	
c	0.13	-	0.23	0.005	-	0.009	
D	30.95	31.20	31.45	1.219	1.228	1.238	
D1	27.90	28.00	28.10	1.098	1.102	1.106	
D3	-	24.80	-	-	0.976	-	REF
e	-	0.80	-	-	0.031	-	BSC
E	30.95	31.20	31.45	1.219	1.228	1.238	
E1	27.90	28.00	28.10	1.098	1.102	1.106	
E3	-	24.80	-	-	0.976	-	REF
L	0.65	0.80	0.95	0.026	0.031	0.037	
L1	-	1.60	--	-	0.063	-	
θ	0°	-	7°	0°	-	7°	

NOTES

1 Lead finish to be 85 Sn/15 Pb solder plate.

2 Maximum lead displacement from the notional center line will be no greater than ± 0.125 mm.

Figure 13. STG1764 128-pin Plastic Quad Flat Pack dimension reference



11 REFERENCES

1 STG1732 and STG1764 *Palette-DAC Datasheet*, SGS-THOMSON, June 1995, SGS-THOMSON Document Number: 42 1648 02 (this document)

2 STG2000 *Multimedia Accelerator Datasheet*, SGS-THOMSON Microelectronics, June 1995, SGS-THOMSON Document Number: 42 1653 02

3 *NVidia Technical Reference*, NVidia Corporation, June 1995, NVidia Document Number: DOC-03-STN

4 *NV Architecture Overview*, NVidia Corporation, June 1995, NVidia Document Number: DOC-03-SUN

5 *Programming NV*, NVidia Corporation, June 1995, NVidia Document Number: DOC-03-SPN

6 *Reference Design Kit (RDK), Design Guide*, SGS-THOMSON Microelectronics, June 1995, SGS-THOMSON Document Number: 72 OEK 290 00

12 ORDERING INFORMATION

Device	Max. pixel rate	Package	Part number
STG1732	135MHz	100 pin PQFP	STG1732X-13
STG1764	135MHz	128 pin PQFP	STG1764X-13
STG1764	170MHz	128 pin PQFP	STG1764X-17*

* STG1764X-17 is preliminary only