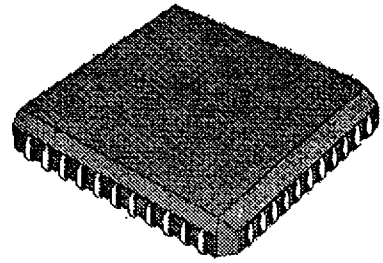
SGS-THOMSON MICROELECTRONICS

STG 1700

TRUE COLOR PALETTE-DAC WITH 16-BIT PIXEL PORT

- Operation up to 135MHz
- 2:1 multiplexing using internal PLL
- Standard VGA and high color operation up to 110MHz
- Synchronous PixMix switching between modes
- Low power sleep mode
- Triple 8-bit DACs with comparators
- External or internal VRef DAC control



PLCC44

DESCRIPTION

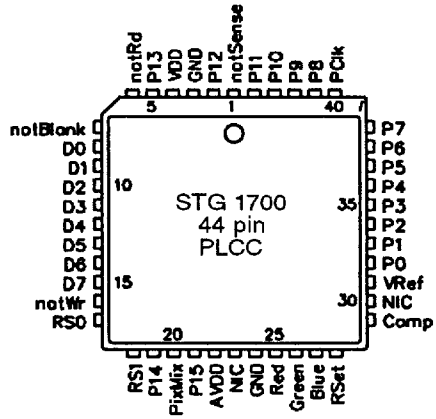
The STG 1700 is a Super VGA compatible Palette-DAC designed for PC systems requiring pixel rates up to 135MHz. It features a 16-bit pixel port and supports a number of different pixel modes which can be grouped into three categories:

- 8-bit pixel port giving standard SVGA and high/true color modes
- 16-bit pixel port giving faster high color/true color operation
- Serializing 16-bit pixel port to give two 8-bit pixels at 2 ψ PClk frequency

The PixMix capability allows pixel-by-pixel switching between modes.

The STG 1700 includes a 135MHz triple 8-bit video DAC, controlled by either an external 1.235V voltage reference or an on-chip voltage reference. A VGA compatible micro port makes use of "magic access" cycles (repeated accesses to the mask register) to control the extended features.

PIN CONNECTIONS

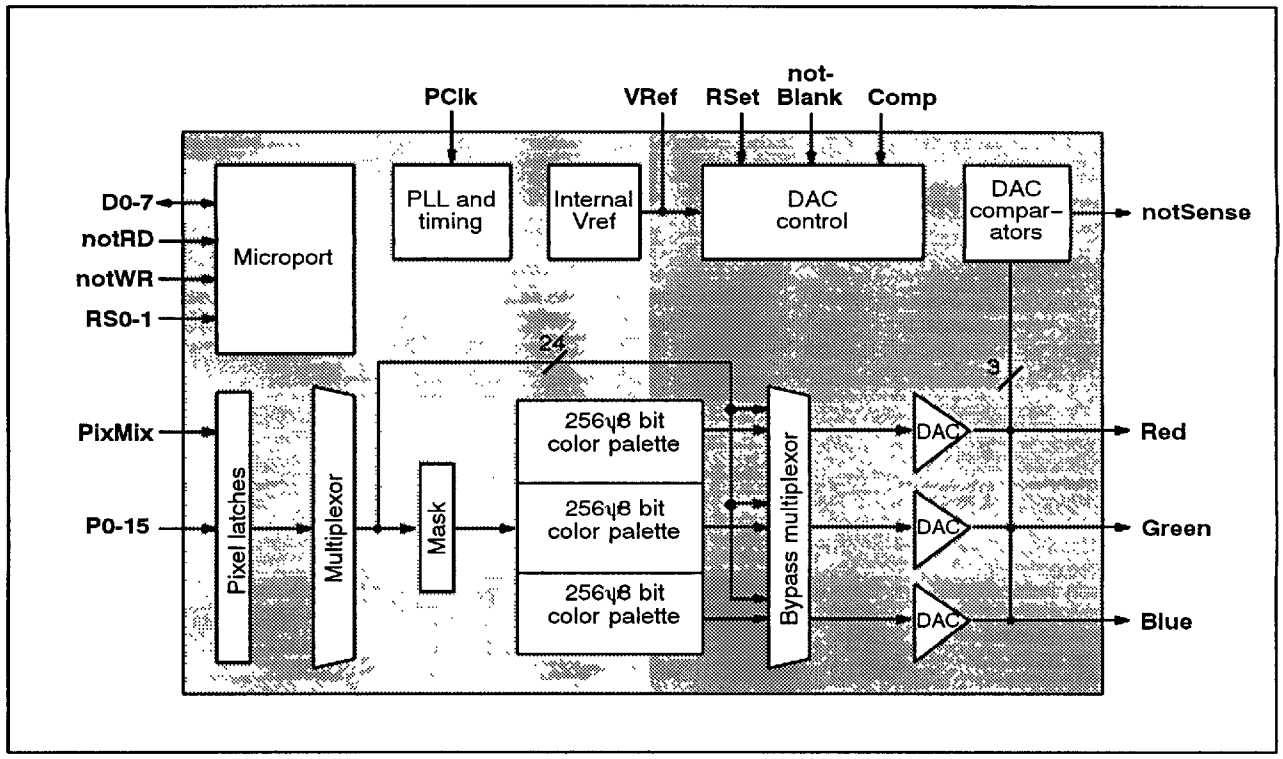


EXAMPLE MODES AND FREQUENCIES

Pixel port mode	Screen resolution	Simultaneous colors	Refresh rate (Hz)	PClk and data frequency (MHz)	Video frequency (MHz)
8-bit pixel port	1280ψ1024	256	60	110	110
	1024ψ768	256	80	90	90
	800ψ600	65K	80	110	55
	640ψ480	16.7M	80	102	34
16-bit pixel port	1024ψ768	65K	80	90	90
	800ψ600	16.7M	80	110	55
Serializing 16-bit pixel port	1280ψ1024	256	75	67.5	135

TABLE OF CONTENTS

1 BLOCK DIAGRAM



2 PIN DESCRIPTIONS

2.1 MICRO PORT

Signal	Description
notRD, notWR	The Read Enable and Write Enable signals, **notRD** and **notWR**, control the timing of read and write operations on the micro port. Most of the operations on the micro port can take place asynchronously to the pixel stream being processed by the color palette. Various minimum periods between operations are specified (in terms of pixel clocks) to allow this asynchronous behavior. **notRD** and **notWR** should not be low at the same time.
RS0-1	The values on **RS0-1** specify which internal register is to be accessed. The **RS0-1** inputs are sampled on the falling edge of the active enable signal (**notRD** or **notWR**). Information on register access and contents is given in Section 3.
D0-7	Data is transferred between the 8-bit wide program data bus and the registers within the STG 1700 under control of the active enable signal (**notRD** or **notWR**). In a write cycle the rising edge of **notWR** validates the data on the program data bus and causes it to be written to the register selected. The rising edge of **notRD** signifies the end of a read cycle, after which the program data bus will cease to carry the contents of the register addressed and will go to a high impedance state.

2.2 PIXEL PORT

Signal	Description
PClk	The rising edge on PClk controls the sampling of data on **P0-15**, **notBlank** and **PixMix** in all modes.
P0-15	The pixel data word. The selected pixel mode determines how this pixel data is interpreted.
PixMix	Controls the switching between primary and secondary pixel modes when the Extended Pixel modes are selected. (**PixMix** = 0 selects primary mode.)
notBlank	A low value sampled on this pin will, after the pipeline delay, turn the DAC outputs off.

2.3 ANALOG INTERFACE

Signal	Description
Red, Green, Blue	The DAC video outputs. These are designed to drive a doubly terminated 75 ohm load.
VRef	External 1.235V Vref input. When used in internal Vref mode this pin should be left floating, with or without the optional external Vref bypass capacitor.
RSet	A precision resistor placed between this pin and GND sets the full-scale DAC current. The required resistor value can be calculated from: Rset (Ω) = (2.1ψVref)/Iout where Vref is the external or internal reference voltage and Iout is the required DAC full scale output current.
Comp	External compensation capacitor for DACs.
notSense	This pin is a logical 0 if one or more of the DAC outputs exceeds the internal DAC comparator trip voltage (which is mid-way between the DAC full scale and GND potentials).

2.4 POWER SUPPLY

Signal	Description
VDD	Digital power supply
AVDD	Analog power supply for the DACs and PLL.
GND	Common GND rail for all circuitry.
NIC	No internal connection.

3 MICRO PORT

The STG 1700 micro port (see Table 1) is an extension of the standard VGA micro port and will power up with a register configuration compatible with standard and high color VGA.

The extended register space is accessed by a special mechanism of successive reads ("magic access") to the mask register location 2h, as shown in Table 2. Reads from RS location 2h cause a state counter to be advanced by 1. Hence, five successive reads of RS location 2h will return the mask register contents four times followed by the pixel command value.

Following this, two accesses to location 2h will access the lower byte and higher byte of the index register respectively. Subsequent reads or writes to location 2h access the extended register space pointed to by the index register. After each access, the index register will increment automatically. In this way the entire extended register space may be "block moved" without the need to keep writing to the index register.

At any point in the above sequence a read or write to any location other than 2h will reset the state counter to state 1.

On power up the magic access sequence is partially disabled through the default setting of Pixel Command Register, bit [4], so that the STG 1700 is identified by existing video BIOS code as a fast ATT20C49X.

Table 1. Micro port register space

RS[1:0]	VGA Register
00	Address Register (write mode)
01	Color Value
10	Pixel Mask/Magic Access
11	Address Register (read mode)

Table 2. Magic access sequence

Current state[1]		Next state			
	Register mapped at RS=2h	Read from RS=2h *and* index space enabled	Read from RS=2h and index space disabled (default)	Write to RS=2h	Read/ write to other RS location
1	Pixel Mask	2	2	1	1
2	Pixel Mask	3	3	1	1
3	Pixel Mask	4	4	1	1
4	Pixel Mask	5	5	1	1
5	Pixel Command	6	1	1	1
6	Index LO byte	7		7	1
7	Index HI byte	8		8	1
8	Indexed register	8*		8*	1

NOTES

1 Power-up state is state 1

* increment index register after access

Table 3. Extended register space

Index	Index register contents
00 00h	Company ID
00 01h	Device ID
00 02h	Reserved
00 03h	Primary pixel mode select
00 04h	Secondary pixel mode select
00 05h	PLL Control
00 06h	Soft reset

3.1 REGISTER DESCRIPTIONS

A write to any register containing reserved bits should always write 0 to the reserved bits. On reads all reserved bits should be masked out.

Bits within registers which are reset on power-up are marked in the column headed "Reset value".

Table 4. Pixel Command register

Bit	Value	Function	Reset value
7:5	000	8-bit indexed color	000
	001	Reserved	
	010	Reserved	
	011	Reserved	
	100	Reserved	
	101	15-bit direct color	
	110	16-bit direct color	
	111	24-bit direct color	
4		'1' = Enable Extended Register space	0
3		'1' = Enable Extended Pixel modes	0
2		'1' = Add 7.5 IRE blanking pedestal	0
1		'1'= Micro port interface to RAM is 8-bit not 6-bit	0
0		'1' = Sleep mode (micro port still enabled)	0

Table 5. Index LO and Index HI registers

Bit	Function	Reset value
7:0	LO/HI byte of 16-bit Index	0

Extended Register Space

Index 0 Company ID register

Bit	Function	Reset value
7:0	44h (= SGS-THOMSON)	read only

Index 1 Device ID register

Bit	Function	Reset value
7:0	00h (= STG 1700)	read only

Indexes 3,4 Pixel Mode Select registers (Primary and Secondary)

Bit	Value	Function	Max PClk (MHz)	Max Video rate (MHz)	Reset value
7:0	00h	8-bit indexed color	110	110	not reset
	01h	15-bit direct color or 8-bit indexed color	110	110	
	02h	15-bit direct color	110	110	
	03h	16-bit 5:6:5 direct color	110	110	
	04h	24-bit direct color	110	55	
	05h	Double 8-bit indexed color (uses PLL)	67.5	135	
	06h–FFh	Reserved			

Index 5 PLL Control register (double 8-bit mode only)

Bit	Value	PClk input frequency (MHz)	Resulting DAC clock frequency (MHz)	Reset value
7:2		Reserved		0
1:0	00	8–16	16–32	
	01	16–32	32–64	
	10	32–67.5	64–135	10
	11	Reserved		

Index 6 Soft Reset register

Bit	Function	Reset value
7:1	Reserved	0
0	'1' = Reset all registers to power-on default state	0

3.2 MICRO PORT TIMING SPECIFICATION

Figure 1. Basic read/write cycle

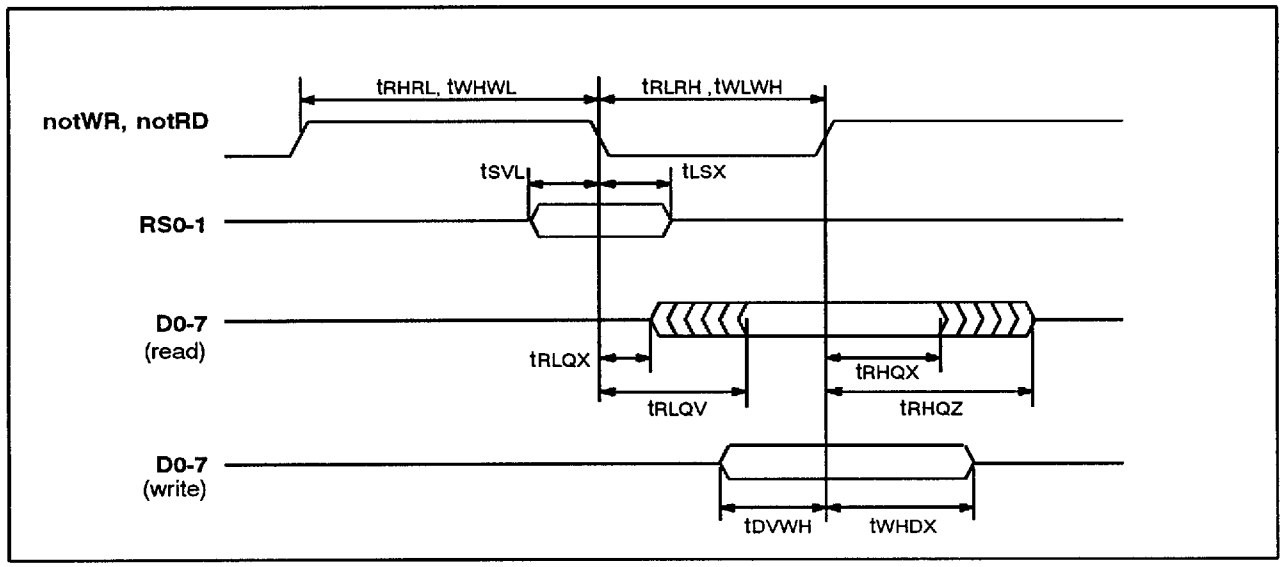


Table 6. Micro port timing parameters

Symbol	Parameter	Min.	Max.	Units	Notes
tWLWH	**notWR** pulse width low	50		ns	
tRLRH	**notRD** pulse width low	50		ns	
tWHWL	Recovery time preceding a write	3½tCHCH		ns	1,2
tRHRL	Recovery time preceding a read	6½tCHCH		ns	1,2
tSVL	**RS** setup time	10		ns	
tLSX	**RS** hold time	4		ns	
tDVWH	Write data setup time	10		ns	
tWHDX	Write data hold time	10		ns	
tRLQX	Output turn-on delay	5		ns	
tRLQV	Read enable access time		40	ns	
tRHQX	Output hold time	5		ns	
tRHQZ	Output turn-off delay		20	ns	
	Write/Read enable transition time		50	ns	
	PLL settling time	500		µs	

NOTE

1 tCHCH (**PCIk** period) is specified in Table 8.

2 Access recovery times are specified as the time *before* a particular access, because the worst case access (reading a RED palette color value) can occur after either reading a BLUE palette color value or after writing to the Address Register (read mode).

4 PIXEL PORT

All pixels are latched on the rising edge of PClk. Modes which require more than one word per pixel accumulate the least significant bytes of the pixel first. **notBlank** going high always identifies the first word within a pixel.

4.1 VGA AND SVGA MODES

SVGA mode	Pixel word latched	Use of pixel input pins[2]															
		P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
8-bit indexed	single P[7:0]	x	x	x	x	x	x	x	x	P7	P6	P5	P4	P3	P2	P1	P0
15-bit direct (5:5:5)	first P[7:0]	x	x	x	x	x	x	x	x	G5	G4	G3	B7	B6	B5	B4	B3
	second P[7:0]	x	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	G7	G6
16-bit direct (5:6:5)	first P[7:0]	x	x	x	x	x	x	x	x	G4	G3	G2	B7	B6	B5	B4	B3
	second P[7:0]	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	G7	G6	G5
24-bit direct (8:8:8)	first P[7:0]	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0
	second P[7:0]	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0
	third P[7:0]	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0

NOTES
1 Pipe delay for all modes = 12 PClks
2 Unspecified bits = 0

4.2 EXTENDED PIXEL MODES

Extended Pixel mode		Pixel word latched	Use of pixel input pins															
Mode	Description		P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
0	8-bit indexed	single P[7:0]	x	x	x	x	x	x	x	x	P7	P6	P5	P4	P3	P2	P1	P0
1	15-bit direct	single P[15:0]	0 or 1	x R7	x R6	x R5	x R4	x R3	x G7	x G6	P7 G5	P6 G4	P5 G3	P4 B7	P3 B6	P2 B5	P1 B4	P0 B3
2	15-bit direct	single P[15:0]	x	R7	R6	R5	R4	R3	G7	G6	G5	G4	G3	B7	B6	B5	B4	B3
3	16-bit direct	single P[15:0]	R7	R6	R5	R4	R3	G7	G6	G5	G4	G3	G2	B7	B6	B5	B4	B3
4	24-bit direct	first P[15:0]	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		second P[15:0]	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0
5	Double 8-bit indexed[2]	single P[15:0]	P7	P6	P5	P4	P3	P2	P1	P0	P7	P6	P5	P4	P3	P2	P1	P0
			second displayed pixel								first displayed pixel							

NOTES
1 Pipe delay for all modes except mode 5 = 12 PClks
2 Mode 5 uses PLL, DAC Clk = 2 ψPClk

Table 7. Primary and secondary pixel mode combinations

Primary Mode	Secondary Mode					
	0	1	2	3	4	5
0	Y	Y	Y	Y	Y	N
1	Y	Y	Y	Y	Y	N
2	Y	Y	Y	Y	Y	N
3	Y	Y	Y	Y	Y	N
4	Y	Y	Y	Y	Y	N
5	Y	Y	Y	Y	Y	Y

Extended Pixel modes are enabled by writing to the pixel command register. Two modes are defined - primary and secondary. The STG 1700 will switch between these two modes on the fly under the control of the **PixMix** pin.

The **PixMix** pin is sampled on PClk together with the pixel pins. The STG 1700 will only switch modes on whole pixel boundaries. If either the primary or secondary mode format requires two PClk edges to build a whole pixel, then PixMix should only change state on every second PClk edge after **notBlank** has gone high at the start of a line.

If **PixMix** is not in use, the Primary and Secondary Pixel Mode Select Registers should be written with the same value.

Programming of pixel mode 5

Programming of pixel mode 5, which uses the PLL, should be performed as follows:

1 Write 05h to index register 3 to select mode 5 as the primary pixel mode.

2 Select the PLL input frequency range by writing an appropriate value to index register 5.

3 Wait for the specified PLL settling time to elapse (see Table 6) before accessing any other register.

4 Program the color palette (through the Color Value Register).

Reprogamming of index register 5 should always be followed by performing steps 3 and 4 given above.

4.3 PIXEL PORT TIMING SPECIFICATION

Figure 2. Pixel port timing diagram

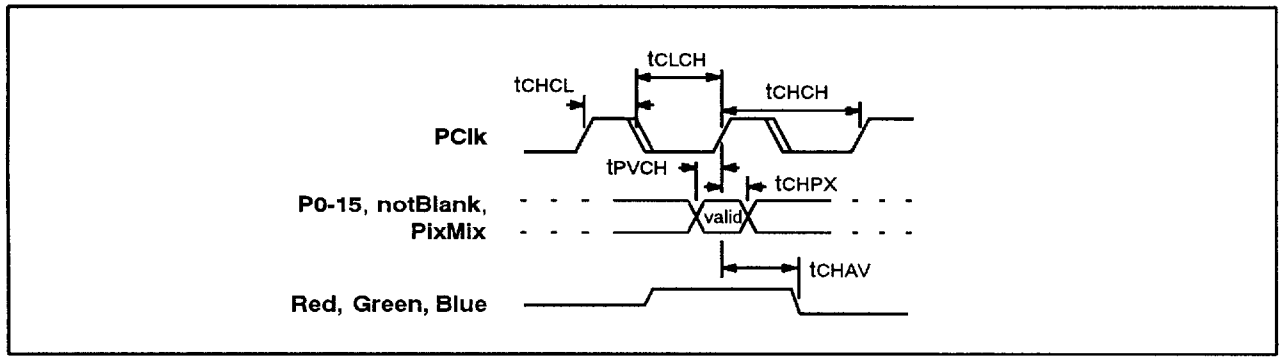


Table 8. Pixel port timing parameters

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
tCHCH	**PCIk** period	9.08			ns	
tCLCH	**PCIk** low time	4.2			ns	
tCHCL	**PCIk** high time	3.2			ns	
tPVCH	Pixel data set-up time	3.0			ns	1
tCHPX	Pixel data hold time	3.0			ns	1
tCHAV	**PCIk** to valid DAC output		6.0	20.0	ns	2
ΔtCHAV	Differential output delay between DAC outputs			1.5	ns	

NOTES

1 The Pixel Address input to the color palette should be set up as a valid logic level with the appropriate setup and hold times to each rising edge of **PCIk** (this requirement must also be met during the blanking period).

2 A valid analog output is defined as when the changing analog signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

5 ELECTRICAL SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Min.	Max.	Units	Notes
VDD/AVDD	DC supply voltage		7.0	V	
	Voltage on input and output pins	GND-1.0	VDD+0.5	V	
TS	Storage temperature (ambient)	-55	125	ºC	
TA	Temperature under bias	-40	85	ºC	2
PDmax	Power dissipation		2.0	W	
	Analog output current (per output)		45	mA	
	DC digital output current		25	mA	

NOTE

1 Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2 For thermal management information on the STG 1700 refer to the Application Note *Designing with the STG 1700 16-bit pixel port Palette-DAC,* Document number 72 TCH 150 00, July 1993.

5.2 DAC CHARACTERISTICS

Parameter	Min.	Typ.	Max.	Units	Notes
Resolution		8		bits	
Operating frequency			135	MHz	
Black level pedestal current	0.95	1.44	1.90	mA	1
White relative to Black current	16.74	17.62	18.50	mA	1
DAC to DAC matching		+1	+2.5	%	1,2
Integral linearity		+0.5	+1.5	LSB	1,6
Differential linearity		+0.25	+1	LSB	1
DAC output voltage			1.2	V	1
DAC output impedance	10	20		kΩ	
Risetime (black to white level)		1	3	ns	1,3,4
Settling time (black to white)		4	7.4	ns	1,3,5
Glitch energy		50	100	pVs	1,3
Comparator trip voltage	280	335	420	mV	
Comparator settling time			100	µs	
Vref input current			100	µA	
Internal Vref voltage		1.235		V	
Internal Vref voltage accuracy		+3	+5	%	

NOTES

1 Vref = 1.235V, Rset = 147Ω

2 About the mid-point of the distribution of the three DACs

3 37.5ohm, 30pF load.

4 10% to 90%

5 Settling to within 2% of fsd

6 Monotonicity guaranteed

5.3 DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
IDD	Average power supply current		250	340	mA	1
IIN	Digital input current			+100	µA	
IOZ	Off state digital output current			+50	µA	
VOH	Output logic 1 level	2.4			V	2
VOL	Output logic 0 level			0.4	V	2

NOTE

1 Typ. and max. figures both measured at 135MHz, with differences due to VDD, pixel mode and part to part variations.

2 I_{load}=5mA

5.4 OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
VDD	Positive supply voltage	4.75	5.0	5.25	V	1
VIH	Input logic '1' voltage	3.5		VDD+0.5	V	
VIL	Input logic '0' voltage	-0.5		0.4	V	
TA	Ambient operating temperature		25	70	℃	

NOTES

1 These voltage ranges apply equally for AVDD and VDD.

6 ANALOG INTERFACE

Figure 3. Recommended circuit in external voltage reference mode

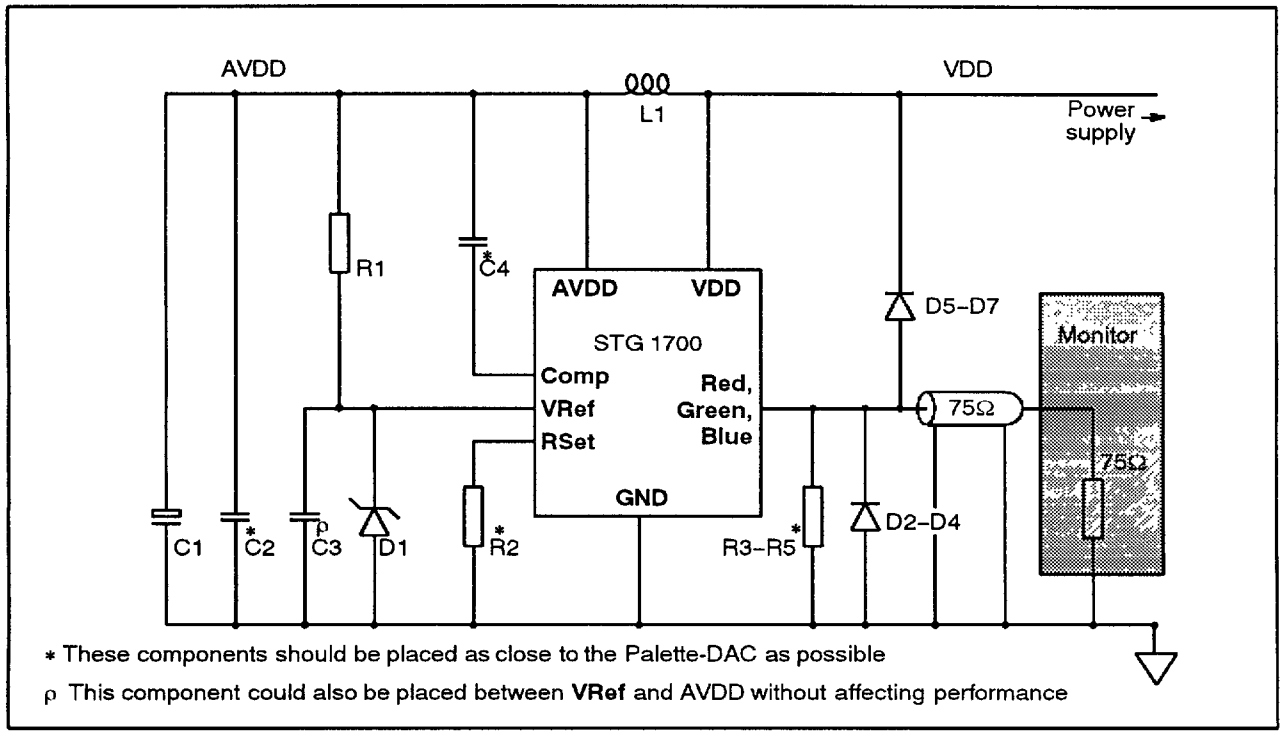


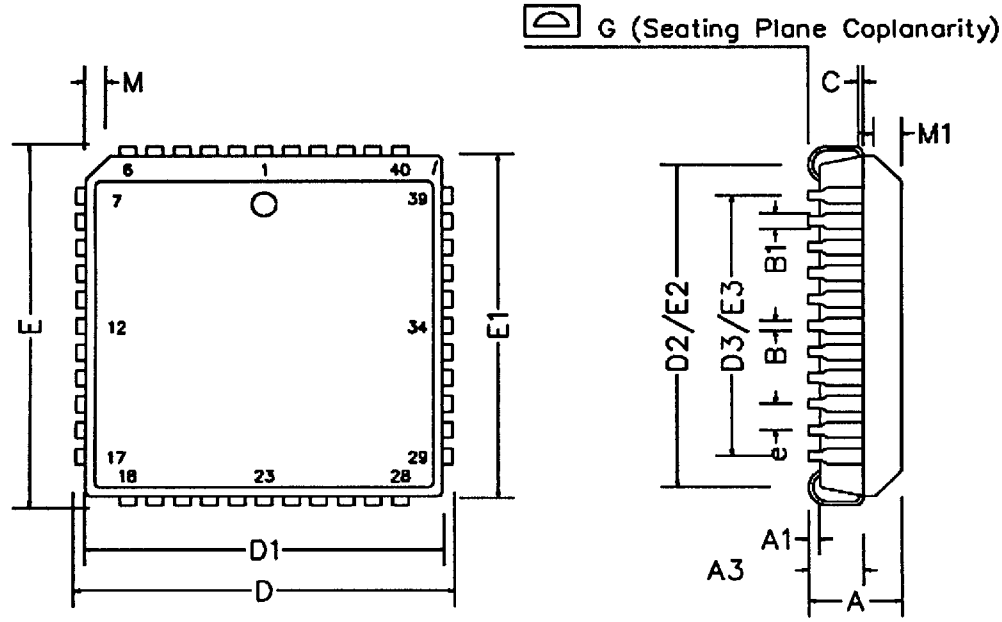
Table 9. Table of parts for recommended circuit (Figure 3)

Part number	Value	Description
C1	47µF	capacitor
C2-C3	100nF	surface mount capacitor
C4	10nF	surface mount capacitor
R1	1KΩ	5% resistor
R2	147Ω	1% resistor
R3-R5	75Ω	resistor
D1	LM385BZ-1.2	voltage reference
D2-D7	1N4148	diode
L1	1µH	inductor

7 PACKAGE DIMENSIONS

Figure 4. STG 1700 44 pin PLCC J-bend package dimensions

DIM	CONTROL DIMENSIONS INCH			ALTERNATIVE DIMENSIONS mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.165	0.170	0.180	4.191	4.318	4.572
A1	0.020	–	–	0.508	–	–
A3	0.095	–	0.110	2.413	–	2.794
B	0.013	–	0.023	0.330	–	0.584
B1	0.025	–	0.035	0.635	–	0.889
C	0.0095	0.010	0.0105	0.241	0.254	0.267
D	0.685	0.690	0.695	17.399	17.526	17.653
D1	0.650	0.655	0.660	16.510	16.637	16.764
D2	0.590	0.610	0.630	14.986	15.494	16.002
D3	–	0.500REF	–	–	12.700REF	–
E	0.685	0.690	0.695	17.399	17.526	17.653
E1	0.650	0.655	0.660	16.510	16.637	16.764
E2	0.590	0.610	0.630	14.986	15.494	16.002
E3	–	0.500REF	–	–	12.700REF	–
e	–	0.050BSC	–	–	1.270BSC	–
G	–	–	0.004	–	–	0.102
L	–	N/A	–	–	N/A	–
L1	–	N/A	–	–	N/A	–
M	0.042	–	0.048	1.067	–	1.219
M1	0.042	–	0.056	1.067	–	1.422



Notes;

1. Maximum lead displacement from notional centre line = ±0.007".

8 ORDERING INFORMATION

Device	Max. pixel rate	Package	Part number
STG 1700	135 MHz	44 pin plastic LCC	STG 1700J-13Z