



# STEVAL-TDR013V1

## Demonstration board using the PD84002 for UHF RFID reader

### Features

- Excellent thermal stability
- Frequency: 8
- 860 - 960 MHz
- Supply voltage: 7.2 V
- Output power: 2 W
- Power gain:  $13.9 \pm 0.5$  dB
- Efficiency: 60 % - 63 %
- Load mismatch: 20:1
- BeO-free amplifier

### Description

The STEVAL-TDR013V1 is an evaluation board using PD84002 LDMOS transistor and designed for UHF RFID reader and 2-way radio applications.

For additional information on PD84002, please refer to its datasheet.

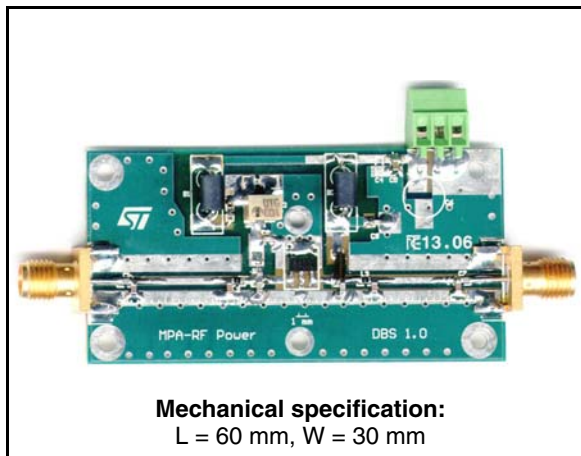


Table 1. Device summary

| Order code      |
|-----------------|
| STEVAL-TDR013V1 |

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# 1 Electrical data

## 1.1 Maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol     | Parameter                   | Value      | Unit |
|------------|-----------------------------|------------|------|
| $V_{DD}$   | Supply voltage              | 16         | V    |
| $I_D$      | Drain current               | 0.75       | A    |
| $T_{CASE}$ | Operating case temperature  | -20 to +85 | °C   |
| $T_A$      | Maximum ambient temperature | +55        | °C   |

# 2 Electrical characteristics

$T_A = +25\text{ °C}$ ,  $V_{DD} = 7.2\text{ V}$ ,  $I_{dq} = 100\text{ mA}$

**Table 3. Electrical specifications**

| Symbol    | Test conditions                                   | Min | Typ            | Max  | Unit |
|-----------|---------------------------------------------------|-----|----------------|------|------|
| Freq      | Frequency range                                   | 860 |                | 960  | MHz  |
| $P_{OUT}$ |                                                   |     | 2              |      | W    |
| Gain      | @ $P_{IN} = 19\text{ dBm}$                        |     | $13.9 \pm 0.5$ |      | dB   |
| ND        | @ $P_{IN} = 19\text{ dBm}$                        |     | 60 - 63        |      | %    |
| H2        | 2nd harmonic @ $P_{OUT} = 2\text{ W}$             |     | -31 / -46      |      | dBc  |
| H3        | 3rd harmonic @ $P_{OUT} = 2\text{ W}$             |     | -62 / -70      |      | dBc  |
| VSWR      | Load mismatch all phases @ $P_{OUT} = 2\text{ W}$ |     |                | 20:1 |      |

### 3 Impedance

Figure 1. Impedance illustration

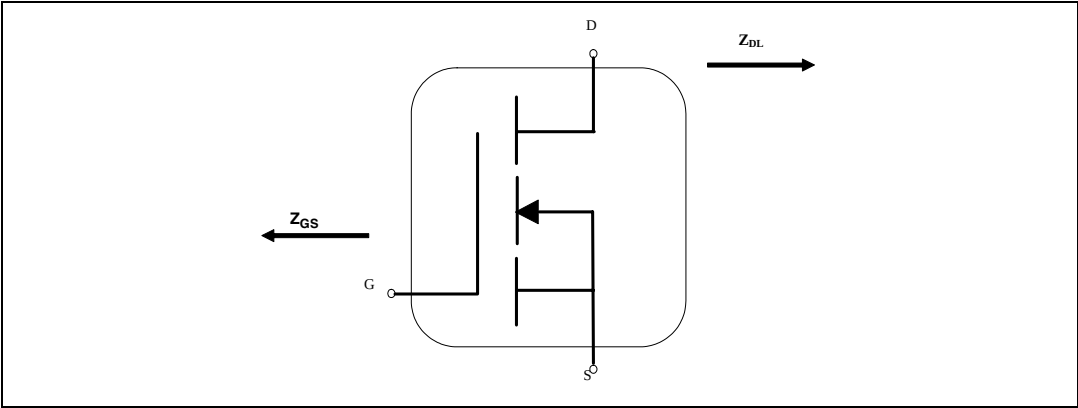
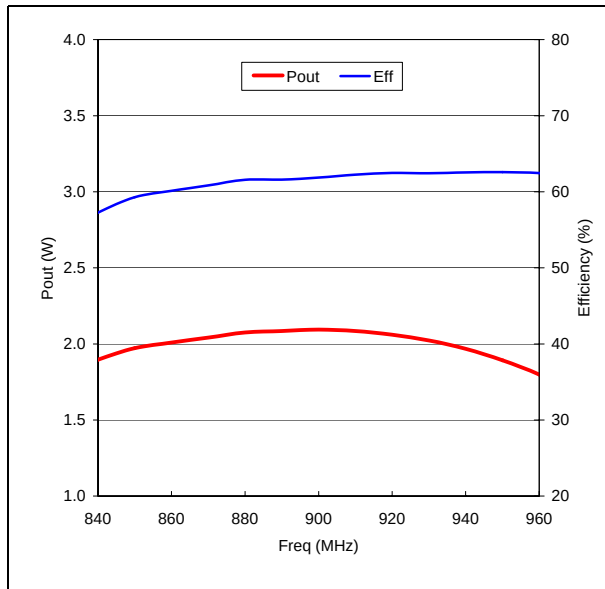


Table 4. Impedance data

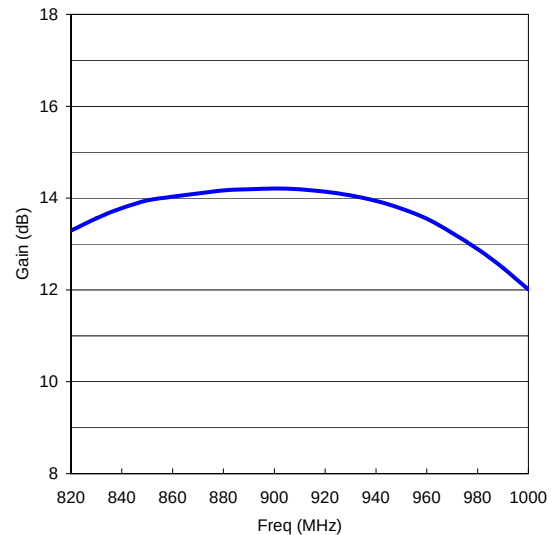
| F(MHz) | $Z_{GS}$         | $Z_{DL}$         |
|--------|------------------|------------------|
| 860    | $1,80 + j\ 7,79$ | $3,88 + j\ 2,41$ |
| 870    | $1,84 + j\ 7,96$ | $3,89 + j\ 2,69$ |
| 880    | $1,83 + j\ 8,01$ | $4,01 + j\ 2,96$ |
| 890    | $1,76 + j\ 8,11$ | $4,17 + j\ 3,16$ |
| 900    | $1,70 + j\ 8,20$ | $4,27 + j\ 3,32$ |
| 910    | $1,63 + j\ 8,30$ | $4,37 + j\ 3,40$ |
| 920    | $1,57 + j\ 8,48$ | $4,41 + j\ 3,46$ |
| 930    | $1,43 + j\ 8,64$ | $4,36 + j\ 3,51$ |
| 940    | $1,41 + j\ 8,83$ | $4,28 + j\ 3,51$ |

## 4 Typical performance

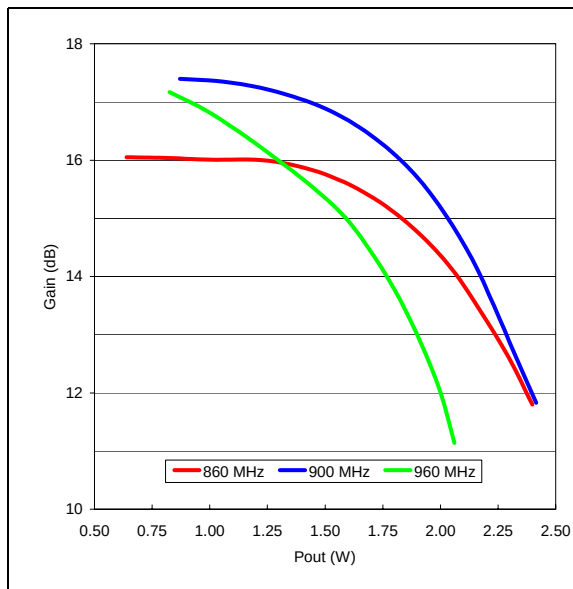
**Figure 2. Output power and efficiency vs frequency**  
7.2 V / 100 mA / Pin = 19 dBm



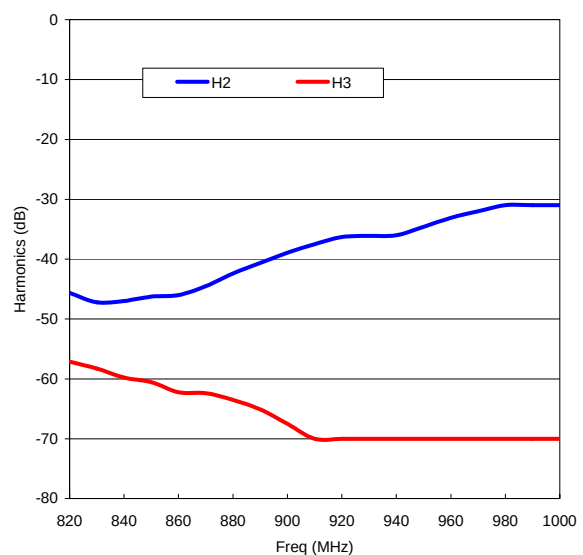
**Figure 3. Gain vs frequency**  
7.2 V / 100 mA / Pin = 19 dBm



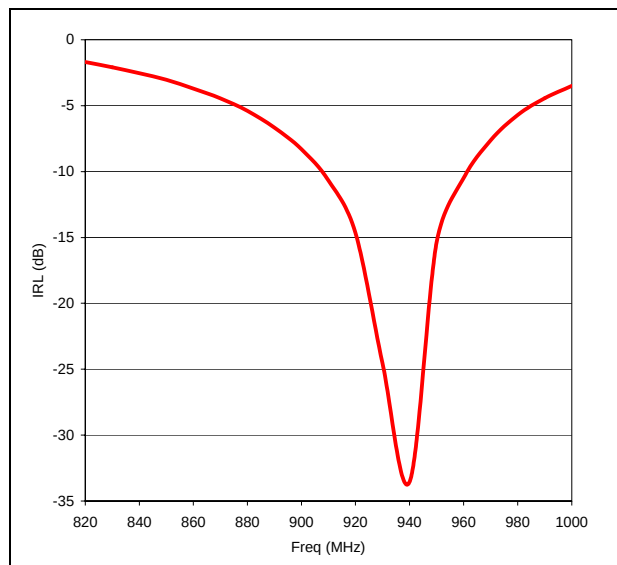
**Figure 4. Gain vs Pout**  
7.2 V / 100 mA



**Figure 5. Harmonics vs frequency**  
7.2 V / 100 mA / Pin = 19 dBm



**Figure 6. Input return loss vs frequency**  
**7.2 V / 100 mA / Pin = 19 dBm**



## 5 Test circuit

Figure 7. Test circuit schematic

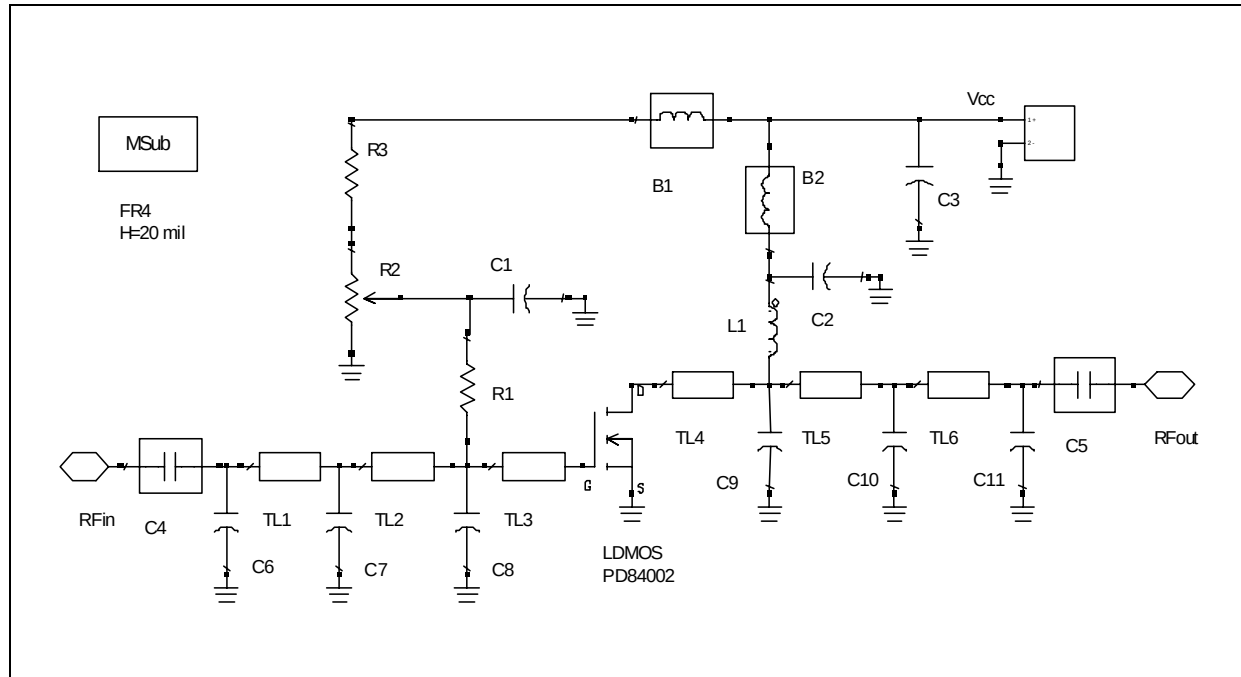


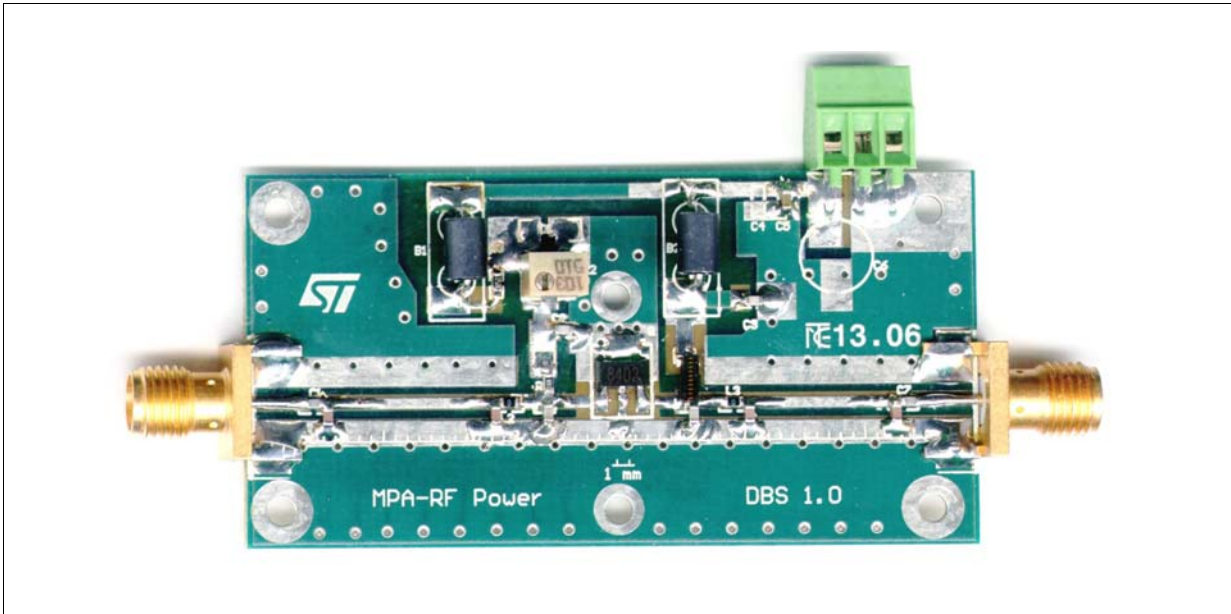
Table 5. Part list

| Component ID | Description   | Value         | Case size | Manufacturer       | Part code           |
|--------------|---------------|---------------|-----------|--------------------|---------------------|
| B1           | Ferrite Bead  |               |           | Panasonic          | EXCELDRC35C         |
| B2           | Ferrite Bead  |               |           | Panasonic          | EXCELDRC35C         |
| C1, C2       | Capacitor     | 120 pF        | 0603      | Murata             | GRM39-C0G121J50D500 |
| C3           | Capacitor     | 1 uF          | 0603      | Murata             | GRM39-X5R105K16D52K |
| C4, C5       | Capacitor     | 39 pF         | 0603      | Murata             | GRM39-C0G390J50D500 |
| C6, C10      | Capacitor     | 3.3 pF        | 0603      | Murata             | GRM39-C0G3R3C50Z500 |
| C7           | Capacitor     | 8.2 pF        | 0603      | Murata             | GRM39-C0G8R2D50Z500 |
| C8           | Capacitor     | 22 pF         | 0603      | Murata             | GRM39-C0G220J50D500 |
| C9           | Capacitor     | 12 pF         | 0603      | Murata             | GRM39-C0G120J50D500 |
| C11          | Capacitor     | 2.7 pF        | 0603      | Murata             | GRM39-C0G2R7C50Z500 |
| L1           | Inductor      | 12.55 nH      |           | Coilcraft          | 1606-10             |
| R1           | Resistor      | 150 $\Omega$  | 0603      | Tyco electronics   |                     |
| R2           | Potentiometer | 10 K $\Omega$ |           | Bourns electronics | 3214W-1-103E        |
| R3           | Resistor      | 1 K           | 0603      | Tyco electronics   | 01623440-1          |

Table 5. Part list (continued)

|               |                                   |             |             |                    |              |
|---------------|-----------------------------------|-------------|-------------|--------------------|--------------|
| TL1           | Transmission line                 | W = 0.92mm  | L = 13.6 mm |                    |              |
| Component ID  | Description                       | Value       | Case size   | Manufacturer       | Part code    |
| TL2           | Transmission line                 | W = 0.92mm  | L = 3.5 mm  |                    |              |
| TL3           | Transmission line                 | W = 0.92mm  | L = 4.2 mm  |                    |              |
| TL4           | Transmission line                 | W = 0.92mm  | L = 3.8 mm  |                    |              |
| TL5           | Transmission line                 | W = 0.92mm  | L = 3.7 mm  |                    |              |
| TL6           | Transmission line                 | W = 0.92mm  | L = 11.3 mm |                    |              |
| RF in, RF out | SMA-CONN                          | 50 $\Omega$ | 60 mils     | Johnson            | 142-0701-801 |
| PD84002       | LDMOS                             |             |             | STMicroelectronics | PD84002      |
| Board         | FR-4 THk=0.020" 2OZ Cu both sides |             |             |                    |              |

Figure 8. Demoboard photo





## 6 Circuit layout

Figure 9. Test fixture component layout

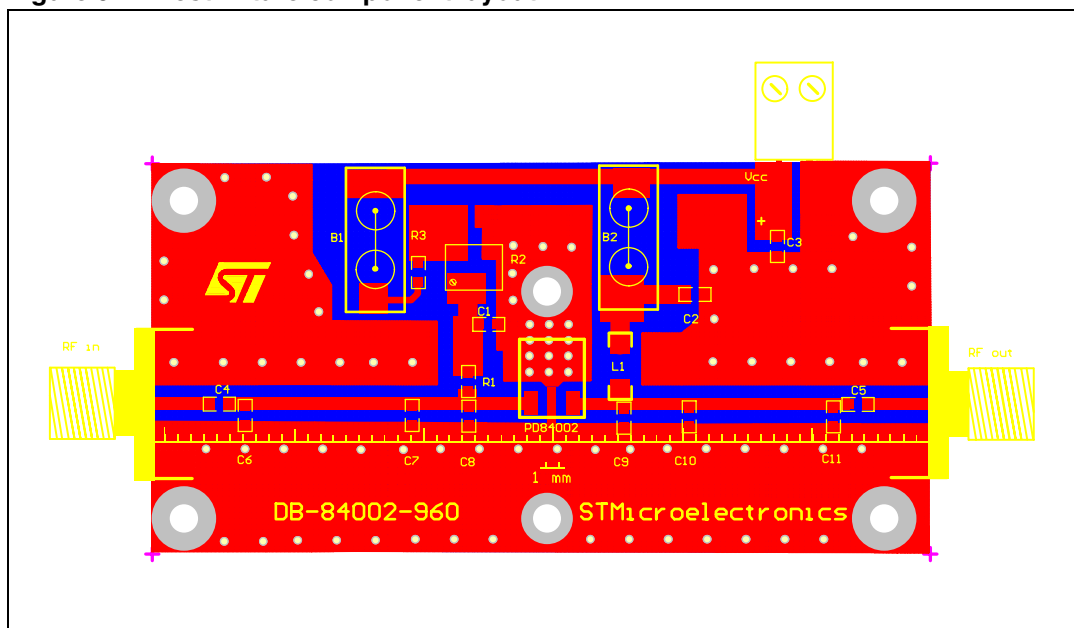
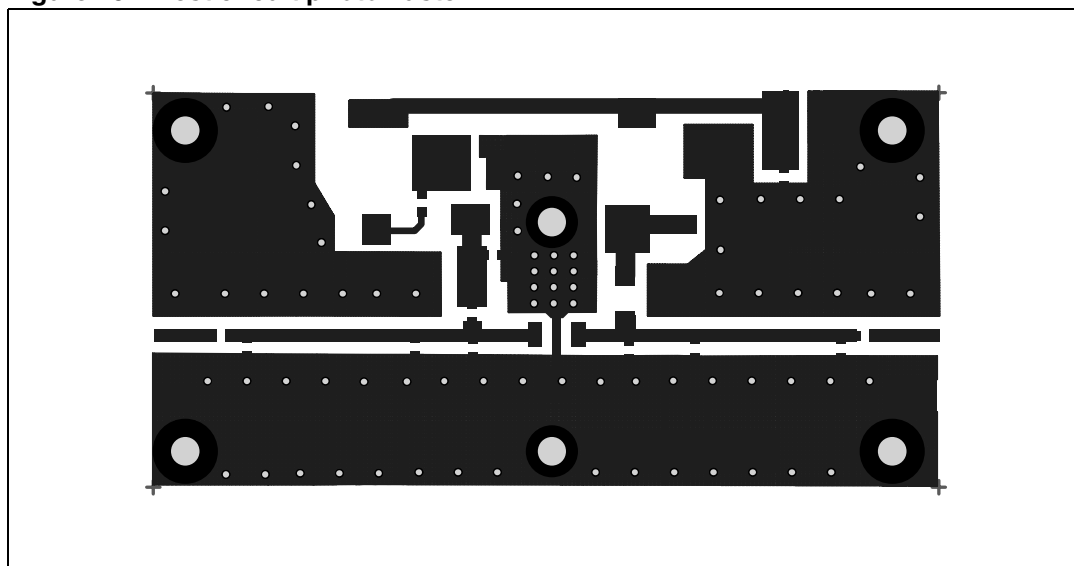


Figure 10. Test circuit photomaster



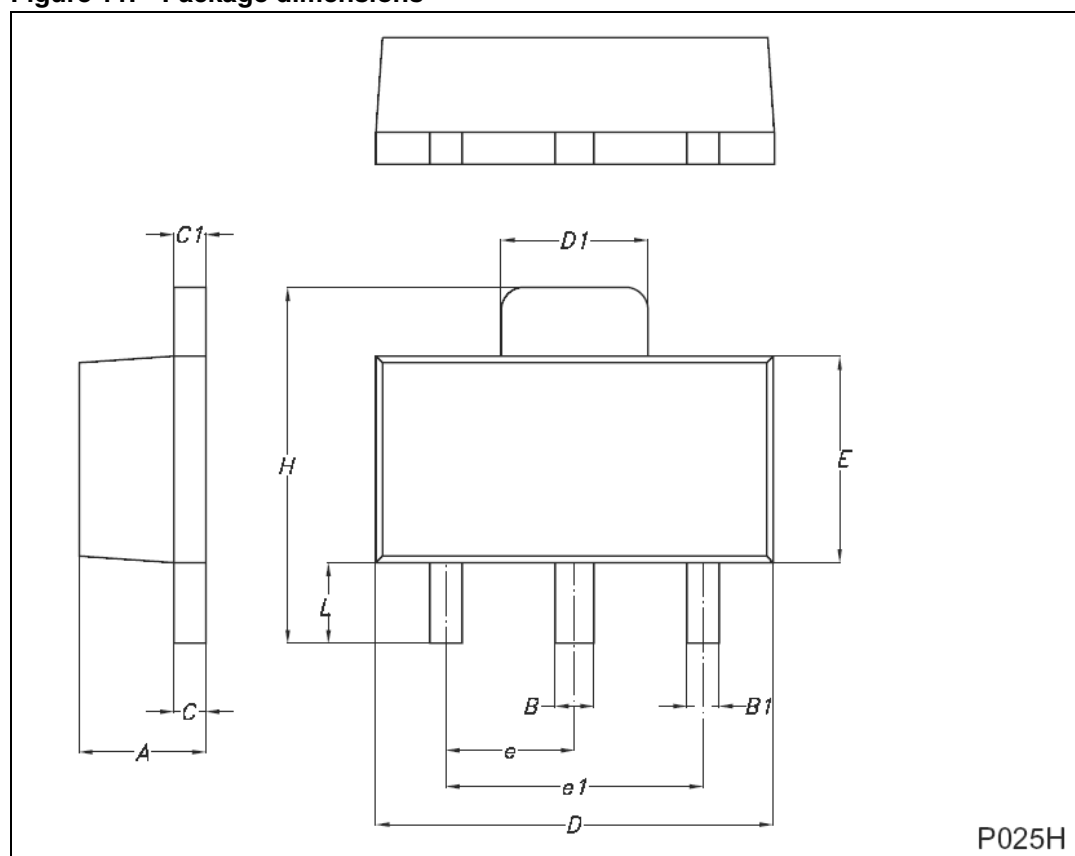
## 7      **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 6. SOT-89 mechanical data

| Dim. | mm.  |     |      | Inch  |     |       |
|------|------|-----|------|-------|-----|-------|
|      | Min  | Typ | Max  | Min   | Typ | Max   |
| A    | 1.4  |     | 1.6  | 55.1  |     | 63.0  |
| B    | 0.44 |     | 0.56 | 17.3  |     | 22.0  |
| B1   | 0.36 |     | 0.48 | 14.2  |     | 18.9  |
| C    | 0.35 |     | 0.44 | 13.8  |     | 17.3  |
| C1   | 0.35 |     | 0.44 | 13.8  |     | 17.3  |
| D    | 4.4  |     | 4.6  | 173.2 |     | 181.1 |
| D1   | 1.62 |     | 1.83 | 63.8  |     | 72.0  |
| E    | 2.29 |     | 2.6  | 90.2  |     | 102.4 |
| e    | 1.42 |     | 1.57 | 55.9  |     | 61.8  |
| e1   | 2.92 |     | 3.07 | 115.0 |     | 120.9 |
| H    | 3.94 |     | 4.25 | 155.1 |     | 167.3 |
| L    | 0.89 |     | 1.2  | 35.0  |     | 47.2  |

Figure 11. Package dimensions

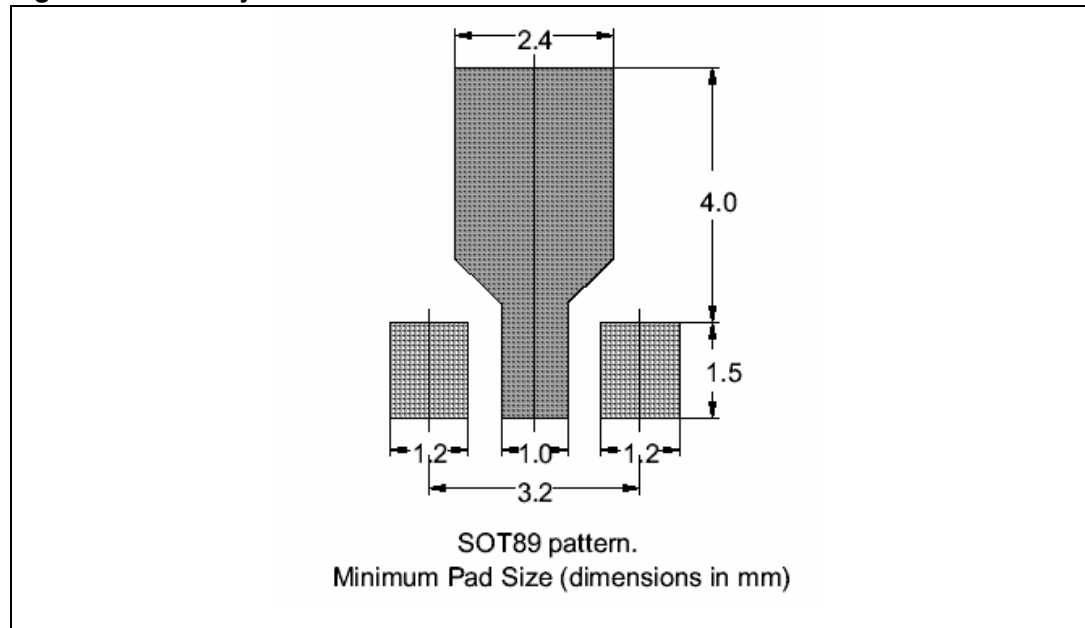


## 7.1 Thermal pad and via design

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device.

The via pattern is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025 plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

**Figure 12. Pad layout details**



## 7.2 Soldering profile

Figure 13 shows the recommended solder for devices that have Pb-free terminal plating and where a Pb-free solder is used.

**Figure 13. Recommended solder profile**

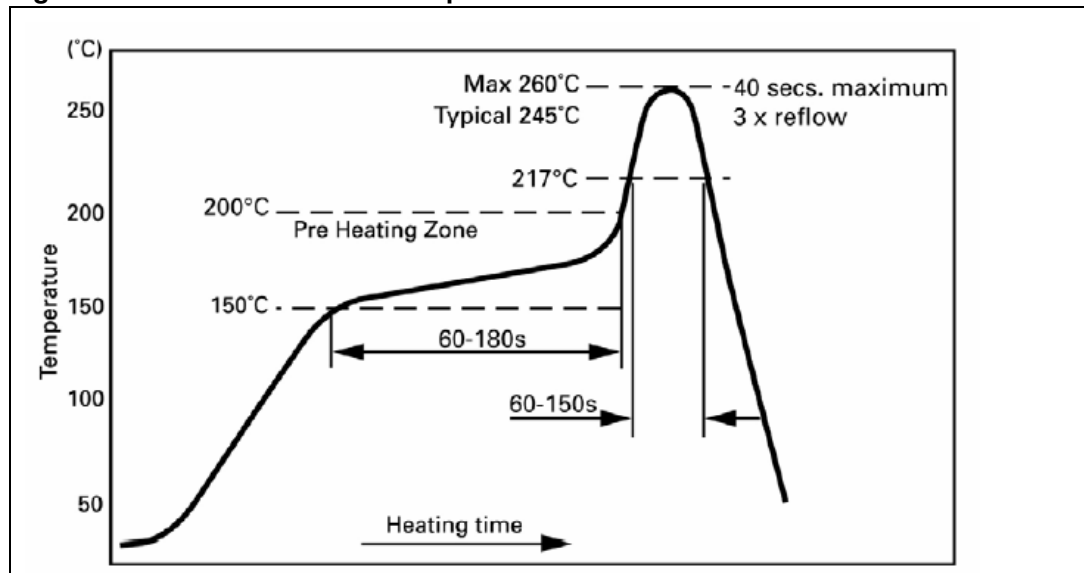


Figure 14 shows the recommended solder for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

**Figure 14. Recommended solder profile for leaded devices**

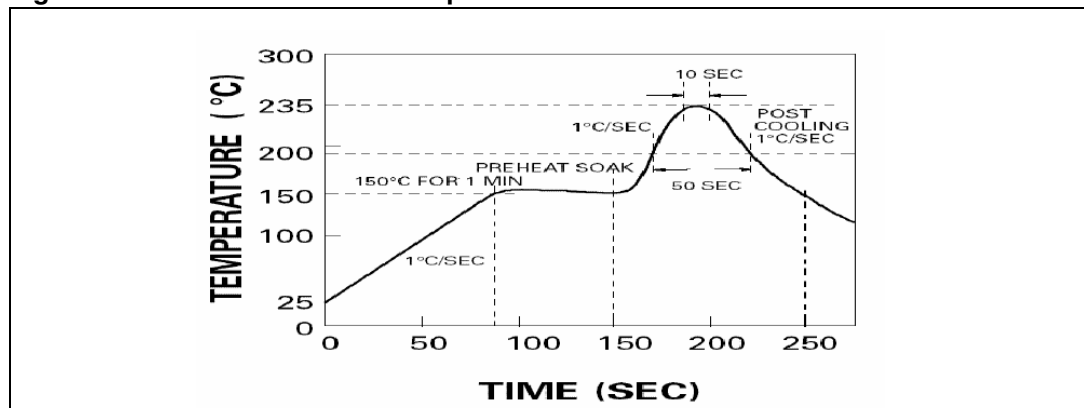
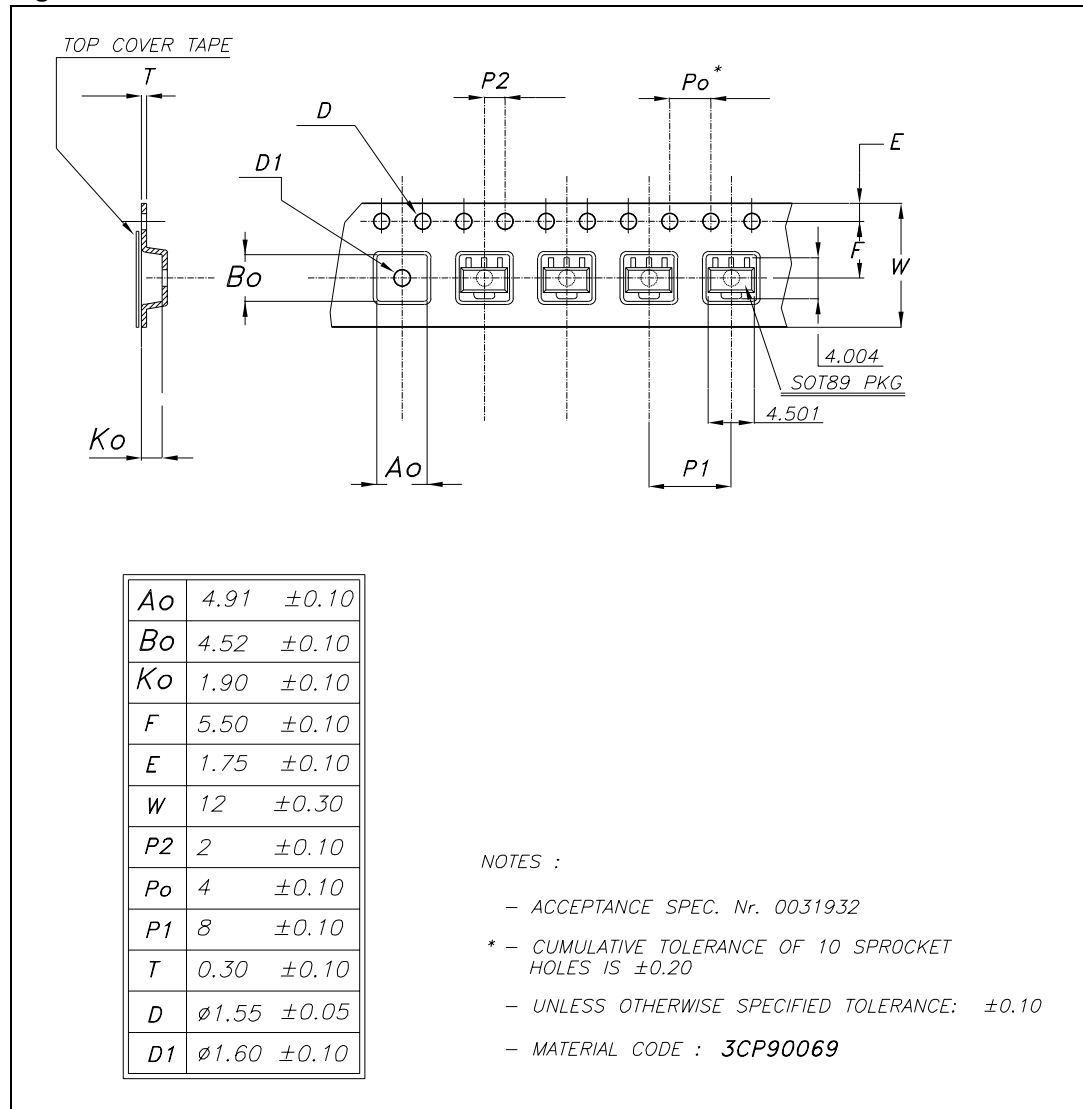


Figure 15. Reel information



## 8 Revision history

**Table 7. Document revision history**

| Date        | Revision | Changes         |
|-------------|----------|-----------------|
| 22-Sep-2007 | 1        | Initial release |

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