STE2130S

240RGB x 320 single chip true 262K color controller/driver

Data Brief

Features

- 240RGB x 320 display matrix
- 1382Kbits display RAM
- 65K and 262K color modes
- Partial display mode
- Vertical scrolling
- Programmable number of lines and columns allows smaller display resolutions
- Programmable N-line polarity inversion
- Selectable input interfaces:
  - 68000 and 8080 parallel interfaces
  - 3- and 4- wire SPI interface
  - 3-wire 9-bit serial Interface
- Selectable scan direction
- 4 programmable gamma look-up tables for gamma setting
- Fully integrated oscillator requires no external components
- Fully integrated biasing and voltage generator
- Designed for chip-on-glass (COG) and chip-on-foil (COF) applications
- Logic supply voltage range from 1.5 to 1.95V
- High-voltage generator supply range from 2.2 to 3.6V
- Integrated low drop-out (LDO) voltage regulator
- Common electrode switch drive
- Cap-On-Common and Cap-on-Gate (patented) TFT structures
- Gate, common and source waveform timing generation digitally tunable
- Gate driver voltage range from -15.0 to 16.5V
- Source driver voltage range from 0.0 to 5.5V
- Common driver voltage range from -2.5 to 4.5V
- One Time Programmable (OTP) non-volatile embedded memory
- On chip calibration (with OTP Cells) of key configuration and gamma curve parameters.
- External non-volatile memory (EEPROM) allows storing key configuration parameters and gamma curve parameters.

Description

The STE2130S is a low power CMOS LCD controller/driver featuring extremely low current consumption.

Designed to drive 240 RGB columns by 320 rows, 65K or 262K color graphics display, with amplitude modulation, the STE2130S provides all necessary functions in a single chip, including an on-chip gate driver supply, source driver supply and source reference voltage generators resulting in a minimum of externals components.

A complete set of digital functions limits host controller overhead to manage complex display configurations and to transfer fast moving image data to the display RAM.

STE2130S features five standard interfaces (3-wire serial, 3-wire SPI, 4-wire SPI, 68000 parallel and 8080 parallel) for easy of interfacing with the host controller.

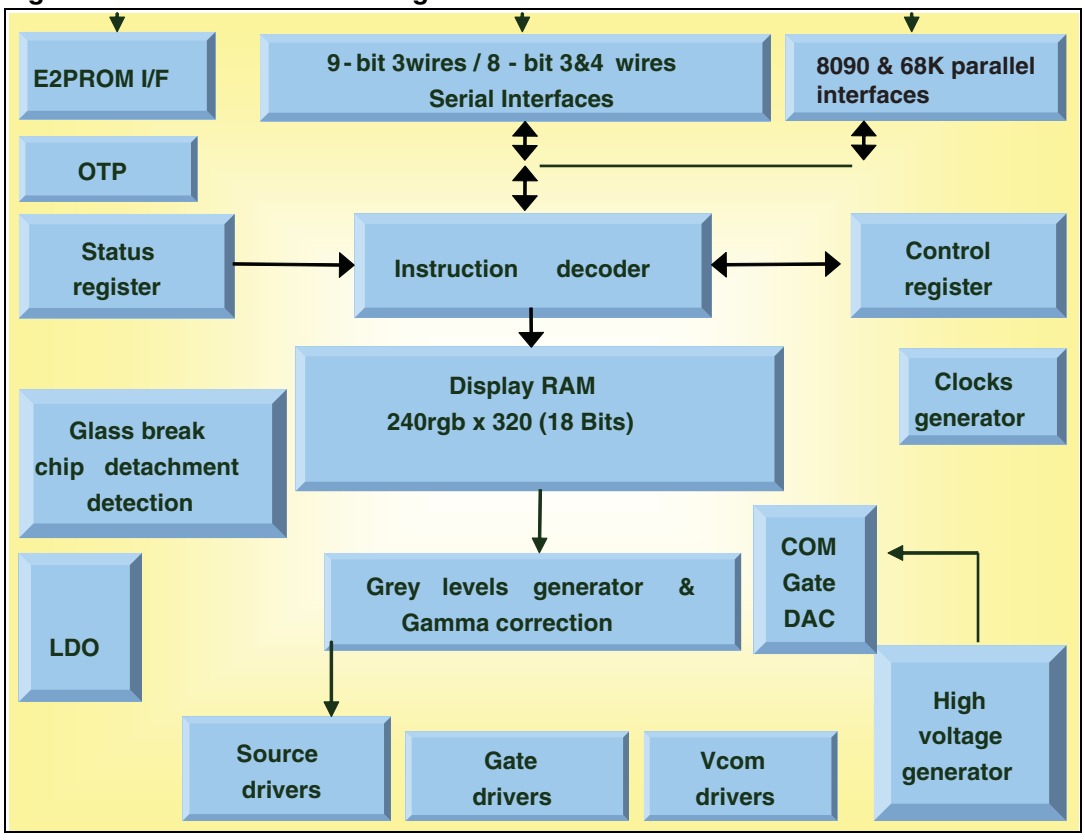
The STE2130S is designed to operate with both traditional Cap-on-Common and Cap-on-Gate panels by means of a switching Common Electrode driving scheme

Key features and benefits

- Full RAM integrated, up to 262kcol
- Integrated LDO
- Fully integrated OTP for parameters setting
- EEPROM I/F selectable for parameters setting
- Up to 4 gamma curves programmable for gamma correction
- Integrated oscillator and charge pump ◊reduced number of external components
- Low power consumption solution

Functional block diagram

Figure 1. Functional block diagram



Ordering information

Table 1. Order codes

Part number	Description
STE2130S	Gold bumped dice

Revision history

Table 2. Document revision history

Date	Revision	Changes
19-Dec-2006	1	Initial release.

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