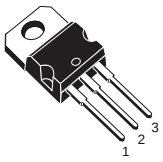
STB120NH03L
STP120NH03L

N-Channel 30V - 0.005Ω - 9A - TO-220/D^{2}PAK
STripFET™ III Power MOSFET for DC-DC Conversion

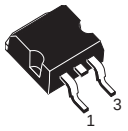
General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STB120NH03L	30V	<0.0055Ω	9A *Note 1*
STP120NH03L	30V	<0.0055Ω	9A *Note 1*

- Typical $R_{DS(on)}$ = 0.005Ω @ 10V
- $R_{DS(on)}$ *Qg Industry's Benchmark Low
- Conduction Losses Reduced
- Switching Losses Reduced
- Low Threshold Device

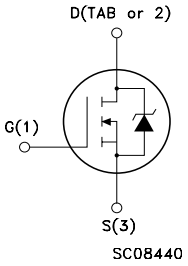


TO-220



D^{2}PAK

Internal schematic diagram



Description

These devices utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. It is ideal in high performance DC-DC converter applications where efficiency is to be achieved at very high output currents.

Applications

- Specifically designed and optimized for high efficiency DC-DC converters

Order codes

Part Number	Marking	Package	Packaging
STB120NH03L	B120NH03L	D^{2}PAK	TAPE & REEL
STP120NH03L	P120NH03L	TO-220	TUBE

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0V)	30	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20kΩ)	30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D *Note 1*	Drain Current (continuous) at T_C = 25°C	60	A
I_D *Note 1*	Drain Current (continuous) at T_C = 100°C	60	A
I_{DM} *Note 2*	Drain Current (pulsed)	240	A
P_{TOT}	Total Dissipation at T_C = 25°C	115	W
	Derating Factor	0.77	W/°C
EAS *Note 3*	Single Pulse Avalanche Energy	700	mJ
T_J T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 175	°C

Table 2. Thermal data

R_{thJC}	Thermal Resistance Junction-case Max	1.30	°C/W
R_{thJA}	Thermal Resistance Junction-amb Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 250µA V_{GS}= 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating, V_{DS} = Max Rating,T_C=125°C			1 10	µA µA
I_{GSS}	Gate Body Leakage Current (V_{DS} = 0)	V_{GS} = ±20V			±100	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250µA	1	1.8	2.5	V
$R_{DS(on)}$	Static Drain-Source On Resistance	V_{GS} = 10V I_D = 30A V_{GS} = 5V I_D = 30A		0.005 0.006	0.0055 0.0105	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} *Note 4*	Forward Transconductance	V_{DS} = 10V I_D = 30A		40		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 15V, f = 1MHz, V_{GS} = 0		4100 680 70		pF pF pF
Rg	Gate Input Resistance	f = 1MHz Gate DC Bias=0 Test Signal Level=20mV Open Drain		1.3		Ω
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=15V, I_D = 60A V_{GS} =10V *Figure 14 on page 7*		57 11.8 7.3	77	nC nC nC
Qoss *Note 5*	Output Charge	V_{DS} = 16V V_{GS} = 0		27		ns
Qgls *Note 6*	Third-quadrant Gate Charge	V_{DS} < 0 V_{GS}= 10V		55		ns

Table 5. Switching times

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 15V, I_D = 30A, R_G = 4.7Ω, V_{GS} = 10V *Figure 13 on page 7*		16 95		ns ns
$t_{d(off)}$ t_f	Off voltage Rise Time FallTime	V_{DD} = 15V, I_D = 30A, R_G = 4.7Ω, V_{GS} = 10V *Figure 15 on page 7*		48 23		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				60 240	A A
V_{SD} *Note 4*	Forward on Voltage	I_{SD} = 30A V_{GS} = 0			1.4	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 60A, di/dt = 100A/µs, V_{DD} = 30V, T_J =150°C *Figure 15 on page 7*		46 64 2.8		ns nC A

Note: 1 Value limited by wire bonding

2 Pulse width limited by safe operating area

3 Starting T_J = 25°C, I_D = 30A, V_{DD} = 15V

4 Pulsed: pulse duration = 300µs, duty cycle 1.5%

5 $Q_{oss} = C_{oss}*\Delta V_{IN}$, $C_{oss} = C_{gd} + C_{ds}$. See Power losses calculation

6 Gate charge for synchronous operation.

2.1 Electrical chraracteristics (curves)

Figure 1. Safe Operating Area

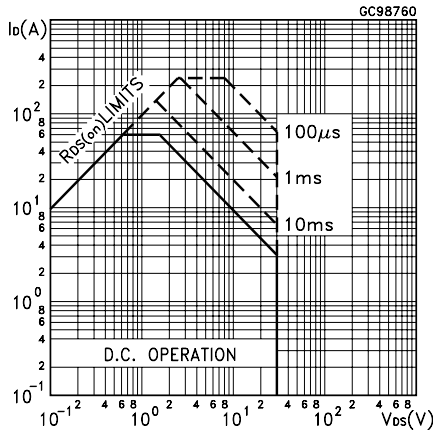


Figure 2. Thermal Impedance

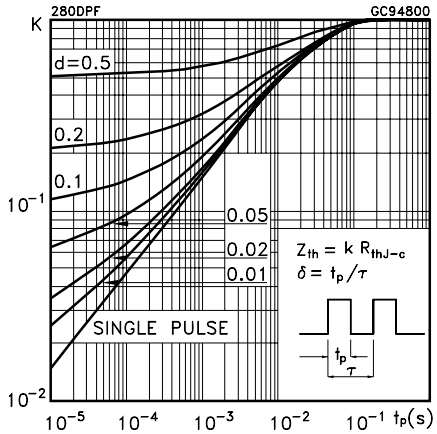


Figure 3. Output Characteristics

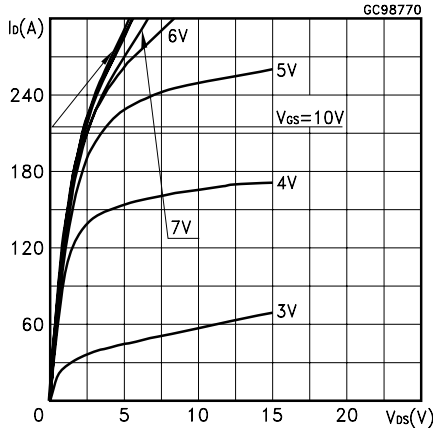


Figure 4. Transfer Characteristics

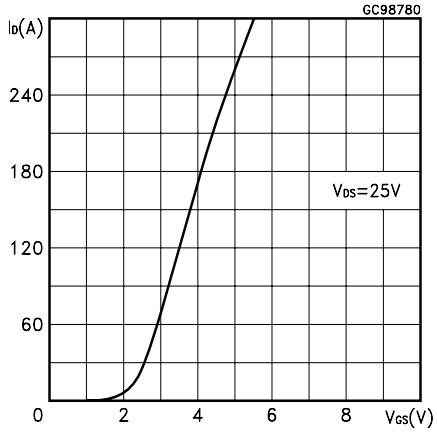


Figure 5. Transconductance

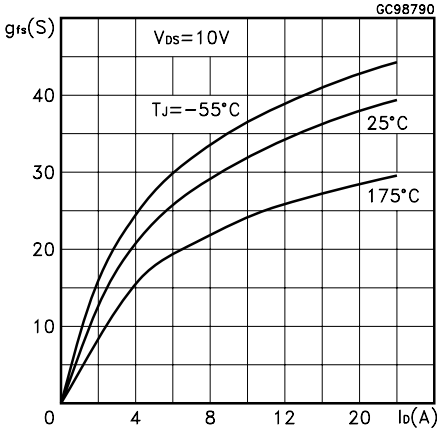


Figure 6. Static Drain-Source on Resistance

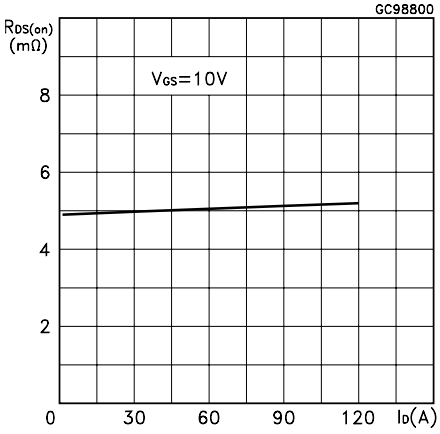


Figure 7. Gate Charge vs Gate-Source Voltage

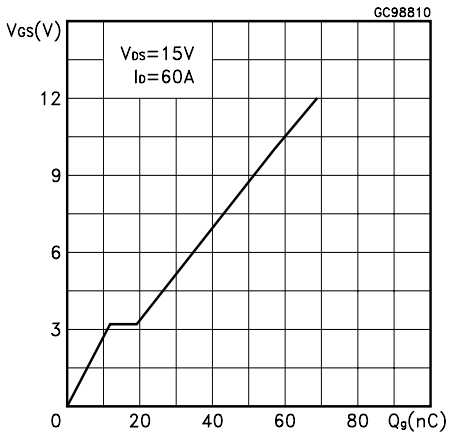


Figure 8. Capacitance Variations

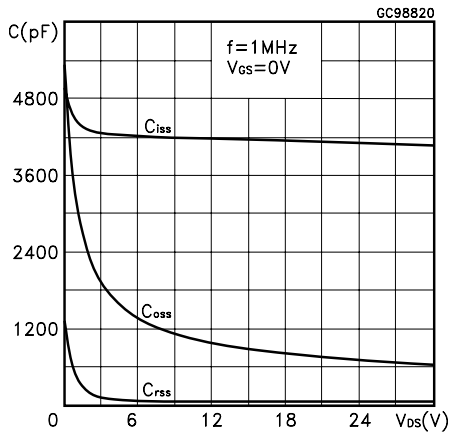


Figure 9. Normalized Gate Threshold Voltage vs Temperature

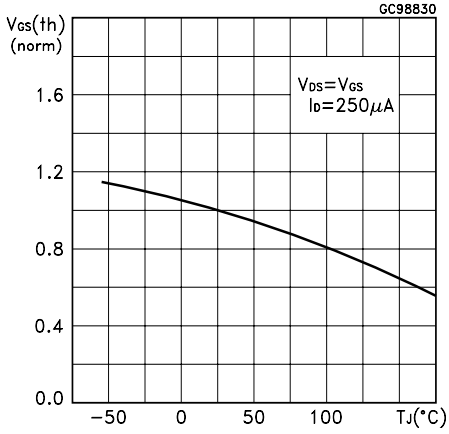


Figure 10. Normalized on Resistance vs Temperature

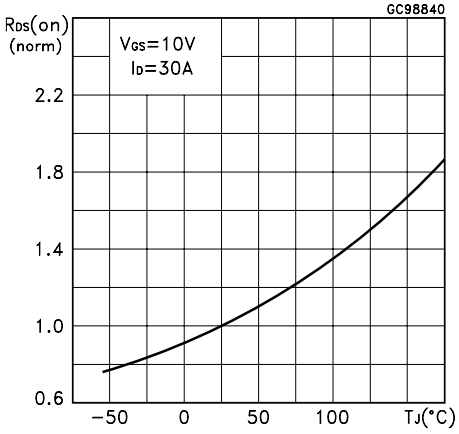


Figure 11. Source-drain Diode Forward Characteristics

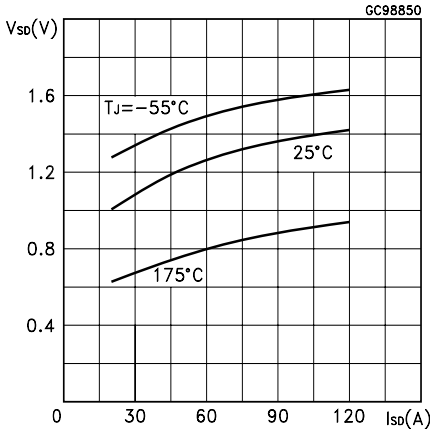
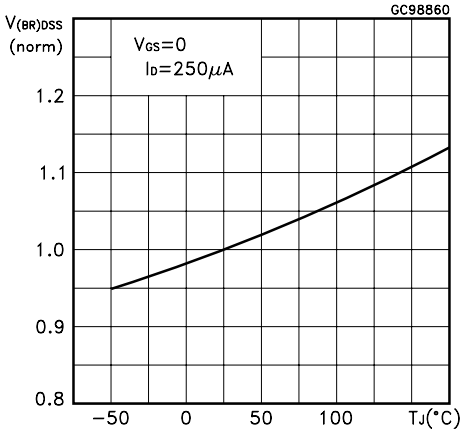


Figure 12. Normalized Breakdown Voltage vs Temperature



3 Test circuits

Figure 13. Switching Times Test Circuit For Resistive Load

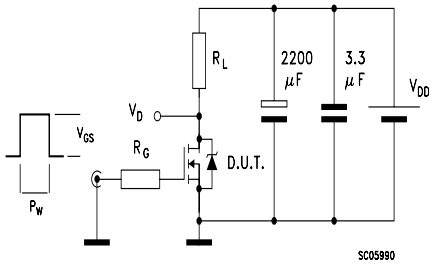


Figure 14. Gate Charge Test Circuit

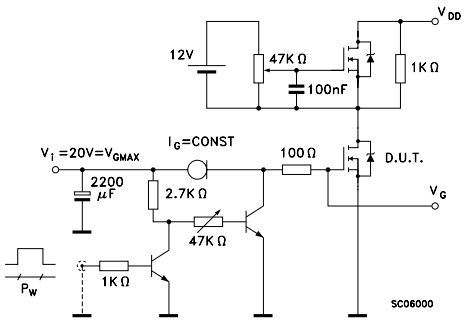


Figure 15. Test Circuit For Inductive Load Switching and Diode Recovery Times

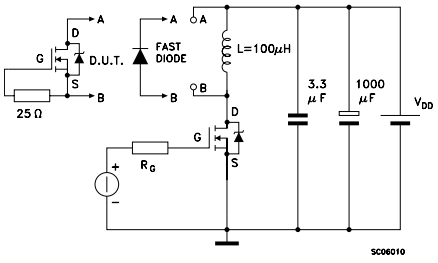


Figure 17. Unclamped Inductive Load Test Circuit

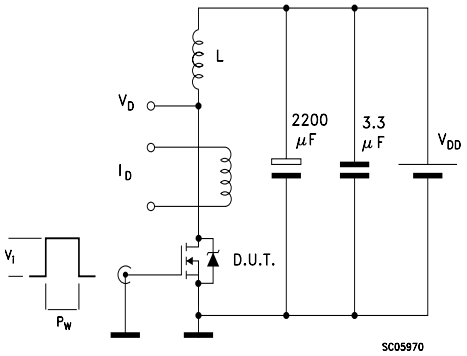
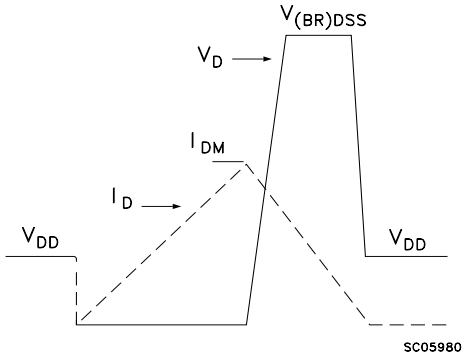


Figure 16. Unclamped Inductive Waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 7. TO-220 Mechanical Data

Dimensions						
Ref.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.035
b1	1.15		1.70	0.045		0.067
c	0.49		0.70	0.019		0.028
D	15.25		15.75	0.600		0.620
E	10.0		10.40	0.394		0.409
e	2.4		2.7	0.094		0.106
e1	4.95		5.15	0.195		0.203
F	1.23		1.32	0.048		0.052
H1	6.2		6.6	0.244		0.260
J1	2.40		2.72	0.094		0.107
L	13.0		14.0	0.512		0.551
L1	3.5		3.93	0.138		0.155
L20		16.4			0.646	
L30		28.9			1.138	
öP	3.75		3.85	0.148		0.152
Q	2.65		2.95	0.104		0.116

Figure 18. TO-220 Package Dimension

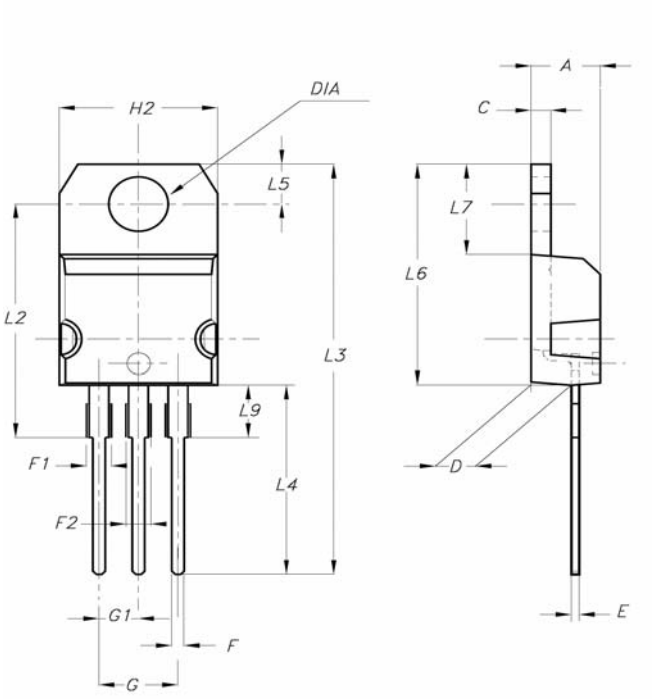
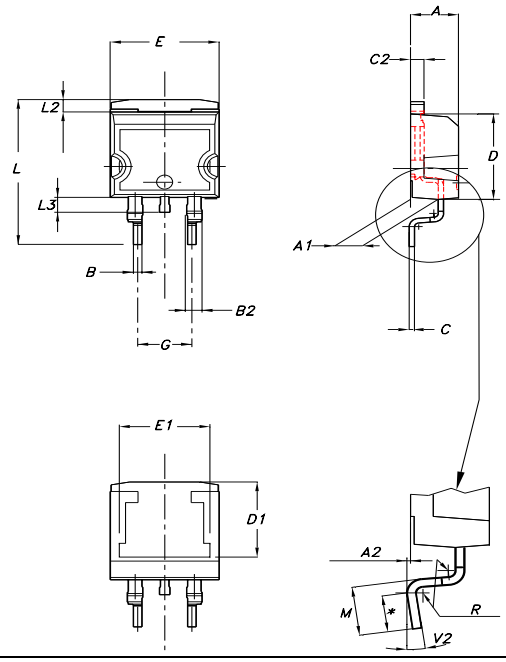


Table 8. D²PAK Mechanical Data

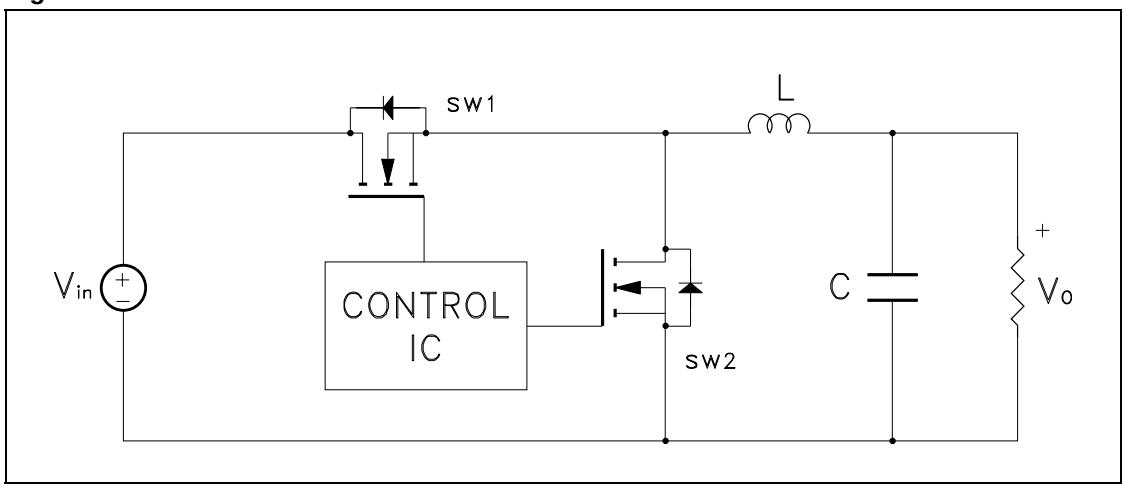
Dimensions						
Ref.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°	0°		8°

Figure 19. D²PAK Package Dimensions



5 Appendix A

Figure 20. Buck Converter: Power Losses Estimation



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Qgls to reduce the gate charge losses
- Small Coss to reduce losses due to output capacitance
- Small Qrr to reduce losses on SW1 during its turn-on
- The Cgd/Cgs ratio lower than Vth/Vgg ratio especially with low drain to source
- voltage to avoid the cross conduction phenomenon;

The high side (SW1) device requires:

- Small Rg and Ls to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Qg to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

Table 9. Power losses calculation

		High Side Switching (SW1)	Low Side Switch (SW2)
Pconduction		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1-\delta)$
Pswitching		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
Pdiode	Recovery (1)	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
Pgate(Q_G)		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P_{Qoss}		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

Table 10. Paramiters meaning

Parameter	Meaning
d	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P_{Qoss}	Output capacitance losses

6 Revision History

Date	Revision	Description of changes
12-Dec-2005	1	First release