



ST21Y068

Smartcard MCU with 68 KBytes High Density EEPROM

Data Brief

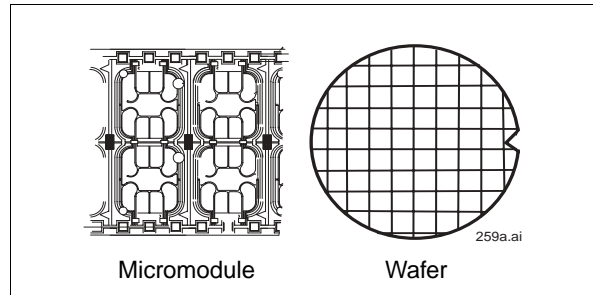
Feature summary

ST21Y068 major applications include:

- Mobile communications (GSM and CDMA)
- Java applications

Hardware features

- Enhanced 8/16-bit CPU core with 16 MBytes linear addressable memory
- 248 Kbytes User ROM
- 6 Kbytes User RAM
- 68 Kbytes User EEPROM including 64 Bytes User OTP area:
 - Highly reliable CMOS EEPROM submicron technology
 - 10-year data retention
 - 500,000 Erase/Write cycles endurance typical at 25°C
 - 1 to 64 Bytes Erase or Program in 1.5 ms
- Asynchronous Receiver Transmitter supporting ISO 7816-3 T=0 and T=1 protocols
- Two 8-bit timers with interrupt capability
- 1.8V, 3V and 5V supply voltage ranges
- External clock frequency from 1 up to 7.5 MHz
- High performance provided by:
 - CPU clock frequency up to 22 MHz
 - External clock multiplier (2x, 3x, and 4x)
- Current consumption complies with GSM specifications
- Power-saving Standby mode
- Contact assignment compatible ISO 7816-2
- ESD protection greater than 4 kV (HBM)



Security features

- Monitoring of environmental parameters
- Protection against faults
- ISO 3309 CRC calculation block
- Cryptographic performances⁽¹⁾:
 - Triple DES (with keys loaded): 9.3 μ s
 - Single DES (with keys loaded): 3.1 μ s
- True Random Number Generator
- Unique serial number on each die
- Hardware DES accelerator

Development environment

Software development and firmware generation are supported by a comprehensive set of development tools dedicated to software design and validation.

1. Typical values at 22 MHz

1 Description

The ST21Y068 product is a serial access microcontroller specially designed for cost-effective secure mobile applications.

It is based on an enhanced STMicroelectronics 8/16-bit CPU core offering **16 MBytes linear addressing space**.

It is manufactured using an advanced highly reliable ST CMOS EEPROM technology.

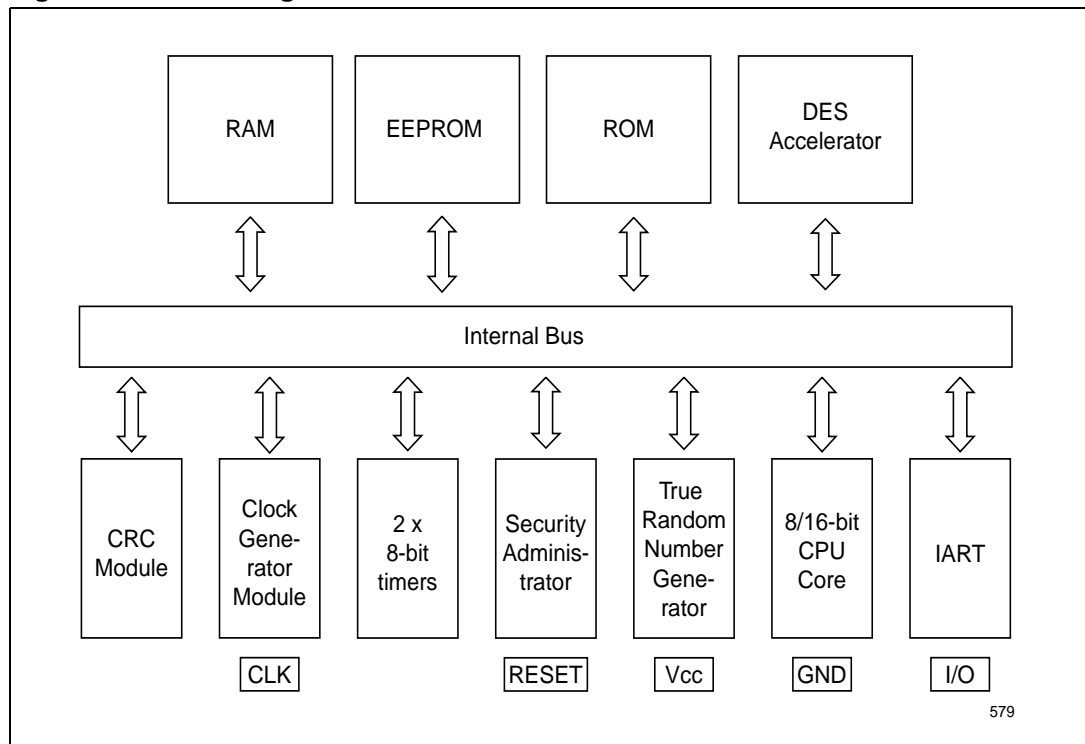
The device includes a DES accelerator.

A serial interface fully compatible with the ISO 7816-3 standard (T = 0 and T = 1) for Smartcard applications is available.

A CRC calculation block is also available and is directly accessible by the User.

The product architecture is optimized for low power consumption applications. A flexible clock generator module provides increased performance for specific current requirements.

Figure 1. Block diagram



1.1 Development environment

Development tools for smartcard products include a complete range of hardware systems and software tools from STMicroelectronics and third-party tool suppliers. The range of tools includes solutions to help you to develop and debug your application and evaluate smartcard products and their peripherals.

An Integrated Development Environment (IDE), the STMicroelectronics Visual Debug (STVD), provides a set of tools for developing embedded applications. This interface manages the project configuration, code edition, code generation and program debugging.

An emulator (SCICS) and a simulator are available for developing and validating your application code.

All the information needed to generate the application code and personalization will be collected in a delivery file (.DLV extension). This file is created using the Delivery menu of the STMicroelectronics configuration software tool, SCool.

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
13-Dec-2005	1	Initial release.
06-Feb-2006	2	Product name confirmed.
16-Mar-2006	3	CPU frequency updated.
3-Oct-2006	4	Updated Features summary
27-Oct-2006	5	Updated Features summary
20-Mar-2007	6	Updated Erase/Write cycles endurance value and Section 1.1: Development environment on page 3 .

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