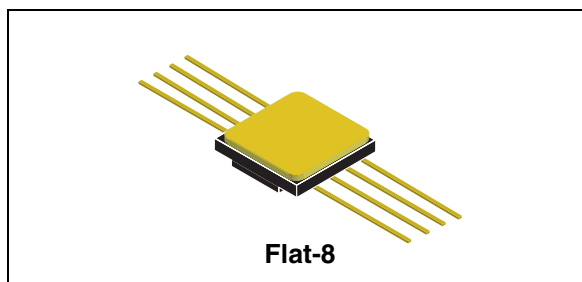


Rad-tolerant current mode PWM controller

Features

- Oscillator frequency guaranteed at 250 kHz
- Trimmed oscillator for precise frequency control
- Current mode operation to 500 kHz automatic feed forward compensation
- Latching PWM for cycle-by-cycle current limiting
- Internally trimmed reference with undervoltage lockout
- High current totem pole output
- Undervoltage lockout with hysteresis
- Low start-up and operating current
- Hermetic package
- 50 and 100 krad (Si)
- SEL free @ 120 MeV/cm²/mg at 125°C



Description

The ST1843HR and ST1845HR ICs are rad-tolerant current mode PWM controllers providing an industry standard solution for the implementation of provides the off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count.

Its radiation hardness and hermetic packaging makes it an ideal choice for aerospace and other harsh environments.

Table 1. Device summary

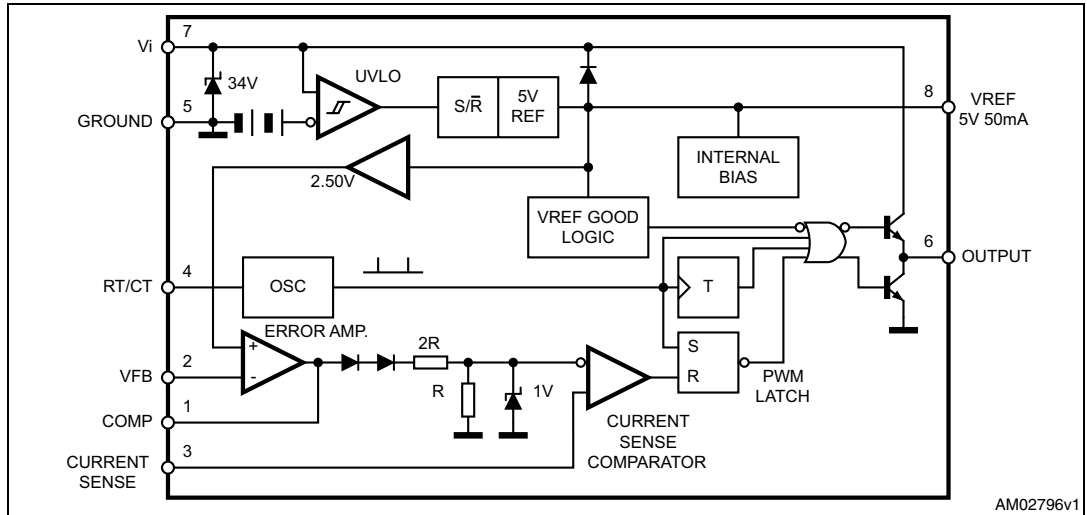
Order codes	Duty cycle max	Radiation level	Quality level	EPPL	Package	Lead finish	Mass (g)
ST1843K1	100%	50 krad (Si)	Engineering Model	-	Flat-8	Gold	0.45
ST1843FKG	100%	50 krad (Si)	According to ESCC	Target	Flat-8	Gold	0.45
ST1845K1	50%	100 krad (Si)	Engineering Model	-	Flat-8	Gold	0.45
ST1845RKG	50%	100 krad (Si)	According to ESCC	Target	Flat-8	Gold	0.45

Contents

1	Block diagram	3
2	Maximum ratings	4
3	Thermal data	4
4	Pin connection	5
5	Electrical characteristics	6
6	Radiation characteristics	9
6.1	Total dose	9
6.1.1	Bias conditions and total dose level for total dose radiation testing	9
6.1.2	Electrical measurements for total dose radiation testing	10
6.1.3	Heavy ions	12
7	Test circuit	13
8	Package mechanical data	22
9	Ordering information	23
10	Revision history	24

1 Block diagram

Figure 1. Block diagram (toggle flip flop used only in UC3844B and UC3845B)



2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_i	Supply voltage (low impedance source)	30	V
	Supply voltage ($I_i < 30\text{mA}$)	Self limiting	
I_O	Output current	± 1	A
E_O	Output energy (capacitive load)	5	mJ
	Analog inputs (pins 2, 3)	– 0.3 to 5.5	V
	Error amplifier output sink current	10	mA
P_{tot}	Power dissipation at $T_A \leq 25\text{ °C}$ (SO8)	800	mW
T_{stg}	Storage temperature range	– 65 to 150	°C
T_J	Junction operating temperature	– 40 to 150	°C

Note: All voltages are with respect to pin 5, all currents are positive into the specified terminal.

3 Thermal data

Table 3. Thermal data

Symbol	Description	Flat-8	Unit
R_{thJA}	Thermal resistance Junction-ambient. max.	100	°C/W

4 Pin connection

Figure 2. Pin connection

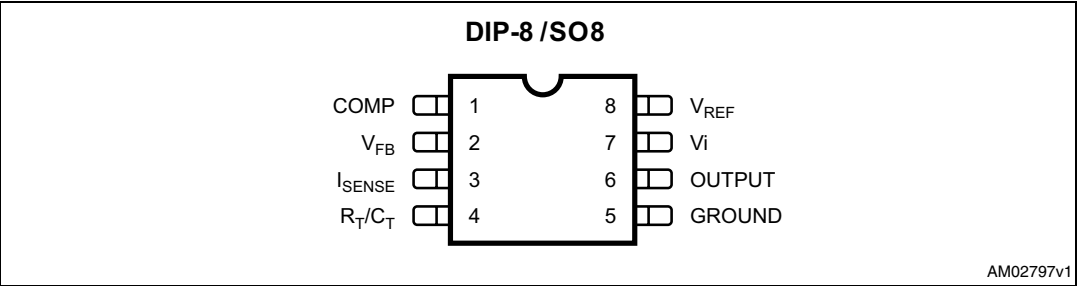


Table 4. Pin functions

No	Function	Description
1	COMP	This pin is the error amplifier output and is made available for loop compensation.
2	V _{FB}	This is the inverting input of the error amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I _{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R _T /C _T	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor R _T to V _{ref} and capacitor C _T to ground. Operation to 500 kHz is possible.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.
7	V _{CC}	This pin is the positive supply of the control IC.
8	V _{ref}	This is the reference output. It provides charging current for capacitor C _T through resistor R _T .

5 Electrical characteristics

Maximum package power dissipation limits must be respected; low duty cycle pulse techniques are used during test maintain T_J as close to T_A as possible.

Unless otherwise stated, these specifications apply for - $T_A = 22 \pm 3^\circ\text{C}$, $V_i = 15\text{ V}$, Adjust V_i above the start threshold before setting at 15 V ; $R_T = 10\text{ k}\Omega$; $C_T = 3.3\text{ nF}$.

Table 5. Electrical characteristics

Symbol	MIL-STD-883 test method	Parameter	Test conditions	Values		Unit
				Min.	Max.	
Reference section						
V _{REF}		Output voltage	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, I _o = 1mA	4.95	5.05	V
ΔV _{REF_LINE}		Line regulation	12V ≤ V _i ≤ 25V, R _T = 10kΩ; C _T = 3.3nF		0.02	V
ΔV _{REF_LOAD}		Load regulation	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, 1 ≤ I _o ≤ 20mA		25	V
I _{SC}	3011	Output short circuit		-0.18	-0.03	A
Oscillator section						
f _{OSC}		Frequency for ST1843	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, 1 ≤ I _o ≤ 20mA	49	55	kHz
		Frequency for ST1845		24.5	27.5	kHz
Δf _{OSC} /Δv		Frequency change with voltage	12V ≤ V _I ≤ 25V; R _T = 10kΩ; C _T = 3.3nF	–	1	%
I _{dischg}		Discharge current	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, 1 ≤ I _o ≤ 20mA, V _{OSC} = 2V	7.8	8.8	mA
				7.5	8.8	mA
Error amp section						
V ₂		Input voltage	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, V _{PIN1} = 2.5V	2.45	2.55	V
I _b	4001	Input bias current	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, V _{FB} = 5V	-1		mA
A _{VOL}		A _{VOL}	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, 2V ≤ V _o ≤ 4V	65		dB
PSRR	4003	Power supply rejec. ratio	12V ≤ V _i ≤ 25V; R _T = 10kΩ; C _T = 3.3nF	60		dB
I _{o_sink}		Output sink current	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, V _{PIN2} = 2.7V, V _{PIN1} = 1.1V	2		mA
I _{o_source}		Output source current	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, V _{PIN2} = 2.2V, V _{PIN1} = 5V		-0.5	mA

Table 5. Electrical characteristics (continued)

Symbol	MIL-STD-883 test method	Parameter	Test conditions	Values		Unit
				Min.	Max.	
V _{OH}		V _{OUT} high	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, V _{PIN2} = 2.3V, R _L = 15kΩ to GND	5		V
V _{OL}		V _{OUT} low	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, V _{PIN2} = 2.3V, R _L = 15kΩ to GND		1.1	V
Current sense section						
G _V	4004	Gain	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, ₍₂₎ ₍₃₎	2.85	3.15	V/V
V ₃		Maximum input signal	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF, V _{PIN1} = 2.3V ⁽²⁾	0.9	1.1	V
SVR		Supply voltage rejection	12 ≤ V _i ≤ 25V; R _T = 10kΩ; C _T = 3.3nF, ⁽¹⁾	60		dB
I _b	4001	Input bias current	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF	-10		mA
D _O	3003	Delay to output	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF		300	ns
Output section						
V _{OL1}	3007	Output low level	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF; I _{SINK} = 20mA		0.4	V
V _{OL2}			V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF; I _{SINK} = 200mA		2.2	V
V _{OH1}	3006	Output high level	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF; I _{SOURCE} = 20mA	13		V
V _{OH2}			V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF; I _{SOURCE} = 200mA	12		V
V _{OLS}		UVLO saturation	V _I = 6V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF; I _{SINK} = 1mA		1.1	V
t _r	3004	Rise time	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF;		150	ns
t _f		Fall time	C _L = 1nF		150	ns
Under-voltage lockout section						
V _{TH}		Start threshold	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF	7.8	9	V
V _{MIN}		Min operating voltage after turn-on	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF	7	8.2	V
DC _{MAX}		Max duty cycle for ST1843	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF	47	50	%
		Max duty cycle for ST1845		94	100	%
DC _{MIN}		Min duty cycle	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF		0	%
Total standby current						
I _{st}		Start-up current	V _I = 15V ⁽¹⁾ ; R _T = 10kΩ; C _T = 3.3nF		0.5	mA

Table 5. Electrical characteristics (continued)

Symbol	MIL-STD-883 test method	Parameter	Test conditions	Values		Unit
				Min.	Max.	
I_i	3005	Operating supply current	$V_I = 15V^{(1)}$; $R_T = 10k\Omega$; $C_T = 3.3nF$ $V_{PIN2} = V_{PIN3} = 0V$		17	mA
V_{IZ}		Zener voltage	$V_I = 15V^{(1)}$; $R_T = 10k\Omega$; $C_T = 3.3nF$ $I_i = 25mA$	30		V

1. Adjust V_i above the start threshold before setting at 15V

2. Parameter measured at trip point of latch with $V_{PIN2} = 0$.

3. Gain defined as:

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}}; 0 \leq \Delta V_{PIN3} \leq 0.8V$$

6 Radiation characteristics

6.1 Total dose

The total dose results are provided in the following table:

Table 6. Total dose performance

Device	Total dose
ST1843HR	50 krad (Si)
ST1845HR	100 krad (Si)

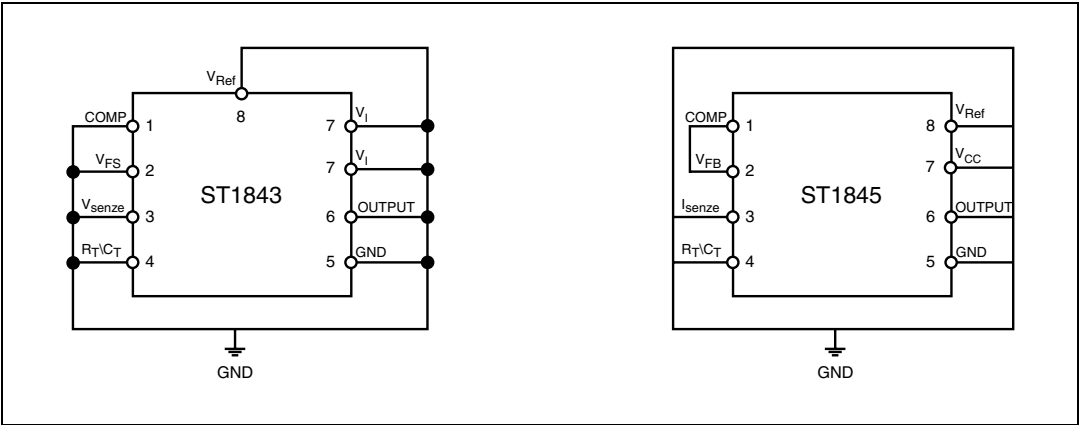
These results are obtained on the following conditions:

6.1.1 Bias conditions and total dose level for total dose radiation testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information here in or in purchaser order.

Figure 3. Unbias conditions



6.1.2 Electrical measurements for total dose radiation testing

Prior to irradiation testing the devices shall have successfully met room temperature electrical measurements specified herein.

Unless otherwise stated the measurements shall be performed at $T_A = +22 \pm 3^\circ\text{C}$

The test methods and test conditions shall be as per the corresponding test defined in electrical measurements at room temperature. The parameters to be measured during and on completion of irradiation testing are shown below.

Table 7. Electrical parameter during irradiation testing

Symbol	Parameter	Test conditions	Values		Unit
			Min.	Max.	
Reference section					
V _{REF}	Output voltage for ST1843	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF, I _o = 1mA	4.95	5.15	V
	Output voltage for ST1845		4.85	5.15	
ΔV _{REF_LINE}	Line regulation	12V ≤ V _i ≤ 25V, R _T = 10kΩ; C _T = 3.3nF		0.02	V
ΔV _{REF_LOAD}	Load regulation	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF, 1 ≤ I _o ≤ 20mA		0.025	V
I _{SC}	Output short circuit current	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF	-0.18	-0.03	A
Oscillator section					
F _{OSC}	Frequency	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF	49	65	kHz
ΔF _{OSC} / ΔV	Frequency change with voltage	12V ≤ V _i ≤ 25V, R _T = 10kΩ; C _T = 3.3nF	-1	1	%
IDISCHG	Discharge current	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; V _{OSC} = 2V	0.0078	0.0088	A
Error amp section					
V ₂	Input voltage for ST1843	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; V _{PIN1} = 2.5V	2.45	2.6	V
	Input voltage for ST1845		2.45	2.55	
I _b	Input bias current ST1843	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; V _{FB} = 5V	-2.75		μA
	Input bias current ST1845		-2.8		
AVOL	AVOL for ST1843	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; 2V ≤ V _o ≤ 4V	60		dB
	AVOL for ST1845		62		
PSRR	Power supply rejection ratio	12V ≤ V _i ≤ 25V, R _T = 10kΩ; C _T = 3.3nF	60		dB
IO_SINK	Output sink current	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; V _{PIN2} = 2.7V; V _{PIN1} = 1.1V	2		mA
IO_SOURCE	Output source current	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; V _{PIN2} = 2.3V; V _{PIN1} = 5V		-0.5	mA
V _{OH}	VOUT high	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; V _{PIN2} = 2.3V; R _L = 15K to GND	5		V
V _{OL}	VOUT low	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; V _{PIN2} = 2.3V; R _L = 15kΩ to pin		1.1	V

Table 7. Electrical parameter during irradiation testing (continued)

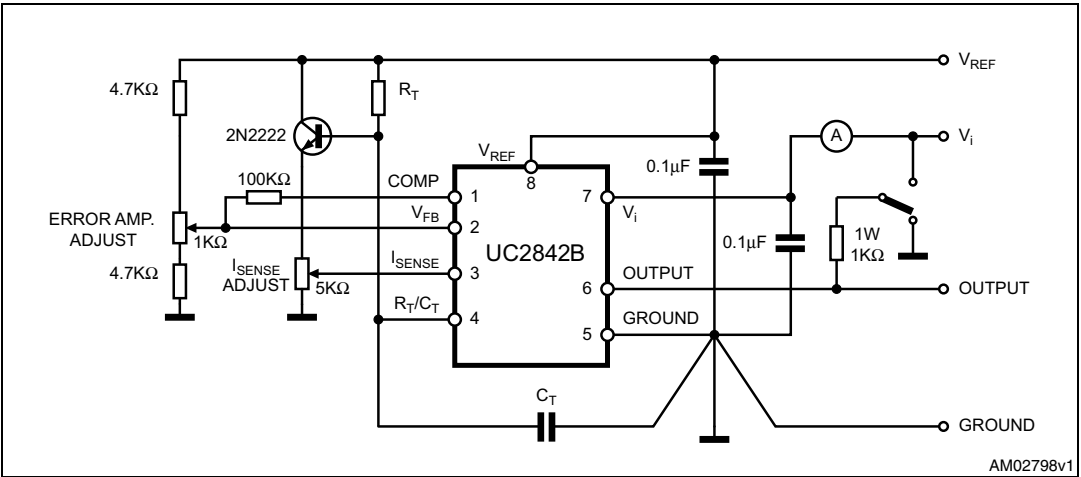
Symbol	Parameter	Test conditions	Values		Unit
			Min.	Max.	
Current sense section					
G _V	Gain	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF;	2.85	3.15	V/V
V3	Maximum input signal	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; VPIN1 = 2.3V;	0.9	1.1	V
SVR	Supply voltage rejection	12V ≤ V _I ≤ 25V; R _T = 10kΩ; C _T = 3.3nF;	60		dB
I _b	Input bias current ST1843	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF;	-50		μA
	Input bias current ST1845		-45		
D _O	Delay to output	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF;		300	ns
Output section					
V _{OL1}	Output low level	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; I _{SINK} = 20mA		0.4	V
V _{OL2}	Output low level	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; I _{SINK} = 200mA		2.2	V
V _{OH1}	Output high level	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; I _{SOURCE} = 20mA	13		V
V _{OH2}	Output high level	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; I _{SOURCE} = 200mA	12		V
V _{OLS}	UVLO saturation	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; I _{SINK} = 1mA		1.1	V
T _R	Rise time	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; C _L = 1nF		180	ns
T _F	Fall time	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; C _L = 1nF		180	ns
Under-voltage lockout section					
V _{TH}	Start threshold for ST1843	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF;	7.8	9.5	V
	Start threshold for ST1845		7.8	10.5	
V _{MIN}	Min operating voltage after turn-on for ST1843	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF;	7	8.6	V
	Min operating voltage after turn-on for ST1845		7	9	
DCMAX	Max duty cycle	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF;	94	100	%
DCMIN	Min duty cycle	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF;		0	%
Total stand-by current					
I _{ST}	Start-up current	V _I = 6.5V; R _T = 10kΩ; C _T = 3.3nF;		0.5	mA
I _i	Operating supply current	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; VPIN2 = VPIN3 = 0V		17	mA
V _{IZ}	Zener voltage	V _I = 15V; R _T = 10kΩ; C _T = 3.3nF; I _i = 25mA	30		V

6.1.3 Heavy Ions

Both devices have been tested SEL free at 120 MeV/cm²/mg at 125°C

7 Test circuit

Figure 4. Open loop test circuit



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5 kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 5. Timing resistor vs. oscillator frequency

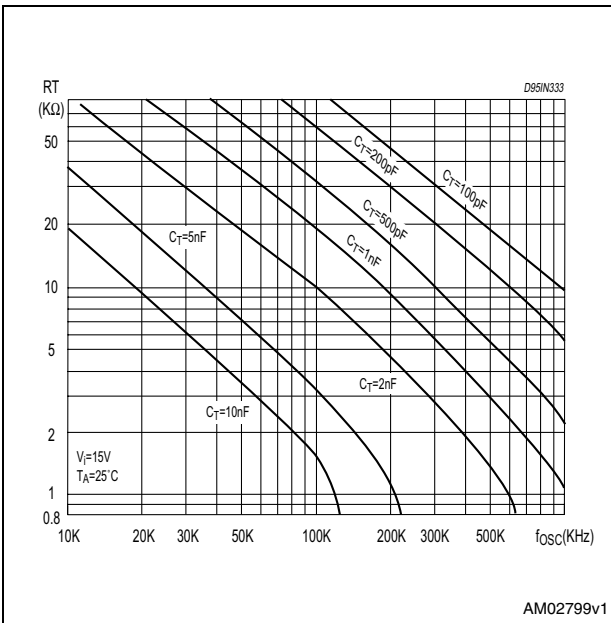


Figure 6. Output dead-time vs. oscillator frequency

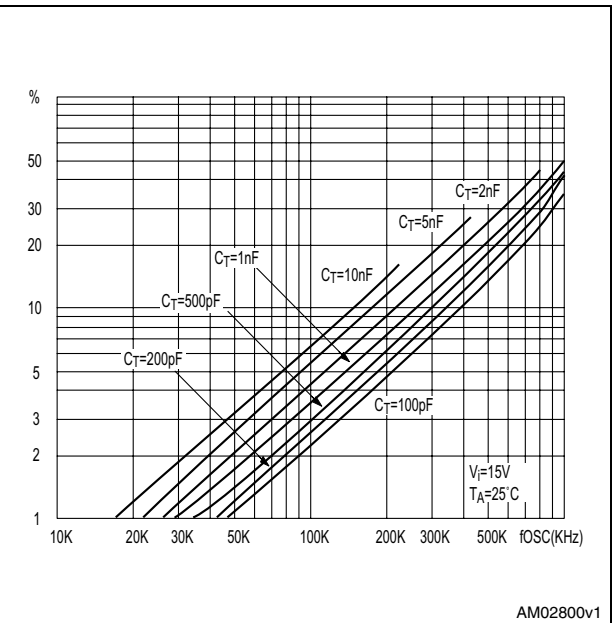


Figure 7. Oscillator discharge current vs. temperature

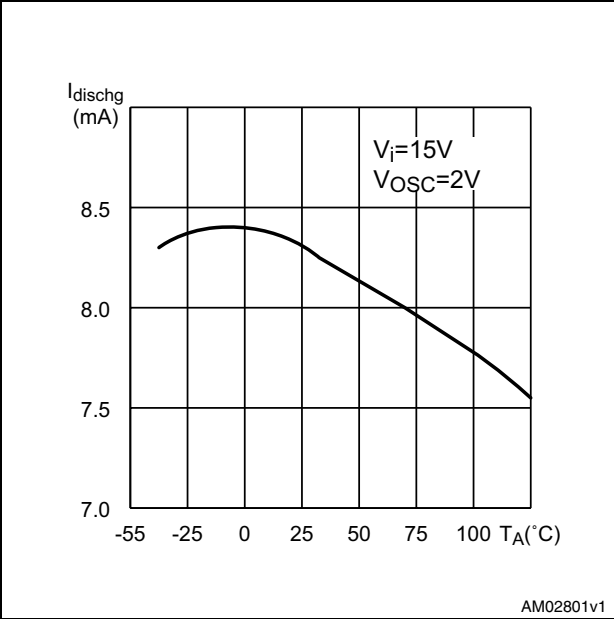


Figure 8. Maximum output duty cycle vs. timing resistor

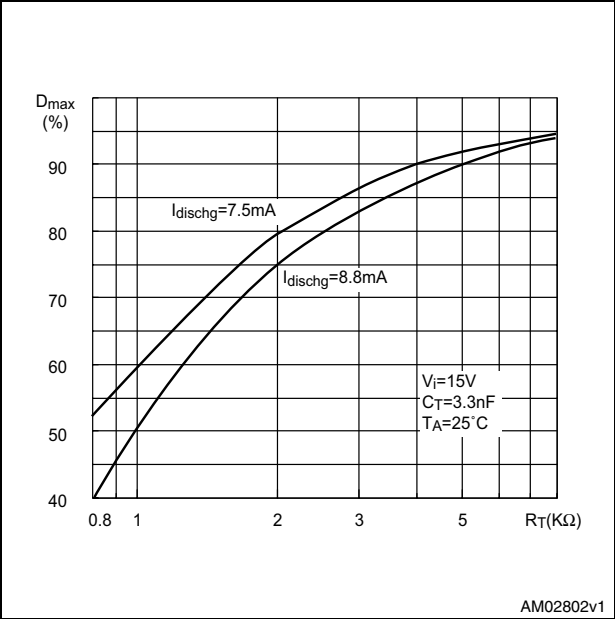


Figure 9. Error amp open-loop gain and phase vs. frequency

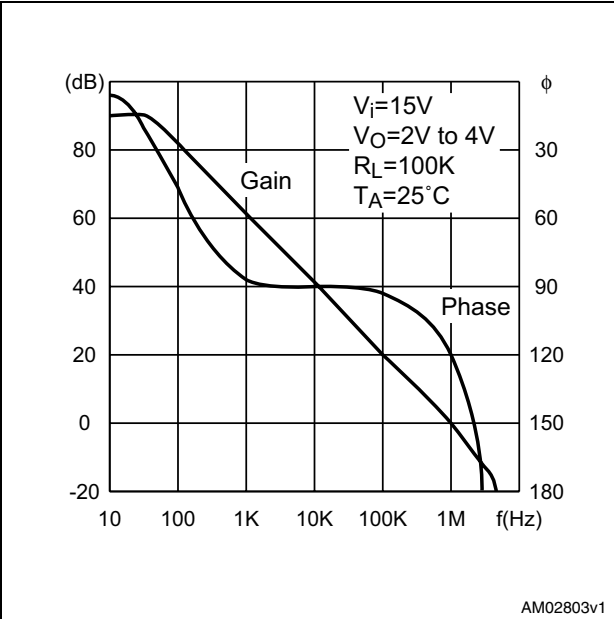


Figure 10. Current sense input threshold vs. error amp output voltage

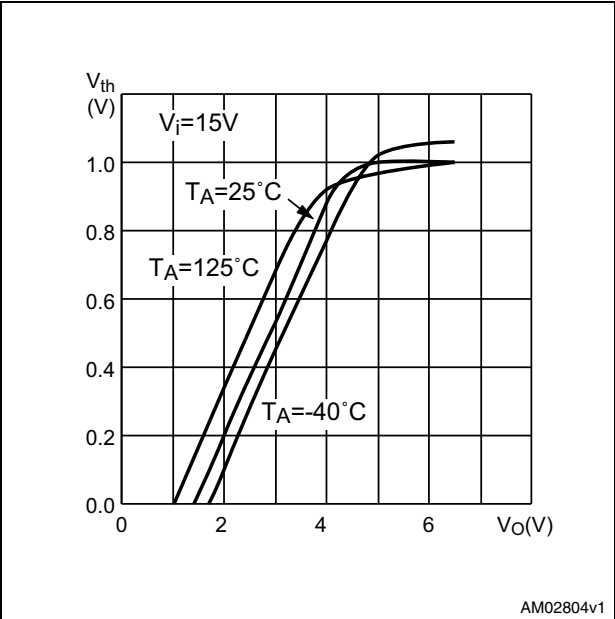


Figure 11. Reference voltage change vs. source current

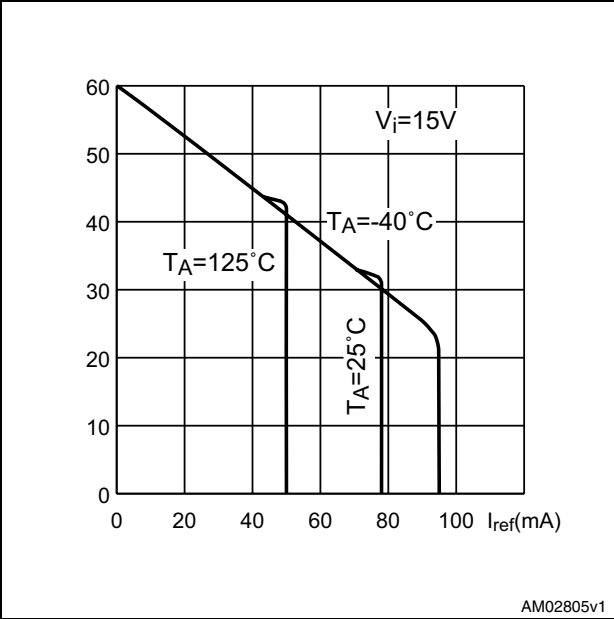


Figure 12. Reference short circuit current vs. temperature

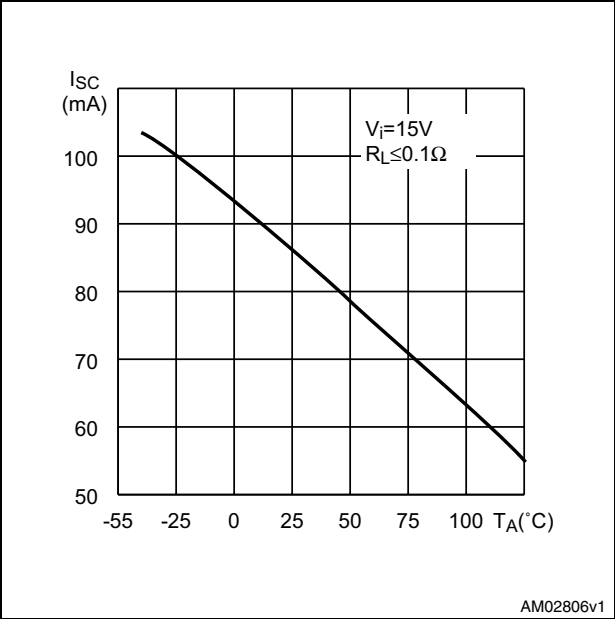


Figure 13. Output saturation voltage vs. load current

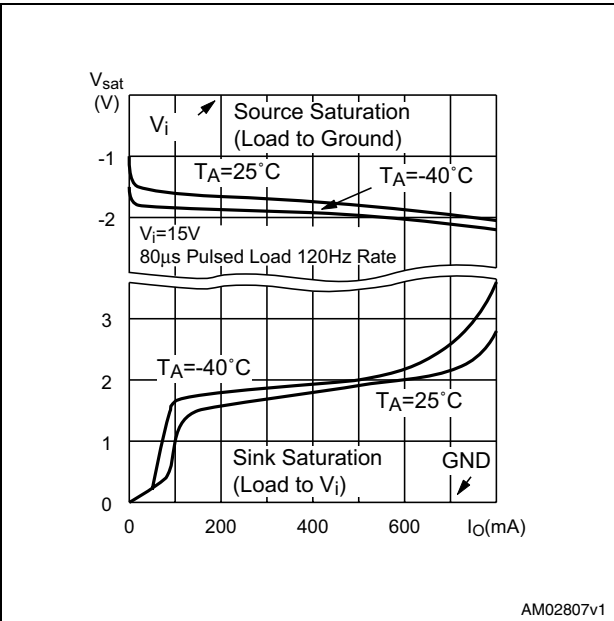


Figure 14. Supply current vs. supply voltage

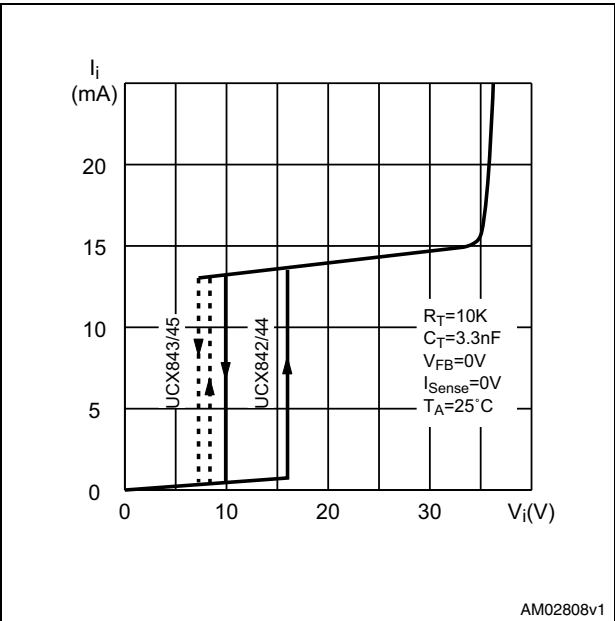


Figure 15. Output waveform

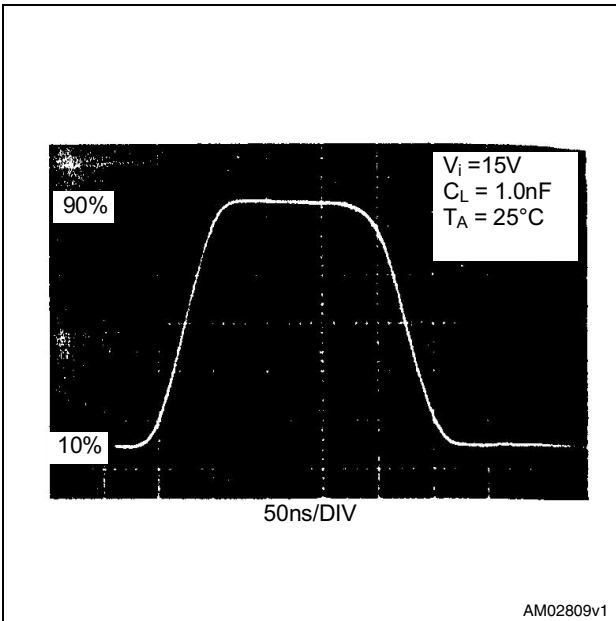


Figure 16. Output cross conduction

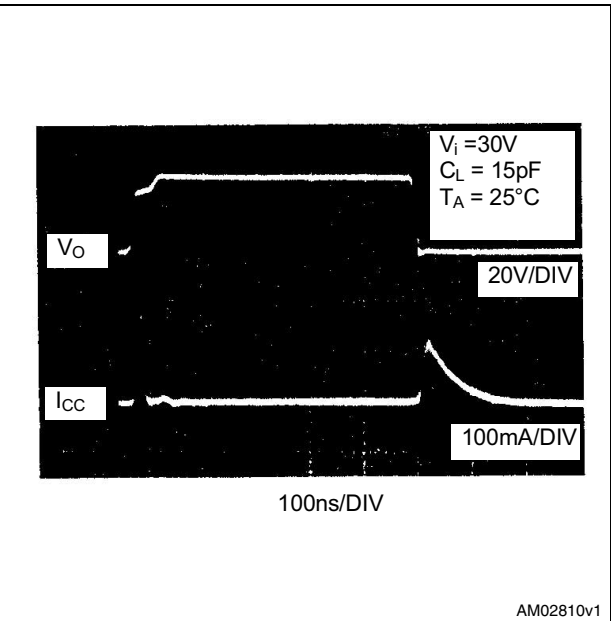


Figure 17. Oscillator and output waveforms

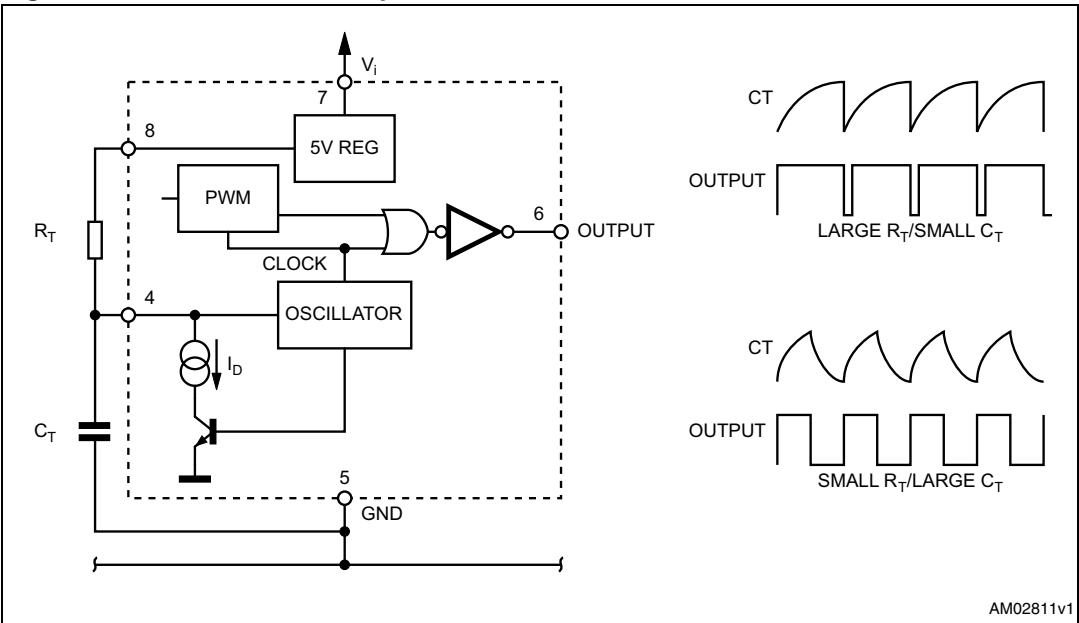


Figure 18. Error amp configuration

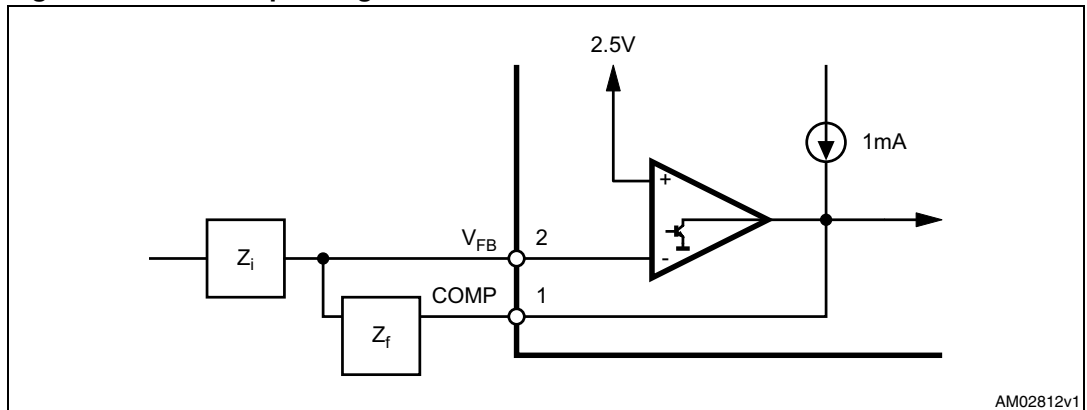


Figure 19. Under voltage lockout

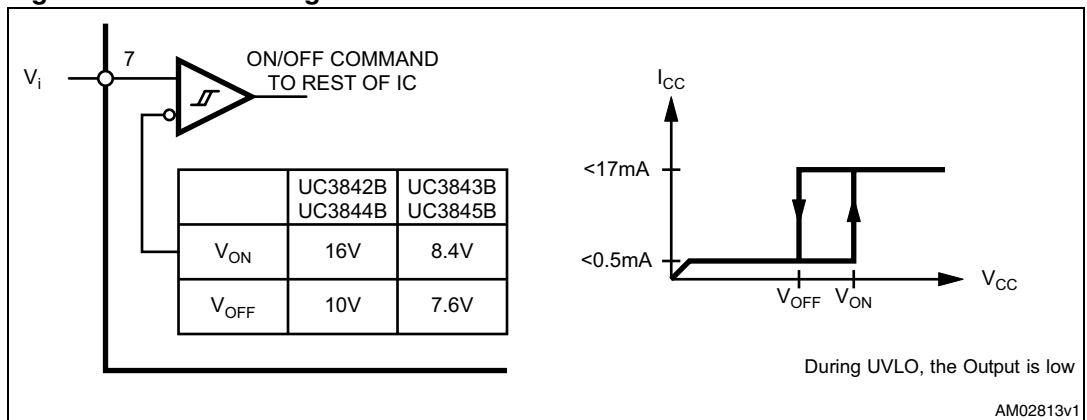
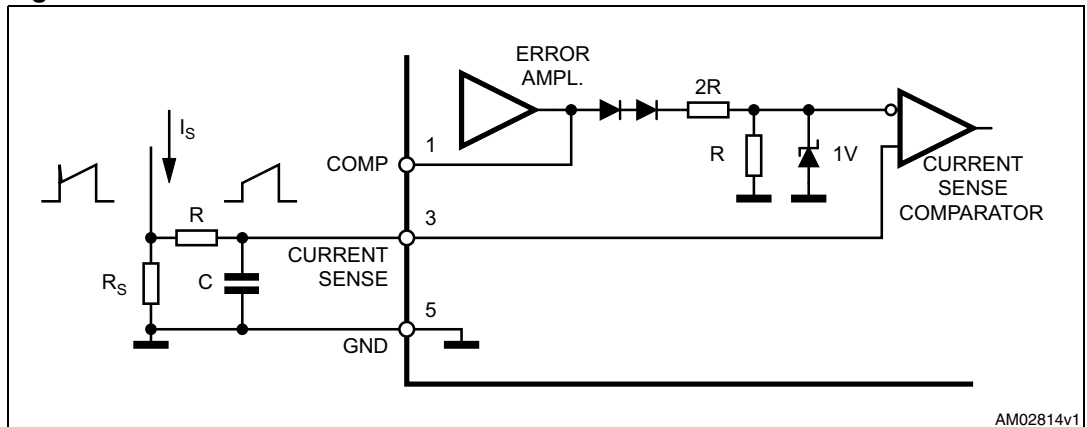


Figure 20. Current sense circuit



Peak current (i_s) is determined by the formula:

$$I_{Smax} \approx \frac{1.0V}{R_S}$$

A small RC filter may be required to suppress switch transients.

The diagram shows a Class-D audio amplifier circuit. The input signal is applied to the non-inverting input of a comparator. The comparator's output is connected to a latch (S, R, Q, L) and a MOSFET driver. The MOSFET driver consists of a MOSFET and a diode. The MOSFET's gate is connected to the output of the comparator. The MOSFET's drain is connected to the primary of a transformer. The secondary of the transformer is connected to a diode, a resistor, and an inductor. The output is taken across the inductor. The feedback loop consists of a transformer, a diode, a resistor, and an inductor. The feedback signal is applied to the inverting input of the comparator. The circuit is divided into two sections by a dashed line labeled 'ISOLATION BOUNDARY'.

ISOLATION BOUNDARY

V_{GS} Waveforms

50% DC

25% DC

$$I_{pk} = \frac{V_{(pin 1)} - 1.4}{3R_S} \left(\frac{N_S}{N_P} \right)$$

AM02816v1

Figure 23. Latched shutdown

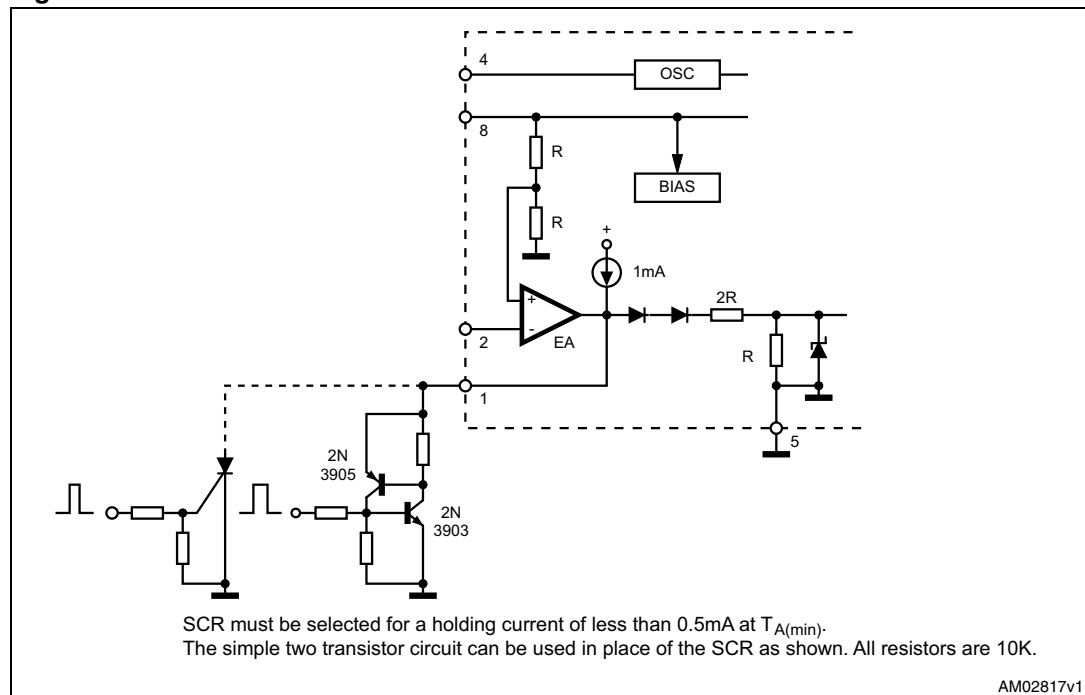


Figure 24. Error amplifier compensation

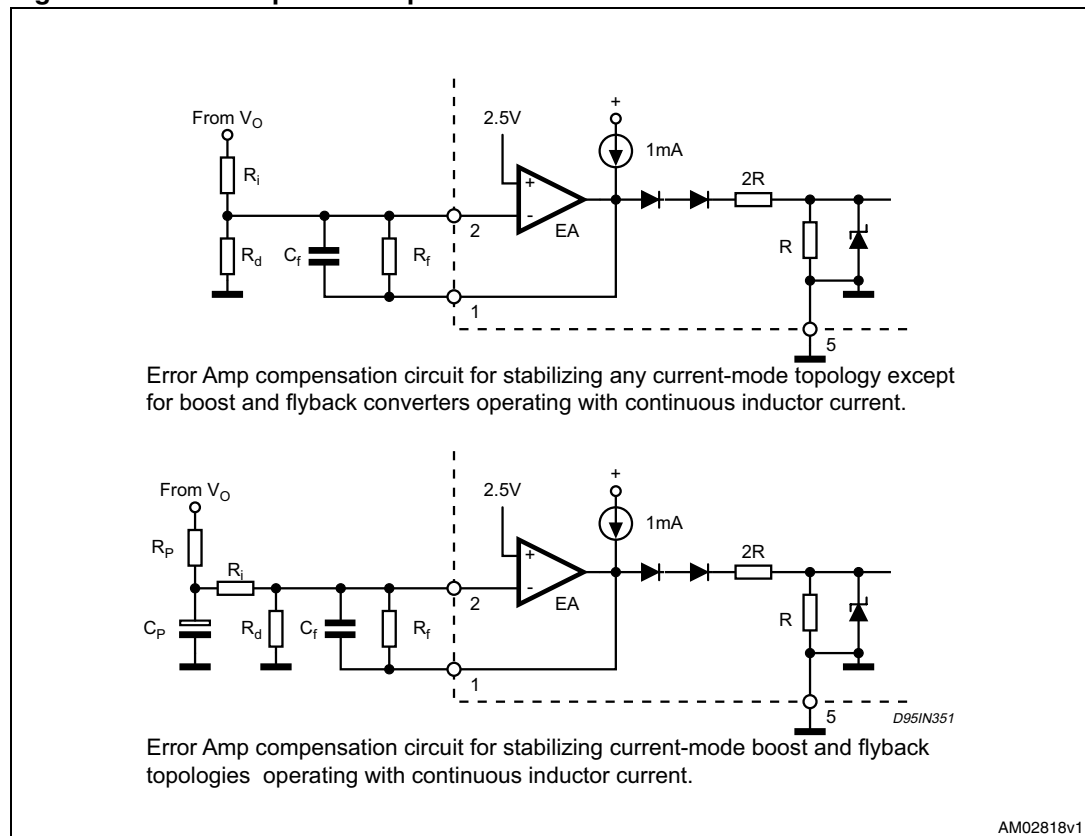


Figure 25. External clock synchronization

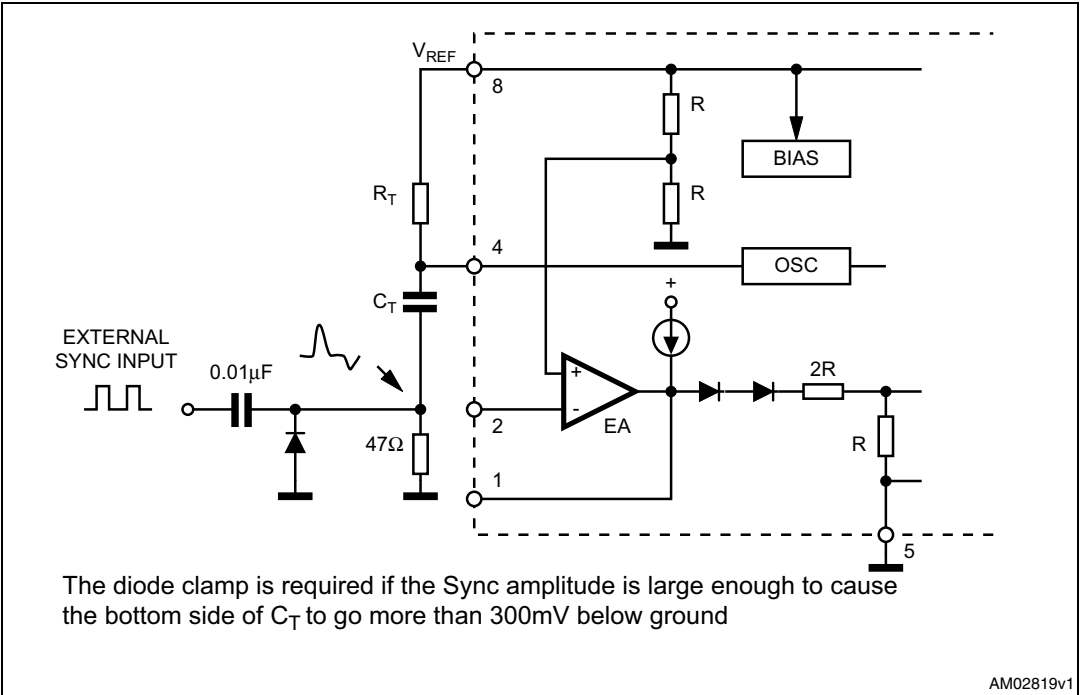


Figure 26. External duty cycle clamp and multi unit synchronization

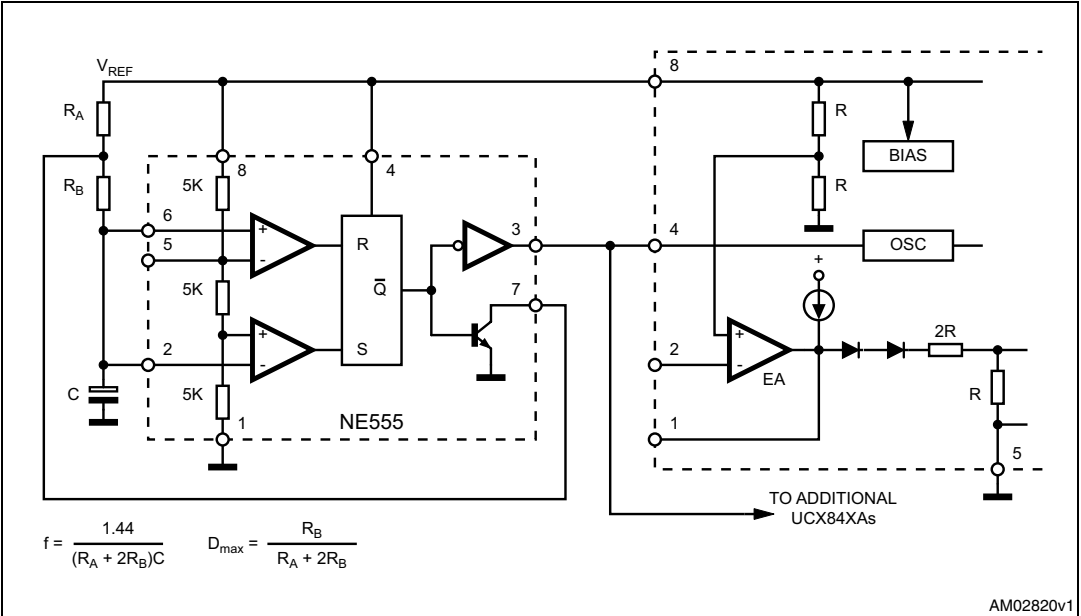


Figure 27. Soft-start circuit

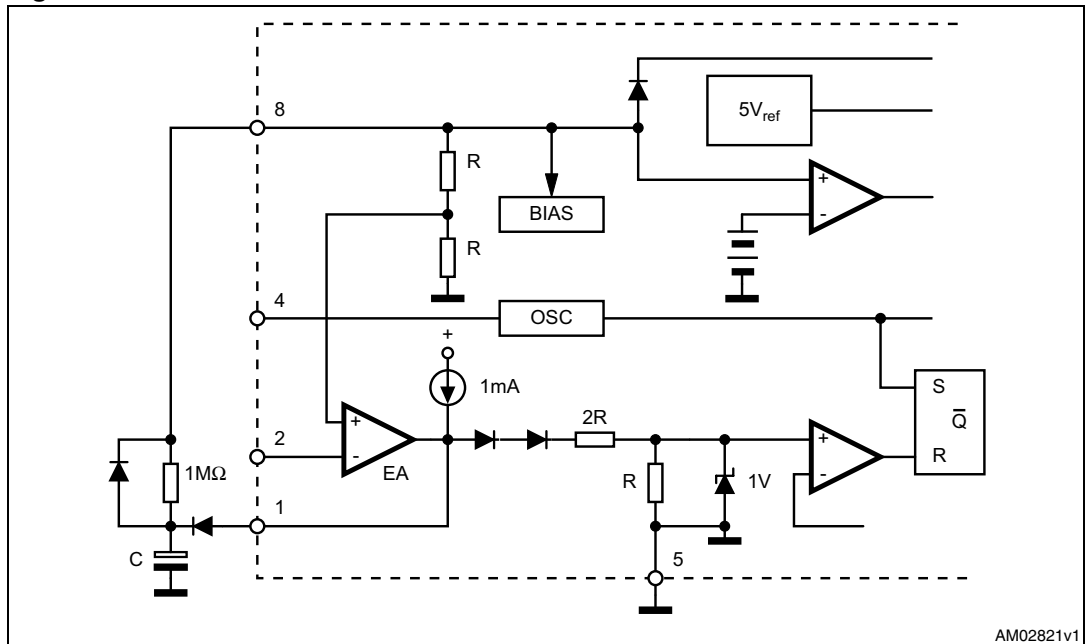
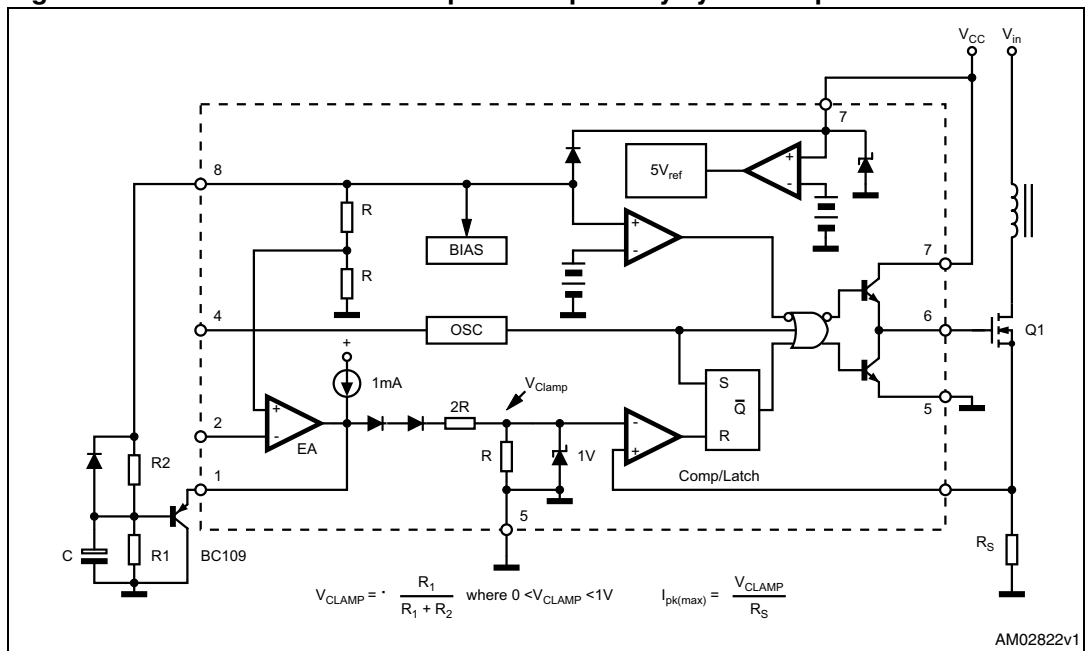


Figure 28. Soft-start and error amplifier output duty cycle clamp



$$V_{CLAMP} = \frac{R_1}{R_1 + R_2} \text{ where } 0 < V_{CLAMP} < 1V$$

$$I_{pk(max)} = \frac{V_{CLAMP}}{R_S}$$

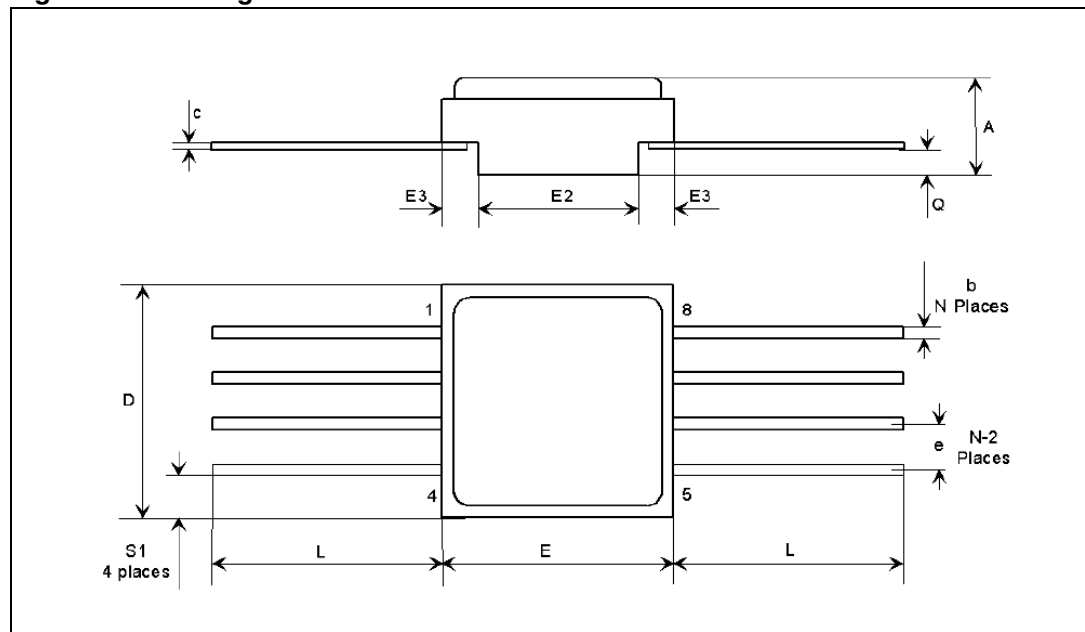
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. Flat-8 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	2.24	2.44	2.64	0.088	0.096	0.104
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.16	0.004	0.005	0.006
D	6.35	6.48	6.61	0.250	0.255	0.260
E	6.35	6.48	6.61	0.250	0.255	0.260
E2	4.32	4.45	4.58	0.170	0.175	0.180
E3	0.88	1.01	1.14	0.035	0.040	0.045
e		1.27			0.050	
L	6.51	-	7.38	0.256	-	0.291
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.92	1.12	1.32	0.036	0.044	0.052
N	08			08		

Figure 29. Package dimensions



9 Ordering information

Table 9. Ordering information

Order codes	Quality level	EPPL	Package	Lead finish	Marking	Packing
ST1843K1	Engineering Model	-	Flat-8	Gold	ST1843K1	Strip pack
ST1843FKG	According to ESCC	Target	Flat-8	Gold	ST1843FKG	Strip pack
ST1845K1	Engineering Model	-	Flat-8	Gold	ST1845K1	Strip pack
ST1845RKG	According to ESCC	Target	Flat-8	Gold	ST1845RKG	Strip pack

10 Revision history

Table 10. Document revision history

Date	Revision	Changes
12-Sep-2011	1	First revision

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