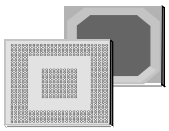
SPEAr1310

Dual-core Cortex A9 embedded MPU for communications

Data brief

Features

- CPU subsystem:
  - 2x ARM Cortex A9 cores, up to 600 MHz
  - Supporting both symmetric (SMP) and asymmetric (AMP) multiprocessing
  - 32+32 KB L1 Instructions/Data cache per core with parity check
  - Shared 512 KB L2 cache (ECC protected) with parity check
  - Accelerator coherence port (ACP)
- Bus: 64-bit multilayer network-on-chip
- Memories:
  - 32 KB BootROM
  - 32 KB internal SRAM
  - Multi-port controller (MPMC) for external DDR2-800/DDR3-1066 with 16/32 bits datapath, up to 1GB addressable with ECC option for SEC/DED
  - Controller (FSMC) for external NAND Flash, parallel NOR Flash and asynchronous SRAM
  - Controller (SMI) for external serial NOR flash
- Connectivity:
  - 2x Giga/Fast Ethernet ports (for external GMII/RGMII/MII PHY)
  - 3x Fast Ethernet (for external SMII/RMII PHY)
  - 3x PCIe 2.0 links (embedded PHY)
  - 3x SATA gen-2 host port
  - 1x 32-bit PCI expansion bus (up to 66 MHz)
  - 2x USB 2.0 host ports with integrated PHYs
  - 1x USB2.0 OTG port with integrated PHY
  - 2x CAN 2.0 a/b interfaces
  - 2x TDM/E1 HDLC controllers with 256/32 time slots per frame respectively
  - 2x HDLC controllers for external RS485 PHYs



PBGA (23 x 23 mm)

  - 2x I2S ports for external audio/modem
  - 6x UARTs (up to 5 Mbaud)
  - 1x SSP port (SPI and other protocols), master/slave, up to 41 Mbps
  - 2x I2C ports master/slave
- Integrated support for external peripherals:
  - TFT LCD controller, up to 1920 x 1200 (60 Hz), 24 bpp
  - Touchscreen I/F (4-wire resistive)
  - 9 x 9 keyboard controller
  - Memory card interface (MCIF) supporting SD/SDIO 2.0, SDHC, MMC 4.2/4.3, CF/CF+ Rev 4.1, XD
- Expansion interface (EXPI)
- Security: C3 cryptographic accelerator
- 13x timers and 1x real time clock
- Miscellaneous functions:
  - 2x high-performance 8-channels DMA controllers
  - JPEG HW codec
  - 10 bit ADC, up to 1 Msps, 8 inputs with autoscan capability
  - Programmable bidirectional GPIO signals with interrupt capability
  - 510 + 209 one time programmable (OTP) bits
  - Embedded sensor for junction temperature monitoring
  - JTAG-PTM (debugging and test interface)
- Power saving features:
  - Power islands for leakage reduction
  - IP clock gating for dynamic power reduction
  - Dynamic frequency scaling

Contents

1 Description

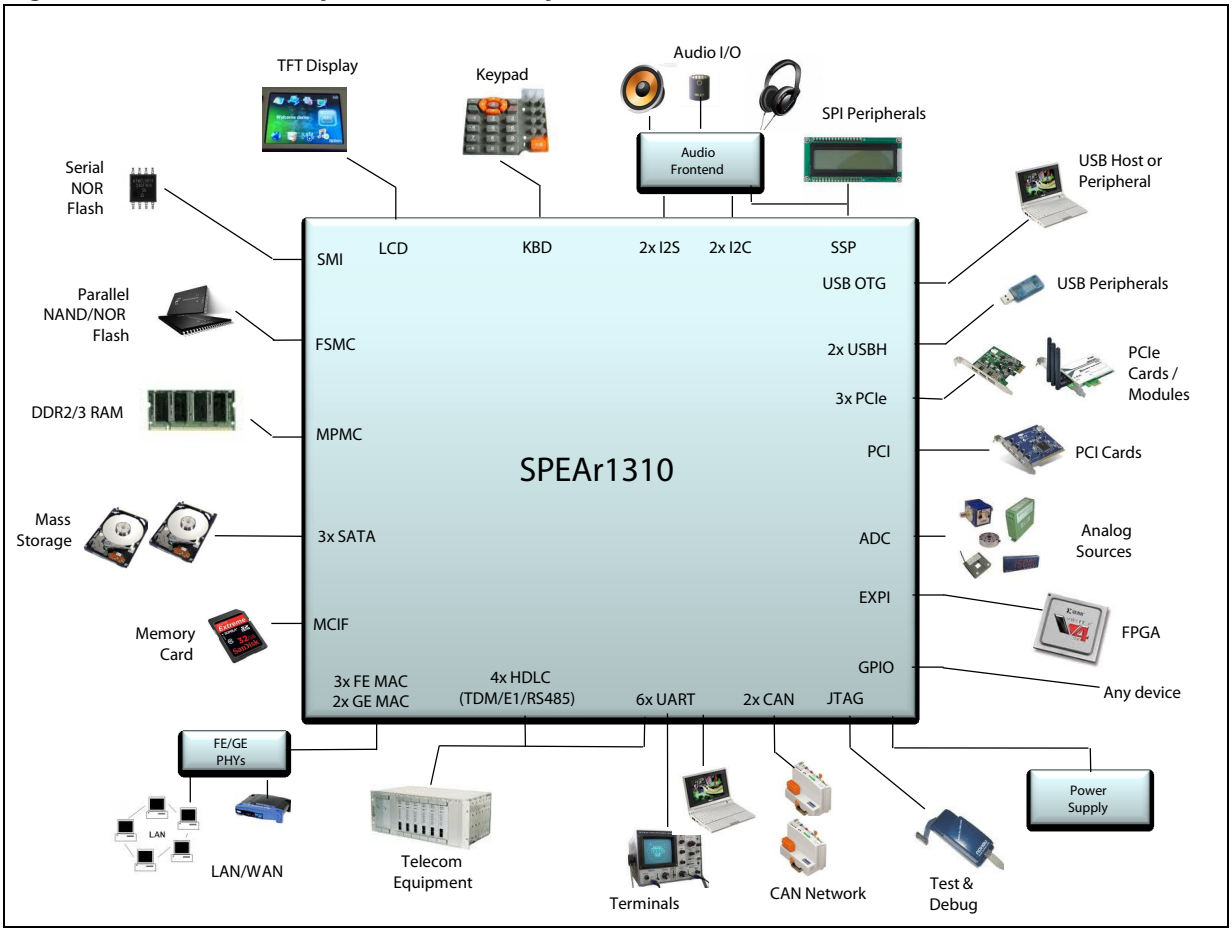
The SPEAr1310 is a member of the SPEAr family of embedded MPUs for network devices.

It offers an unprecedented combination of processing performance and aggressive power reduction control for next-generation communication appliances.

The SPEAr1310 is based on ARM's new multi-core technology (Cortex-A9 SMP/AMP) and it is manufactured with ST's 55nm HCMOS low power silicon process.

SPEAr1310 targets cost and power sensitive networking applications for the home and small business as well as telecom infrastructure equipment, with lowest overall leakage under real operating conditions. The device integrates ARM's latest generation ARMv7 CPU cores, ST's proven C3 security coprocessor, and advanced connectivity interfaces and controllers.

Figure 1. SPEAr1310 system connectivity



The SPEAr1310 internal architecture is based on several shared subsystem logic blocks that are interconnected through a multilayer interconnection matrix (the BUSMATRIX). The switch matrix structure allows different subsystem data flows to be executed in parallel improving the core platform efficiency.

High performance master agents are directly interconnected with the memory controller to reduce memory access latency. The overall memory bandwidth assigned to each master

port can be programmed and optimized through an internal, weighted round-robin (WRR) arbitration scheme.

Figure 2 is the internal connectivity block diagram.

Figure 2. SPEAr1310 block diagram of the internal connectivity

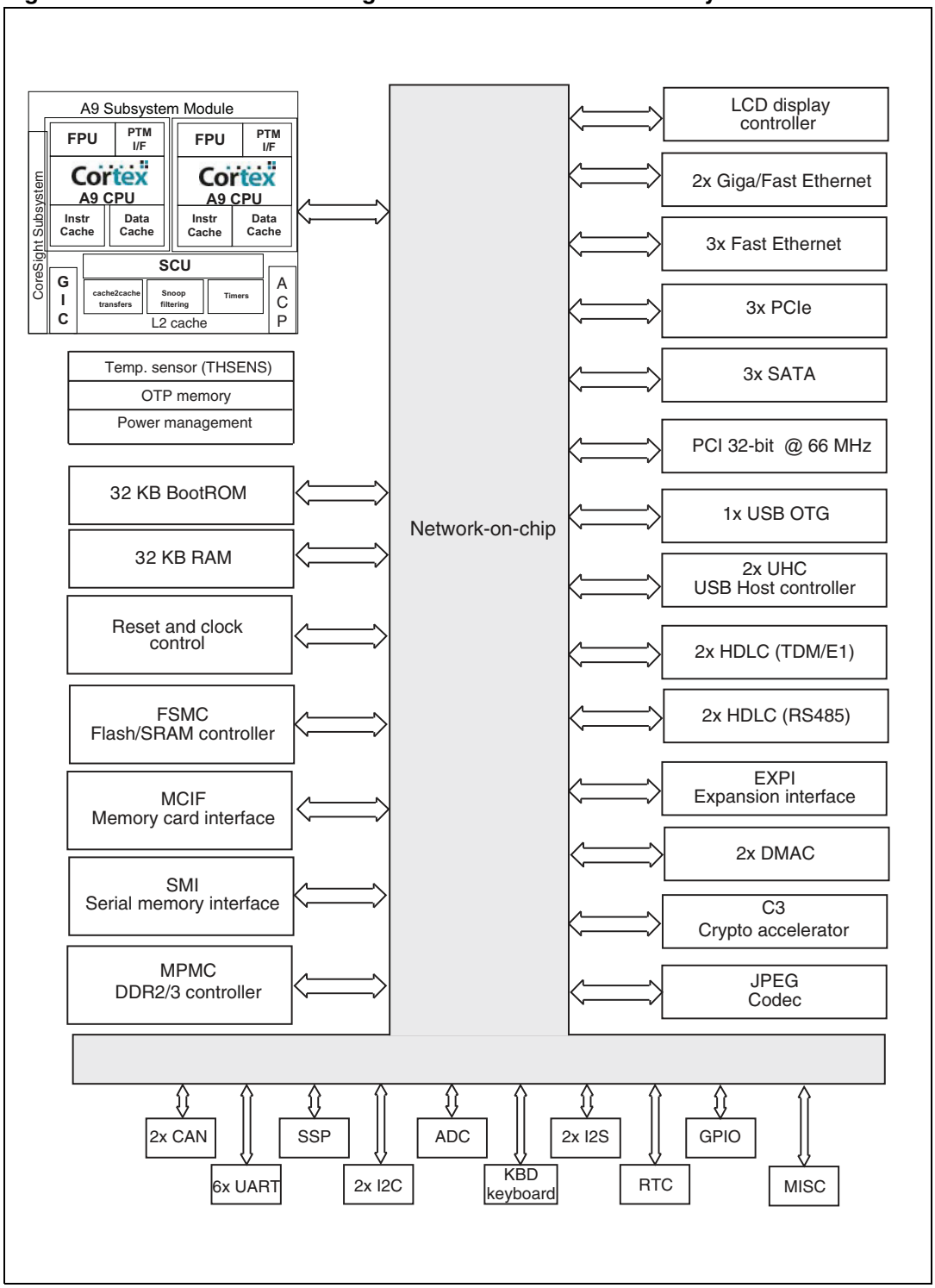


Table 1 provides an overview of SPEAr1310 features and capabilities.

Table 1. SPEAr1310 features and capabilities overview

Category	Feature	Instances / Details	Notes
CPU subsystem	Processor cores	2x Cortex A9@600 MHz 32+32 KB L1 per core	Includes: – 1x 64-bit global timer – 2x 32-bit timers – 2x watchdog/timers
	L2 Cache	1x 512 KB ECC	
	Debug & test	2x JTAG-PTM	
Interconnect	Internal bus	1x 64 bit @ 166 MHz	Network-on-chip
Reset and clock	RCG generator	1x	Reset and clock generation module
Configuration	MISC	1x	Miscellaneous SoC configuration registers
Power management	PCM	1x	Power control module
Memories	BootROM	1x 32 KB	On-chip ROM for boot firmware
	SRAM	2x 32 KB + 4 KB	Static RAM
	MPMC	1x up to 1 GB DDR2: 400 MHz + ECC DDR3: 533 MHz + ECC	DDR 2/3 controller
	FSMC	1x 16-/32-bit Parallel NAND/NOR Flash	Parallel Flash controller
	SMI	1x 4x 16 MB C.S.@50Mbps Serial NOR Flash	SPI Flash controller

Table 1. SPEAr1310 features and capabilities overview (continued)

Category	Feature	Instances / Details	Notes
Connectivity	Ethernet	2x Giga 3x Fast (see *Table 2*)	MAC controllers
	MIPHY	3x PHYs (single + dual macro)	PHYs for PCIe and SATA
	PCIe	3x root complex/endpoint	PCIe controllers
	SATA	3x gen.2	SATA controllers
	PCI	1x 32 bit @ 66 MHz host/device	Legacy PCI bus controller
	USB	2x USB2.0 Host 1x USB2.0 OTG	USB controllers with PHYs
	CAN bus	2x CAN2.0 a/b	CAN controllers
	HDLC	2x TDM/E1 2x RS485	HDLC controllers
	I2S	2x	Digital audio
	UART	6x	Async. serial ports
	SSP/SPI	1x	Sync. serial port (master/slave)
	I2C	2x	I2C bus (master/slave)
Integrated support for external peripherals	TFT LCD controller	1x 24bpp, 1920x1200 @ 60 fps + PWM	
	Keyboard controller	1x 9x9 matrix	
	Memory card interfaces	1x SD/SDIO 2.0/SDHC/MMC 4.x 1x CF/CF+ Rev 4.1, XD	
Expansion	EXPI	1x 32 bit AHB like @83 MHz	
Security	C3	1x DES, 3DES, AES univ. hashing SHA1/2, MD5, HMAC PKA, True_RNG	Cryptography accelerator
	OTP	1x 510+209	One-time programmable antifuse

Table 1. SPEAr1310 features and capabilities overview (continued)

Category	Feature	Instances / Details	Notes
Other	GPT	4x (total 8 timers)	General purpose timers
	RTC	1x	Real-time clock
	DMAC	2x (total 16 channels)	DMA controller
	JPEG Codec	1x	JPEG encoder/decoder
	ADC	1x 8 channels x 10bit, 1Msps	A/D converter Also used for touchscreen I/F
	GPIO	2x (total 16 I/O)	General-purpose I/O
	THSENS	1x	Temperature sensor

Table 2. MAC Phy interfaces available

MAC controller	Rate	Interfaces
MAC1	GE (1 Gbps)	GMII / RGMII
	FE (10/100 Mbps)	MII / RMII
MAC2	GE (1 Gbps)	RGMII
MAC3	FE (10/100 Mbps)	SMII / RMII
MAC4	FE (10/100 Mbps)	SMII / RMII
MAC5	FE (10/100 Mbps)	SMII / RMII

2 Multilayer interconnect matrix (BUSMATRIX)

The multilayer interconnect matrix is the connectivity infrastructure that enables data exchange between the various blocks of the device. This structure supports parallel communications between master and slave components, and ensures the maximum level of system throughput.

Note: In this document, the words initiator agent (IA) and master are synonyms ; target agent (TA) and slave are synonyms.

2.1 Main features

- Hierarchical structure to meet the requirements of different system blocks and peripherals:
  - High performance low latency
  - High performance medium latency
  - Medium performance medium/long latency
  - Slow peripherals and configurations
- Power awareness through the power down request/acknowledgement of the power management module
- Single interrupt for outbound signaling

3 CortexA9 subsystem (A9SM)

The CPU subsystem is based on the ARM Cortex A9 processor, and has a dual core configuration.

3.1 Main features

Each core has the following features:

- ARM v7 CPU at 600 MHz
- 32 KB of L1 instruction CACHE with parity check
- 32 KB of L1 data CACHE with parity check
- Embedded FPU for single and double data precision scalar floating-point operations
- Memory management unit (MMU)
- ARM, Thumb2 and Thumb2-EE instruction set support
- TrustZone© security extension
- Program Trace Macrocell and CoreSight© component for software debug
- JTAG interface
- AMBA© 3 AXI 64-bit interface
- 32-bit timer with 8-bit prescaler
- Internal watchdog (working also as timer)

The dual core configuration is completed by a common set of components:

- Snoop control unit (SCU) to manage inter-process communication, cache-2-cache and system memory transfer, cache coherency
- Generic interrupt control (GIC) unit configured to support 128 independent interrupt sources with software configurable priority and routing between the two cores
- 64-bit global timer with 8-bit prescaler
- Asynchronous accelerator coherency port (ACP)
- Parity support to detect internal memory failures during runtime
- 512 KB of unified 8-way set associative L2 cache with support for parity check and ECC
- L2 Cache controller based on PL310 IP released by ARM
- Dual 64-bit AMBA 3 AXI interface with possible filtering on the second one to use a single port for DDR memory access

4 Clock and reset system

This centralized structure provides system synchronization and includes the following features:

- Six PLLs. Four of them are fully programmable and offer an EMI reduction mode (spread spectrum clock generation through dithering) that can replace all traditional EMI reduction techniques.
  - PLL1 programmable dithered pll, dedicated for Core1 & 2 & AXI/AHB bus & peripherals. Both core need to run at the same speed
  - PLL2 programmable dithered PLL, dedicated for the 125 MHz clock of the Gigabit Ethernet MACs
  - PLL3 programmable dithered PLL, for specific embedded IP functions
  - PLL4 programmable dithered PLL, dedicated for the DDR memory controller (Asynchronous access memory mode)
  - PLL5 low jitter, dedicated for the USB
  - PLL6 for the PCIe controllers
- Several synthesizers provide different frequencies for different IPs
- Fully programmable control of clock and reset signals for all slave blocks allowing sophisticated power management.

5 Reset and clock generator (RCG)

The reset and clock generator (RCG) provides the system clocks and resets. It is highly configurable through the miscellaneous registers.

5.1 Main features

- Three main clock sources:
  - osci1: 24 MHz clock coming from internal oscillator connected to external quartz.
  - osci2: 32 kHz clock coming from internal oscillator used for RTC block (optional)
  - osci3: 25/100 MHz clock coming from MIPHY macro (optional).
- Three programmable dithered PLLs (to reduce EMI):
  - PLL1: primarily used to generate the 1 GHz clock for the AMBA subsystem
  - PLL2, PLL3: primarily used to generate clocks for RAS logic and generic IPs
- Seven configurable clock generators:
  - SSCG1-4: dedicated to RAS logic
  - SSCG5: for CLCD clock
  - SSCG6: for EXPI clock
  - SSCG7: for AMBA system clocks
- Three operating modes for AMBA clocks:
  - DOZE: the clock source is osci2 (osci1 after power on)
  - SLOW: the clock source is the osci1 or a divided version
  - NORMAL: the clock source is PLL1 (by default), PLL2, PLL3 or SSCG7
- Configurable clock gating and software reset for most peripherals
- Global software reset and watchdog reset

6 Power control module (PCM)

PCM is the core of the SPEAr1310 leakage power management system. Its role is to properly manage the power supply shutoff of the switchable sections of the embedded MPU.

6.1 Main features

- Generation of supply switch control signals for SPEAr1310 power islands
- Generation of isolation control signals for SPEAr1310 power islands
- Generation of shutoff commands for external DDR 1V2 and 1V5/1V8 supply lines
- Acknowledge generation for user requested power island configuration
- Monitoring of voltage detector outputs for each power island
- Wake-up source management

7 BootROM

The term BootROM refers to the on-chip 32 KB ROM as well as the booting firmware pre-stored in such memory. Supported booting devices are:

- Serial NOR Flash
- Parallel NOR Flash
- NAND Flash
- I2C EEPROM
- PCIe
- USB Device
- UART

The BootROM firmware selects the booting device after reset by reading the status of the STRAP[3:0] pins.

8 Static RAM (SRAM)

SPEAr1310 has internal static RAM (SRAM) areas. A part of these memory areas is used during the bootstrap phase by BootROM firmware. After booting, all SRAM areas are fully available for general purpose applications.

8.1 Main features

- 4 KB of Always-on RAM (SYSRAM1, single port)
  When all of the power islands are switched off, SYSRAM1 maintains its data content.
- 32 KB of system RAM (SYSRAM0, single port)
  When all of the power islands are switched off, SYSRAM0 loses its data content.

9 Multiport memory controller (MPMC)

MPMC is a high performance multichannel memory controller able to support DDR2 and DDR3 double data rate memory devices. The multiport architecture ensures that memory is shared efficiently among different high-bandwidth client modules.

9.1 Main features

- Supports both DDR3 and DDR2 devices. Wide range of memory device cuts supported: from 128 Mb to 4 Gb for each chip select. Two chip selects supported.
- Programmable memory datapath size of full memory 32-bit data width or half memory 16 bits data width
- Clock frequencies from 100 MHz to 533 MHz supported
- 6 AXI interfaces with a data interface width of 64 bits. Each port is configured with a thread ID of 4 bits
- Exclusive and locked accesses support Weighted Round-Robin arbitration scheme support to ensure high memory bandwidth utilization
- DRAM command processing
- Register port with an AHB Interface with a data interface width of 32 bits
- A programmable register interface to control memory device parameters and protocols including auto pre-charge
- Full initialization of memory on memory controller reset
- Automatically maps user addresses to the DRAM memory in a contiguous block addressing starts at user address 0 and ends at the highest available address according to the size and number of DRAM devices present
- Fully pipelined command, read and write data interfaces to the memory controller
- Advanced bank look-ahead features for high memory throughput
- 7-bit ECC functionality with single-bit and double-bit error reporting and automatic correction of single-bit error events. Programmable reporting and correction. Programmable removal of ECC storage

10 Flexible static memory controller (FSMC)

The flexible static memory controller (FSMC) is an AHB peripheral that interfaces AHB masters to a wide variety of memories. A wrapper is designed to contain this IP and a MUX which selects the appropriate signals to connect to the pads depending on the type of memory.

10.1 Main features

- Support for NAND Flash (8 bit parallel data bus that can be extended up to 32 bits in specific configurations)
- ECC hardware: the NAND Flash controller contains a hardware acceleration block for error correction code computation, for pages ranging from 256 to 8192
- Independent chip select control for each memory bank
- Write FIFO: 16 words deep, each word is 32 bits wide
- Support for asynchronous NOR Flash (additional signals multiplexed on PL_GPIOs, address and data on dedicated IOs); 26 bit address bus supported
- Support for asynchronous static RAM (signals multiplexed on PL_GPIOs, address and data on dedicated IOs); 26 bit address bus supported
- Support for muxed NOR and SRAM
- Independent read/write timings and protocol, allowing matching the widest variety of memories and timings

11 Serial memory interface (SMI)

The serial memory interface integrated in SPEAr1310 acts as an AHB slave interface (32, 16- or 8-bit) to SPI-compatible off-chip memories. SMI allows the CPU to use these serial memories either as data storage or for code execution.

11.1 Main features

- Supports a group of SPI-compatible Flash and EEPROM devices
- Acts always as a SPI master and up to 4 SPI slave memory devices are supported (through as many chip select signals), with up to 16 MB address space each; 2 out of the 4 chip select are available on PL_GPIOs.
- The SMI clock signal (smi_clk_o) is generated by SMI (and input to all slaves) using clock provided by the AHB bus
- smi_clk_o can be up to 50 MHz in fast read mode (or 20 MHz in normal mode), and it can be controlled by a programmable 7-bit prescaler allowing 127 different clock frequencies.

12 Giga/Fast Ethernet media access controller (GMAC)

The GMAC IP provides the capability to transmit and receive data over Ethernet.

12.1 Main features

- Supports 10/100/1000 Mbps data transfer rates with the following PHY interfaces:
  - IEEE 802.3-compliant GMII/MII (default) interface to communicate with an external Gigabit/Fast Ethernet PHY
  - RGMII (specification version 2.0) interface to communicate with an external gigabit PHY
  - SGMII (specification version 1.8) interface to communicate with an external gigabit PHY

    Note that the SGMII block inside GMAC comprises the rate adapter layer (RAL) and the physical coding scheme (PCS) modules: these modules implement a TBI "like" interface. Outside the chip the SerDes and high-speed I/O modules are needed to implement the actual SGMII interface.
  - RMII (specification version 1.2 from RMII consortium) interface to communicate with an external Fast Ethernet PHY (for 10/100 Mbps operations only)
- Full-duplex operation
  - IEEE 802.3x flow control automatic transmission of zero-quanta pause frame on flow control input de-assertion
  - Optional forwarding of received pause control frames to the user application
- Half-duplex operation
  - CSMA/CD Protocol support
  - Flow control using back-pressure support
  - Frame bursting and frame extension in 1000 Mbps half-duplex operation
- Automatic CRC and pad generation controllable on a per-frame basis
- Provides options for automatic pad/CRC stripping on receive frames
- Supports a variety of flexible address filtering modes, such as:
  - Up to 31 48-bit SA address comparison check with masks for each byte
  - 64-bit hash filter for multicast and unicast (DA) addresses
  - Option to pass all multicast addressed frames
  - Promiscuous mode support to pass all frames without any filtering for network monitoring
  - Passes all incoming packets (per filter) with a status report
- Programmable frame length to support standard or jumbo Ethernet frames with up to 16 KB of size
- Programmable interframe gap (IFG) (40-96 bit times in steps of 8)
- Separate 32-bit status for transmit and receive packets
- IEEE 802.1Q VLAN tag detection for reception frames
- Self-managed DMA transfers with an internal DMA block

- Separate transmission, reception, and control interfaces to the application
  - The host CPU uses a 32-bit AHB (AMBA 2.0) slave interface to access the GMAC subsystem control and status registers (CSRs)
  - The GMAC transfers data to system memory through a 32-bit AXI (AMBA 3.0) master interface
- Support for network statistics with RMON/MIB counters (RFC2819/RFC2665)
- A module for detection of LAN remote wake-up frames and AMD magic packet frames: power management module (PMT)
- A receive module for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame (Type 1)
- An enhanced receive module for checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams (Type 2)
- A module to support Ethernet frame time stamping as described in IEEE 1588- 2002 and IEEE 1588-2008 (standard for precision networked clock synchronization). Sixty-four-bit time stamps are given in the transmit or receive status of each frame
- MDIO master interface for PHY device configuration and management: station management agent (SMA), MDIO module
- Supports the standard IEEE P802.3az, version D2.0 for energy efficient Ethernet; allows physical layers to operate in the low-power idle (LPI) mode

The MAC transaction level (MTL) block consists of two sets of FIFOs: a transmit FIFO with programmable threshold capability, and a receive FIFO with a programmable threshold (default of 64 bytes). The MTL block has the following features:

- 32-bit transaction layer block that provides a bridge between the application and the GMAC
- Single-channel transmit and receive engines
- Synchronization for all clocks in the design (transmit, receive, and system clocks)
- Optimization for packet-oriented transfers with frame delimiters
- Four separate ports for system-side and GMAC side transmission and reception
- FIFO instantiation outside the top-level module to facilitate memory testing/instantiation
- 4-KB receive FIFO size on reception
- Supports receive status vectors insertion into the receive FIFO after the EOF transfer. This enables multiple-frame storage in the receive FIFO without requiring another FIFO to store those frames
- Configurable receive FIFO threshold (default fixed at 64 bytes) in cut-through or threshold mode
- Provides an option to filter all error frames on reception and not forward them to the application in store-and-forward mode.
- Provides an option to forward under-sized good frames
- Supports statistics by generating pulses for frames dropped or corrupted (due to overflow) in the receive FIFO
- 2-KB FIFO size on transmission
- Store and forward mechanism for transmission to the GMAC
- Threshold control for transmit buffer management
- Automatic retransmission of collision frames for transmission

- Discards frames on late collision, excessive collisions, excessive deferral, and under-run conditions
- Software control to flush TX FIFO

The DMA block exchanges data between the MTL block and host memory. The host can use a set of registers (DMA CSR) to control the DMA operations. The DMA block supports the following features:

- 32-bit data transfers
- Single-channel transmit and receive engines
- Fully synchronous design operating on a single system clock (except for CSR module, when a separate CSR clock is configured)
- Optimization for packet-oriented DMA transfers with frame delimiters
- Byte-aligned addressing for data buffer support
- Dual-buffer (ring) or linked-list (chained) descriptor chaining
- Descriptor architecture that allows large blocks of data transfer with minimum CPU intervention
- Comprehensive status reporting for normal operation and transfers with errors
- Individual programmable burst size for transmit and receive DMA engines for optimal host bus utilization
- Programmable interrupt options for different operational conditions
- Complete per-frame transmit/receive interrupt control
- Round-robin or fixed-priority arbitration between receive and transmit engines
- Start/stop modes
- Separate ports for host CSR access and host data interface

The GMAC audio video (AV) feature enables transmission of time-sensitive traffic over bridged local area networks (LANs). The GMAC AV has the following features:

- Compliant to IEEE 802.1-AS standard, version D6.0: specifies the protocol and procedures used to ensure that the synchronization requirements are met for time-sensitive applications
- Compliant to IEEE 802.1-Qav standard, version D6.0: allows the bridges to provide time-sensitive and loss-sensitive real-time audio video data transmission (AV traffic). It specifies the priority regeneration and controlled bandwidth queue draining algorithms that are used in bridges and AV traffic sources
- Supports one additional channel (channel 1) on the transmit and receive paths for AV traffic in 100 Mbps and 1000 Mbps modes. The channel 0 is available by default and carries the legacy best-effort Ethernet traffic on the transmit side
- Supports IEEE 802.1-Qav specified credit-based shaper (CBS) algorithm for the additional transmit channels
- Provides separate DMA, TxFIFO, and RxFIFO MTL for the additional channel (to avoid "head of line blocking" issues); the system-side interface remains the same

The GMAC has the following additional features for monitoring, testing, and debugging:

- Supports internal loopback on the GMII/MII for debugging
- Provides DMA states (Tx and Rx) as status bits
- Provides debug status register that gives status of FSMs in transmit and receive data-paths and FIFO fill-levels
- Application abort status bits
- MMC (RMON) module in the GMAC core
- Current Tx/Rx buffer pointer as status registers
- Current Tx/Rx descriptor pointer as status registers
- Statistical counters that help in calculating the bandwidth served by each transmit channel when AV support is enabled

13 PCI Express (PCIe)

The PCI Express (PCIe) core incorporates a dual mode (DM) core which can implement a PCIe interface for a PCIe Root Complex (RC) or Endpoint (EP). The dual mode core can operate in EP or RC port modes, depending on the value sampled on the core input at power-on reset. The DM core can be switched between modes at runtime by applying a power-on reset.

PCI Express is compliant with the PCI Express Base 2.0 specification and supports PHYs with the PIPE 1.87 or PxPIPE interface specification. As a consequence, it is also compliant with the PCIe 1.1 specification.

The core features a proprietary user-configurable and high-performance application interface for generating and receiving PCIe traffic. It is available with standard AMBA 3 AXI interfaces.

13.1 Main features

Typical applications for a PCI Express device built with the DM core include:

- Motherboard components for desktop and mobile computers
- Graphics devices
- Add-in cards for desktop and mobile computers
- Components and add-in cards in server applications
- Embedded applications
- Data communications equipment
- Telecommunications equipment
- Storage devices
- Wireless devices
- Other applications

The DM core in EP mode supports PCI Express Legacy Endpoint devices. However, the application must ensure that the device obeys the Legacy Endpoint device rules defined in the PCI Express Base 2.0 specification.

Note: The core is not intended for use in a root complex integrated endpoint.

The features common to both EP and RC mode of the DM cores are:

- Support for all non-optional features and some optional features defined in the PCI Express Base 2.0 specification.
- Ultra-low transmit and receive latency
- Support a max payload size of 256 bytes
- 4-KB maximum request size
- Very high accessible bandwidth
- Support for both Gen1 (at 125 MHz) and Gen2 (at 250 MHz) operation
- 2.5 Gbps (Gen1) or 5.0 Gbps (gen2) Lane (x1)
- Automatic Lane reversal as specified in the PCI Express 2.0 specification (transmit and receive)
- Polarity inversion on receive
- Multiple virtual channels (VCs) (maximum of 2)
- Multiple traffic classes (TCs)
- Supports ECRC generation and checking
- Supports PCI Express beacon and wake-up mechanism
- Supports PCI power management
- Supports PCI Express active state power management (ASPM)
- Supports PCI Express advanced error reporting
- Supports Vital product data (VPD)
- Supports PCIe messages for both transmit and receive.
- Supports external priority arbitration (in addition to the internally-implemented transmit arbitration)
- Supports expansion ROM

Additional features specific to RC mode

The features specific to the RC mode are:

- Type 1 configuration space
- Application-initiated Lane reversal for situations where the core does not detect Lane 0 (for example, an x4 core connected to an x8 device that has its Lanes reversed)

Additional features specific to EP mode

The features specific to the EP mode are:

- Alternate routing-ID (ARI)
- Address translation services (ATS)
- Completion timeout ranges
- Function level reset (FLR)
- Type 0 configuration space
- MSI interrupt capability

14 SATA gen-2 controller

The SATA AHCI Core implements the serial advanced technology attachment (SATA) storage interface for physical storage devices.

14.1 Main features

This functional block supports the following features:

- SATA 3.0 Gb/s Gen II
- eSATA (external analog logic also needs to support eSATA)
- Compliant with the following specifications:
  - Serial ATA 3.0 (except FIS-based switching)
  - AHCI Revision 1.3 (except FIS-based switching)
  - AMBA 3 AXI interfaces
- User-defined PHY status and control ports
- RX data buffer for recovered clock systems
- Data alignment circuitry when RX data buffer is also included
- OOB signaling detection and generation
- 8b/10b encoding/decoding
- Asynchronous signal recovery, including retry polling
- Digital support of device hot-plugging
- Power management features including automatic partial-to-slumber transition
- BIST loopback modes
- Single SATA deviceInternal DMA engine per port
- Hardware-assisted native command queuing for up to 32 entries
- Port Multiplier with command-based switching
- Disabling RX and TX Data clocks during power down modes
- Integrated SATA link layer and transport layer logic
- Supports PIO, first party and legacy DMA modes
- Supports legacy command queuing
- Supports ATA and ATAPI master-only emulation mode (for instance, register and command compatible with these standards)
- Power-down mode
- Data scrambling
- CRC computation
- Automatic data flow control
- Far end loop-back re-timed

15 PCIe/SATA physical interface (MiPHY)

To be completed.

16 32-bit PCI expansion bus

SPEAr1310 supports legacy PCI, providing both the host and device interfaces. The device interface is used for intelligent expansions in PCI machines (like PCs). The "host interface" is used to provide additional peripherals to SPEAr1310 cores - for instance, dedicated signals (clock, bus request and grant) for up to four external devices.

16.1 Main features

- PCI specification 2.3 compliant
- 32-bit address/data paths
- Up to 66 MHz interface clock
- Programmable for acting as Host or Device
- Four dedicated interrupts

17 USB Host controller (UHC)

17.1 Main features

The USB 2.0 Host controller has 2 physical ports that are fully compliant with the Universal Serial Bus specification (version 2.0), and provides an interface to the industry-standard AHB bus.

The main features of the UHC are:

- A PHY interface implementing a USB 2.0 transceiver macro-cell interface plus (UTMI+) fully compliant with UTMI+ specification (revision 1.0), to execute serialization and de-serialization of transmissions over the USB line
- Either 30 MHz clock for 16-bit interface or 60 MHz for 8-bit interface supported by the UTMI + PHY interface
- A USB 2.0 Host controller (UHC) connected to the AHB bus that generates the commands for the UTMI+PHY
- Complies with both the enhanced host controller interface (EHCI) specification (version 1.0) and the open host controller interface (OHCI) specification (version 1.0a)
- The UHC supports the 480 Mbps high-speed (HS) for USB 2.0 through an embedded EHCI Host Controller, as well as the 12 Mbps full-speed (FS) and the 1.5 Mbps low-speed (LS) for USB 1.1 through one integrated OHCI Host controller
- All clock synchronization is handled within the UHC
- An AHB slave for each controller (1 EHCI and 1 OHCI), acting as programming interface to access to control and status registers
- An AHB master for each controller (1 EHCI and 1 OHCI) for data transfer to system memory, supporting 8-, 16-, and 32-bit wide data transactions on the AHB bus
- 32-bit AHB bus addressing

18 USB On-The-Go controller (OTG)

18.1 Main features

- Complies with the On-The-Go supplement to the USB 2.0 specification (revision 1.3)
- Supports the session request protocol (SRP)
- Supports the Host negotiation protocol (HNP)
- A PHY interface implementing the USB 2.0 transceiver macrocell interface (UTMI+ specification, revision 1.0 (Level 3)) to execute serialization and de-serialization of transmissions over the USB line
- Unidirectional and bidirectional 16-bit UTMI data bus interfaces
- Support for the following speeds:
  - High-speed (HS): 480-Mbps
  - Full-speed (FS): 12-Mbps
  - Low-speed (LS): 1.5-Mbps (only in Host mode)
- Both of the DMA and slave-only modes are supported

19 Controller area network interfaces (CAN)

19.1 Main features

- CAN protocol version 2.0 part A and B
- Bit rates up to 1 Mbps
- 32 message objects (136 x 32-bit message RAM)
- Each message object has its own identifier mask
- Maskable interrupt
- Programmable loop-back mode for self-test operation
- Disabled automatic retransmission mode for time triggered CAN applications

20 TDM/E1 HDLC controller

20.1 Main features

The main features of the TDM/E1 HDLC design are:

- AMBA 2.0 compliant
- AMBA slave interface, used to program TDM/E1
- AMBA master interface, used to transfer data between DDR and IP
- DMA engine included to alleviate CPU from transferring data
- Data buffer queue making bulk data transfer more efficient
- Interrupt Queue supplying more interrupt information
- Miscellaneous Interrupt generation
  - Frame transmitted/received
  - End of data buffer queue
  - Buffer empty/ buffer filled
  - Tx/Rx DMA FIFO underflow/overflow
  - Interrupt queue overflow
  - Interrupt FIFO overflow
  - Abort generation and detection
  - Oversize and non-octet-aligned frame detection
  - CRC and alignment error generation

TDM interface features:

- Six signals
- Duplex Tx/Rx communication
- Up to 16 Mbps pre Tx/Rx channel
- 256 time slots / frame(125 us)
- Supports any time-slot banding to any Tx/Rx channel
- Data sending/sampling time configurable
- Delay between bit 0 of TS0 and the SYNC signal configurable

E1 interface main features:

- Six signals
- Duplex Tx/Rx communication
- Up to 2 Mbps pre Tx/Rx channel
- 32 time slot / frame(125 us)
- Supports any time-slot banding to any Tx/Rx channel
- Data sending/sampling time configurable
- Delay between the bit 0 of TS0 and the SYNC signal is configurable

HDLC controller main features:

- Compliant with ISO/IEC13239
- Standard HDLC frame code/decode

21 RS485 HDLC controller

21.1 Main features

The main features of the RS485 HDLC controllers are:

- AMBA 2.0 compliant
- AMBA slave interface, used to program RS485/HDLC
- AMBA master interface, used to transfer data between DDR and IP
- DMA engine included to alleviate CPU from transferring data
- Data buffer queue making bulk data transfer more efficient
- Interrupt Queue supplying more interrupt information
- Miscellaneous Interrupt generation
  - Frame transmitted/received
  - End of data buffer queue
  - Buffer empty/ buffer filled
  - Tx/Rx DMA FIFO underflow/overflow
  - Interrupt queue overflow
  - Interrupt FIFO overflow
  - Abort generation and detection
  - Oversize and non-octet-aligned frame detection
  - CRC and alignment error generation

RS485 interface main features:

- Five signals for each RS485 interface
- Duplex Tx/Rx communication
- Maximum Tx/Rx data rate 3.88 Mbps
- Collision detection and automatic frame re-transmition
- Data sending/sampling timing configurable
- Tx data can be sent out after the rising/falling edge of Tx clock
- Rx data are sampling at the rising/falling edge of Rx clock
- No constraints on clock duty cycle, data sending/receiving only depends on the rising/falling edge of Tx/Rx clock

HDLC controller main features:

- Compliant with ISO/IEC13239
- Standard HDLC frame code/decode

22 Inter-IC sound controller (I2S)

The I2S controller is a highly configurable IP for use in audio applications. It provides a simple interface to standard audio components.

22.1 Main features

- Compliant to Philips I2S serial bus specifications
- Concurrent I2S master and slave operations
- Supports 12/16/20/24/32 bit data interface
- Fully synchronous design with serial clock and system clock
- Interrupt support for reporting FIFO and other conditions
- Programmable FIFO thresholds
- Supports data exchange to the system memory through DMA interface
- Software controlled block resets and enables
- Software controlled FIFO flush

23 Universal asynchronous receiver/transmitter (UART)

A UART is responsible for performing the main task in serial communications with computers. The device changes incoming parallel information to serial data that can be sent on a communication line. The UART performs all the tasks, timing, parity checking, etc. needed for the communication.

The UART is an APB module in the power bus subsystem; it supports standard asynchronous communication bits (start, stop and parity), which are added prior to transmission and removed on reception.

The UART can support serial data baud rate, dc up to UARTCLK_max_freq/16. It supports modem control functions CTS, DCD, DSR, RTS, DTR and RI.

23.1 Main features

- Separate 16x8 transmit and 16x12 receive first-in, first-out memory buffers (FIFOs)
- Programmable FIFO disabling for 1-byte depth
- Programmable baud rate generator
- Independent masking of transmit FIFO, receive FIFO, receive timeout, modem status, and error condition interrupts
- Support for direct memory access (DMA)
- False start bit detection
- Line break generation and detection
- Programmable hardware flow control
- Fully-programmable serial interface characteristics:
  - data can be 5, 6, 7, or 8 bits
  - even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation

The following key parameters are programmable:

- Communication baud rate, integer, and fractional parts
- Number of data bits
- Number of stop bits
- Parity mode
- FIFO enable (16 deep) or disable (1 deep)
- FIFO trigger levels selectable between 1/8, 1/4, 1/2, 3/4, and 7/8
- Hardware flow control
- The UART clock can be fixed at 48 MHz or can be programmed using the miscellaneous register UART_CLK_SYNT.

24 Synchronous serial port (SSP)

The synchronous serial port (SSP) block includes a master or slave interface to enable synchronous serial communication with slave or master peripherals.

24.1 Main features

- Master or slave operation
- Programmable clock bit rate and prescaler
- Separate transmit and receive first-in, first-out memory buffers, 16-bit wide, 8 locations deep
- Programmable choice of interface operation, SPI, Microwire, or TI synchronous serial
- Programmable data frame size from 4 to 16 bits
- Independent masking of transmit FIFO, receive FIFO, and receive overrun interrupts
- Internal loopback test mode available
- Support for direct memory access (DMA)

25 I2C controller

The I2C controller acts as an APB slave interface to the two-wire serial I2C bus.

25.1 Main features

- Compliance to the I2C-bus specification from Philips
- Operates in three different modes:
  - Standard-speed mode (data rates up to 100 Kb/s)
  - Fast-speed mode (data rates up to 400 Kb/s)
  - High-speed mode (data rates up to 3.4 Mb/s)
- Provides clock synchronization
- Supports either master or slave I2C operation mode.
- Supports multimaster operation mode (bus arbitration)
- Provides 7-bit or 10-bit addressing
- Supports 7-bit or 10-bit combined format transfers
- Provides slave bulk transfer mode
- Ignores CBUS addresses (an older ancestor of I2C that used to share the I2C bus)
- Transmits and receives buffers
- Provides interrupt or polled-mode operation
- Handles bit and byte waiting at all bus speeds
- Provides digital filter for the received SDA and SCL lines
- Handles component parameters for a configurable software driver support
- Provides a DMA handshaking interface compatible with the DW_ahb_dmac handshaking interface
- Supports for APB data bus widths of 8, 16 and 32 bits

26 TFT LCD controller (CLCD)

The TFT LCD controller provides all the necessary control signals to interface directly to a variety of TFT LCD panels.

26.1 Main features

- Wide range of programmable LCD panel resolutions
- Support for 1 port TFT LCD panel interfaces:
  - 18-bit digital (6-bits/color)
  - 24-bit digital (8-bits/color) CMOS
- Support for 2 Port TFT LCD panel interfaces (2^{nd} port available on PL_GPIOs)
- Programmable frame buffer bits-per-pixel (bpp) color depths:
  - 1, 2, 4, 8 bpp mapped through the color palette to 18-bit LCD pixel
  - up to 18 bpp directly drive 18-bit LCD pixel
  - 24 bpp directly drive 24-bit LCD pixel
- Color Palette RAM to reduce Frame Buffer memory storage requirements bandwidth
- Programmable output format support:
  - RGB 6:6:6 or 5:6:5 or 5:5:5 on 18-bit digital interface
  - RGB 8:8:8 on 24-bit digital interface
- Programmable horizontal timing parameters:
  - horizontal front porch, back porch, sync width, pixels-per-line
  - horizontal sync polarity
- Programmable vertical timing parameters:
  - vertical front porch, back porch, sync width, lines-per-panel
  - vertical sync polarity
- Programmable pixel clock frequency up to bus clock frequency
- Programmable data enable timing signal:
  - derived from horizontal and vertical timing parameters
  - display enable polarity
- Power up and down sequencing support
- Programmable endianness
- Pulse width modulation for LCD panel LED backlight brightness control

27 Keyboard controller (KBD)

The GPIO keyboard controller integrated in SPEAr1310 offers a 4-mode input and output port. It provides an 18-bit GPIO, 6x6/9x9/2x2 keyboard functionality, and offers an interface to the industry standard APB bus.

27.1 Main features

- 18-bit general-purpose parallel port (GPIO) with input or output single pin programmability
- 36 (6x6)/81 (9x9)/4 (2x2) key keyboard
- GPIO or keyboard functionality
- Selection of any one of the three keyboard matrices
- AMBA APB interface

28 Memory card interface (MCIF)

MCIF is a hardware IP that interfaces with the most common memory card on the market:

- SD/SDIO 2.0
- SDHC
- CF/CF+ Rev 4.1
- MMC 4.2/4.3
- xD

The device interface multiplexes different memory cards on the same IOs; only one memory card is accessible at a given time. At the board level, discrete elements are required to handle host-swap management.

28.1 Main features

SD/SDIO/MMC controller

- Compliant with:
  - SD Host controller standard specification version 2.0
  - SDIO card specification version 2.0
  - SD memory card specification draft version 2.0
  - SD memory card security specification version 1.01
  - MMC specification version 3.31, 4.2 and 4.3
  - AMBA specification AHB (version 2.0)
- Data transfer with the system core through:
  - PIO mode on the Host AHB slave interface
  - DMA mode on the Host AHB master interface
- Host clock rate variable from 0 to 50 MHz
- Maximum data rate achievable:
  - 200 Mbps (sd4 bit mode)
  - 400 Mbps (mmc8 bit mode)
- Data transfer:
  - SD mode: 1 bit, 4 bit, and SPI mode
  - MMC mode: 1 bit, 4 bit, 8 bit, and SPI mode
- Cyclic redundancy check for commands (CRC7) and for data integrity (CRC16)
- Variable length data transfer
- Read wait control and suspend/resume operations supported
- Works with I/O cards, read-only cards and read/write cards
- Supports MMC Plus and MMC Mobile
- Error correction code support for MMC 4.3 cards
- Card detection (Insertion/Removal)
- Card password protection
- Two 4K FIFO to aid data transfer between the CPU and the controller
- FIFO overrun and underrun handled by stopping the SD clock

CF/CF+ Host controller

- CF Specification Revision 4.1 compliance (True IDE Mode only)
- Multiword DMA to transfer data between the host and the CF/+ device
- Ultra DMA mode for accessing the CF/+ card using the 16-bit data path
- PIO timing mode0 through mode6
- Multiword DMA timing mode0 through mode4
- Ultra DMA timing mode0 through mode6
- Data transfers up to 256 (512-byte) blocks
- Variable-length data transfer in multiword DMA and Ultra DMA modes
- Interrupt-driven data transfers in PIO mode

xD Host controller (Xtreme Digital)

- Comfortable erase mechanism
- Programmable access timing
- Supports Read, Write, Erase, Read device ID, Status and Reset Commands.
- Supports ECC Generation and Checking
- Supports multiblock programming and multiblock erase.
- Supports 1 Gbit, 2 Gbit

29 Expansion interface (EXPI)

The auxiliary bidirectional interface (EXPI) is multiplexed with the programmable PL_GPIOs signals to connect an external component (for instance, emulation FPGA).

SPEAr1310 provides an AHB master (81) and an AHB slave (I) interface that are used by the EXPI block in order to give access from the external world to the internal resources and vice versa.

The EXPI is in charge of decoupling outside speed from the internal speed on the bus using asynchronous bridges taking also care of multiplexing the first 100 PL_GPIO and the 4 PL_CLK between RAS and its functionality.

29.1 Main features

- Master and slave mode supported
- Full connectivity between SPEAr1310 IAs and EXPI TA port
- Configurable internal/external sources for clock and reset
- Configurable internal source clock operating frequency
- 16 dedicated PL_GPIOs for DMA handshaking.
  - Up to 5 handshaking interfaces with programmable flow control (3 signals):
  - Up to 8 handshaking interface with DMA flow control without TC (2 signals)
- Handshaking interface programmability
- Reduced 24 bit addressing mode with translation table
- 8 more signals can be used
  - Other 3 handshaking interfaces with programmable flow control
  - Other 4 handshaking interface with DMA flow control without TC
- 4 interrupt signal from external to SoC
- 1 interrupt signal from SoC to external

30 Security co-processor (C3)

C3 is a multipurpose, instruction driven, programmable DMA-based co-processor. It is configured to accelerate cryptographic and network security functions.

30.1 Main features

- AMBA AHB 2.0 master and slave interfaces
- Scatter and gather DMA engine (implemented only by MPCM channel)
- Instruction dispatchers
  - ID0 and ID1 available
  - ID2 and ID3 empty
- Internal RAM: 4Kx32
- Coupling/Chaining: 2 paths

The hardware accelerator crypto algorithms available in SPEAr1310 have the following channels supported by mentioned operations:

- **Channel 0**: Move channel
  - ID: 0x00001020
  - Supported operations: copy, AND, OR, XOR
  - Chained mode: either master or slave
  - Cascaded mode: both master and slave
  - Input FIFO: 8x32 bits
  - Output FIFO: 8x32 bits
- **Channel 1**: Data encryption standard (DES and TripleDES)
  - ID: 0x00002001
  - Supported algorithms: DES (56-bit keys, ECB and CBC encryption/decryption, no parity check) and TripleDES (168-bit keys, ECB and CBC encryption/decryption, EncDecEnc)
  - Input FIFO: 16x32 bits
  - Output FIFO: 16x32 bits
- **Channel 2:** MPCM for the advanced encryption standard (AES)
  - ID: 0x0000E000
  - Supported algorithms: AES (128-, 192-, 256-bit keys, ECB and CBC encryption/decryption, with programmable operation modes to support almost all possible modes, including Counter and XTS mode)
  - Memory for modes of operation: 512 words of 62 bits each
  - Input FIFO: 16x32 bits
  - Output FIFO: 16x32 bits
  - Read scatter/gather list: 4x32 bits
  - Write scatter/gather list: 4x32 bits

- **Channel 3:** Unified hash with HMAC
  - ID: 0x00004014
  - Supported algorithms: HMAC MD5 (hash with 128-bit digest), HMAC SHA1 (hash with 160-bit digest) and HMAC SHA2 (SHA256 and SHA224 with 256- and 224-bit digest respectively)
  - Input FIFO: 16x32 bits
  - Output FIFO: 8x32 bits
- **Channel 4**: Unified hash 2 with HMAC
  - ID: 0x00011001
  - Supported algorithms: HMAC SHA384 (hash with 384-bit digest) and HMAC SHA512 (hash with 512-bit digest)
  - Input FIFO: 16x32 bits
  - Output FIFO: 8x32 bits
- **Channel 5**: Public key accelerator (PKA) v6
  - ID: 0x00006001
  - Supported algorithms: modular exponentiation for RSA and Diffie-Hellman (up to 2048 bits), scalar multiplication of elliptic curve points over prime fields for ECC (up to 384 bits) and Montgomery's parameter for finite field operations
  - Input FIFO: 8x32 bits
  - Output FIFO: 8x32 bits
- **Channel 6**: Random number generator (RNG)
  - ID: 0x0000F000
  - Generates a sequence of true random numbers, based on a contiguous analog oscillator; the sequence has a success ratio of more than 85 % for 20.000 bits, according to FIPS 140-1 tests
  - Monitors the entropy of the generated sequence
  - Input FIFO: 2x32 bits
  - Output FIFO: 4x32 bits
- **Channel 7**: empty

31 One-time programmable antifuse (OTP)

The OTP block is an array of one-time programmable antifuse memory cells.

All OTP banks feature an embedded charge pump which provides internally the high voltage necessary for antifuse programming sessions. Therefore, it is not necessary to use an additional high voltage pad at the chip interface. OTP is software programmable, so no dedicated programming interface is needed at chip level.

31.1 Main features

OTP embeds three 255-bit banks, with these features:

- BANK 1: 255-bit data bank with write-protect mechanism
- BANK 2: 255-bit data bank with write-protect mechanism
- BANK M: 255-bit bank, logically partitioned as follows:
  - 32 bits (16 + redundancy) used for BANK1/BANK2 write protection
  - 4 bits (2 + redundancy) reserved for selecting usage of 2 following sections (ID and key)
  - 72 bits free or reserved for USB/PCI ID data (64 + ECC)
  - 137 bits free or reserved for key storage (128 + ECC)
  - 2 bits (1 + redundancy) reserved for disabling ARM debug feature
  - 8 bits reserved

32 General purpose timer (GPT)

General purpose timers can be used for precise timing measurement and for measurement of frequency of any input signal. They are essentially counters that increment based on the clock cycle and the timer prescaler. An application can monitor these counters to determine how much time has elapsed. GPT can have timer and capture mode capabilities.

32.1 Main features

- It is constituted by 2 channels; each one consists of a programmable 16-bit counter and a dedicated 8-bit timer clock prescaler
- The programmable 8-bit prescaler unit performs a clock division by 1, 2, 4, 8, 16, 32, 64, 128, and 256
- Three interrupt sources (MATCH, REDG, and FEDG) are available for each timer channel. They are mapped to a single interrupt line for each channel but may be individually masked and acknowledged
- Each timer has a separate register set to control, enable and run each channel separately
- Three modes of operations are available for each timer channel:
  - Auto-reload mode
  - Single-shot mode
  - Capture function

Auto-reload mode

When the timer is enabled, the counter is cleared and starts incrementing. When it reaches the compare register value, an interrupt source is activated, the counter is automatically cleared and restarts incrementing. The process is repeated until the timer is disabled.

Single-shot mode

When the timer is enabled, the counter is cleared and starts incrementing. When it reaches the compare register value, an interrupt source is activated, the counter stopped and the timer disabled.

Capture function

This function is provided for the measurement of input timing signals. After being initialized, when a rising transition occurs at the GPTx_TMR_CAPX (x =1,2 depending upon the timer used)(X =1,2 depending upon the channel used for the timer) input, the actual counter value is stored into the rising edge capture register In the same way, when a falling edge transition occurs at the CAPT input, the actual counter value is stored into the falling edge capture register. You can read the value stored in the two capture registers and compute the duration of the rising to falling edge (or vice versa) time interval.

33 Real-time clock (RTC)

The RTC is a block that keeps track of the real time of day. It also functions as an alarm and a calendar. The time is displayed in 24-hour format, and time/calendar values are stored in binary-coded decimal format.

The time of day, alarm and calendar, status and control registers can all be accessed via a standard 32 APB bus. All read/write operations last 2 cycles.

RTC provides a self isolation mode that is activated during power down. This feature allows RTC to continue working if power is not supplied to the rest of the circuit. This feature is realized by supplying separate power and clock connections.

A set of 16 general purpose registers (GP-Reg) are provided which can be used to save data during the power down state.GP-Reg-set runs on 32 K oscillator clock and powered by RTC battery. Each register is 32-bit and addressed mapped on the 32-bit APB bus. A bit in status register reflects the status of any pending write to GP-Reg-set. This means that write operation to the GP-Reg-set should be sequential, so you should wait for this pending status bit to be cleared before writing again to GP-Reg-set.

33.1 Main features

- Works on dedicated 32768 Hz external clock and power supply
- 9999- year calendar
- Leap years support
- Programmable alarm interrupt
- Power management and self-isolation
- Prescaler and timer registers bypass for TEST
- Time and date update monitors
- 16 general purpose registers which can be used to save data during power down state.

34 Direct memory access controller (DMAC)

The DMAC is an AHB-central DMA controller core that transfers data from a source peripheral to a destination peripheral over two AHB buses. A wrapper is designed to instantiate 2 DMAC cores (each with 2 AHB master interfaces), 2 ICMs (which arbitrate the same master interface of each DMAC) and a MUX (which manages multiple peripheral handshaking interfaces).

34.1 Main features

- AMBA 2.0-compliant
- AHB slave interface – used to program the DMAC
- 8 channels, one per source and destination pair
- Unidirectional channels – data transfers in one direction only
- Programmable channel priority
- 2 independent AHB master interfaces
- Data bus width configured to 64 bits for each AHB master interface
- Configurable endianness for master interfaces
- Support for memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral DMA transfers
- Component ID parameters for configurable software driver support
- Programmable source and destination addresses (on AHB bus)
- Address increment, decrement or no change
- Multiblock transfers achieved through linked lists (block chaining)
- Independent source and destination selection of multiblock transfer type
- Scatter/Gather
- Single FIFO per channel for source and destination
- FIFO depth configured to 16 bytes for the first 4 channels and to 128 bytes for the last 4 channels
- D flip-flop-based FIFO
- Automatic data packing or unpacking to fit FIFO width
- Programmable source and destination for each channel
- Programmable transfer type for each channel (memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral)
- Programmable burst transaction size for each channel
- Programmable enable and disable of DMA channel
- Support for disabling channel without data loss
- Support for suspension of DMA operation
- Support for RETRY, SPLIT, and ERROR responses

- Programmable maximum burst transfer size per channel
- Maximum transaction size configured to 256 for all the channels
- Maximum block size configured to 4095 for all the channels
- Bus locking – can be programmed to be over the transaction, block, or DMA transfer level
- Channel locking – can be programmed to be over the transaction, block, or DMA transfer level
- 16 Handshaking interfaces for source and destination peripherals
- Hardware and Software handshaking interfaces
- Peripheral interrupt handshaking interface
- Handshaking interface supports single or burst DMA transactions
- Polarity control for hardware handshaking interface
- Enabling and disabling of individual DMA handshaking interface
- Programmable flow control at block transfer level (source, destination or DMAC core)
- Software control of source data pre-fetch when destination is flow controller
- Combined and separate interrupt requests
- Interrupt generation on DMA transfer (multiblock) completion, block transfer completion, single and burst transaction completion and error condition
- Support of interrupt enabling and masking.

35 JPEG Codec (JPGC)

The design ware (DW) JPEG Codec with header processing is part of a SoC-based multimedia solution that enables fast and simple image compression and decompression.

35.1 Main features

The main features of DW JPEG Codec are:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Four-channel interface: Pixel In, Compressed Out, Compressed In, Pixel Out
- Stallable design
- Hardware support for restart marker insertion
- Support for single, greyscale component
- Functionality to enable/disable header processing
- Internal registers interface
- Fully synchronous design
- Configured for high-speed decode mode.

36 Analog-to-digital converter (ADC)

The ADC integrated in the device has the following features.

36.1 Main features

- Successive approximation A/D conversion
- 10-bit resolution
- 1 MSPS
- 8 analog input channels (0 – 2.5 V)
- INL ± 1 LSB
- DNL ± 1 LSB
- Programmable conversion speed – minimum conversion time 1 µs

37 General purpose input/output (GPIO)

The general purpose input/output (GPIO) block provides 8 programmable inputs or outputs. Each input/output can be controlled in software mode through an APB interface.

37.1 Main features

- Eight individually programmable input/output pins (default to input at reset)
- An APB slave acting as control interface in software mode
- Programmable interrupt generation capability on any number of pins
- Bit masking in both read and writes operation through address lines

38 Temperature sensor (THSENS)

The THSENS block is an embedded sensor for junction temperature monitoring.

38.1 Main features

- Embeds a thermal sensor providing digital measurement of junction temperature
- Allows offset correction of digital measurement (calibrated at testing)
- Generates a “high temperature” interrupt when junction temperature exceeds a software programmable higher bound threshold
- Generates a “low temperature” interrupt when junction temperature is lower than a software programmable lower bound threshold
- Supports operating conditions ranging from –40 to 125°C
- Allows measurement of junction temperature starting at 0°C
- Software programmable power-down functionality for lower power consumption
- Continuous (periodic) sensing of temperature when not powered down.

39 Revision history

Table 3. Document revision history

Date	Revision	Changes
4-Jun-2010	1	Initial release.
20-Aug-2010	2	Modified confidentiality level from public to confidential. Minor text changes.
26-Aug-2010	3	Modified confidentiality level from confidential to public for the announce of the product.
2-Sep-2010	4	Updated information about PCIe and SATA: – Modified the feature list in the first page. – Modified *Figure 1: SPEAr1310 system connectivity* – Modified *Figure 2: SPEAr1310 block diagram of the internal connectivity* Reviewed the structure of the document. Reviewed *Chapter 8: Static RAM (SRAM)* Added *Chapter 7: Reset and clock generator (RCG)* Updated *Chapter 9: Multiport memory controller (MPMC)* Updated *Chapter 10: Flexible static memory controller (FSMC)* Updated *Chapter 12: Giga/Fast Ethernet media access controller (GMAC)* Updated *Chapter 16: 32-bit PCI expansion bus* Updated *Chapter 23: Universal asynchronous receiver/transmitter (UART)* Updated *Chapter 30: Security co-processor (C3)* Updated *Chapter 32: General purpose timer (GPT)* Updated *Chapter 33: Real-time clock (RTC)* Updated *Chapter 35: JPEG Codec (JPGC)*

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