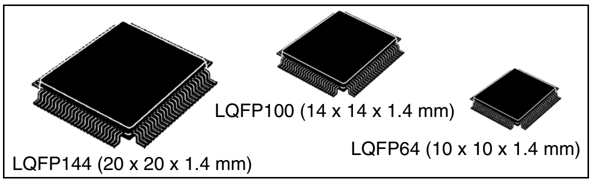
SPC560B40x, SPC560B50x SPC560C40x, SPC560C50x

32-bit MCU family built on the Power Architecture® for automotive body electronics applications



Features

- High-performance 64 MHz e200z0h CPU
  - 32-bit Power Architecture® technology
  - Up to 60 DMIPs operation
  - Variable length encoding (VLE)
- Memory
  - Up to 512 Kbytes Code Flash, with ECC
  - 64 Kbytes Data Flash, with ECC
  - Up to 48 Kbytes SRAM, with ECC
  - 8-entry memory protection unit (MPU)
- Interrupts
  - 16 priority levels
  - Non-maskable interrupt (NMI)
  - Up to 34 ext. int. including 18 wakeup lines
- GPIO: LQFP64/45, LQFP100/75, LQFP144/123
- Timer units
  - 6-channel 32-bit periodic interrupt timers
  - 4-channel 32-bit system timer module
  - System watchdog timer
  - Real-time clock timer
- 16-bit counter time-triggered I/Os
  - Up to 56 channels with PWM/MC/IC/OC
  - ADC diagnostic via CTU
- Communications interface
  - Up to 6 FlexCAN interfaces (2.0B active) with 64-message objects each
  - Up to 4 LINFlex/UART
  - 3 DSPI / I^2C
- 10-bit A/D converter with up to 36 channels
  - Up to 64 channels via external multiplexing
  - Individual conversion registers
  - Cross triggering unit
- Dedicated diagnostic module for lighting
  - Advanced PWM generation
  - Time-triggered diagnostic
  - PWM-synchronized ADC measurements
- Clock generation
  - 4 to 16 MHz fast external crystal oscillator
  - 32 KHz slow external crystal oscillator
  - 16 MHz fast internal RC oscillator
  - 128 kHz slow internal RC oscillator
  - Software-controlled FMPLL
  - Clock monitoring unit
- Exhaustive debugging capability
  - Nexus1 on all devices
  - Nexus2+ available on emulation package
- Low power capabilities
  - Ultra-low power standby with RTC, SRAM and CAN monitoring
  - Fast wakeup schemes
- Operating temp. range up to -40 to 125 °C
- Single 5 V or 3.3 V supply

Table 1. Device summary

Package	Part number			
	256 KB code Flash memory		512 KB code Flash memory	
LQFP144	SPC560B40L5	—	SPC560B50L5	—
LQFP100	SPC560B40L3	SPC560C40L3	SPC560B50L3	SPC560C50L3
LQFP64[(1)]	SPC560B40L1	SPC560C40L1	SPC560B50L1	SPC560C50L1

1. All LQFP64 information is indicative and must be confirmed during silicon validation.

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Contents

List of tables

List of figures

1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

1.2 Description

The SPC560B40x/50x and SPC560C40x/50x is a family of next generation microcontrollers built on the Power Architecture embedded category.

The SPC560B40x/50x and SPC560C40x/50x family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 2. SPC560B40x/50x and SPC560C40x/50x device comparison[1]

Feature	Device										
	SPC560B 40L1	SPC560B 40L3	SPC560B 40L5	SPC560C 40L1	SPC560C 40L3	SPC560B 50L1	SPC560B 50L3	SPC560B 50L5	SPC560C 50L1	SPC560C 50L3	SPC560B 50B2
CPU	e200z0h										
Execution speed[2]	Static – up to 64 MHz										
Code Flash	256 KB					512 KB					
Data Flash	64 KB (4 × 16 KB)										
RAM	24 KB			32 KB		32 KB			48 KB		
MPU	8-entry										
ADC (10-bit)	12 ch	28 ch	36 ch	8 ch	28 ch	12 ch	28 ch	36 ch	8 ch	28 ch	36 ch
CTU	Yes										
Total timer I/O[3] eMIOS	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit
– PWM + MC + IC/OC[4]	2 ch	5 ch	10 ch	2 ch	5 ch	2 ch	5 ch	10 ch	2 ch	5 ch	10 ch
– PWM + IC/OC[4]	10 ch	20 ch	40 ch	10 ch	20 ch	10 ch	20 ch	40 ch	10 ch	20 ch	40 ch
– IC/OC[4]	—	3 ch	6 ch	—	3 ch	—	3 ch	6 ch	—	3 ch	6 ch
SCI (LINFlex)	3[5]			4							
SPI (DSPI)	2	3		2	3	2	3		2	3	
CAN (FlexCAN)	2[6]			5	6	3[7]			5	6	
I^2C	1										
32 kHz oscillator	Yes										
GPIO[8]	45	79	123	45	79	45	79	123	45	79	123

Table 2. SPC560B40x/50x and SPC560C40x/50x device comparison(1) (continued)

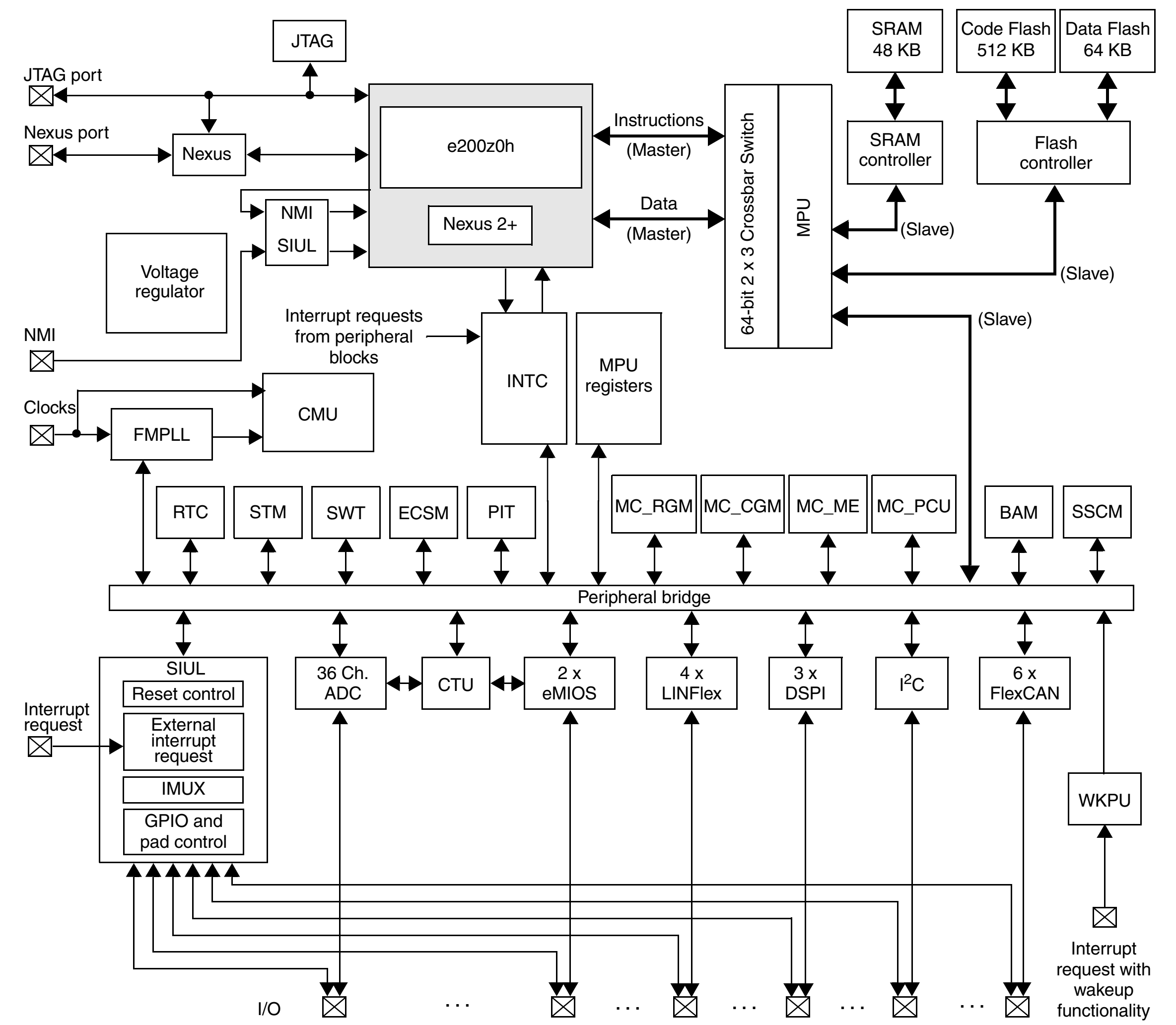
Feature	Device										
	SPC560B 40L1	**SPC560B 40L3**	**SPC560B 40L5**	**SPC560C 40L1**	**SPC560C 40L3**	**SPC560B 50L1**	**SPC560B 50L3**	**SPC560B 50L5**	**SPC560C 50L1**	**SPC560C 50L3**	**SPC560B 50B2**
Debug	JTAG										Nexus2+
Package	LQFP64(9)	LQFP100	LQFP144	LQFP64(9)	LQFP100	LQFP64(9)	LQFP100	LQFP144	LQFP64(9)	LQFP100	LBGA208 (10)

1. Feature set dependent on selected peripheral multiplexing—table shows example implementation
2. Based on 125 °C ambient operating temperature
3. See the eMIOS section of the device reference manual for information on the channel configuration and functions.
4. IC – Input Capture; OC – Output Compare; PWM – Pulse Width Modulation; MC – Modulus counter
5. SCI0, SCI1 and SCI2 are available. SCI3 is not available.
6. CAN0, CAN1 are available. CAN2, CAN3, CAN4 and CAN5 are not available.
7. CAN0, CAN1 and CAN2 are available. CAN3, CAN4 and CAN5 are not available.
8. I/O count based on multiplexing with peripherals
9. All LQFP64 information is indicative and must be confirmed during silicon validation.
10. LBGA208 available only as development package for Nexus2+

2 Block diagram

Figure 1 shows a top-level block diagram of the SPC560B40x/50x and SPC560C40x/50x device series.

Figure 1. SPC560B40x/50x and SPC560C40x/50x block diagram



Legend:

ADC	Analog-to-Digital Converter	MC_CGM	Clock Generation Module
BAM	Boot Assist Module	MC_ME	Mode Entry Module
FlexCAN	Controller Area Network	MC_PCU	Power Control Unit
CMU	Clock Monitor Unit	MC_RGM	Reset Generation Module
CTU	Cross Triggering Unit	MPU	Memory Protection Unit
DSPI	Deserial Serial Peripheral Interface	Nexus	Nexus Development Interface (NDI) Level
eMIOS	Enhanced Modular Input Output System	NMI	Non-Maskable Interrupt
FMPLL	Frequency-Modulated Phase-Locked Loop	PIT	Periodic Interrupt Timer
I^2C	Inter-integrated Circuit Bus	RTC	Real-Time Clock
IMUX	Internal Multiplexer	SIUL	System Integration Unit Lite
INTC	Interrupt Controller	SRAM	Static Random-Access Memory
JTAG	JTAG controller	SSCM	System Status Configuration Module
LINFlex	Serial Communication Interface (LIN support)	STM	System Timer Module
ECSM	Error Correction Status Module	SWT	Software Watchdog Timer
		WKPU	Wakeup Unit

Table 3 summarizes the functions of all blocks present in the SPC560B40x/50x and SPC560C40x/50x series of microcontrollers. Please note that the presence and number of blocks vary by device and package.

Table 3. SPC560B40x/50x and SPC560C40x/50x series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Error Correction Status Module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via “*n*” programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Inter-integrated circuit (I^2C™) bus	A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications

Table 3. SPC560B40x/50x and SPC560C40x/50x series block summary (continued)

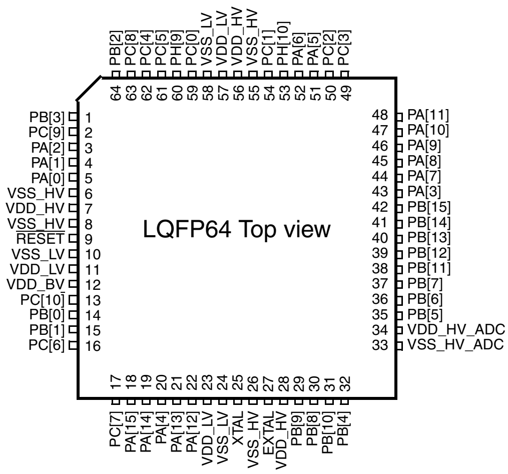
Block	Function
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
Nexus development interface (NDI)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2003 standard
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Real-time counter (RTC)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode)
System integration unit (SIU)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System status configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	The wakeup unit supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.
Crossbar (XBAR) switch	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

3 Package pinouts and signal descriptions

3.1 Package pinouts

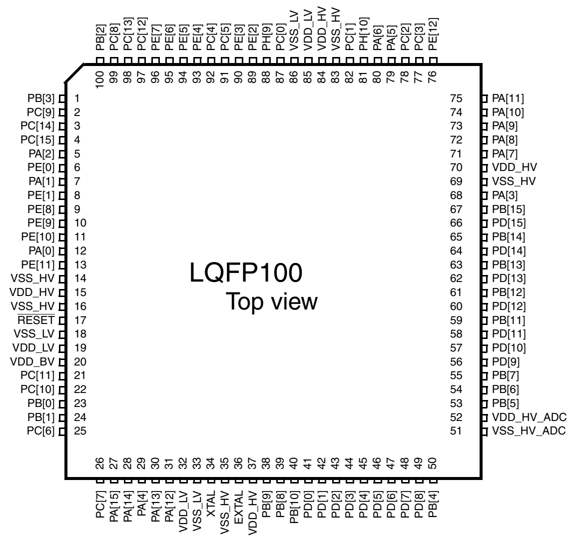
The available LQFP pinouts and the LBGA208 ballmap are provided in the following figures. For pin signal descriptions, please refer to the device reference manual (RM0017).

Figure 2. LQFP 64-pin configuration[a]



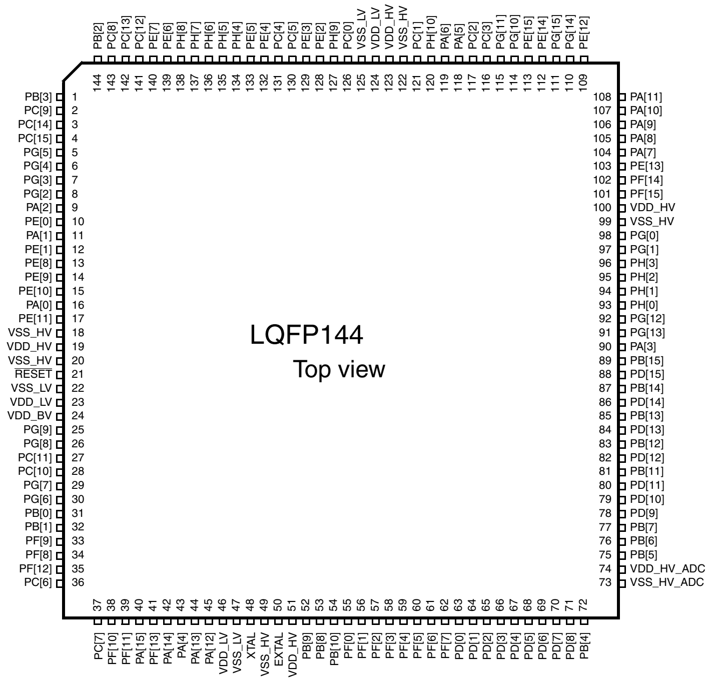
a. All LQFP64 information is indicative and must be confirmed during silicon validation.

Figure 3. LQFP 100-pin configuration



Note:
Availability of port pin alternate functions depends on product selection.

Figure 4. LQFP 144-pin configuration



Note:
Availability of port pin alternate functions depends on product selection.

Figure 5. LBGA208 confguration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[8]	PC[13]	NC	NC	PH[8]	PH[4]	PC[5]	PC[0]	NC	NC	PC[2]	NC	PE[15]	NC	NC	NC	A
B	PC[9]	PB[2]	NC	PC[12]	PE[6]	PH[5]	PC[4]	PH[9]	PH[10]	NC	PC[3]	PG[11]	PG[15]	PG[14]	PA[11]	PA[10]	B
C	PC[14]	VDD_HV	PB[3]	PE[7]	PH[7]	PE[5]	PE[3]	VSS_LV	PC[1]	NC	PA[5]	NC	PE[14]	PE[12]	PA[9]	PA[8]	C
D	NC	NC	PC[15]	NC	PH[6]	PE[4]	PE[2]	VDD_LV	VDD_HV	NC	PA[6]	NC	PG[10]	PF[14]	PE[13]	PA[7]	D
E	PG[4]	PG[5]	PG[3]	PG[2]									PG[1]	PG[0]	PF[15]	VDD_HV	E
F	PE[0]	PA[2]	PA[1]	PE[1]									PH[0]	PH[1]	PH[3]	PH[2]	F
G	PE[9]	PE[8]	PE[10]	PA[0]			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV	NC	NC	MSEO	G
H	VSS_HV	PE[11]	VDD_HV	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			MDO3	MDO2	MDO0	MDO1	H
J	RESET	VSS_LV	NC	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			NC	NC	NC	NC	J
K	EVTI	NC	VDD_BV	VDD_LV			VSS_HV	VSS_HV	VSS_HV	VSS_HV			NC	PG[12]	PA[3]	PG[13]	K
L	PG[9]	PG[8]	NC	EVTO									PB[15]	PD[15]	PD[14]	PB[14]	L
M	PG[7]	PG[6]	PC[10]	PC[11]									PB[13]	PD[13]	PD[12]	PB[12]	M
N	PB[1]	PF[9]	PB[0]	NC	NC	PA[4]	VSS_LV	EXTAL	VDD_HV	PF[0]	PF[4]	NC	PB[11]	PD[10]	PD[9]	PD[11]	N
P	PF[8]	NC	PC[7]	NC	NC	PA[14]	VDD_LV	XTAL	PB[10]	PF[1]	PF[5]	PD[0]	PD[3]	VDD_HV_ADC	PB[6]	PB[7]	P
R	PF[12]	PC[6]	PF[10]	PF[11]	VDD_HV	PA[15]	PA[13]	NC	OSC32K_XTAL	PF[3]	PF[7]	PD[2]	PD[4]	PD[7]	VSS_HV_ADC	PB[5]	R
T	NC	NC	NC	MCKO	NC	PF[13]	PA[12]	NC	OSC32K_EXTAL	PF[2]	PF[6]	PD[1]	PD[5]	PD[6]	PD[8]	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Note: LBGA208 available only as development package for Nexus 2+.

NC = Not connected

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are forced to tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS[0]) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS and TDI) are pull-up whilst TDO remains tristate.
- Precise ADC pads (PB[7:4] and PD[11:0]) are left tristate (no output buffer available).
- Main oscillator pads (EXTAL, XTAL) are tristate.
- Nexus output pads (MDO[n], MCKO, EVTO, MSEO) are forced to output.

3.3 Voltage supply pins

Voltage supply pins are used to provide power to the device. Three dedicated VDD_LV/VSS_LV supply pairs are used for 1.2 V regulator stabilization.

Table 4. Voltage supply pin descriptions

Port pin	Function	Pin number			
		LQFP64	LQFP100	LQFP144	LBGA208(1)
VDD_HV	Digital supply voltage	7, 28, 56	15, 37, 70, 84	19, 51, 100, 123	C2, D9, E16, G13, H3, N9, R5
VSS_HV	Digital ground	6, 8, 26, 55	14, 16, 35, 69, 83	18, 20, 49, 99, 122	G7, G8, G9, G10, H1, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10
VDD_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{SS_LV} pin.(2)	11, 23, 57	19, 32, 85	23, 46, 124	D8, K4, P7
VSS_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{DD_LV} pin.(2)	10, 24, 58	18, 33, 86	22, 47, 125	C8, J2, N7
VDD_BV	Internal regulator supply voltage	12	20	24	K3
VSS_HV_ADC	Reference ground and analog ground for the ADC	33	51	73	R15
VDD_HV_ADC	Reference voltage and analog supply for the ADC	34	52	74	P14

1. LBGA208 available only as development package for Nexus2+.
2. A decoupling capacitor must be placed between each of the three VDD_LV/VSS_LV supply pairs to ensure stable voltage (see the recommended operating conditions in the device datasheet for details).

3.4 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[b]

M = Medium [b][c]

F = Fast [b][c]

I = Input only with analog feature[b]

J = Input/Output (‘S’ pad) with analog feature

X = Oscillator

3.5 System pins

The system pins are listed in *Table 5*.

Table 5. System pin descriptions

System pin	Function	I/O direction	Pad type	RESET configuration	Pin number			
					LQFP64	LQFP100	LQFP144	LBGA208[1]
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	9	17	21	J1
EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.[2]	I/O	X	Tristate	27	36	50	N8
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.[2]	I	X	Tristate	25	34	48	P8

1. LBGA208 available only as development package for Nexus2+.
2. See the relevant section of the datasheet .

b. See the I/O pad electrical characteristics in the device datasheet for details.

c. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium (see PCR.SRC in section Pad Configuration Registers (PCR0–PCR122) in the device reference manual).

3.6 Functional ports

The functional port pins are listed in *Table 6*.

Table 6. Functional port pin descriptions

Port pin	PCR	Alternate function(1)	Function	Peripheral	I/O direction(2)	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208(3)
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT — WKPU[19](4)	SIUL eMIOS_0 CGL — WKPU	I/O I/O O — I	M	Tristate	5	12	16	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — —	GPIO[1] E0UC[1] — — NMI(5) WKPU[2](4)	SIUL eMIOS_0 — — WKPU WKPU	I/O I/O — — I I	S	Tristate	4	7	11	F3
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — — WKPU[3](4)	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	3	5	9	F2
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 —	GPIO[3] E0UC[3] — — EIRQ[0]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	43	68	90	K15
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — — WKPU[9](4)	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	20	29	43	N6

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	51	79	118	C11
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — — EIRQ[1]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	52	80	119	D11
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2]	SIUL eMIOS_0 LINFlex_3 — SIUL	I/O I/O O — I	S	Tristate	44	71	104	D16
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[6] —	GPIO[8] E0UC[8] — — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 — — SIUL BAM LINFlex_3	I/O I/O — — I I I	S	Input, weak pull-up	45	72	105	C16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[6]	GPIO[9] E0UC[9] — — FAB	SIUL eMIOS_0 — — BAM	I/O I/O — — I	S	Pull-down	46	73	106	C15
PA[10]	PCR[10]	AF0 AF1 AF2 AF3	GPIO[10] E0UC[10] SDA —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	S	Tristate	47	74	107	B16

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function(1)	Function	Peripheral	I/O direction(2)	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208(3)
PA[11]	PCR[11]	AF0 AF1 AF2 AF3	GPIO[11] E0UC[11] SCL —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	S	Tristate	48	75	108	B15
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 —	GPIO[12] — — — SIN_0	SIUL — — — DSPI0	I/O — — — I	S	Tristate	22	31	45	T7
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 — —	SIUL DSPI_0 — —	I/O O — —	M	Tristate	21	30	44	R7
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 — EIRQ[4]	SIUL DSPI_0 DSPI_0 — SIUL	I/O I/O I/O — I	M	Tristate	19	28	42	P6
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 — WKPU[10](4)	SIUL DSPI_0 DSPI_0 — WKPU	I/O I/O I/O — I	M	Tristate	18	27	40	R6
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX — —	SIUL FlexCAN_0 — —	I/O O — —	M	Tristate	14	23	31	N3

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function(1)	Function	Peripheral	I/O direction(2)	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208(3)
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — —	GPIO[17] — — — WKPU[4](4) CAN0RX	SIUL — — — WKPU FlexCAN_0	I/O — — — I I	S	Tristate	15	24	32	N1
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA —	SIUL LINFlex_0 I2C_0 —	I/O O I/O —	M	Tristate	64	100	144	B2
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] — SCL — WKPU[11](4) LIN0RX	SIUL — I2C_0 — WKPU LINFlex_0	I/O — I/O — I I	S	Tristate	1	1	1	C3
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 —	GPIO[20] — — — GPI[0]	SIUL — — — ADC	I — — — I	I	Tristate	32	50	72	T16
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 —	GPIO[21] — — — GPI[1]	SIUL — — — ADC	I — — — I	I	Tristate	35	53	75	R16
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 —	GPIO[22] — — — GPI[2]	SIUL — — — ADC	I — — — I	I	Tristate	36	54	76	P15

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number LQFP64	Pin number LQFP100	Pin number LQFP144	Pin number LBGA208[3]
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — GPI[3]	SIUL — — — ADC	I — — — I	I	Tristate	37	55	77	P16
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — ANS[0] OSC32K_XTAL[7]	SIUL — — — ADC SXOSC	I — — — I I/O	I	Tristate	30	39	53	R9
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — ANS[1] OSC32K_EXTAL[7]	SIUL — — — ADC SXOSC	I — — — I I/O	I	Tristate	29	38	52	T9
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ANS[2] WKPU[8][4]	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	40	54	P9
PB[11][8]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ANS[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	59	81	N13

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function(1)	Function	Peripheral	I/O direction(2)	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208(3)
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ANX[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	61	83	M16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ANX[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	63	85	M13
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ANX[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	65	87	L16
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ANX[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	67	89	L13
PC[0](9)	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	87	126	A8
PC[1](9)	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO(10) —	SIUL — JTAGC —	I/O — O —	M	Tristate	54	82	121	C9

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX[11] — EIRQ[5]	SIUL DSPI_1 FlexCAN_4 — SIUL	I/O I/O O — I	M	Tristate	50	78	117	A11
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] — CAN1RX CAN4RX[11] EIRQ[6]	SIUL DSPI_1 ADC — FlexCAN_1 FlexCAN_4 SIUL	I/O I/O O — I I I	S	Tristate	49	77	116	B11
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — —	GPIO[36] — — — SIN_1 CAN3RX[11]	SIUL — — — DSPI_1 FlexCAN_3	I/O — — — I I	M	Tristate	62	92	131	B7
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 CAN3TX[11] — EIRQ[7]	SIUL DSPI1 FlexCAN_3 — SIUL	I/O O O — I	M	Tristate	61	91	130	A7
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX — —	SIUL LINFlex_1 — —	I/O O — —	S	Tristate	16	25	36	R2

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function(1)	Function	Peripheral	I/O direction(2)	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208(3)
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — — — LIN1RX WKPU[12](4)	SIUL — — — LINFlex_1 WKPU	I/O — — — I I	S	Tristate	17	26	37	P3
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX — —	SIUL LINFlex_2 — —	I/O O — —	S	Tristate	63	99	143	A1
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — — — LIN2RX WKPU[13](4)	SIUL — — — LINFlex_2 WKPU	I/O — — — I I	S	Tristate	2	2	2	B1
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX(11) MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC	I/O O O O	M	Tristate	13	22	28	M3
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — — CAN1RX CAN4RX(11) WKPU[5](4)	SIUL — — — FlexCAN_1 FlexCAN_4 WKPU	I/O — — — I I I	S	Tristate	—	21	27	M4

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — SIN_2	SIUL eMIOS_0 — — DSPI_2	I/O I/O — — I	M	Tristate	—	97	141	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	—	98	142	A2
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	—	3	3	C1
PC[15]	PCR[47]	AF0 AF1 AF2 AF3	GPIO[47] E0UC[15] CS0_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O I/O —	M	Tristate	—	4	4	D3
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 —	GPIO[48] — — — GPI[4]	SIUL — — — ADC	I — — — I	I	Tristate	—	41	63	P12
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 —	GPIO[49] — — — GPI[5]	SIUL — — — ADC	I — — — I	I	Tristate	—	42	64	T12

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function(1)	Function	Peripheral	I/O direction(2)	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208(3)
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 —	GPIO[50] — — — GPI[6]	SIUL — — — ADC	I — — — I	I	Tristate	—	43	65	R12
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 —	GPIO[51] — — — GPI[7]	SIUL — — — ADC	I — — — I	I	Tristate	—	44	66	P13
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 —	GPIO[52] — — — GPI[8]	SIUL — — — ADC	I — — — I	I	Tristate	—	45	67	R13
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 —	GPIO[53] — — — GPI[9]	SIUL — — — ADC	I — — — I	I	Tristate	—	46	68	T13
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 —	GPIO[54] — — — GPI[10]	SIUL — — — ADC	I — — — I	I	Tristate	—	47	69	T14
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 —	GPIO[55] — — — GPI[11]	SIUL — — — ADC	I — — — I	I	Tristate	—	48	70	R14

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 —	GPIO[56] — — — GPI[12]	SIUL — — — ADC	I — — — I	I	Tristate	—	49	71	T15
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 —	GPIO[57] — — — GPI[13]	SIUL — — — ADC	I — — — I	I	Tristate	—	56	78	N15
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 —	GPIO[58] — — — GPI[14]	SIUL — — — ADC	I — — — I	I	Tristate	—	57	79	N14
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 —	GPIO[59] — — — GPI[15]	SIUL — — — ADC	I — — — I	I	Tristate	—	58	80	N16
PD[12][8]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ANS[4]	SIUL DSPI_0 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	60	82	M15
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ANS[5]	SIUL DSPI_1 eMIOS_0 — ADC	I/O I/O I/O — I	J	Tristate	—	62	84	M14

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function(1)	Function	Peripheral	I/O direction(2)	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208(3)
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — ANS[6]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	64	86	L15
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — ANS[7]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	66	88	L14
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] — — CAN5RX(11) WKPU[6](4)	SIUL eMIOS_0 — — FlexCAN_5 WKPU	I/O I/O — — I I	S	Tristate	—	6	10	F1
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] CAN5TX(11) —	SIUL eMIOS_0 FlexCAN_5 —	I/O I/O O —	M	Tristate	—	8	12	F4
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 —	GPIO[66] E0UC[18] — — SIN_1	SIUL eMIOS_0 — — DSPI_1	I/O I/O — — I	M	Tristate	—	89	128	D7
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS_0 DSPI_1 —	I/O I/O O —	M	Tristate	—	90	129	C7

Table 6. **Functional port pin descriptions (continued)**

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 — EIRQ[9]	SIUL eMIOS_0 DSPI_1 — SIUL	I/O I/O I/O — I	M	Tristate	—	93	132	D6
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC	I/O I/O I/O O	M	Tristate	—	94	133	C6
PE[6]	PCR[70]	AF0 AF1 AF2 AF3	GPIO[70] E0UC[22] CS3_0 MA[1]	SIUL eMIOS_0 DSPI_0 ADC	I/O I/O O O	M	Tristate	—	95	139	B5
PE[7]	PCR[71]	AF0 AF1 AF2 AF3	GPIO[71] E0UC[23] CS2_0 MA[0]	SIUL eMIOS_0 DSPI_0 ADC	I/O I/O O O	M	Tristate	—	96	140	C4
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX[12] E0UC[22] CAN3TX[11]	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M	Tristate	—	9	13	G2
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKPU[7][4] CAN2RX[12] CAN3RX[11]	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	—	10	14	G1

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 — EIRQ[10]	SIUL LINFlex_3 DSPI_1 — SIUL	I/O O O — I	S	Tristate	—	11	15	G3
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] — CS4_1 — LIN3RX WKPU[14][4]	SIUL — DSPI_1 — LINFlex_3 WKPU	I/O — O — I I	S	Tristate	—	13	17	H2
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — —	GPIO[76] — E1UC[19][13] — SIN_2 EIRQ[11]	SIUL — eMIOS_1 — DSPI_2 SIUL	I/O — I/O — I I	S	Tristate	—	76	109	C14
PE[13]	PCR[77]	AF0 AF1 AF2 AF3	GPIO[77] SOUT2 E1UC[20] —	SIUL DSPI_2 eMIOS_1 —	I/O O I/O —	S	Tristate	—	—	103	D15
PE[14]	PCR[78]	AF0 AF1 AF2 AF3 —	GPIO[78] SCK_2 E1UC[21] — EIRQ[12]	SIUL DSPI_2 eMIOS_1 — SIUL	I/O I/O I/O — I	S	Tristate	—	—	112	C13
PE[15]	PCR[79]	AF0 AF1 AF2 AF3	GPIO[79] CS0_2 E1UC[22] —	SIUL DSPI_2 eMIOS_1 —	I/O I/O I/O —	M	Tristate	—	—	113	A13

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PF[0]	PCR[80]	AF0 AF1 AF2 AF3 —	GPIO[80] E0UC[10] CS3_1 — ANS[8]	SIUL eMIOS_0 DSPI_1 — ADC	I/O I/O O — I	J	Tristate	—	—	55	N10
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ANS[9]	SIUL eMIOS_0 DSPI_1 — I	I/O I/O O — I	J	Tristate	—	—	56	P10
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ANS[10]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O I/O — I	J	Tristate	—	—	57	T10
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ANS[11]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	—	58	R10
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ANS[12]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	—	59	N11
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ANS[13]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	—	60	P11

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function(1)	Function	Peripheral	I/O direction(2)	Pad type	RESET configuration	Pin number LQFP64	Pin number LQFP100	Pin number LQFP144	Pin number LBGA208(3)
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] — — ANS[14]	SIUL eMIOS_0 — — ADC	I/O I/O — — I	J	Tristate	—	—	61	T11
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — — — ANS[15]	SIUL — — — ADC	I/O — — — I	J	Tristate	—	—	62	R11
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX(14) CS4_0 CAN2TX(15)	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M	Tristate	—	—	34	P1
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — —	GPIO[89] — CS5_0 — CAN2RX(15) CAN3RX(14)	SIUL — DSPI_0 — FlexCAN_2 FlexCAN_3	I/O — O — I I	S	Tristate	—	—	33	N2
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] — — —	SIUL — — —	I/O — — —	M	Tristate	—	—	38	R3
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 —	GPIO[91] — — — WKPU[15](4)	SIUL — — — WKPU	I/O — — — I	S	Tristate	—	—	39	R4

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function(1)	Function	Peripheral	I/O direction(2)	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208(3)
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	35	R1
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 —	GPIO[93] E1UC[26] — — WKPU[16](4)	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	S	Tristate	—	—	41	T6
PF[14]	PCR[94]	AF0 AF1 AF2 AF3	GPIO[94] CAN4TX(11) E1UC[27] CAN1TX	SIUL FlexCAN_4 eMIOS_1 FlexCAN_4	I/O O I/O O	M	Tristate	—	—	102	D14
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — —	GPIO[95] — — — CAN1RX CAN4RX(11) EIRQ[13]	SIUL — — — FlexCAN_1 FlexCAN_4 SIUL	I/O — — — I I I	S	Tristate	—	—	101	E15
PG[0]	PCR[96]	AF0 AF1 AF2 AF3	GPIO[96] CAN5TX(11) E1UC[23] —	SIUL FlexCAN_5 eMIOS_1 —	I/O O I/O —	M	Tristate	—	—	98	E14
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — —	GPIO[97] — E1UC[24] — CAN5RX(11) EIRQ[14]	SIUL — eMIOS_1 — FlexCAN_5 SIUL	I/O — I/O — I I	S	Tristate	—	—	97	E13

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number LQFP64	LQFP100	LQFP144	LBGA208[3]
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	8	E4
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] — — WKPU[17][4]	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	S	Tristate	—	—	7	E3
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	6	E1
PG[5]	PCR[101]	AF0 AF1 AF2 AF3 —	GPIO[101] E1UC[14] — — WKPU[18][4]	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	S	Tristate	—	—	5	E2
PG[6]	PCR[102]	AF0 AF1 AF2 AF3	GPIO[102] E1UC[15] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	30	M2
PG[7]	PCR[103]	AF0 AF1 AF2 AF3	GPIO[103] E1UC[16] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	29	M1

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number LQFP64	Pin number LQFP100	Pin number LQFP144	Pin number LBGA208[3]
PG[8]	PCR[104]	AF0 AF1 AF2 AF3 —	GPIO[104] E1UC[17] — CS0_2 EIRQ[15]	SIUL eMIOS_1 — DSPI_2 SIUL	I/O I/O — I/O I	S	Tristate	—	—	26	L2
PG[9]	PCR[105]	AF0 AF1 AF2 AF3	GPIO[105] E1UC[18] — SCK_2	SIUL eMIOS_1 — DSPI_2	I/O I/O — I/O	S	Tristate	—	—	25	L1
PG[10]	PCR[106]	AF0 AF1 AF2 AF3	GPIO[106] E0UC[24] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	—	114	D13
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	115	B12
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	92	K14
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	91	K16
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	—	110	B14

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PG[15]	PCR[111]	AF0 AF1 AF2 AF3	GPIO[111] E1UC[1] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	111	B13
PH[0]	PCR[112]	AF0 AF1 AF2 AF3 —	GPIO[112] E1UC[2] — — SIN1	SIUL eMIOS_1 — — DSPI_1	I/O I/O — — I	M	Tristate	—	—	93	F13
PH[1]	PCR[113]	AF0 AF1 AF2 AF3	GPIO[113] E1UC[3] SOUT1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O O —	M	Tristate	—	—	94	F14
PH[2]	PCR[114]	AF0 AF1 AF2 AF3	GPIO[114] E1UC[4] SCK_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	M	Tristate	—	—	95	F16
PH[3]	PCR[115]	AF0 AF1 AF2 AF3	GPIO[115] E1UC[5] CS0_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	M	Tristate	—	—	96	F15
PH[4]	PCR[116]	AF0 AF1 AF2 AF3	GPIO[116] E1UC[6] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	134	A6
PH[5]	PCR[117]	AF0 AF1 AF2 AF3	GPIO[117] E1UC[7] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	—	135	B6

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number			
								LQFP64	LQFP100	LQFP144	LBGA208[3]
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] — MA[2]	SIUL eMIOS_1 — ADC	I/O I/O — O	M	Tristate	—	—	136	D5
PH[7]	PCR[119]	AF0 AF1 AF2 AF3	GPIO[119] E1UC[9] CS3_2 MA[1]	SIUL eMIOS_1 DSPI_2 ADC	I/O I/O O O	M	Tristate	—	—	137	C5
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC	I/O I/O O O	M	Tristate	—	—	138	A5
PH[9][9]	PCR[121]	AF0 AF1 AF2 AF3	GPIO[121] — TCK —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	60	88	127	B8
PH[10][9]	PCR[122]	AF0 AF1 AF2 AF3	GPIO[122] — TMS —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	60	81	120	B9

1. Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 → AF0; PCR.PA = 01 → AF1; PCR.PA = 10 → AF2; PCR.PA = 11 → AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".
2. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.
3. LBGA208 available only as development package for Nexus2+.
4. All WKPU pins also support external interrupt capability. See wakeup unit chapter for further details.
5. NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.
6. "Not applicable" because these functions are available only while the device is booting. Refer to BAM chapter of the reference manual for details.
7. Value of PCR.IBE bit must be 0.

8. Be aware that this pad is used on the SPC560B64L3 and SPC560B64L5 to provide VDD_HV_ADC and VSS_HV_ADC1. Therefore, you should be careful in ensuring compatibility between SPC560B40x/50x and SPC560C40x/50x and SPC560B64.
9. Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
   PC[0:1] are available as JTAG pins (TDI and TDO respectively).
   PH[9:10] are available as JTAG pins (TCK and TMS respectively).
   If the user configures these JTAG pins in GPIO mode the device is no longer compliant with IEEE 1149.1-2001.
10. The TDO pad has been moved into the STANDBY domain in order to allow low-power debug handshaking in STANDBY mode. However, no pull-resistor is active on the TDO pad while in STANDBY mode. At this time the pad is configured as an input. When no debugger is connected the TDO pad is floating causing additional current consumption. To avoid the extra consumption TDO must be connected. An external pull-up resistor in the range of 47–100 kΩ should be added between the TDO pin and VDD. Only in case the TDO pin is used as application pin and a pull-up cannot be used then a pull-down resistor with the same value should be used between TDO pin and GND instead.
11. Available only on SPC560Cx versions and SPC560B50B2 devices.
12. Not available on SPC560B40L3 and SPC560B40L5 devices.
13. Not available in 100 LQFP package.
14. Available only on SPC560B50B2 devices.
15. Not available on SPC560B44L3 devices.

3.7 Nexus 2+ pins

In the LBGA208 package, eight additional debug pins are available (see *Table 7*).

Table 7. Nexus 2+ pin descriptions

Debug pin	Function	I/O direction	Pad type	Function after reset	Pin number		
					LQFP 100	LQFP 144	LBGA 208[(1)]
MCKO	Message clock out	O	F	—	—	—	T4
MDO0	Message data out 0	O	M	—	—	—	H15
MDO1	Message data out 1	O	M	—	—	—	H16
MDO2	Message data out 2	O	M	—	—	—	H14
MDO3	Message data out 3	O	M	—	—	—	H13
EVTI	Event in	I	M	Pull-up	—	—	K1
EVTO	Event out	O	M	—	—	—	L4
MSEO	Message start/end out	O	M	—	—	—	G16

1. LBGA208 available only as development package for Nexus2+.

4 Electrical characteristics

4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

Caution: All LQFP64 information is indicative and must be confirmed during silicon validation.

4.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.3 NVUSRO register

Bit values in the Non-Volatile User Options (NVUSRO) Register control portions of the device configuration, namely electrical parameters such as high voltage supply and oscillator margin, as well as digital functionality (watchdog enable/disable after reset).

For a detailed description of the NVUSRO register, please refer to the device reference manual.

4.3.1 NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. *Table 9* shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 9. PAD3V5V field description

Value(1)	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

4.3.2 NVUSRO[OSCILLATOR_MARGIN] field description

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value. *Table 10* shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 10. OSCILLATOR_MARGIN field description

Value(1)	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

1. Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

4.3.3 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. *Table 11* shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 11. WATCHDOG_EN field description

Value(1)	Description
0	Disable after reset
1	Enable after reset

1. Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

4.4 Absolute maximum ratings

Table 12. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	–0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_BV}	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	–0.3	V_{DD}+0.3	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_ADC}	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} –0.3	V_{DD}+0.3	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	—	V_{DD}+0.3	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	64	
I_{CORELV}	SR	Low voltage static current sink through VDD_BV	—	—	150	mA
$T_{STORAGE}$	SR	Storage temperature	—	–55	150	°C

Note: *Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.*

4.5 Recommended operating conditions

Table 13. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}(1)	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}(2)	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_BV}(3)	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V_{DD}	V_{DD}–0.1	V_{DD}+0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_ADC}(4)	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	3.0(5)	3.6	V
			Relative to V_{DD}	V_{DD}–0.1	V_{DD}+0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS}–0.1	—	V
			Relative to V_{DD}	—	V_{DD}+0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up(6)	—	—	0.25	V/µs

1. 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.
2. 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.
3. 400 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).
4. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.
6. Guaranteed by device validation.

Table 14. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}(1)	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
V_{SS_LV}(3)	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS}–0.1	V_{SS}+0.1	V

Table 14. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value Min	Value Max	Unit
V_{DD_BV}[4]	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
			Relative to V_{DD}	V_{DD}–0.1	V_{DD}+0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS}	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_ADC}[5]	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
			Relative to V_{DD}	V_{DD}–0.1	V_{DD}+0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS}–0.1	—	V
			Relative to V_{DD}	—	V_{DD}+0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up[6]	—	—	0.25	V/µs

1. 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.
2. Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.
3. 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.
4. 100 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).
5. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
6. Guaranteed by device validation.

Note: RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

4.6 Thermal characteristics

4.6.1 Package thermal characteristics

Table 15. LQFP thermal characteristics[1]

Symbol		C	Parameter	Conditions[2]	Pin count	Value	Unit
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[3]	Single-layer board - 1s	64	60	°C/W
					100	64	
					144	64	
				Four-layer board - 2s2p	64	42	
					100	51	
					144	49	
$R_{\theta JB}$	CC	D	Thermal resistance, junction-to-board[4]	Single-layer board - 1s	64	24	°C/W
					100	36	
					144	37	
				Four-layer board - 2s2p	64	24	
					100	34	
					144	35	
$R_{\theta JC}$	CC	D	Thermal resistance, junction-to-case[5]	Single-layer board - 1s	64	11	°C/W
					100	22	
					144	22	
				Four-layer board - 2s2p	64	11	
					100	22	
					144	22	
Ψ_{JB}	CC	D	Junction-to-board thermal characterization parameter, natural convection	Single-layer board - 1s	64	TBD	°C/W
					100	33	
					144	34	
				Four-layer board - 2s2p	64	TBD	
					100	34	
					144	35	
Ψ_{JC}	CC	D	Junction-to-case thermal characterization parameter, natural convection	Single-layer board - 1s	64	TBD	°C/W
					100	9	
					144	10	
				Four-layer board - 2s2p	64	TBD	
					100	9	
					144	10	

1. Thermal characteristics are based on simulation.
2. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C.

3. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
4. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
5. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4.6.2 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using *Equation 1*:

Equation 1 $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

Equation 2 $P_D = K / (T_J + 273\ °C)$

Therefore, solving equations *Equation 1* and *Equation 2*:

Equation 3 $K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2$

Where:

K is a constant for the particular part, which may be determined from *Equation 3* by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations *Equation 1* and *Equation 2* iteratively for any value of T_A.

4.7 I/O pad electrical characteristics

4.7.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—These pads provide maximum speed. There are used for improved Nexus debugging capability.
- Input only pads—These pads are associated to ADC channels and the external 32 kHz crystal oscillator (SXOSC) providing low input leakage.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

4.7.2 I/O input DC characteristics

Table 16 provides input DC electrical characteristics as described in *Figure 6*.

Figure 6. I/O input DC electrical characteristics definition

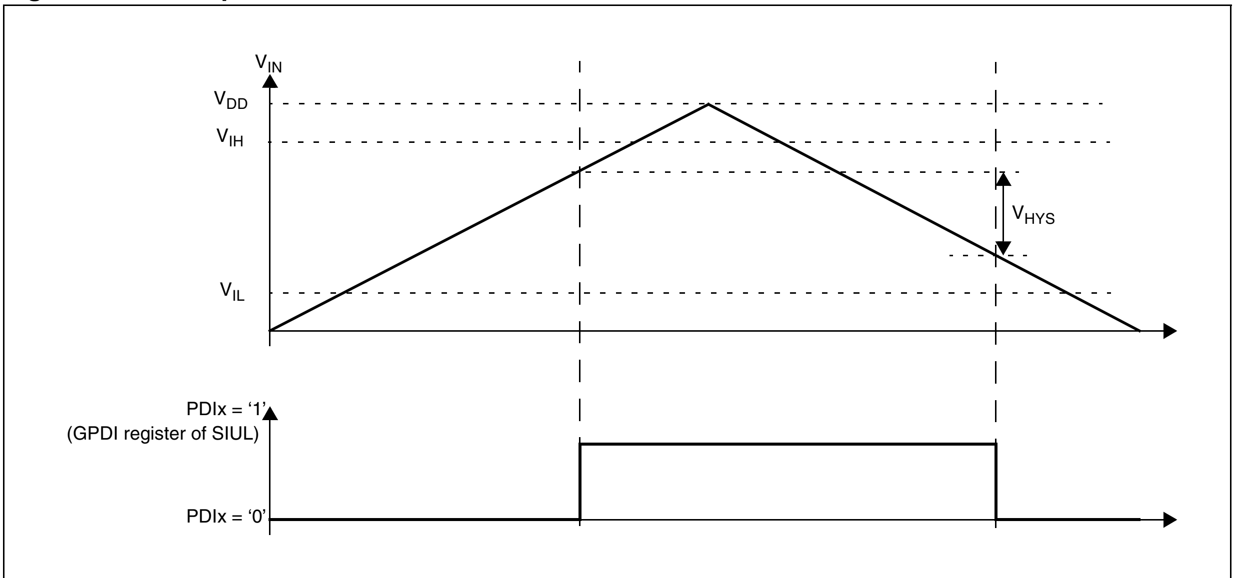


Table 16. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions(1)		Value Min	Typ	Max	Unit
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	V
I_{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	200	nA
		D			T_A = 25 °C	—	2	200	
		D			T_A = 85 °C	—	5	300	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}(2)	SR	P	Wakeup input filtered pulse	—		—	—	40	ns
W_{NFI}(2)	SR	P	Wakeup input not filtered pulse	—		1000	—	—	ns

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

4.7.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- *Table 17* provides weak pull figures. Both pull-up and pull-down resistances are supported.
- *Table 18* provides output driver characteristics for I/O pads when in SLOW configuration.
- *Table 19* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 20* provides output driver characteristics for I/O pads when in FAST configuration.

Table 17. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions(1)		Value Min	Typ	Max	Unit
$\lvert I_{WPU}\rvert$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1(2)	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\lvert I_{WPD}\rvert$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 18. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions(1)		Value Min	Typ	Max	Unit
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(2)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD}–0.8	—	—	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(2)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 19. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions(1)		Value Min	Typ	Max	Unit
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(2)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD}–0.8	—	—	
		C			I_{OH} = –100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	

Table 19. MEDIUM configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions(1)		Value Min	Typ	Max	Unit
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		P			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(2)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
		C			I_{OL} = 100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 20. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions(1)		Value Min	Typ	Max	Unit
V_{OH}	CC	P	Output high level FAST configuration	Push Pull	I_{OH} = –14mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –7mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(2)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –11mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD}–0.8	—	—	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull	I_{OL} = 14mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 7mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(2)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 11mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

4.7.4 Output pin transition times

Table 21. Output pin transition times

Symbol		C	Parameter	Conditions[(1)]		Value Min	Value Typ	Value Max	Unit
t_{tr}	CC	D	Output transition time output pin[(2)] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
t_{tr}	CC	D	Output transition time output pin[(2)] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
t_{tr}	CC	D	Output transition time output pin[(2)] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).

4.7.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 22*.

Table 22. I/O supply segment

Package	Supply segment 1	2	3	4	5	6
LBGA208[(1)]	Equivalent to LQFP144 segment pad distribution				MCKO	MDOn/MSEO
LQFP144	pin20–pin49	pin51–pin99	pin100–pin122	pin 123–pin19	—	—
LQFP100	pin16–pin35	pin37–pin69	pin70–pin83	pin 84–pin15	—	—
LQFP64[(2)]	pin8–pin26	pin28–pin55	pin56–pin7	—	—	—

1. LBGA208 available only as development package for Nexus2+.
2. All LQFP64 information is indicative and must be confirmed during silicon validation.

Table 23 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 23. I/O consumption

Symbol		C	Parameter	Conditions(1)		Min	Typ	Max	Unit
I_{SWTSLW}(2)	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}(2)	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}(2)	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	
I_{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to125 °C, unless otherwise specified.
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 24 provides the weight of concurrent switching I/Os.

Due to the dynamic current limitations, the sum of the weight of concurrent switching I/Os on a single segment must not exceed 100% to ensure device functionality.

Table 24. I/O weight(1)

Supply segment			Pad	LQFP144/LQFP100				LQFP64(2)			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
LQFP 144	LQFP 100	LQFP 64		SRC(3) = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
4	4	3	PB[3]	10%	—	12%	—	10%	—	12%	—
			PC[9]	10%	—	12%	—	10%	—	12%	—
		—	PC[14]	9%	—	11%	—	—	—	—	—
		—	PC[15]	9%	13%	11%	12%	—	—	—	—
	—	—	PG[5]	9%	—	11%	—	—	—	—	—
	—	—	PG[4]	9%	12%	10%	11%	—	—	—	—
	—	—	PG[3]	9%	—	10%	—	—	—	—	—
4	—	—	PG[2]	8%	12%	10%	10%	—	—	—	—
	4	3	PA[2]	8%	—	9%	—	8%	—	9%	—
		—	PE[0]	8%	—	9%	—	—	—	—	—
		3	PA[1]	7%	—	9%	—	7%	—	9%	—
		—	PE[1]	7%	10%	8%	9%	—	—	—	—
		—	PE[8]	7%	9%	8%	8%	—	—	—	—
		—	PE[9]	6%	—	7%	—	—	—	—	—
		—	PE[10]	6%	—	7%	—	—	—	—	—
		3	PA[0]	5%	8%	6%	7%	5%	8%	6%	7%
		—	PE[11]	5%	—	6%	—	—	—	—	—

Table 24. I/O weight(1) (continued)

Supply segment			Pad	LQFP144/LQFP100				LQFP64(2)			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
LQFP 144	LQFP 100	LQFP 64		SRC(3) = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
1	—	—	PG[9]	9%	—	10%	—	—	—	—	—
	—	—	PG[8]	9%	—	11%	—	—	—	—	—
	1	—	PC[11]	9%	—	11%	—	—	—	—	—
		1	PC[10]	9%	13%	11%	12%	9%	13%	11%	12%
	—	—	PG[7]	10%	14%	11%	12%	—	—	—	—
	—	—	PG[6]	10%	14%	12%	12%	—	—	—	—
	1	1	PB[0]	10%	14%	12%	12%	10%	14%	12%	12%
			PB[1]	10%	—	12%	—	10%	—	12%	—
	—	—	PF[9]	10%	—	12%	—	—	—	—	—
	—	—	PF[8]	10%	15%	12%	13%	—	—	—	—
	—	—	PF[12]	10%	15%	12%	13%	—	—	—	—
	1	1	PC[6]	10%	—	12%	—	10%	—	12%	—
			PC[7]	10%	—	12%	—	10%	—	12%	—
	—	—	PF[10]	10%	14%	12%	12%	—	—	—	—
	—	—	PF[11]	10%	—	11%	—	—	—	—	—
	1	1	PA[15]	9%	12%	10%	11%	9%	12%	10%	11%
	—	—	PF[13]	8%	—	10%	—	—	—	—	—
	1	1	PA[14]	8%	11%	9%	10%	8%	11%	9%	10%
			PA[4]	8%	—	9%	—	8%	—	9%	—
			PA[13]	7%	10%	9%	9%	7%	10%	9%	9%
			PA[12]	7%	—	8%	—	7%	—	8%	—

Table 24. I/O weight(1) (continued)

Supply segment			Pad	LQFP144/LQFP100				LQFP64(2)			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
LQFP 144	LQFP 100	LQFP 64		SRC(3) = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	2	2	PB[9]	1%	—	1%	—	1%	—	1%	—
			PB[8]	1%	—	1%	—	1%	—	1%	—
			PB[10]	6%	—	7%	—	6%	—	7%	—
	—	—	PF[0]	6%	—	7%	—	—	—	—	—
	—	—	PF[1]	7%	—	8%	—	—	—	—	—
	—	—	PF[2]	7%	—	8%	—	—	—	—	—
	—	—	PF[3]	7%	—	9%	—	—	—	—	—
	—	—	PF[4]	8%	—	9%	—	—	—	—	—
	—	—	PF[5]	8%	—	10%	—	—	—	—	—
	—	—	PF[6]	8%	—	10%	—	—	—	—	—
	—	—	PF[7]	9%	—	10%	—	—	—	—	—
	2	—	PD[0]	1%	—	1%	—	—	—	—	—
		—	PD[1]	1%	—	1%	—	—	—	—	—
		—	PD[2]	1%	—	1%	—	—	—	—	—
		—	PD[3]	1%	—	1%	—	—	—	—	—
		—	PD[4]	1%	—	1%	—	—	—	—	—
		—	PD[5]	1%	—	1%	—	—	—	—	—
		—	PD[6]	1%	—	1%	—	—	—	—	—
		—	PD[7]	1%	—	1%	—	—	—	—	—
		—	PD[8]	1%	—	1%	—	—	—	—	—
		2	PB[4]	1%	—	1%	—	1%	—	1%	—
			PB[5]	1%	—	1%	—	1%	—	2%	—
			PB[6]	1%	—	1%	—	1%	—	2%	—
			PB[7]	1%	—	1%	—	1%	—	2%	—
		—	PD[9]	1%	—	1%	—	—	—	—	—
		—	PD[10]	1%	—	1%	—	—	—	—	—
		—	PD[11]	1%	—	1%	—	—	—	—	—
		2	PB[11]	11%	—	13%	—	17%	—	21%	—
		—	PD[12]	11%	—	13%	—	—	—	—	—
		2	PB[12]	11%	—	13%	—	18%	—	21%	—
		—	PD[13]	10%	—	12%	—	—	—	—	—

Table 24. I/O weight(1) (continued)

Supply segment			Pad	LQFP144/LQFP100				LQFP64(2)			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
LQFP 144	LQFP 100	LQFP 64		SRC(3) = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	2	2	PB[13]	10%	—	12%	—	18%	—	21%	—
		—	PD[14]	10%	—	12%	—	—	—	—	—
		2	PB[14]	10%	—	12%	—	18%	—	21%	—
		—	PD[15]	10%	—	11%	—	—	—	—	—
		2	PB[15]	9%	—	11%	—	18%	—	21%	—
			PA[3]	9%	—	11%	—	18%	—	21%	—
	—	—	PG[13]	9%	13%	10%	11%	—	—	—	—
	—	—	PG[12]	9%	12%	10%	11%	—	—	—	—
	—	—	PH[0]	5%	8%	6%	7%	—	—	—	—
	—	—	PH[1]	5%	7%	6%	6%	—	—	—	—
	—	—	PH[2]	5%	6%	5%	6%	—	—	—	—
	—	—	PH[3]	4%	6%	5%	5%	—	—	—	—
	—	—	PG[1]	4%	—	4%	—	—	—	—	—
	—	—	PG[0]	3%	4%	4%	4%	—	—	—	—
3	—	—	PF[15]	3%	—	4%	—	—	—	—	—
	—	—	PF[14]	4%	5%	5%	5%	—	—	—	—
	—	—	PE[13]	4%	—	5%	—	—	—	—	—
	3	2	PA[7]	5%	—	6%	—	16%	—	19%	—
			PA[8]	5%	—	6%	—	16%	—	19%	—
			PA[9]	5%	—	6%	—	15%	—	18%	—
			PA[10]	6%	—	7%	—	15%	—	18%	—
			PA[11]	6%	—	8%	—	14%	—	17%	—
		—	PE[12]	7%	—	8%	—	—	—	—	—
	—	—	PG[14]	7%	—	8%	—	—	—	—	—
	—	—	PG[15]	7%	10%	8%	9%	—	—	—	—
	—	—	PE[14]	7%	—	8%	—	—	—	—	—
	—	—	PE[15]	7%	9%	8%	8%	—	—	—	—
	—	—	PG[10]	6%	—	8%	—	—	—	—	—
	—	—	PG[11]	6%	9%	7%	8%	—	—	—	—
	3	2	PC[3]	6%	—	7%	—	7%	—	9%	—
			PC[2]	6%	8%	7%	7%	6%	9%	8%	8%

Table 24. I/O weight[1] (continued)

Supply segment			Pad	LQFP144/LQFP100				LQFP64[2]			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
LQFP 144	LQFP 100	LQFP 64		SRC[3] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
3	3	2	PA[5]	5%	7%	6%	6%	6%	8%	7%	7%
			PA[6]	5%	—	6%	—	5%	—	6%	—
			PH[10]	4%	6%	5%	5%	5%	7%	6%	6%
			PC[1]	5%	—	5%	—	5%	—	5%	—
4	4	3	PC[0]	6%	9%	7%	8%	6%	9%	7%	8%
			PH[9]	7	7	8	8	7	7	8	8
		—	PE[2]	7%	10%	9%	9%	—	—	—	—
		—	PE[3]	8%	11%	9%	9%	—	—	—	—
		3	PC[5]	8%	11%	9%	10%	8%	11%	9%	10%
			PC[4]	8%	12%	10%	10%	8%	12%	10%	10%
		—	PE[4]	8%	12%	10%	11%	—	—	—	—
		—	PE[5]	9%	12%	10%	11%	—	—	—	—
	—	—	PH[4]	9%	13%	11%	11%	—	—	—	—
	—	—	PH[5]	9%	—	11%	—	—	—	—	—
	—	—	PH[6]	9%	13%	11%	12%	—	—	—	—
	—	—	PH[7]	9%	13%	11%	12%	—	—	—	—
	—	—	PH[8]	10%	14%	11%	12%	—	—	—	—
	4	—	PE[6]	10%	14%	12%	12%	—	—	—	—
		—	PE[7]	10%	14%	12%	12%	—	—	—	—
		—	PC[12]	10%	14%	12%	13%	—	—	—	—
		—	PC[13]	10%	—	12%	—	—	—	—	—
		3	PC[8]	10%	—	12%	—	10%	—	12%	—
			PB[2]	10%	15%	12%	13%	10%	15%	12%	13%

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to125 °C, unless otherwise specified.
2. All LQFP64 information is indicative and must be confirmed during silicon validation.
3. SRC: “Slew Rate Control” bit in SIU_PCR.

4.8 RESET electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 7. Start-up reset requirements

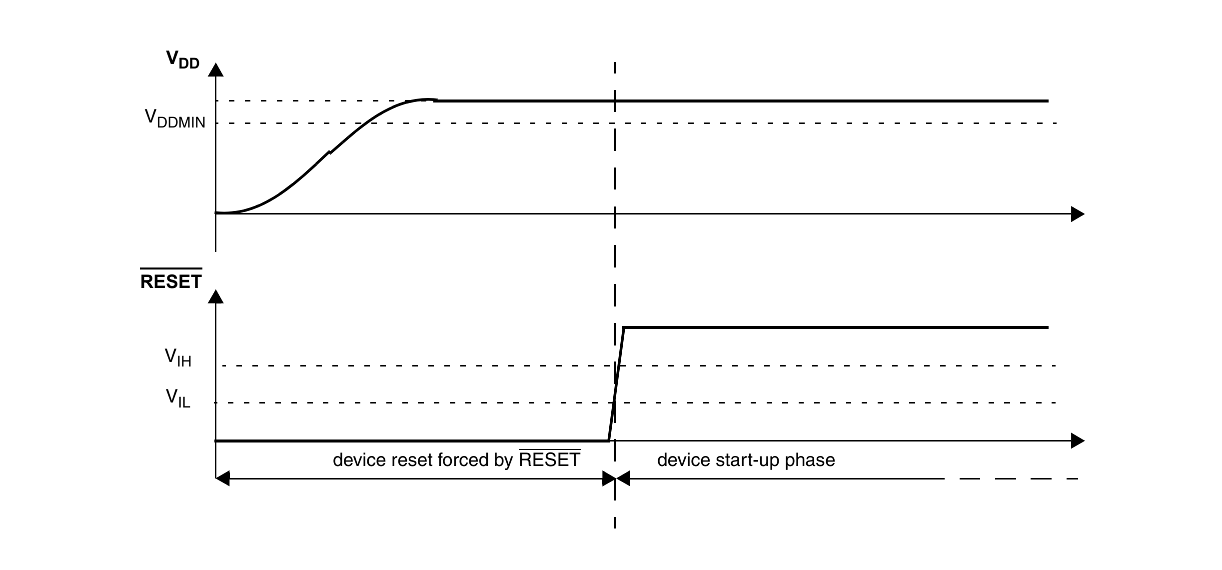


Figure 8. Noise filtering on reset signal

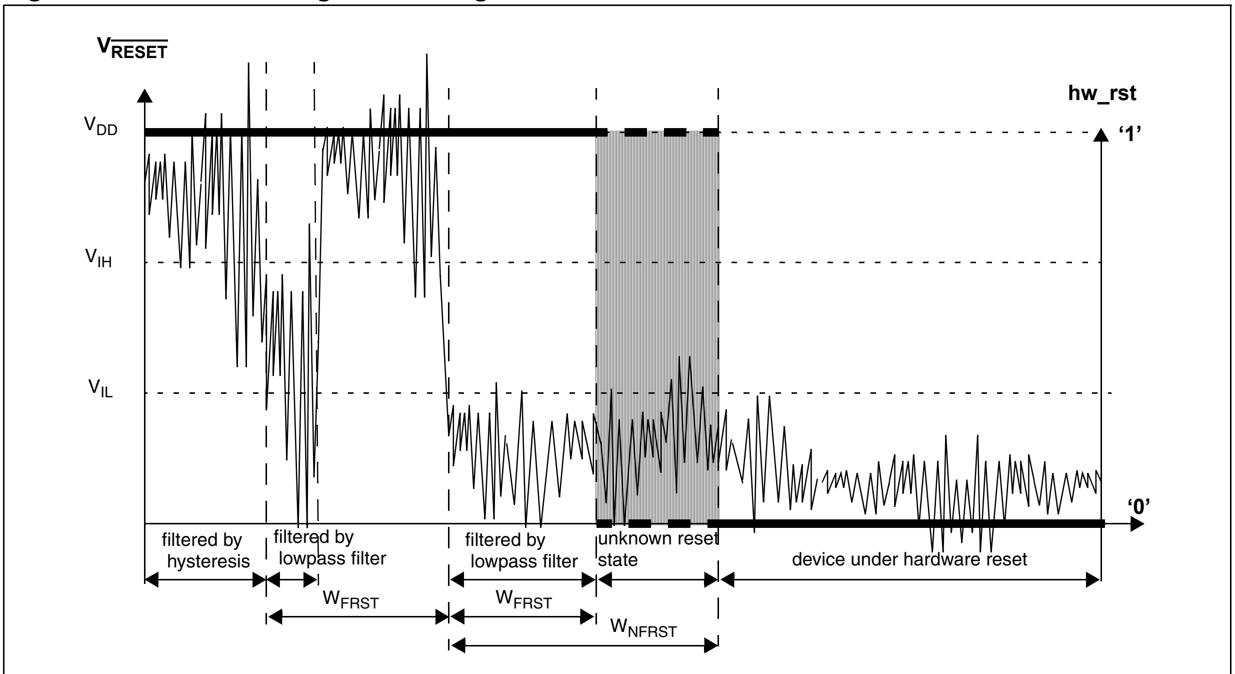


Table 25. Reset electrical characteristics

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V

Table 25. Reset electrical characteristics (continued)

Symbol		C	Parameter	Conditions(1)	Value Min	Value Typ	Value Max	Unit
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C		Push Pull, I_{OL} = 1mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(2)	—	—	$0.1V_{DD}$	
		C		Push Pull, I_{OL} = 1mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
t_{tr}	CC	D	Output transition time output pin(3)	C_L = 25pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	1000	—	—	ns
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
		D		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
		P		V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(2)	10	—	250	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This transient configuration does not occurs when device is used in the V_{DD} = 3.3 V ± 10% range.
3. C_L includes device and package capacitance (C_{PKG} < 5 pF).

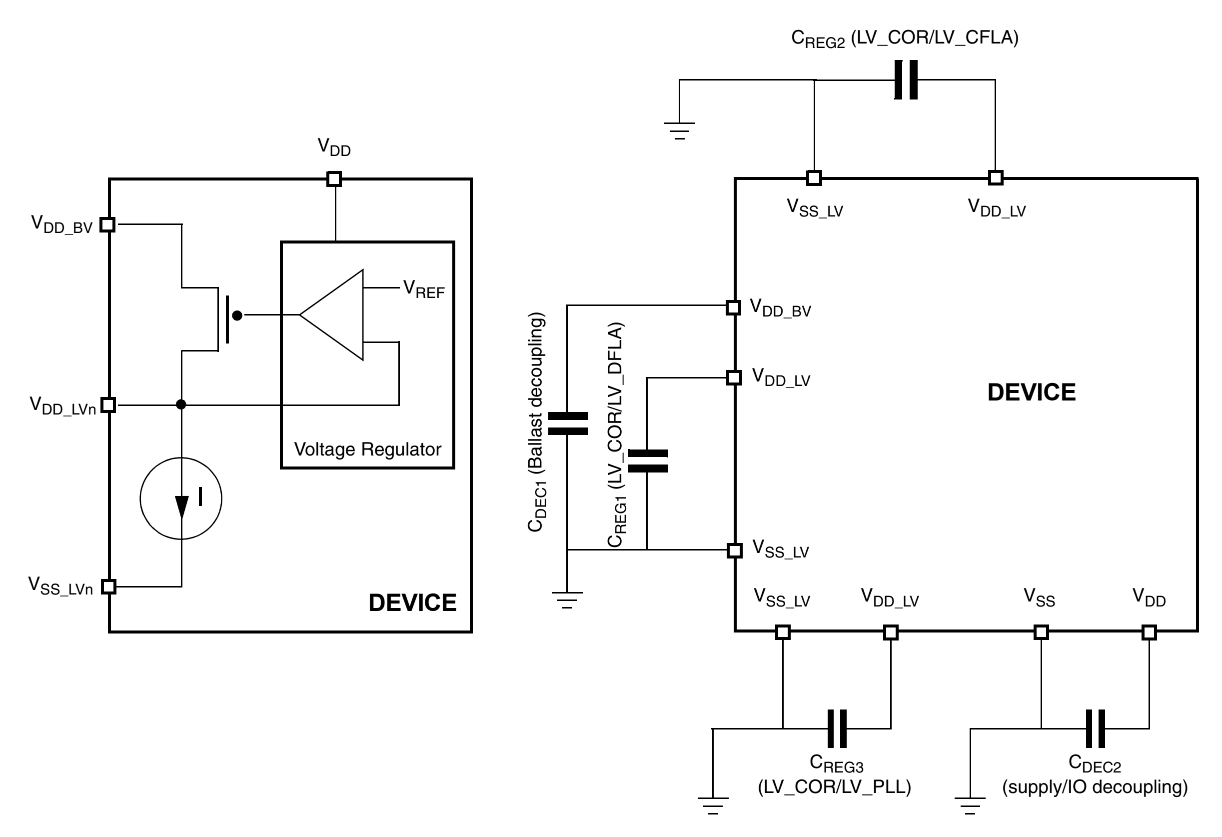
4.9 Power management electrical characteristics

4.9.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply V_{DD_BV}. The regulator itself is supplied by the common I/O supply V_{DD}. The following supplies are involved:

- HV—High voltage external power supply for voltage regulator module. This must be provided externally through V_{DD} power pin.
- BV—High voltage external power supply for internal ballast module. This must be provided externally through V_{DD_BV} power pin. Voltage values should be aligned with V_{DD}.
- LV—Low voltage internal power supply for core, FMPLL and flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR—Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
  - LV_CFLA—Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_DFLA—Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL—Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

Figure 9. Voltage regulator capacitance connection

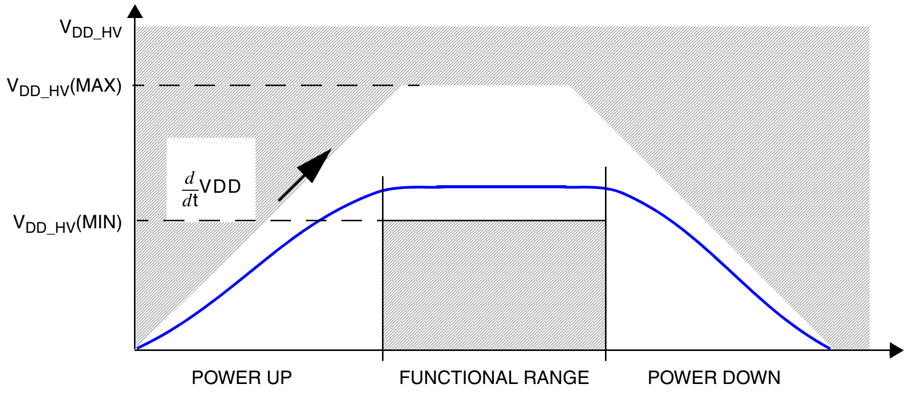


The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see *Section 4.5: Recommended operating conditions*).

The internal voltage regulator requires controlled slew rate of V_{DD}/V_{DD_BV} as described on *Figure 10*.

Figure 10. V_{DD} and V_{DD_BV} maximum slope



When STANDBY mode is used, further constraints apply to the V_{DD}/V_{DD_BV} in order to guarantee correct regulator functionality during STANDBY exit. This is described on *Figure 11*.

STANDBY regulator constraints should normally be guaranteed by implementing equivalent of CSTDBY capacitance on application board (capacitance and ESR typical values), but would actually depend on exact characteristics of application external regulator.

Figure 11. VDD and VDD_BV supply constraints during STANDBY mode exit

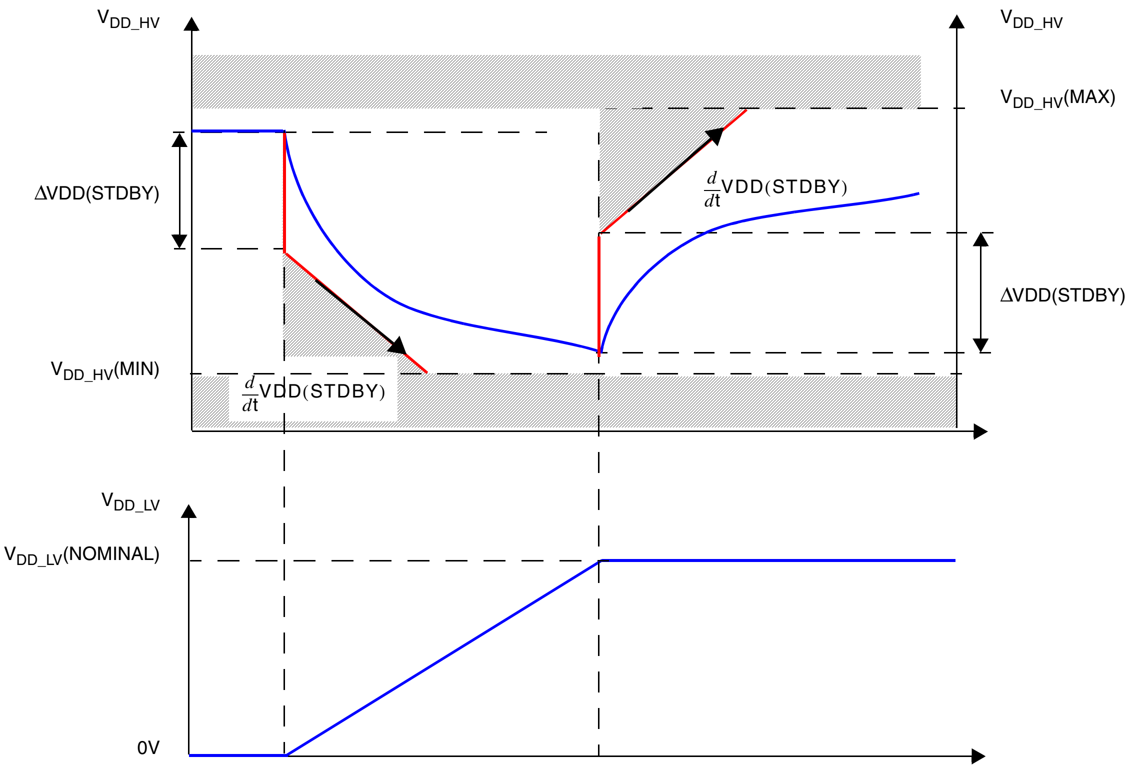


Table 26. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	W
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
$\left\lvert\frac{d}{dt}VDD\right\rvert$	SR	—	Maximum slope on V_{DD}		—	—	250	mV/µs
$\lvert\Delta_{VDD(STDBY)}\rvert$	SR	—	Maximum instant variation on V_{DD} during standby exit		—	—	30	mV
$\frac{d}{dt}VDD(STDBY)$	SR	—	Maximum slope on V_{DD} during standby exit		—	—	15	mV/µs
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.16	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V

Table 26. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	—	
I_{DD_BV}	CC	D	In-rush average current on V_{DD_BV} during power-up(5)	—	—	—	300 (6)	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.
3. This value is acceptable to guarantee operation from 4.5 V to 5.5 V.
4. External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.
5. In-rush average current is seen only for short time (maximum 20 µs) during power-up and on standby exit. It is dependant on the sum of the C_{REGn} capacitances.
6. The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

The $|\Delta_{VDD(STDBY)}|$ and dVDD(STDBY)/dt system requirement can be used to define the component used for the V_{DD} supply generation. The following two examples describe how to calculate capacitance size:

Example 1 No regulator (worst case)

The $|\Delta_{VDD(STDBY)}|$ parameter can be seen as the V_{DD} voltage drop through the ESR resistance of the regulator stability capacitor when the I_{DD_BV} current required to load V_{DD_LV} domain during the standby exit. It is thus possible to define the maximum equivalent resistance ESR_{STDBY}(MAX) of the total capacitance on the V_{DD} supply:

$ESR_{STDBY}(MAX) = |\Delta_{VDD(STDBY)}|/I_{DD\_BV} = (30\ mV)/(300\ mA) = 0.1\Omega$ [d]

The dVDD(STDBY)/dt parameter can be seen as the V_{DD} voltage drop at the capacitance pin (excluding ESR drop) while providing the I_{DD_BV} supply required to load V_{DD_LV} domain during the standby exit. It is thus possible to define the minimum equivalent capacitance C_{STDBY}(MIN) of the total capacitance on the V_{DD} supply:

$C_{STDBY}(MIN) = I_{DD\_BV}/dVDD(STDBY)/dt = (300\ mA)/(15\ mV/\mu s) = 20\ \mu F$

This configuration is a worst case, with the assumption no regulator is available.

Example 2 Simplified regulator

The regulator should be able to provide significant amount of the current during the standby exit process. For example, in case of an ideal voltage regulator providing 200 mA current, it is possible to recalculate the equivalent ESR_{STDBY}(MAX) and C_{STDBY}(MIN) as follows:

d. Based on typical time for standby exit sequence of 20 µs, ESR(MIN) can actually be considered at ~50 kHz.

$ESR_{STDBY}(MAX) = |\Delta_{VDD(STDBY)}|/(I_{DD\_BV} - 200\text{ mA}) = (30\text{ mV})/(100\text{ mA}) = 0.3\ \Omega$

$C_{STDBY}(MIN) = (I_{DD\_BV} - 200\text{ mA})/dVDD(STDBY)/dt = (300\text{ mA} - 200\text{ mA})/(15\text{ mV/µs}) = 6.7\text{ µF}$

In case optimization is required, C_{STDBY}(MIN) and ESR_{STDBY}(MAX) should be calculated based on the regulator characteristics as well as the board V_{DD} plane characteristics.

4.9.2 Low voltage detector electrical characteristics

The device implements a Power-on Reset (POR) module to ensure correct power-up initialization, as well as four low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state (refer to RGM Destructive Event Status (RGM_DES) Register flag F_POR in device reference manual)
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27 in device reference manual)
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range (refer to RGM Functional Event Status (RGM_FES) Register flag F_LVD45 in device reference manual)
- LVDLVCOR monitors power domain No. 1 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD1 in device reference manual
- LVDLVBKP monitors power domain No. 0 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD0 in device reference manual)

Note: When enabled, power domain No. 2 is monitored through LVDLVBKP.

Figure 12. Low voltage detector vs reset

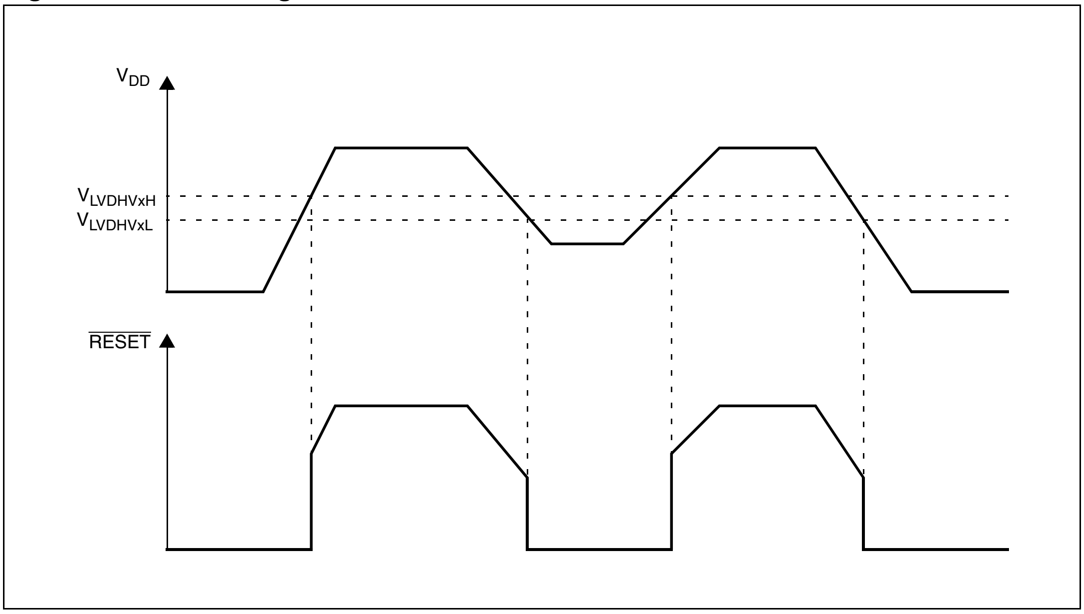


Table 27. Low voltage detector electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{PORUP}	SR	P	Supply for functional POR module	—	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold	T_A = 25 °C, after trimming	1.5	—	2.6	V
		T		—	1.5	—	2.6	V
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold	—	—	—	2.95	V
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold	—	2.6	—	2.9	V
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold	—	—	—	4.5	V
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold	—	3.8	—	4.4	V
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold	—	1.08	—	1.16	V
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold	—	1.08	—	1.16	V

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

4.10 Power consumption

Table 28 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 28. Power consumption on VDD_BV and VDD_HV

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{DDMAX}[2]	CC	D	RUN mode maximum average current	—		—	115	140[3]	mA
I_{DDRUN}[4]	CC	T	RUN mode typical average current[5]	f_{CPU} = 8 MHz		—	7	—	mA
		T		f_{CPU} = 16 MHz		—	18	—	mA
		T		f_{CPU} = 32 MHz		—	29	—	mA
		P		f_{CPU} = 48 MHz		—	40	100	mA
		P		f_{CPU} = 64 MHz		—	51	125	mA
I_{DDHALT}	CC	C	HALT mode current[6]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	8	15	mA
		P			T_A = 125 °C	—	14	25	mA
I_{DDSTOP}	CC	P	STOP mode current[7]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	180	700[8]	µA
		D			T_A = 55 °C	—	500	—	µA
		D			T_A = 85 °C	—	1	6[8]	mA
		D			T_A = 105 °C	—	2	9[8]	mA
		P			T_A = 125 °C	—	4.5	12[8]	mA

Table 28. Power consumption on VDD_BV and VDD_HV (continued)

Symbol		C	Parameter	Conditions(1)		Value Min	Typ	Max	Unit
$I_{DDSTDBY2}$	CC	P	STANDBY2 mode current(9)	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	30	100	µA
		D			T_A = 55 °C	—	75	—	
		D			T_A = 85 °C	—	180	700	
		D			T_A = 105 °C	—	315	1000	
		P			T_A = 125 °C	—	560	1700	
$I_{DDSTDBY1}$	CC	T	STANDBY1 mode current(10)	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	20	60	µA
		D			T_A = 55 °C	—	45	—	
		D			T_A = 85 °C	—	100	350	
		D			T_A = 105 °C	—	165	500	
		D			T_A = 125 °C	—	280	900	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. --------Running consumption does not include I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation ongoing on data flash. Notice that this value can be significantly reduced by application: switch off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.
3. Higher current may be sinked by device during power-up and standby exit. Please refer to in rush current on *Table 26*.
4. RUN current measured with typical application with accesses on both flash and RAM.
5. Only for the “P” classification: Data and Code Flash in Normal Power. Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled.
6. Data Flash Power Down. Code Flash in Low Power. SIRC (128 kHz) and FIRC (16 MHz) on. 10 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clock gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 clock gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication). RTC/API ON. PIT ON. STM ON. ADC ON but not conversion except 2 analog watchdog.
7. Only for the “P” classification: No clock, FIRC (16 MHz) off, SIRC (128 kHz) on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.
8. When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.
9. Only for the “P” classification: ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.
10. ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

4.11 Flash memory electrical characteristics

4.11.1 Program/Erase characteristics

Table 29 shows the program and erase characteristics.

Table 29. Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ(1)	Initial max(2)	Max(3)	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time(4)	—	22	50	500	µs
$T_{16Kpperase}$	CC	C	16 KB block preprogram and erase time	—	300	500	5000	ms
$T_{32Kpperase}$	CC	C	32 KB block preprogram and erase time	—	400	600	5000	ms
$T_{128Kpperase}$	CC	C	128 KB block preprogram and erase time	—	800	1300	7500	ms
T_{esus}	CC	D	Erase suspend latency	—	—	30	30	µs

1. Typical program and erase times assume nominal supply values and operation at 25 °C.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.

Table 30. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block over the operating temperature range (T_J)	16 KB blocks	100000	—	—	cycles
				32 KB blocks	10000	100000	—	
				128 KB blocks	1000	100000	—	
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0–1000 P/E cycles	20	—	—	years
				Blocks with 1001–10000 P/E cycles	10	—	—	
				Blocks with 10001–100000 P/E cycles	5	—	—	

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 31. Flash read access timing

Symbol		C	Parameter	Conditions(1)	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

4.11.2 Flash power supply DC characteristics

Table 32 shows the power supply DC characteristics on external supply.

Table 32. Flash memory power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
I_{FREAD}[2]	CC	D	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} on read access	Code flash memory module read f_{CPU} = 64 MHz[3]	—	15	33	mA
				Data flash memory module read f_{CPU} = 64 MHz[3]	—	15	33	
I_{FMOD}[2]	CC	D	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} on matrix modification (program/erase)	Program/Erase ongoing while reading code flash memory registers f_{CPU} = 64 MHz[3]	—	15	33	mA
				Program/Erase ongoing while reading data flash memory registers f_{CPU} = 64 MHz[3]	—	15	33	
I_{FLPW}	CC	D	Sum of the current consumption on V_{DD_HV} and V_{DD_BV}	During code flash memory low-power mode	—	—	900	µA
				During data flash memory low-power mode	—	—	900	
I_{FPWD}	CC	D	Sum of the current consumption on V_{DD_HV} and V_{DD_BV}	During code flash memory power-down mode	—	—	150	µA
				During data flash memory power-down mode	—	—	150	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This value is only relative to the actual duration of the read cycle.
3. f_{CPU} 64 MHz can be achieved only at up to 105 °C.

4.11.3 Start-up/Switch-off timings

Table 33. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
$T_{FLARSTEXIT}$	CC	T	Delay for Flash module to exit reset mode	Code Flash	—	—	125	µs
		T		Data Flash	—	—	125	
$T_{FLALPEXIT}$	CC	T	Delay for Flash module to exit low-power mode	Code Flash	—	—	0.5	
		T		Data Flash	—	—	0.5	
$T_{FLAPDEXIT}$	CC	T	Delay for Flash module to exit power-down mode	Code Flash	—	—	30	
		T		Data Flash	—	—	30	
$T_{FLALPENTRY}$	CC	T	Delay for Flash module to enter low-power mode	Code Flash	—	—	0.5	
		T		Data Flash	—	—	0.5	
$T_{FLAPDENTRY}$	CC	T	Delay for Flash module to enter power-down mode	Code Flash	—	—	1.5	
		T		Data Flash	—	—	1.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

4.12 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

4.12.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations: The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers...)
- Prequalification trials: Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note *Software Techniques For Improving Microcontroller EMC Performance* (AN1015)).

4.12.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC 61967-1 standard, which specifies the general conditions for EMI measurements.

Table 34. EMI radiated emission measurement(1)(2)

Symbol		C	Parameter	Conditions		Value Min	Value Typ	Value Max	Unit
—	SR	—	Scan range	—		0.150	—	1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	64	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP144 package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 64 MHz	No PLL frequency modulation	—	—	18	dBµV
					±2% PLL frequency modulation	—	—	14	dBµV

1. EMI testing and I/O port waveforms per IEC 61967-1, -2, -4.
2. For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

4.12.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard. For more details, refer to the application note *Electrostatic Discharge Sensitivity Measurement* (AN1181).

Table 35. ESD absolute maximum ratings(1) (2)

Symbol		C	Ratings	Conditions	Class	Max value	Unit
$V_{ESD(HBM)}$	CC	T	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	CC	T	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	CC	T	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
						750 (corners)	

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 36. Latch-up results

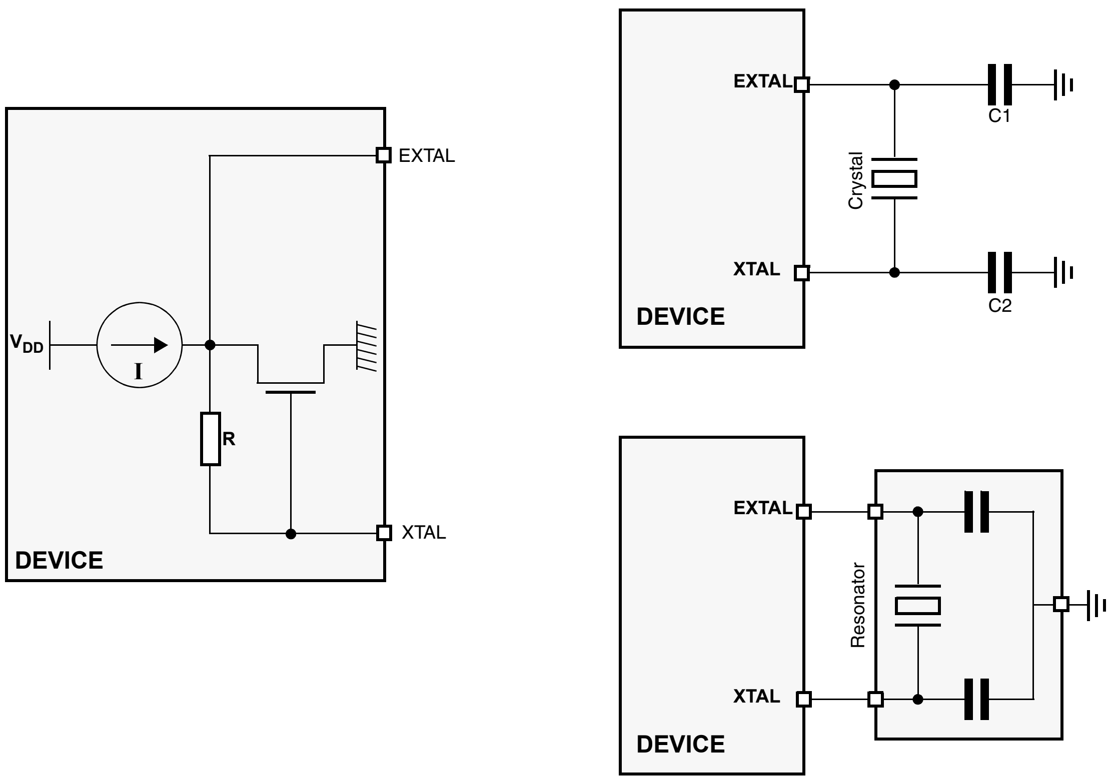
Symbol		C	Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

4.13 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. *Figure 13* describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 37 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

Figure 13. Crystal oscillator and resonator connection scheme



Notes:
1. XTAL/EXTAL must not be directly used to drive external circuits
2. A series resistor may be required, according to crystal oscillator supplier recommendations.

Table 37. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout C1 = C2 (pF)(1)	Shunt capacitance between xtalout and xtalin C0(2) (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

1. The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.
2. The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

Figure 14. Fast external crystal oscillator (4 to 16 MHz) timing diagram

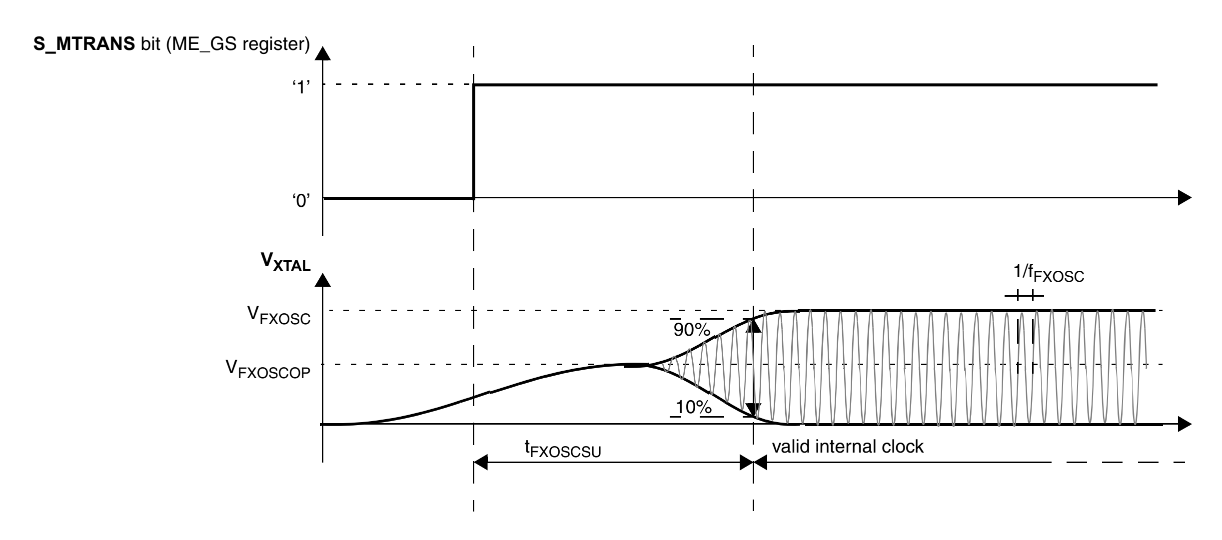


Table 38. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value Min	Value Typ	Value Max	Unit
f_{FXOSC}	SR	—	Fast external crystal oscillator frequency	—	4.0	—	16.0	MHz
g_{mFXOSC}	CC	C	Fast external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	—	8.2	mA/V
	CC	P		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	—	7.4	
	CC	C		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	—	9.7	
	CC	C		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	—	9.2	
V_{FXOSC}	CC	T	Oscillation amplitude at EXTAL	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	1.3	—	—	V
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	1.3	—	—	
$V_{FXOSCOP}$	CC	C	Oscillation operating point	—	—	0.95	—	V
I_{FXOSC}[2]	CC	T	Fast external crystal oscillator consumption	—	—	2	3	mA
$t_{FXOSCSU}$	CC	T	Fast external crystal oscillator start-up time	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	

Table 38. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics (continued)

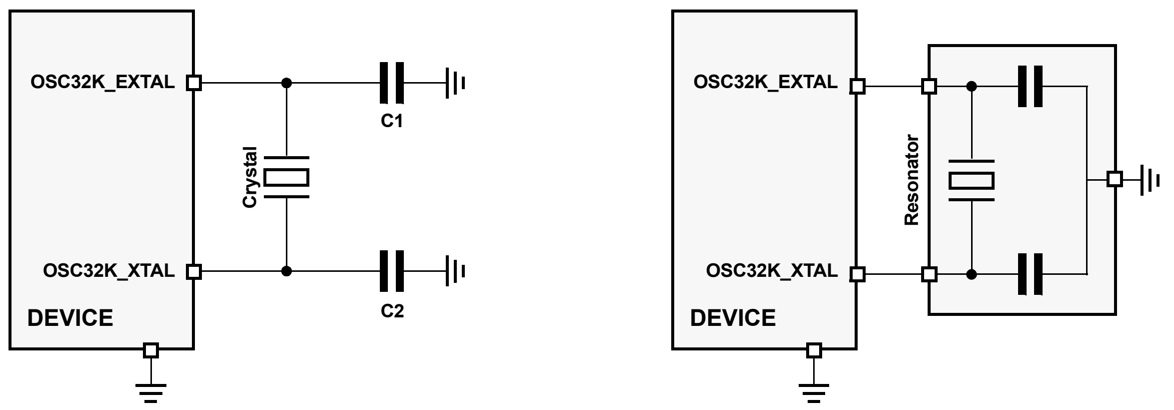
Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	$0.65V_{DD}$	—	V_{DD}+0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	–0.4	—	$0.35V_{DD}$	V

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

4.14 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

Figure 15. Crystal oscillator and resonator connection scheme



Note: OSC32K_XTAL/OSC32K_EXTAL must not be directly used to drive external circuits.

Figure 16. Equivalent circuit of a quartz crystal

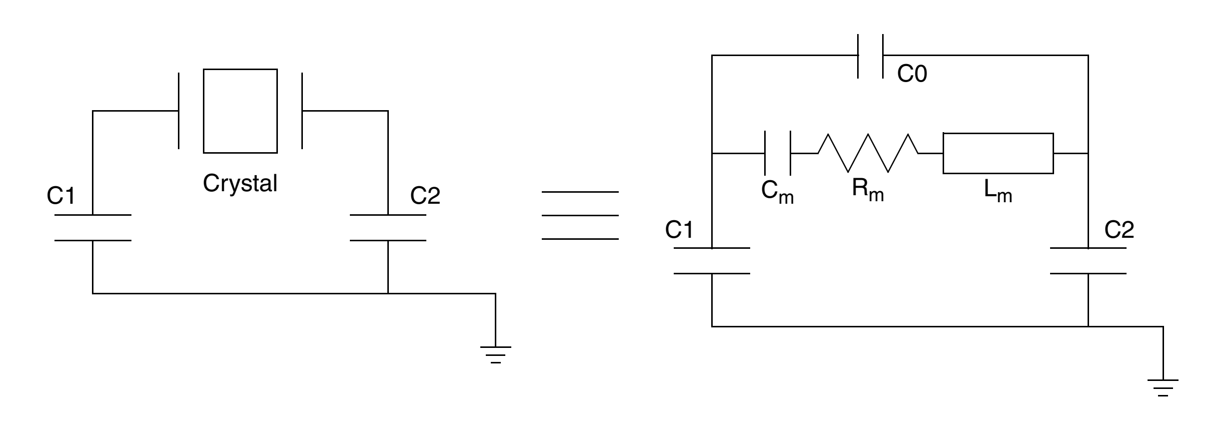


Table 39. Crystal motional characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground[2]	—	18	—	28	pF
R_m[3]	Motional resistance	AC coupled @ C0 = 2.85 pF[4]	—	—	65	kW
		AC coupled @ C0 = 4.9 pF[4]	—	—	50	
		AC coupled @ C0 = 7.0 pF[4]	—	—	35	
		AC coupled @ C0 = 9.0 pF[4]	—	—	30	

1. Crystal used: Epson Toyocom MC306.
2. This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.
3. Maximum ESR (R_m) of the crystal is 50 kΩ.
4. C0 includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins.

Figure 17. Slow external crystal oscillator (32 kHz) timing diagram

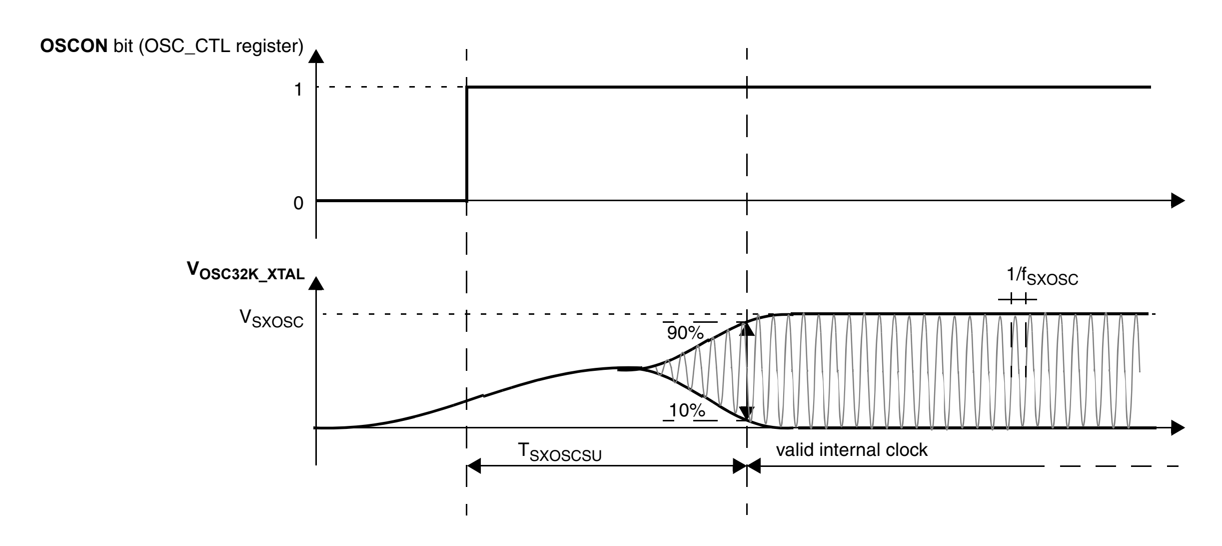


Table 40. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	—	—	2.1	—	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—	—	2.5	—	µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	8	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[2]	s

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified. Values are specified for no neighbor GPIO pin activity. If oscillator is enabled (OSC32K_XTAL and OSC32K_EXTAL pins), neighboring pins should not toggle.
2. Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

4.15 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 41. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[2]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[2]	—	40	—	60	%
f_{PLLOUT}	CC	D	FMPLL output clock frequency	—	16	—	64	MHz

Table 41. FMPLL electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value Min	Value Typ	Value Max	Unit
f_{VCO}[3]	CC	P	VCO frequency without frequency modulation	—	256	—	512	MHz
		C	VCO frequency with frequency modulation	—	245	—	533	
f_{CPU}	SR	—	System clock frequency	—	—	—	64	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	40	100	µs
Δt_{STJIT}	CC	—	FMPLL short term jitter[4]	f_{sys} maximum	–4	—	4	%
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} @ 64 MHz, 4000 cycles	—	—	10	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	4	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
3. Frequency modulation is considered ±4%.
4. Short term jitter is measured on the clock rising edge at cycle n and n+4.

4.16 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz fast internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 42. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value Min	Value Typ	Value Max	Unit
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed		—	16	—	MHz
	SR	—		—		12		20	
$I_{FIRCRUN}$[2]	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed		—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 125 °C		—	—	10	µA
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	

Table 42. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions(1)	Value Min	Typ	Max	Unit
t_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	V_{DD} = 5.0 V ± 10%	—	1.1	2.0	µs
$\Delta_{FIRCPRE}$	CC	T	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C	–1	—	+1	%
$\Delta_{FIRCTRIM}$	CC	T	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6		%
$\Delta_{FIRCVAR}$	CC	P	Fast internal RC oscillator variation in overtemperature and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration	—	–5	—	+5	%

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.17 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 43. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions(1)	Value Min	Typ	Max	Unit
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		—	100	—	150	
I_{SIRC}(2)	CC	C	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA
t_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	+2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at T_A = 55 °C in high frequency configuration	High frequency configuration	–10	—	+10	%

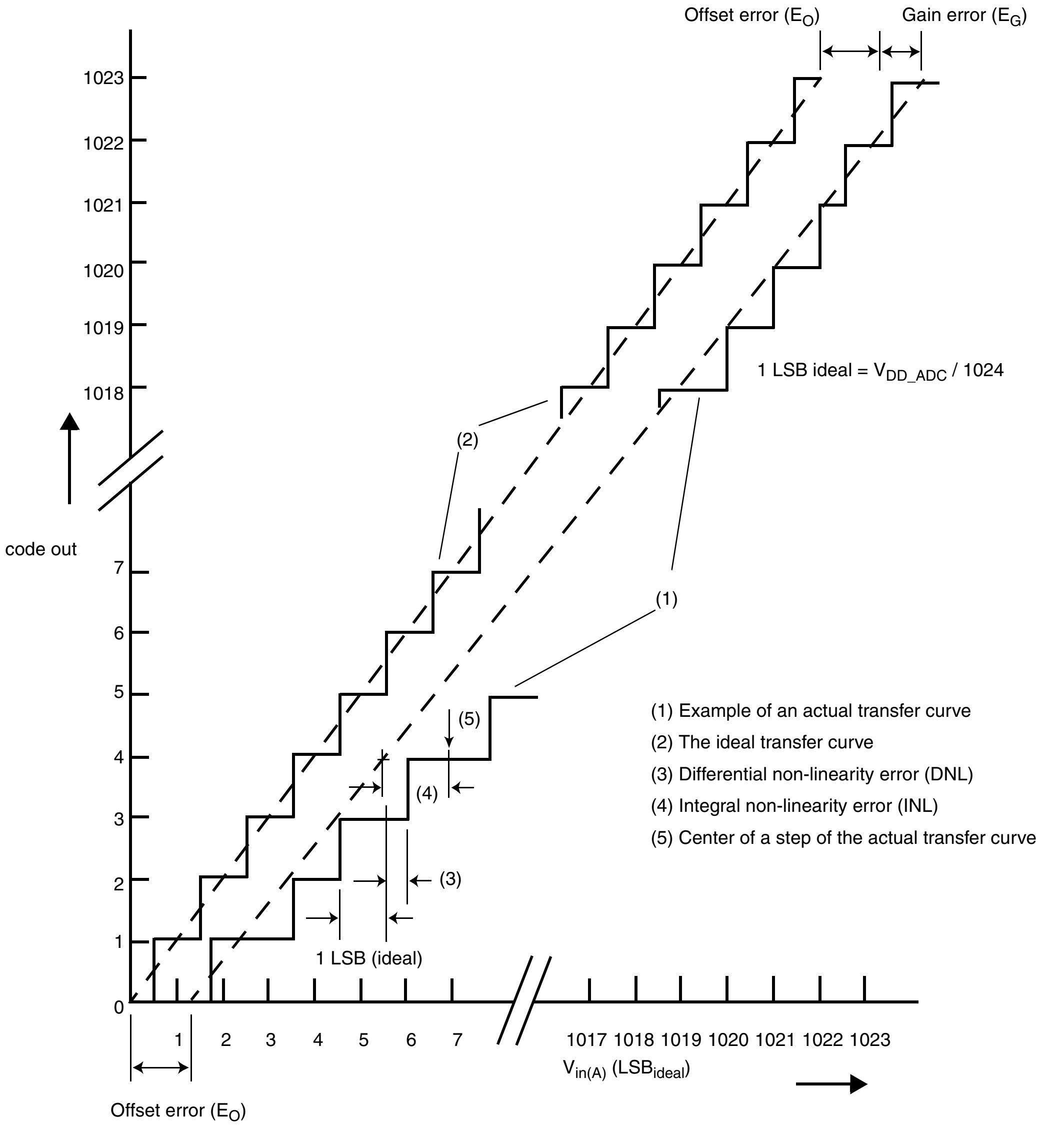
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.18 ADC electrical characteristics

4.18.1 Introduction

The device provides a 10-bit Successive Approximation Register (SAR) analog-to-digital converter.

Figure 18. ADC characteristic and error definitions



4.18.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

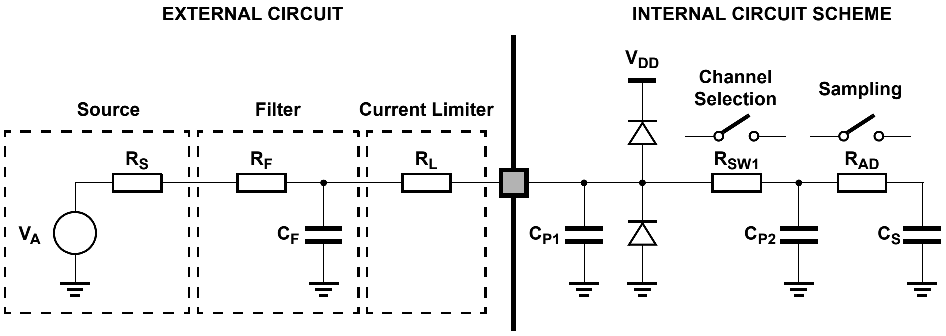
In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_c{*}C_S)$, where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the *Equation 4*:

Equation 4

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

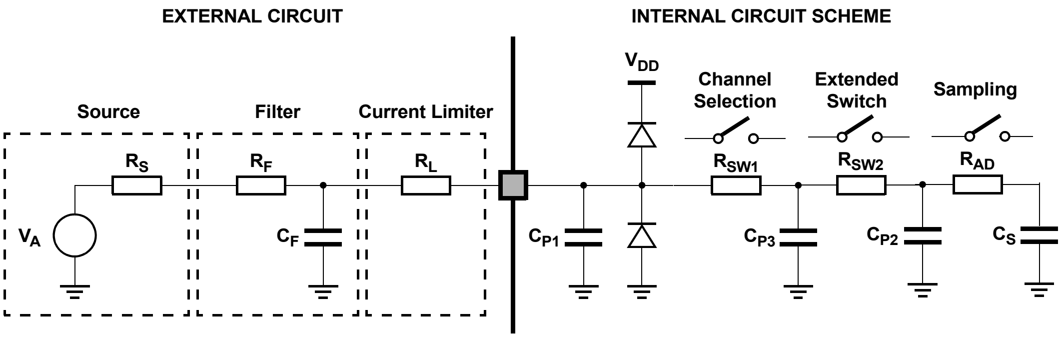
Equation 4 generates a constraint for external network design, in particular on a resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

Figure 19. Input equivalent circuit (precise channels)



R_S: Source impedance
R_F: Filter resistance
C_F: Filter capacitance
R_L: Current limiter resistance
R_{SW1}: Channel selection switch impedance
R_{AD}: Sampling switch impedance
C_P: Pin capacitance (two contributions, C_{P1} and C_{P2})
C_S: Sampling capacitance

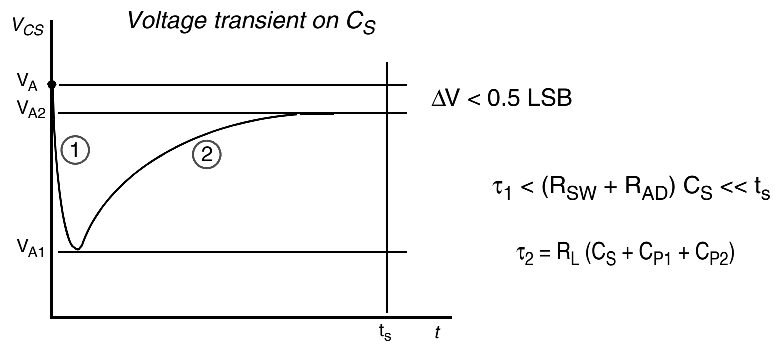
Figure 20. Input equivalent circuit (extended channels)



R_S: Source impedance
R_F: Filter resistance
C_F: Filter capacitance
R_L: Current limiter resistance
R_{SW1}: Channel selection switch impedance (two contributions, R_{SW1} and R_{SW2})
R_{AD}: Sampling switch impedance
C_P: Pin capacitance (two contributions, C_{P1}, C_{P2} and C_{P3})
C_S: Sampling capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit in *Figure 19*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Figure 21. Transient behavior during sampling phase



In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time t_s is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll t_s$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time t_s, a constraints on R_L sizing is obtained:

Equation 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < t_s$$

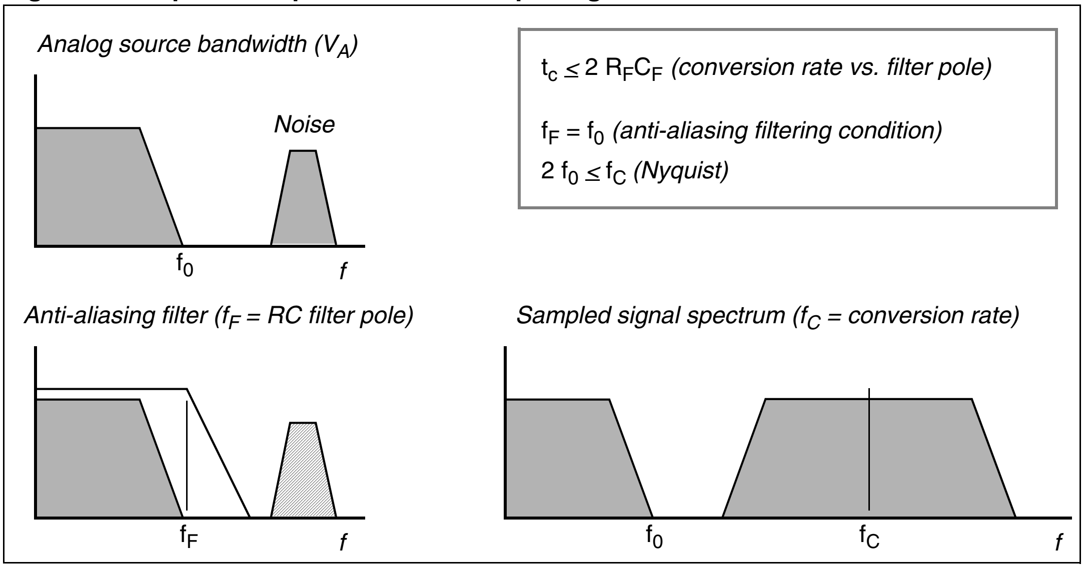
Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (t_s). The filter is typically designed to act as anti-aliasing.

Figure 22. Spectral representation of input signal



Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (t_c). Again the conversion period t_c is longer than the sampling time t_s, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time t_s, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive *Equation 11* between the ideal and real sampled voltage on C_S:

Equation 11

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Equation 12

$$C_F > 2048 \bullet C_S$$

4.18.3 ADC electrical characteristics

Table 44. ADC input leakage current

Symbol		C	Parameter	Conditions		Value Min	Value Typ	Value Max	Unit
I_{LKG}	CC	D	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	70	nA
		D		T_A = 25 °C		—	1	70	
		D		T_A = 85 °C		—	3	100	
		D		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 45. ADC conversion characteristics

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
V_{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})(2)	—	–0.1	—	0.1	V
V_{DD_ADC}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD}–0.1	—	V_{DD}+0.1	V
V_{AINx}	SR	—	Analog input voltage(3)	—	V_{SS_ADC}–0.1	—	V_{DD_ADC}+0.1	V
f_{ADC}	SR	—	ADC analog frequency	—	6	—	32 + 4%	MHz
Δ_{ADC_SYS}	SR	—	ADC digital clock duty cycle (ipg_clk)	ADCLKSEL = 1(4)	45	—	55	%
I_{ADCPWD}	SR	—	ADC0 consumption in power down mode	—	—	—	50	µA
I_{ADCRUN}	SR	—	ADC0 consumption in running mode	—	—	—	4	mA
t_{ADC_PU}	SR	—	ADC power up delay	—	—	—	1.5	µs
t_s	CC	T	Sampling time(5)	f_{ADC} = 32 MHz, INPSAMP = 17	0.5	—		µs
				f_{ADC} = 6 MHz, INPSAMP = 255	—	—	42	
t_c	CC	P	Conversion time(6)	f_{ADC} = 32 MHz, INPCMP = 2	0.625	—		µs
C_S	CC	D	ADC input sampling capacitance	—	—	—	3	pF
C_{P1}	CC	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC input pin capacitance 3	—	—	—	1	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	3	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ

Table 45. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions(1)		Value Min	Value Typ	Value Max	Unit
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
| INL |	CC	T	Absolute value for integral non-linearity	No overload		—	0.5	1.5	LSB
| DNL |	CC	T	Absolute differential non-linearity	No overload		—	0.5	1.0	LSB
| E_O |	CC	T	Absolute offset error	—		—	0.5	—	LSB
| E_G |	CC	T	Absolute gain error	—		—	0.6	—	LSB
TUEp	CC	P	Total unadjusted error(7) for precise channels, input only pins	Without current injection		–2	0.6	2	LSB
		T		With current injection		–3		3	
TUEx	CC	T	Total unadjusted error7 for extended channel	Without current injection		–3	1	3	LSB
		T		With current injection		–4		4	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. Analog and digital V_{SS} **must** be common (to be tied together externally).
3. V_{AINx} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.
4. Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.
5. During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_s. After the end of the sampling time t_s, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_s depend on programming.
6. This parameter does not include the sampling time t_s, but only the time for determining the digital result and the time to load the result's register with the conversion result.
7. Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

4.19 On-chip peripherals

4.19.1 Current consumption

Table 46. On-chip peripherals current consumption(1)

Symbol		C	Parameter	Conditions		Typical value(2)	Unit
$I_{DD\_BV(CAN)}$	CC	T	CAN (FlexCAN) supply current on V_{DD_BV}	Bitrate: 500 Kbyte/s	Total (static + dynamic) consumption: – FlexCAN in loop-back mode – XTAL @ 8 MHz used as CAN engine clock source – Message sending period is 580 µs	8 * f_{periph} + 85	µA
				Bitrate: 125 Kbyte/s		8 * f_{periph} + 27	
$I_{DD\_BV(eMIOS)}$	CC	T	eMIOS supply current on V_{DD_BV}	Static consumption: – eMIOS channel OFF – Global prescaler enabled		29 * f_{periph}	µA
				Dynamic consumption: – It does not change varying the frequency (0.003 mA)		3	
$I_{DD\_BV(SCI)}$	CC	T	SCI (LINFlex) supply current on V_{DD_BV}	Total (static + dynamic) consumption: – LIN mode – Baudrate: 20 Kbyte/s		5 * f_{periph} + 31	µA
$I_{DD\_BV(SPI)}$	CC	T	SPI (DSPI) supply current on V_{DD_BV}	Ballast static consumption (only clocked)		1	µA
				Ballast dynamic consumption (continuous communication): – Baudrate: 2 Mbit/s – Transmission every 8 µs – Frame: 16 bits		16 * f_{periph}	
$I_{DD\_BV(ADC)}$	CC	T	ADC supply current on V_{DD_BV}	V_{DD} = 5.5 V	Ballast static consumption (no conversion)	41 * f_{periph}	µA
					Ballast dynamic consumption (continuous conversion)(3)	5 * f_{periph}	
$I_{DD\_HV\_ADC(ADC)}$	CC	T	ADC supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	2 * f_{periph}	µA
					Analog dynamic consumption (continuous conversion)	75 * f_{periph} + 32	
$I_{DD\_HV(FLASH)}$	CC	T	Code Flash + Data Flash supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	8.21	mA
$I_{DD\_HV(PLL)}$	CC	T	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	30 * f_{periph}	µA

1. Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 64 MHz.
2. f_{periph} is an absolute value.
3. During the conversion, the total current consumption is given from the sum of the static and dynamic consumption, i.e., (41 + 5) * f_{periph}.

4.19.2 DSPI characteristics

Table 47. DSPI characteristics[1]

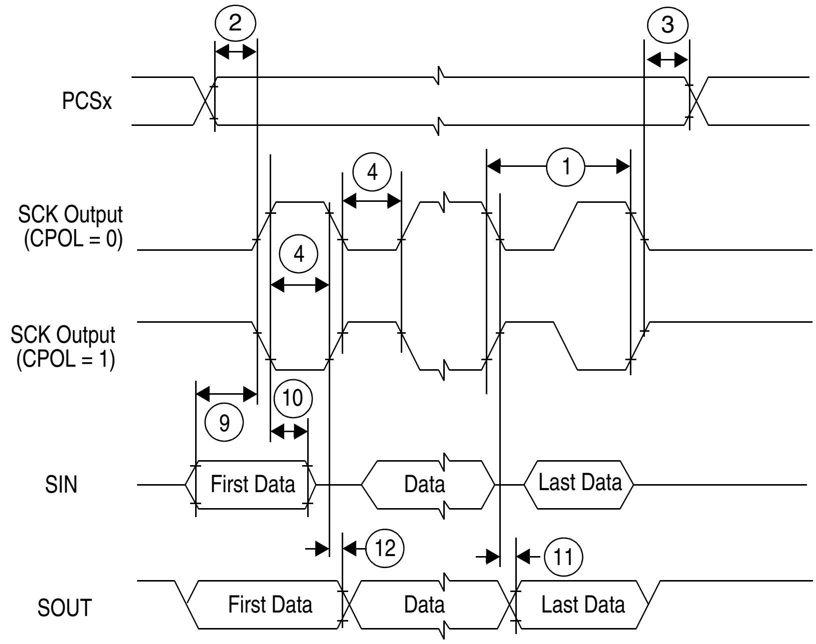
No.	Symbol		C	Parameter		DSPI0/DSPI1			DSPI2			Unit
						Min	Typ	Max	Min	Typ	Max	
1	t_{SCK}	SR	D	SCK cycle time	Master mode (MTFE = 0)	125	—	—	333	—	—	ns
			D		Slave mode (MTFE = 0)	125	—	—	333	—	—	
			D		Master mode (MTFE = 1)	83	—	—	125	—	—	
			D		Slave mode (MTFE = 1)	83	—	—	125	—	—	
—	f_{DSPI}	SR	D	DSPI digital controller frequency		—	—	f_{CPU}	—	—	f_{CPU}	MHz
—	Δt_{CSC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1→0	Master mode	—	—	130[2]	—	—	15[3]	ns
—	Δt_{ASC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1→1	Master mode	—	—	130[3]	—	—	130[3]	ns
2	t_{CSCext}[4]	SR	D	CS to SCK delay	Slave mode	32	—	—	32	—	—	ns
3	t_{ASCext}[5]	SR	D	After SCK delay	Slave mode	$1/f_{DSPI} + 5$	—	—	$1/f_{DSPI} + 5$	—	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	Master mode	—	$t_{SCK}/2$	—	—	$t_{SCK}/2$	—	ns
		SR	D		Slave mode	$t_{SCK}/2$	—	—	$t_{SCK}/2$	—	—	
5	t_A	SR	D	Slave access time	Slave mode	—	—	$1/f_{DSPI} + 70$	—	—	$1/f_{DSPI} + 130$	ns
6	t_{DI}	SR	D	Slave SOUT disable time	Slave mode	7	—	—	7	—	—	ns
7	t_{PCSC}			PCSx to $\overline{PCSS}$ time		0			0			ns
8	t_{PASC}			$\overline{PCSS}$ to PCSx time		0			0			ns

Table 47. DSPI characteristics[1] (continued)

No.	Symbol		C	Parameter		DSPI0/DSPI1			DSPI2			Unit
						Min	Typ	Max	Min	Typ	Max	
9	t_{SUI}	SR	D	Data setup time for inputs	Master mode	43	—	—	145	—	—	ns
					Slave mode	5	—	—	5	—	—	
10	t_{HI}	SR	D	Data hold time for inputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	2[6]	—	—	2[6]	—	—	
11	t_{SUO}[7]	CC	D	Data valid after SCK edge	Master mode	—	—	32	—	—	50	ns
					Slave mode	—	—	52	—	—	160	
12	t_{HO}[7]	CC	D	Data hold time for outputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	8	—	—	13	—	—	

1. Operating conditions: C_L = 10 to 50 pF, $Slew_{IN}$ = 3.5 to 15 ns.
2. Maximum value is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM. A positive value means that SCK starts before CSn is asserted. DSPI2 has only SLOW SCK available.
3. Maximum value is reached when CSn pad is configured as MEDIUM pad while SCK pad is configured as SLOW. A positive value means that CSn is deasserted before SCK. DSPI0 and DSPI1 have only MEDIUM SCK available.
4. The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext}.
5. The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext}.
6. This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of the DSPI_MCR.
7. SCK and SOUT configured as MEDIUM pad.

Figure 23. DSPI classic SPI timing – master, CPHA = 0



Note: Numbers shown reference *Table 47*.

Figure 24. DSPI classic SPI timing – master, CPHA = 1

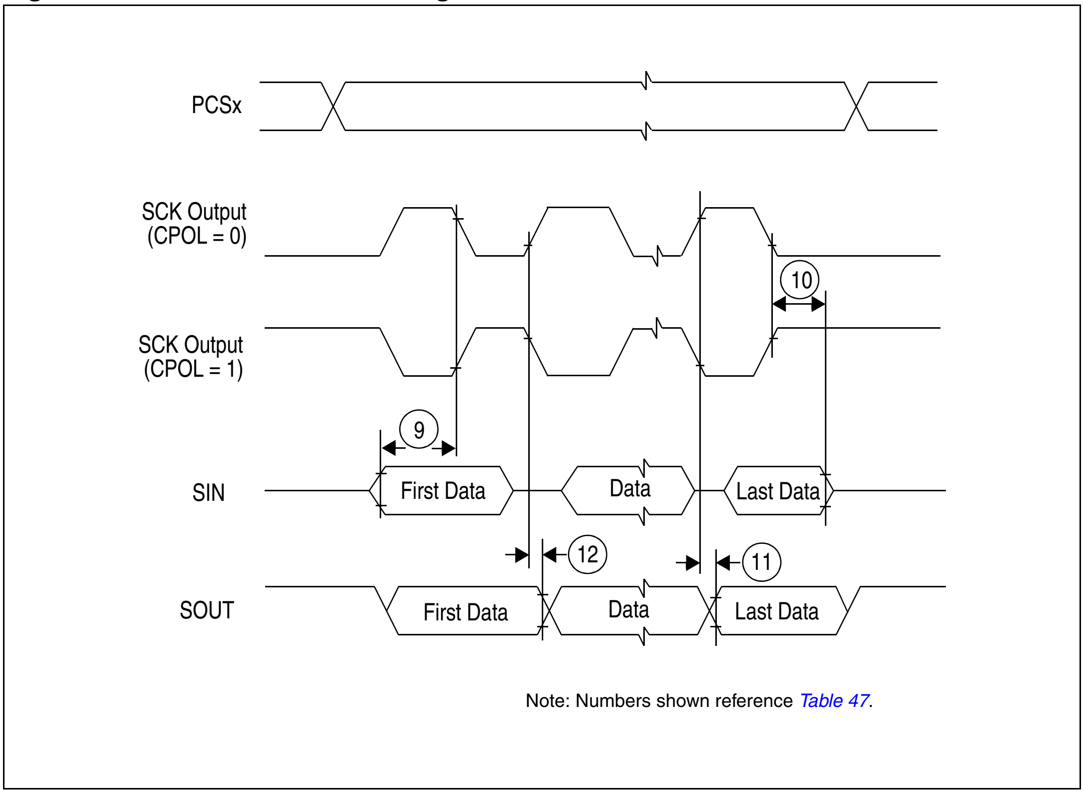


Figure 25. DSPI classic SPI timing – slave, CPHA = 0

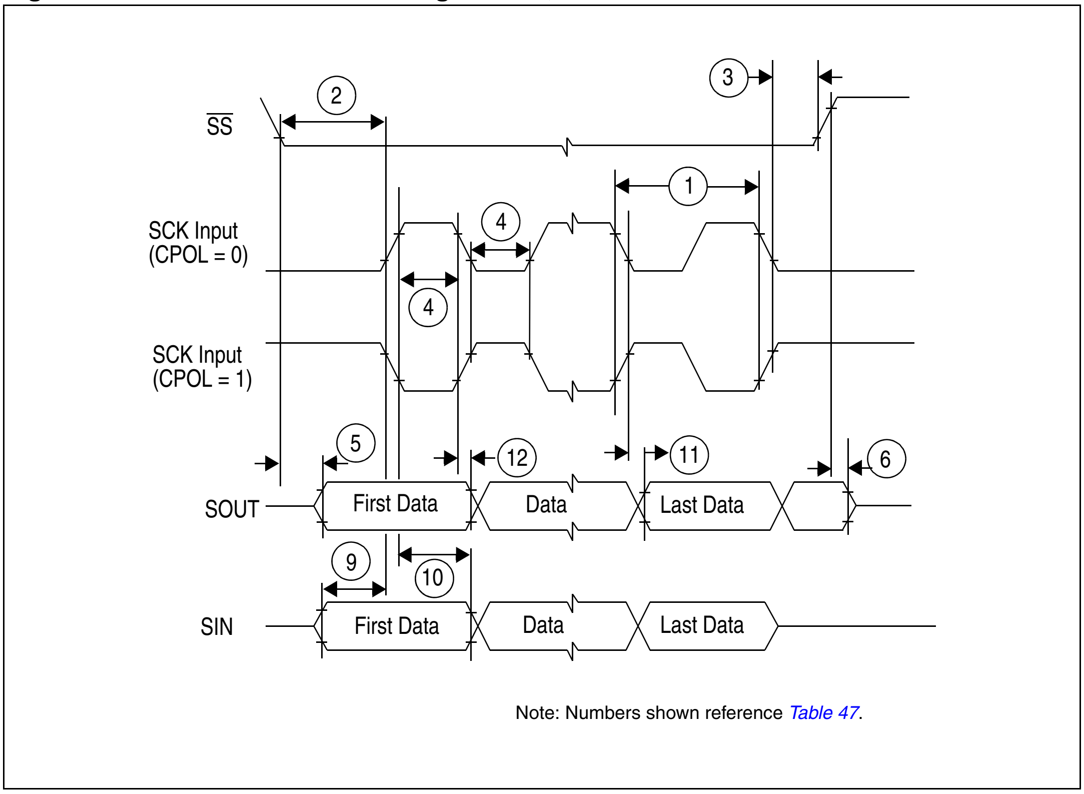
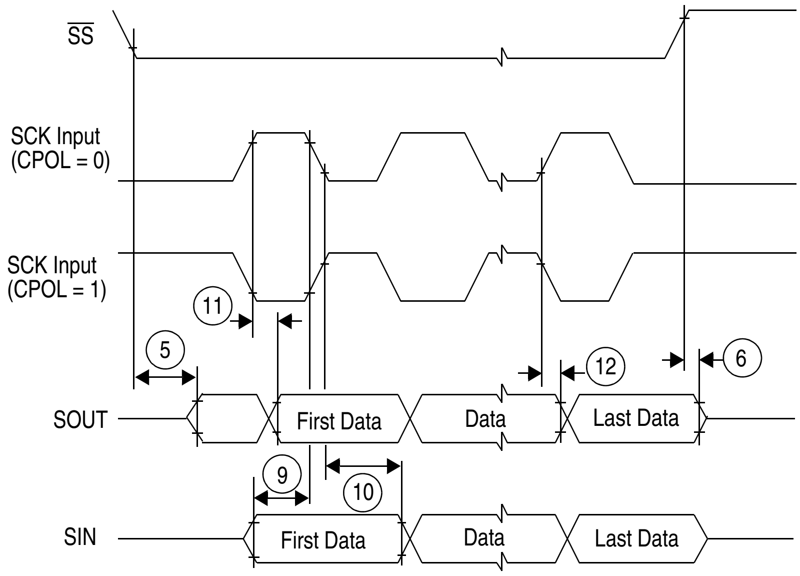
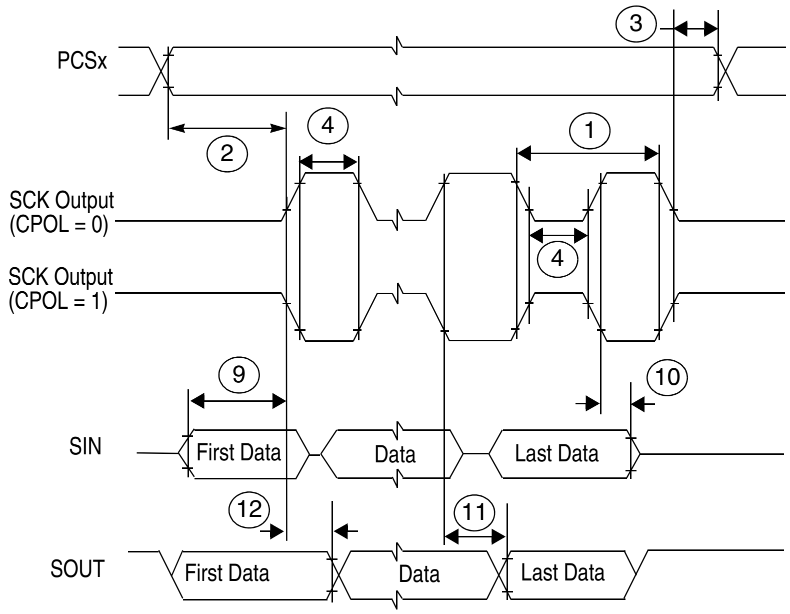


Figure 26. DSPI classic SPI timing – slave, CPHA = 1



Note: Numbers shown reference *Table 47*.

Figure 27. DSPI modified transfer format timing – master, CPHA = 0



Note: Numbers shown reference *Table 47*.

Figure 28. DSPI modified transfer format timing – master, CPHA = 1

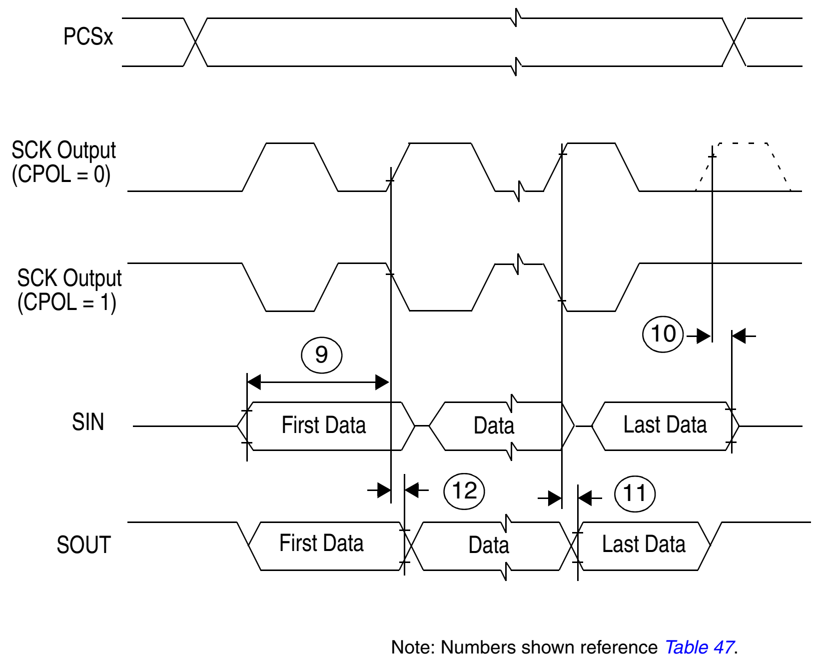


Figure 29. DSPI modified transfer format timing – slave, CPHA = 0

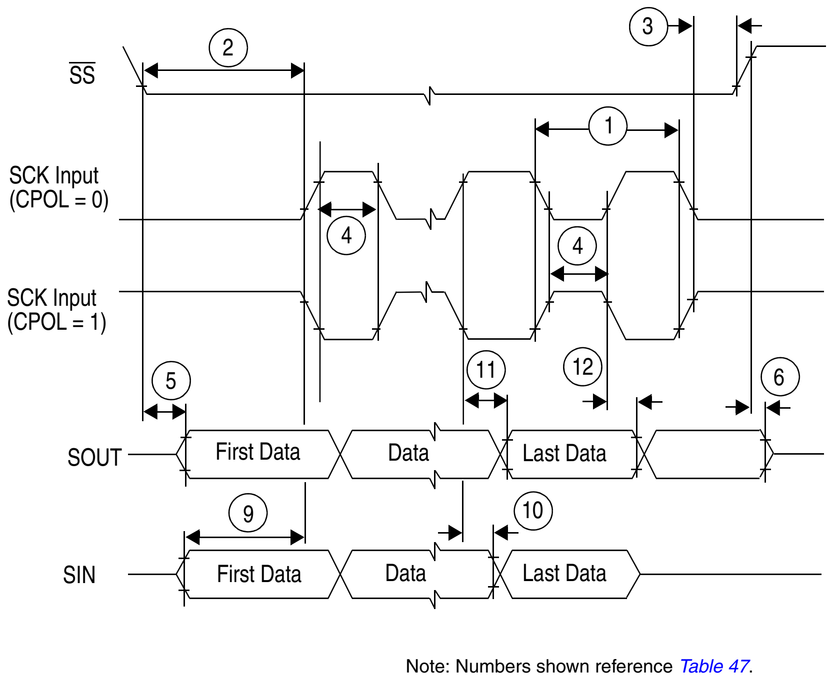
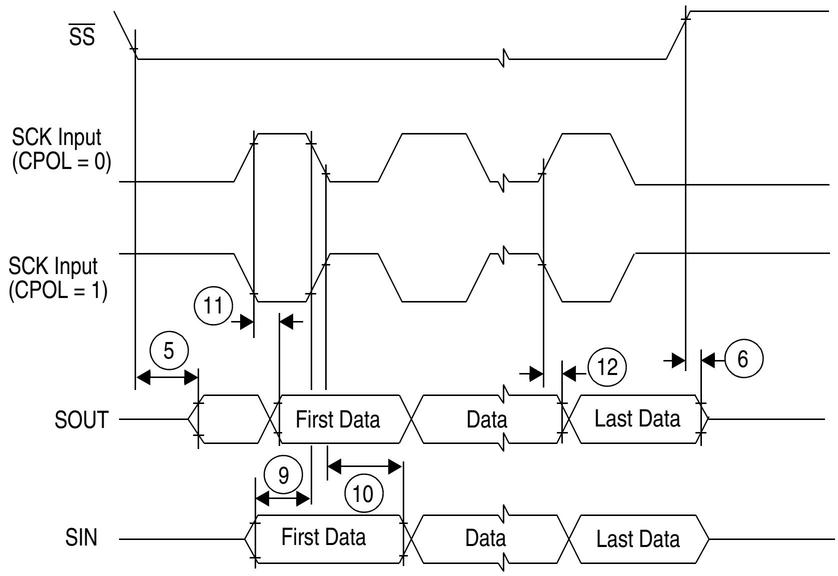
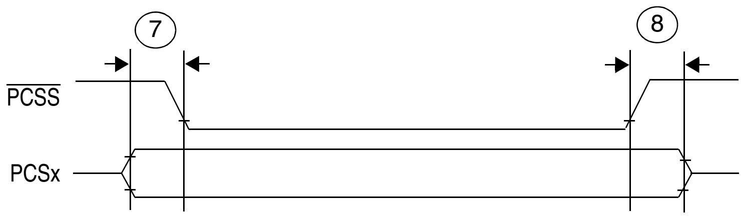


Figure 30. DSPI modified transfer format timing – slave, CPHA = 1



Note: Numbers shown reference *Table 47*.

Figure 31. DSPI PCS strobe (PCSS) timing



Note: Numbers shown reference *Table 47*.

4.19.3 Nexus characteristics

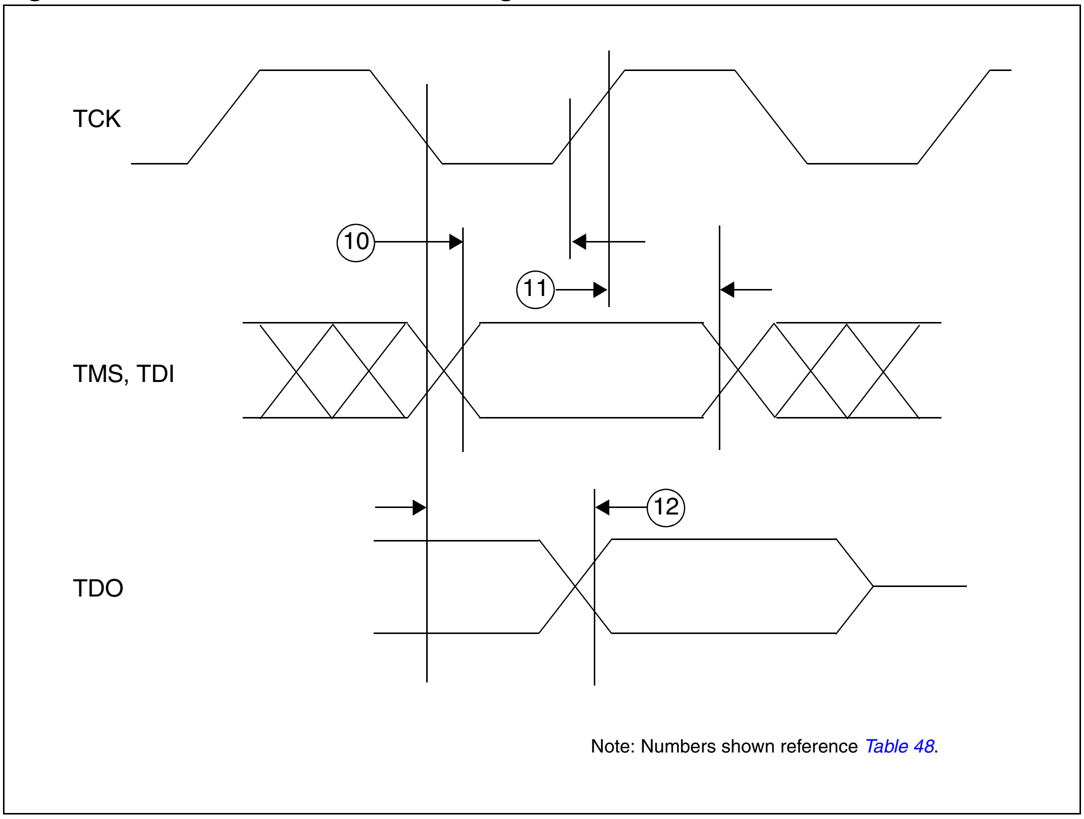
Table 48. Nexus characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{TCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
3	t_{MDOV}	CC	D	MCKO low to MDO data valid	—	—	8	ns

Table 48. Nexus characteristics (continued)

No.	Symbol		C	Parameter	Value Min	Value Typ	Value Max	Unit
4	t_{MSEOV}	CC	D	MCKO low to MSEO_b data valid	—	—	8	ns
5	t_{EVTOV}	CC	D	MCKO low to EVTO data valid	—	—	8	ns
10	t_{NTDIS}	CC	D	TDI data setup time	15	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	15	—	—	ns
11	t_{NTDIH}	CC	D	TDI data hold time	5	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	5	—	—	ns
12	t_{TDOV}	CC	D	TCK low to TDO data valid	35	—	—	ns
13	t_{TDOI}	CC	D	TCK low to TDO data invalid	6	—	—	ns

Figure 32. Nexus TDI, TMS, TDO timing

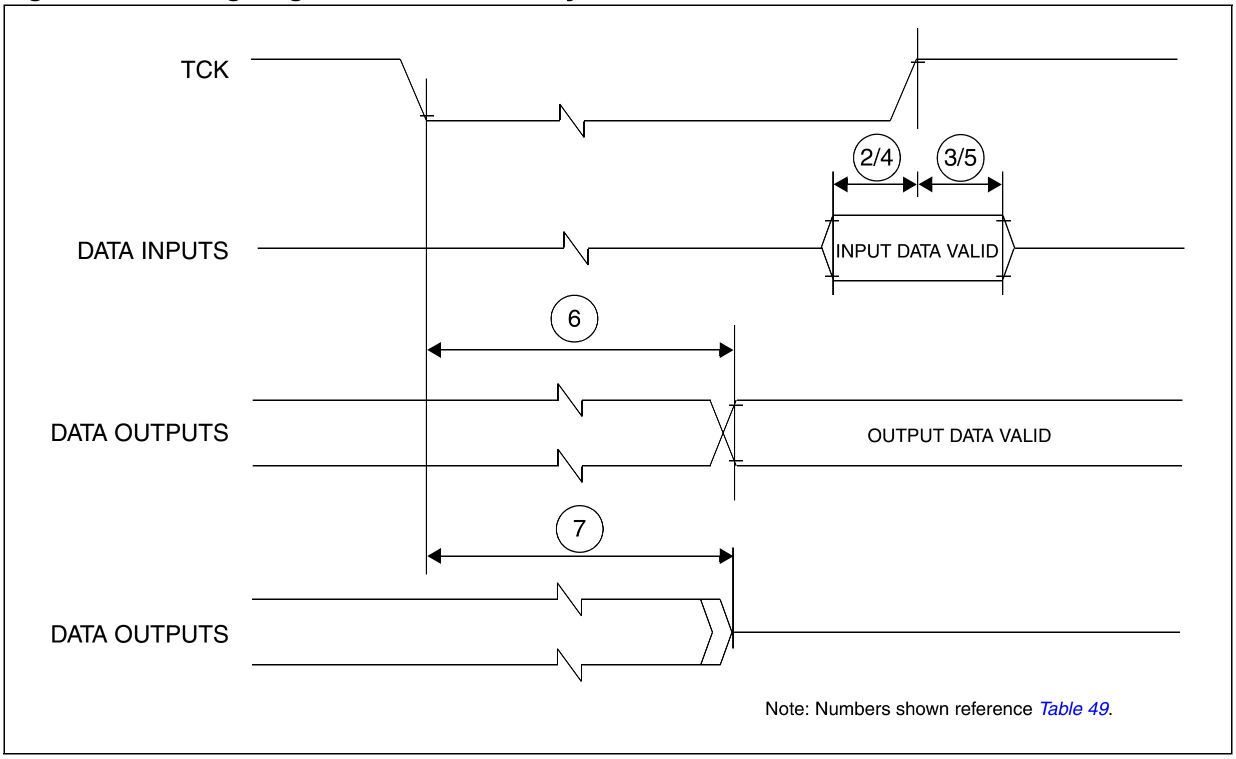


4.19.4 JTAG characteristics

Table 49. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	15	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns
4	t_{TMSS}	CC	D	TMS setup time	15	—	—	ns
5	t_{TMSH}	CC	D	TMS hold time	5	—	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	33	ns
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns

Figure 33. Timing diagram – JTAG boundary scan



5 Package characteristics

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.2 Package mechanical data

5.2.1 LQFP64

Figure 34. LQFP64 package mechanical drawing

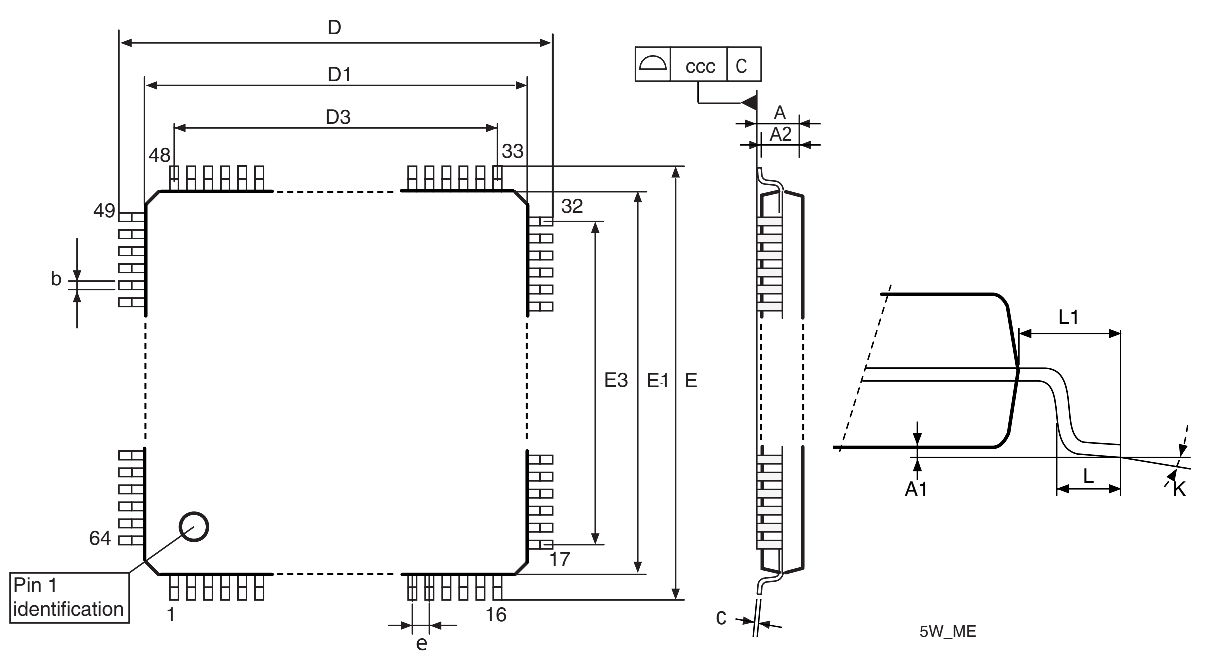


Table 50. LQFP64 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.6	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.0059
A2	1.35	1.4	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	—	0.2	0.0035	—	0.0079
D	11.8	12	12.2	0.4646	0.4724	0.4803

Table 50. LQFP64 mechanical data (continued)

Symbol	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
D1	9.8	10	10.2	0.3858	0.3937	0.4016
D3	—	7.5	—	—	0.2953	—
E	11.8	12	12.2	0.4646	0.4724	0.4803
E1	9.8	10	10.2	0.3858	0.3937	0.4016
E3	—	7.5	—	—	0.2953	—
e	—	0.5	—	—	0.0197	—
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1	—	1	—	—	0.0394	—
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	—	—	0.08	—	—	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

5.2.2 LQFP100

Figure 35. LQFP100 package mechanical drawing

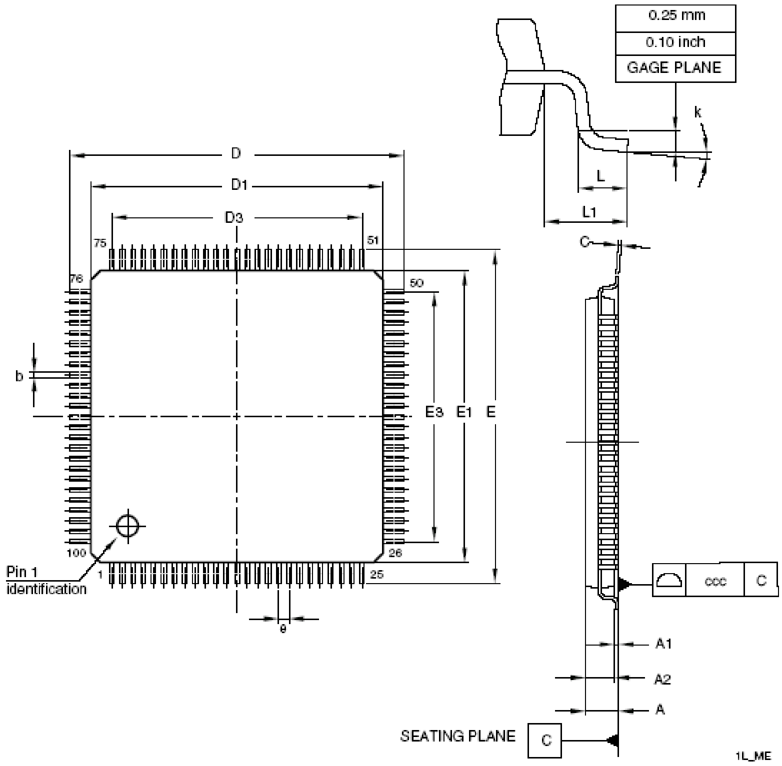


Table 51. LQFP100 mechanical data

Symbol	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 51. LQFP100 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

5.2.3 LQFP144

Figure 36. LQFP144 package mechanical drawing

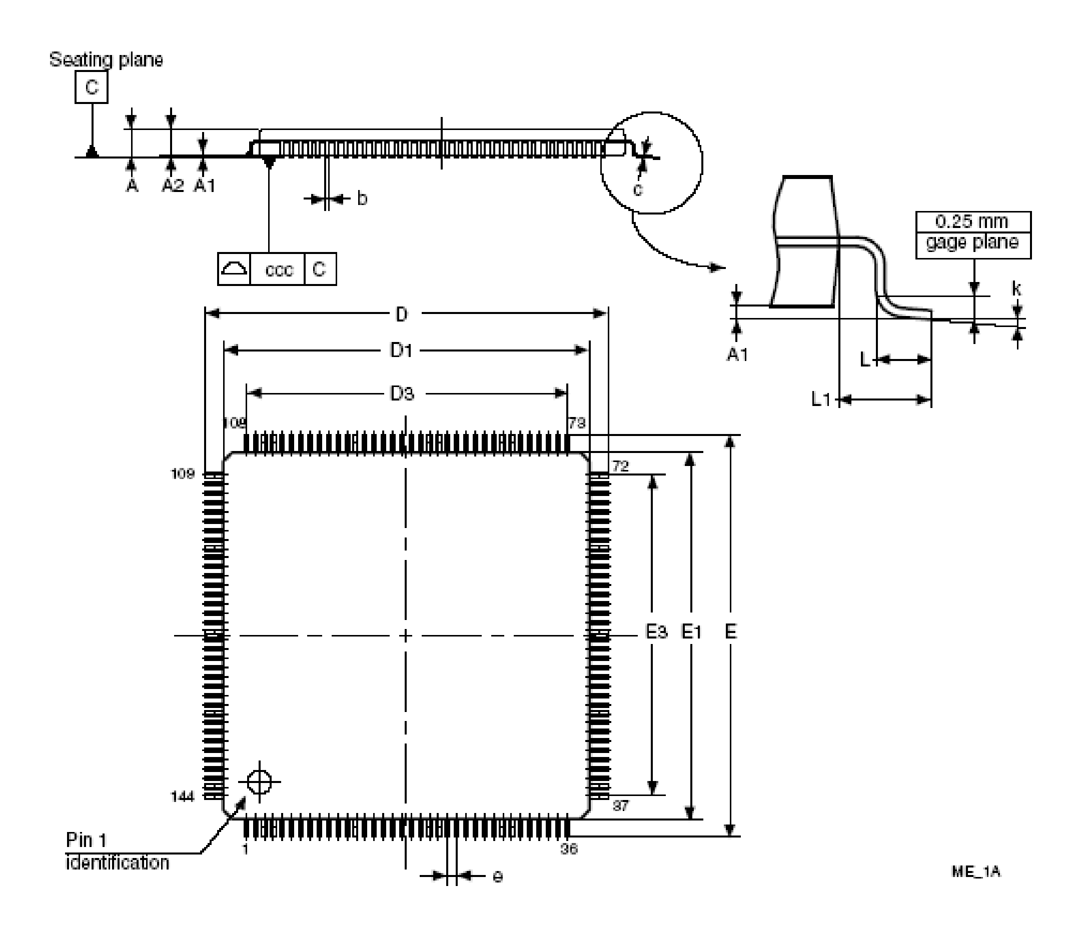


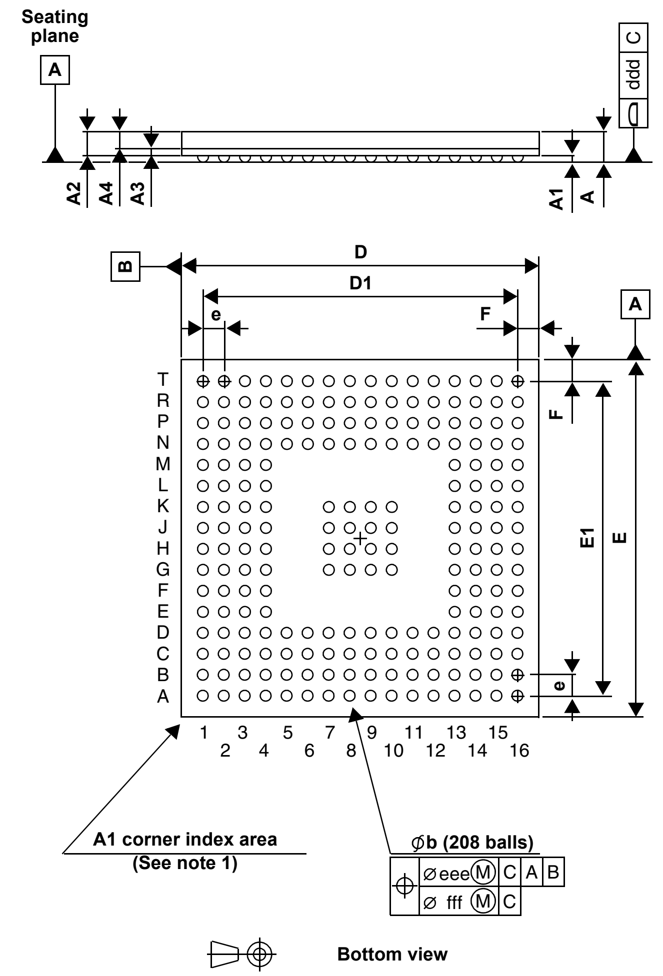
Table 52. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	—	17.500	—	—	0.6890	—
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	—	17.500	—	—	0.6890	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0°	3.5 °	0.0 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

5.2.4 LBGA208

Figure 37. LBGA208 package mechanical drawing



1. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 53. LBGA208 mechanical data

Symbol	mm			inches(1)			Notes
	Min	Typ	Max	Min	Typ	Max	
A	—	—	1.70	—	—	0.0669	(2)
A1	0.30	—	—	0.0118	—	—	—
A2	—	1.085	—	—	0.0427	—	—
A3	—	0.30	—	—	0.0118	—	—
A4	—	—	0.80	—	—	0.0315	—
b	0.50	0.60	0.70	0.0197	0.0236	0.0276	(3)

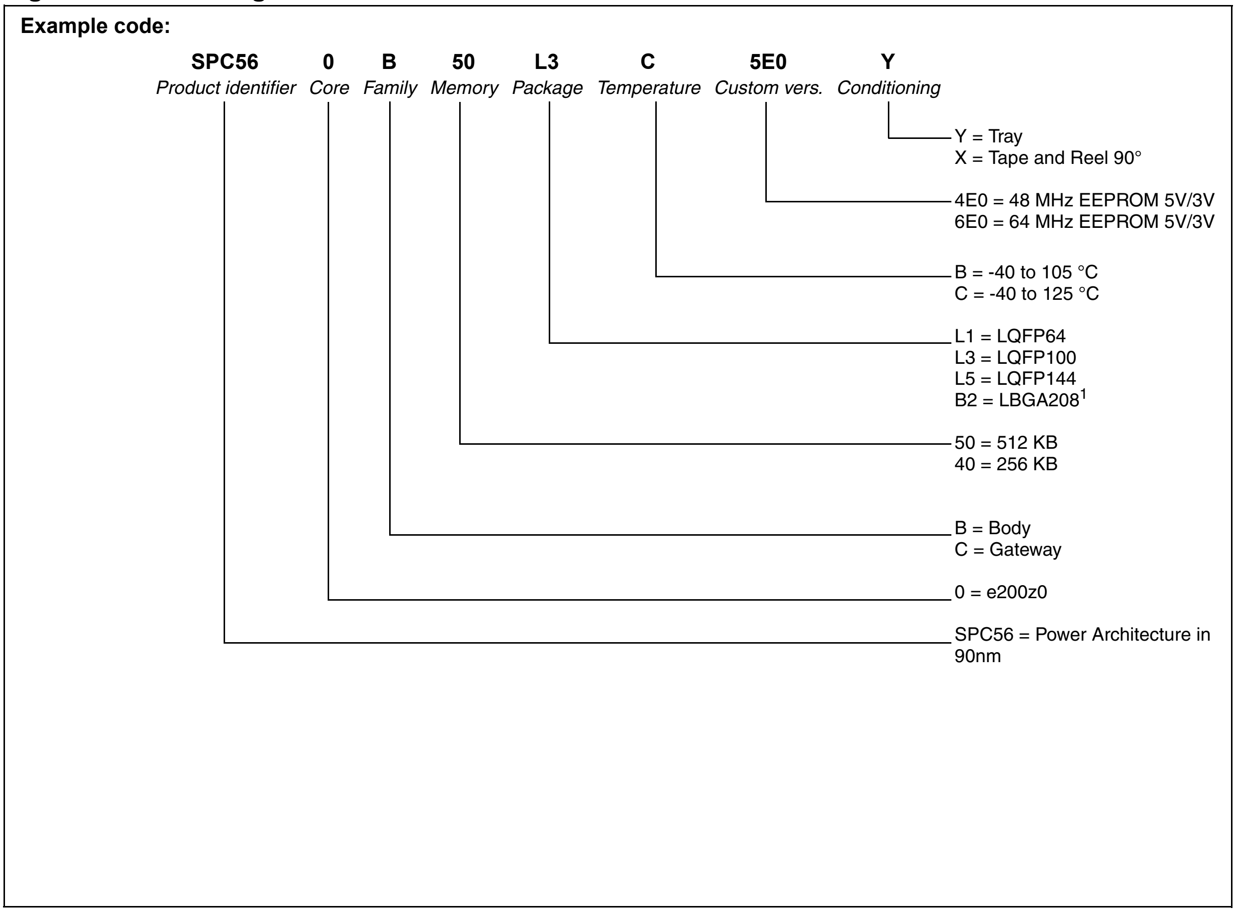
Table 53. LBGA208 mechanical data (continued)

Symbol	mm			inches(1)			Notes
	Min	Typ	Max	Min	Typ	Max	
D	16.80	17.00	17.20	0.6614	0.6693	0.6772	—
D1	—	15.00	—	—	0.5906	—	—
E	16.80	17.00	17.20	0.6614	0.6693	0.6772	—
E1	—	15.00	—	—	0.5906	—	—
e	—	1.00	—	—	0.0394	—	—
F	—	1.00	—	—	0.0394	—	—
ddd	—	—	0.20	—	—	0.0079	—
eee	—	—	0.25	—	—	0.0098	(4)
fff	—	—	0.10	—	—	0.0039	(5)

1. Values in inches are converted from mm and rounded to four decimal digits.
2. LBGA stands for **L**ow profile **B**all **G**rid **A**rray.
   — Low profile: The total profile height (Dim A) is measured from the seating plane to the top of the component
   — The maximum total package height is calculated by the following methodology:
   A2 Typ + A1 Typ +√ ($A1^2$ + $A3^2$ + $A4^2$ tolerance values)
   — Low profile: 1.20 mm < A ≤ 1.70 mm
3. The typical ball diameter before mounting is 0.60 mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
   Each tolerance zone fff in the array is contained entirely in the respective zone eee above.
   The axis of each ball must lie simultaneously in both tolerance zones.

6 Ordering information

Figure 38. Ordering information scheme



1. LBGA208 available only as development package for Nexus2+.

Appendix A Abbreviations

Table 54 lists abbreviations used but not defined elsewhere in this document.

Table 54. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

Revision history

Table 55. Document revision history

Date	Revision	Changes
04-Apr-2008	1	Initial release.
06-Mar-2009	2	Made minor editing and formatting changes to improve readability Harmonized oscillator naming throughout document Modified document title Updated “Feature” on cover page Replaced LFBGA208 with LBGA208 Updated “Description” Section Updated “SPC560B40x/50x and SPC560C40x/50x device comparison” table Added “Block diagram” section Section 3 “Package pinouts and signal descriptions”: – Removed signal descriptions (these are found in the device reference manual) Updated “LQFP 144-pin configuration (top view)” figure: – Replaced VPP with VSS_HV on pin 18 – Added MA[1] as AF3 for PC[10] (pin 28) – Added MA[0] as AF2 for PC[3] (pin 116) – Changed description for pin 120 to PH[10] / GPIO[122] / TMS – Changed description for pin 127 to PH[9] / GPIO[121] / TCK – Replaced NMI[0] with NMI on pin 11 Updated “LQFP 100-pin configuration (top view)” figure: – Replaced VPP with VSS_HV on pin 14 – Added MA[1] as AF3 for PC[10] (pin 22) – Added MA[0] as AF2 for PC[3] (pin 77) – Changed description for pin 81 to PH[10] / GPIO[122] / TMS – Changed description for pin 88 to PH[9] / GPIO[121] / TCK – Removed E1UC[19] from pin 76 – Replaced [11] with WKUP[11] for PB[3] (pin 1) – Replaced NMI[0] with NMI on pin 7 Updated “LBGA208 configuration” figure: – Changed description for ball B8 from TCK to PH[9] – Changed description for ball B9 from TMS to PH[10] – Updated descriptions for balls R9 and T9 Added “Parameter classification” section and tagged parameters in tables where appropriate Added “NVUSRO register” section Updated “Absolute maximum ratings” table “Recommended operating conditions” section : – Added note on RAM data retention to end of section Updated “Recommended operating conditions (3.3 V)” and “Recommended operating conditions (5.0 V)” Added “Package thermal characteristics” section Updated “Power considerations” section Updated I/O input DC electrical characteristics definition” figure

Table 55. Document revision history (continued)

Date	Revision	Changes
06-Mar-2009	2 (continued)	Updated tables: – “I/O input DC electrical characteristics” – “I/O pull-up/pull-down DC electrical characteristics” – “SLOW configuration output buffer electrical characteristics” – “MEDIUM configuration output buffer electrical characteristics” – “FAST configuration output buffer electrical characteristics” Added “Output pin transition times” section Updated “I/O consumption” table Updated “Start-up reset requirements” figure Updated “Reset electrical characteristics” table “Voltage regulator electrical characteristics” section: – Amended description of LV_PLL “Voltage regulator capacitance connection” figure: – Exchanged position of symbols C_{DEC1} and C_{DEC2} Updated tables” – “Voltage regulator electrical characteristics” – “Low voltage monitor electrical characteristics” – “Low voltage power domain electrical characteristics” Added “Low voltage monitor vs reset” figure Updated “Flash memory electrical characteristics” section Added “Electromagnetic compatibility (EMC) characteristics” section Updated “Fast external crystal oscillator (4 to 16 MHz) electrical characteristics” section Updated “Slow external crystal oscillator (32 kHz) electrical characteristics” section Updated tables: – “FMPLL electrical characteristics” – “Fast internal RC oscillator (16 MHz) electrical characteristics” – “Slow internal RC oscillator (128 kHz) electrical characteristics” Added “On-chip peripherals” section Added “ADC input leakage current” table Updated “ADC conversion characteristics” table Updated “ECOPACK®” section Corrected inverted column headings for typical and minimum dimensions in “LQFP64 mechanical data” and “LQFP100 mechanical data” tables Added “Abbrevation” appendix
03-Jun-2009	3	Corrected “Commercial product code structure” figure

Table 55. Document revision history (continued)

Date	Revision	Changes
06-Aug-2009	4	Updated “LBGA208 configuration” figure “Absolute maximum ratings” table: – V_{DD_ADC}, V_{IN}: changed min value for “relative to V_{DD}” condition – I_{CORELV}: added new row “Recommended operating conditions (5.0 V)” table: – $T_{A\ C\text{-}Grade\ Part}$, $T_{J\ C\text{-}Grade\ Part}$, $T_{A\ V\text{-}Grade\ Part}$, $T_{J\ V\text{-}Grade\ Part}$, $T_{A\ M\text{-}Grade\ Part}$, $T_{J\ M\text{-}Grade\ Part}$: added new rows – Changed capacitance value in footnote “Output pin transition times” table: – MEDIUM configuration: added condition for PAD3V5V = 0 Updated “Voltage regulator capacitance connection” “Voltage regulator electrical characteristics” table: – C_{DEC1}: changed min value – I_{MREG}: changed max value – I_{DD_BV}: added max value footnote “Low voltage monitor electrical characteristics” table: – $V_{LVDHV3H}$, $V_{LVDHV5H}$: changed max value – $V_{LVDHV3L}$, $V_{LVDHV5L}$: added max value Updated “Low voltage power domain electrical characteristics” table “Flash module life” table: – Retention: deleted min value footnote for “Blocks with 100000 P/E cycles“ “Fast external crystal oscillator (4 to 16 MHz) electrical characteristics” table: – I_{FXOSC}: added typ value “Slow external crystal oscillator (32 kHz) electrical characteristics” table – V_{SXOSC}: changed typ value – $T_{SXOSCSU}$: added max value footnote “FMPLL electrical characteristics” table – Δt_{LTJIT}: added max value Updated “LQFP100 package mechanical drawing”

Table 55. Document revision history (continued)

Date	Revision	Changes
20-Jan-2010	5	Table: “Absolute maximum ratings” – V_{DD_BV}, V_{DD_ADC}, V_{IN}: changed max value Table: ”Recommended operating conditions (3.3 V)” – TV_{DD}: deleted min value Table: “Reset electrical characteristics“ – Changed footnotes 2 and 5 Table: “Voltage regulator electrical characteristics“ – C_{REGn}: changed max value – C_{DEC1}: split into 2 rows – Updated voltage values in footnote 3 Table: “Low voltage monitor electrical characteristics“ – Updated column Conditions – $V_{LVDLVCORL}$, $V_{LVDLVBKPL}$: changed min/max value Table: “Program and erase specifications“ – $T_{dwprogram}$: added initial max value Table: “Flash module life“ – Retention: changed min value for blocks with 100K P/E cycles Table: “Flash power supply DC electrical characteristics“ – IFREAD, IFMOD: added typ value – Added a footnote Added Section: “ NVUSRO[WATCHDOG_EN] field description“ Section 4.18: “ADC electrical characteristics“ has been moved up in hierarchy (it was Section 4.18.5). Table: “ ADC conversion characteristics“ – R_{AD}: changed initial max value Table: “On-chip peripherals current consumption“ – Removed min/max from the heading – Changed unit of measurement and consequently rounded the values
15-Mar-2010	6	Internal release.

Table 55. Document revision history (continued)

Date	Revision	Changes
22-Jul-2010	7	**Changes between revisions 5 and 7** Added LQFP64 package information Updated the “Features“ section. Section “Introduction” – Relocated a note Table: “SPC560B40x/50x and SPC560C40x/50x device comparison“ – Added footnote regarding SCI and CAN Added eDMA block in the “SPC560B40x/50x and SPC560C40x/50x series block diagram” figure Removed alternate function information from “LQFP 100-pin configuration” and “LQFP 100-pin configuration” figures. Added “Functional port pin descriptions” table Deleted the “NVUSRO[WATCHDOG_EN] field description“ section Table: “Absolute maximum ratings“ – Removed the min value of V_{IN} relative tio V_{DD} Table ”Recommended operating conditions (3.3 V)” – TV_{DD}: made single row ”Recommended operating conditions (5.0 V)” – deleted $T_{A\ C\text{-}Grade\ Part}$, $T_{J\ C\text{-}Grade\ Part}$, $T_{A\ V\text{-}Grade\ Part}$, $T_{J\ V\text{-}Grade\ Part}$, $T_{A\ M\text{-}Grade\ Part}$, $T_{J\ M\text{-}Grade\ Part}$ rows Table: “LQFP thermal characteristics” – Added more rows – Rounded the values Removed table “LBGA208 thermal characteristics” Table “I/O input DC electrical characteristics” – W_{FI}: insered a footnote – W_{NFI}: insered a footnote Table “I/O consuption“ – Removed I_{DYNSEG} row – Added “I/O weight “ table Replaced “nRSTIN” with “$\overline{\text{RESET}}$” in the “$\overline{\text{RESET}}$ electrical characteristics” section. Table “Voltage regulator electrical characteristics“ – Updated the values – Removed $I_{VREGREF}$ and $I_{VREDLVD12}$ – Added a note about I_{DD_BC} Table: “Low voltage monitor electrical characteristics“ – changed min value$V_{LVDHV3L}$, from 2.7 to 2.6 – Inserted max value of $V_{LVDLVCORL}$ – Updated V_{PORH} values – Updated $V_{LVDLVCORL}$ value Table “Low voltage power domain electrical characteristics“ – Entirely updated Table “Program and erase specifications“ – Inserted T_{eslat} row Table “Flash power supply DC electrical characteristics“ – Entirely updated

Table 55. Document revision history (continued)

Date	Revision	Changes
22-Jul-2010	7 (continued)	Table “Start-up time/Switch-off time“ – Entirely updated Figures “Crystal oscillator and resonator connection scheme“ – Relocated a note Table ”Slow external crystal oscillator (32 kHz) electrical characteristics” – Removed g_{mSXOSC} row – Inserted values of $I_{SXOSCBIAS}$ Table ”FMPLL electrical characteristics” – Rounded the values of f_{VCO} Table “Fast internal RC oscillator (16 MHz) electrical characteristics“ – Entirely updated. Table “ADC conversion characteristics” – Updated the description of the conditions of t_{ADC_PU} and t_{ADC_S}. – Added “I_{ADCPWD}” and “I_{ADCRUN}” rows Table “DSPI characteristics“ – Entirely updated. Updated “Order codes” table. Figure “Commercial product code structure” – Replaced PowerPC with “Power Architecture™“ in the product identifier – Removed the note about the condition from “Flash read access timing“ table – Removed the notes that assert the values need to be confirmed before validation – Exchanged the order of “LQFP 100-pin configuration” and “LQFP 144-pin configuration” – Exchanged the order of “LQFP 100-pin package mechanical drawing” and “LQFP 144-pin package mechanical drawing”
25-Nov-2010	8	Editorial changes and improvements. In the “SPC560B40x/50x and SPC560C40x/50x device comparison” table, changed the temperature value from 105 to 125 °C, in the footnote regarding “Execution speed”. In the “LQFP thermal characteristics” table, added values concerning LQFP64 package. In the “MEDIUM configuration output buffer electrical characteristics” table: fixed a typo in last row of conditions column, there was I_{OH} that now is I_{OL}. In the “Reset electrical characteristics” table, changed the parameter classification tag for V_{OL} and $\|I_{WPU}\|$. In the “Low voltage monitor electrical characteristics” table, changed the max value of $V_{LVDLVCORL}$ from 1.5V to 1.15V. In the “Program and erase specifications” table, replaced “T_{eslat}” with “T_{esus}”. In the “FMPLL electrical characteristics” table, changed the parameter classification tag for f_{VCO}.

Table 55. Document revision history (continued)

Date	Revision	Changes
01-Oct-2011	9	Formatting and minor editorial changes throughout Harmonized oscillator nomenclature Device summary table: removed 384 KB code flash device versions Device comparison table: changed temperature value in footnote 2 from 105 °C to 125 °C; removed 384 KB code flash device versions LQFP 64-pin configuration: renamed pin 6 from VPP_TEST to VSS_HV Removed “Pin Muxing” section; added sections “Pad configuration during reset phases”, “Voltage supply pins”, “Pad types”, “System pins,” “Functional ports”, and “Nexus 2+ pins” Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality; updated footnote describing default value of ‘1’ in field descriptions NVUSRO[PAD3V5V] and NVUSRO[OSCILLATOR_MARGIN] Added section “NVUSRO[WATCHDOG_EN] field description” Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V): updated conditions for ambient and junction temperature characteristics I/O input DC electrical characteristics: updated I_{LKG} characteristics Section “I/O pad current specification”: removed content referencing the I_{DYNSEG} maximum value I/O consumption: replaced instances of “Root medium square” with “Root mean square” I/O weight: replaced instances of bit “SRE” with “SRC”; added pads PH[9] and PH[10]; added supply segments; removed weight values in 64-pin LQFP for pads that do not exist in that package Reset electrical characteristics: updated parameter classification for $\|I_{WPU}\|$ Updated Voltage regulator electrical characteristics Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$; replaced “LVD_DIGBKP” with “LVDLVBKP” in note Updated section “Power consumption” Fast external crystal oscillator (4 to 16 MHz) electrical characteristics: updated parameter classification for $V_{FXOSCOP}$ Crystal oscillator and resonator connection scheme: added footnote about possibility of adding a series resistor Slow external crystal oscillator (32 kHz) electrical characteristics: updated footnote 1 FMPLL electrical characteristics: added short term jitter characteristics; inserted “—” in empty min value cell of t_{lock} row Section “Input impedance and ADC accuracy”: changed “V_A/V_{A2}” to “V_{A2}/V_A” in Equation 11 ADC input leakage current: updated I_{LKG} characteristics ADC conversion characteristics: updated symbols On-chip peripherals current consumption: changed “supply current on “$V_{DD\_HV\_ADC}$” to “supply current on” V_{DD_HV}” in $I_{DD\_HV(FLASH)}$ row; updated $I_{DD\_HV(PLL)}$ value—was 3 * f_{periph}, is 30 * f_{periph}; updated footnotes DSPI characteristics: added rows t_{PCSC} and t_{PASC} Added DSPI PCS strobe (PCSS) timing diagram Updated order codes.