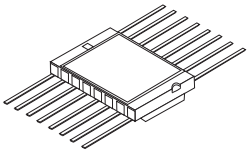
RHFL4913A

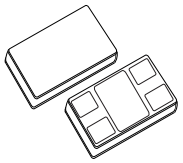
Rad-hard adjustable positive voltage regulator

Features

- 3 A low dropout voltage
- Embedded overtemperature and overcurrent protection
- Adjustable overcurrent limitation
- Output overload monitoring/signalling
- Adjustable output voltage
- Inhibit (ON/OFF) TTL-compatible control
- Programmable output short-circuit current
- Remote sensing operation
- Rad-hard: guaranteed up to 300 krad Mil Std 883E Method 1019.6 high dose rate and 0.01 rad/s in ELDRS conditions
- Heavy ion, SEL immune



FLAT-16



SMD5C:
5-connection SMD

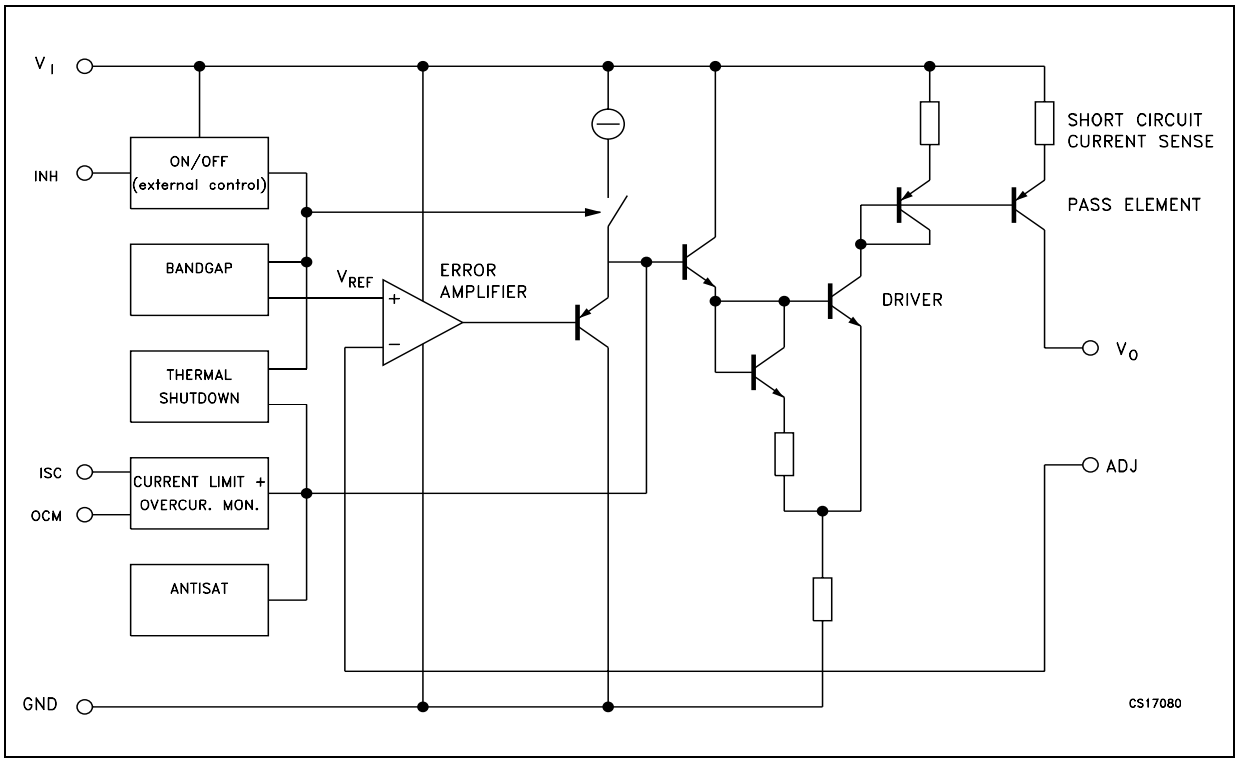
Description

The RHFL4913A high-performance adjustable positive voltage regulator provides exceptional radiation performance. It is tested in accordance with Mil Std 883E Method 1019.6, in ELDRS conditions. The device is available in the FLAT-16 and the new SMD5C hermetic ceramic package, and the QML-V die is specifically designed for space and harsh radiation environments. It operates with an input supply of up to 12 volts. The RHFL4913A is QML-V qualified, DSCC SMD #5962F02524.

Contents

1 Diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin configuration (top view for FLAT-16, bottom view for SMD5C)

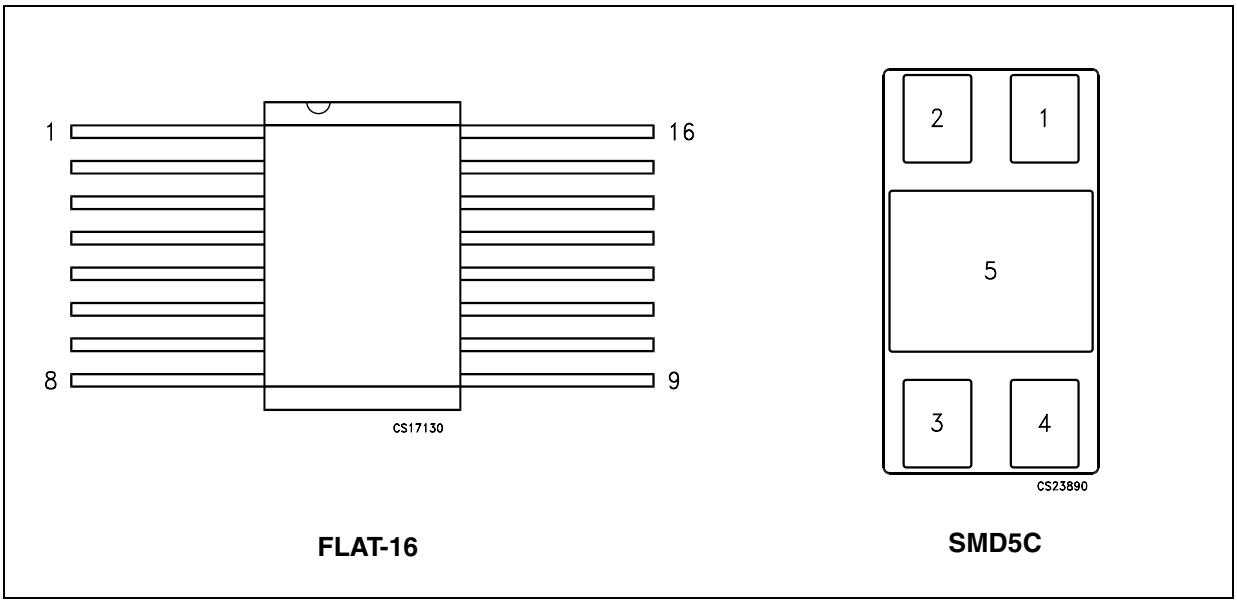


Table 1. Pin description

Pin name	FLAT-16 (1)	SMD5C (2)
V_O	1, 2, 6, 7	1
V_I	3, 4, 5	4
GND	13	5
I_{SC}	8	
OCM	10	
INHIBIT	14	3
ADJ	15	2
NC	9, 11, 12, 16	

1. The upper metallic package lid and the bottom metallization are neither connected to regulator die nor to package terminals, hence electrically floating.
2. The upper metallic package lid is neither connected to regulator die nor to package terminals, hence electrically floating.

3 Maximum ratings

Table 2. Recommended maximum operating ratings (1)

Symbol	Parameter	Value	Unit
V_I	DC input voltage, V_I - V_{GROUND}	12	V
V_O	DC output voltage range	1.23 to 9	V
I_O	Output current, RHFL4913KPA	2	A
I_O	Output current, RHFL4913SCA	3	
P_D	T_C = 25 °C power dissipation	15	W
T_{STG}	Storage temperature range	-65 to +150	°C
T_{OP}	Operating junction temperature range	-55 to +150	°C
ESD	Electrostatic discharge capability	Class 3	

1. Exceeding maximum ratings may damage the device.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case, FLAT-16 and SMD5C	8.3	°C/W
T_{SOLD}	Maximum soldering temperature, 10 sec.	300	°C

4 Electrical characteristics

T_J = 25 °C, $V_I = V_O$ + 2.5 V, $C_I = C_O$ = 1 µF, unless otherwise specified.

Table 4. Electrical characteristics

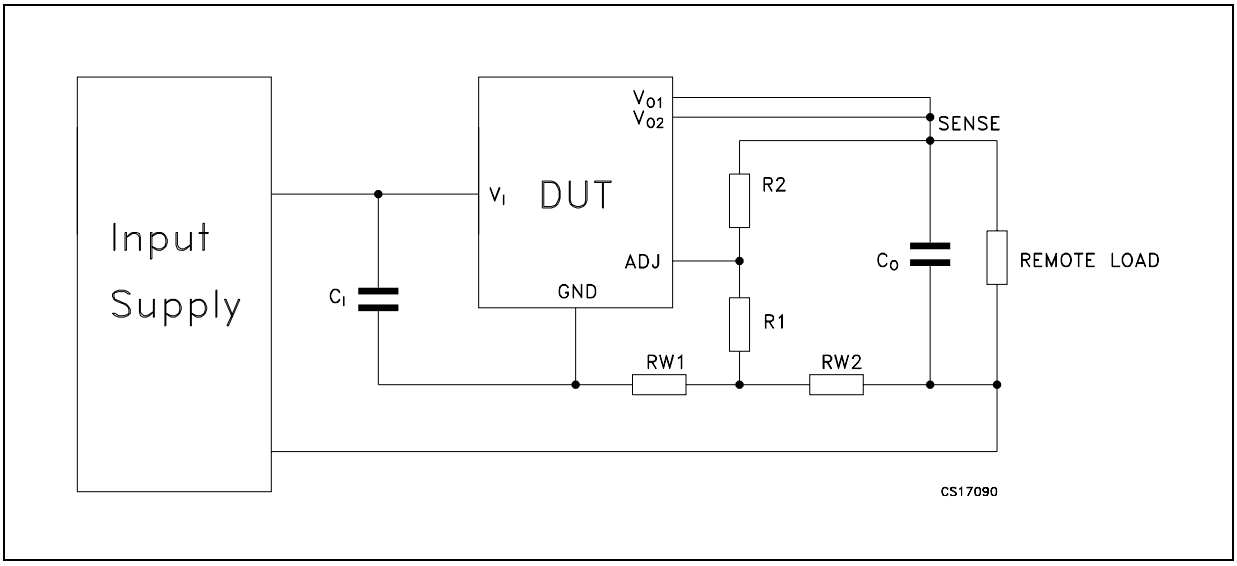
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Operating input voltage	I_O = 1 A, T_J = -55 to 125°C	3		12	V
V_O	Operating output voltage	I_O = 1 A and or 2, V_O = 1.23 V	1.19		1.27	V
		I_O = 1 A and or 2, V_O = 9 V	8.7		9.3	V
I_{SHORT}	Output current limit (1)	Adjustable by mask/external resistor	1	4.5		A
$\Delta V_O/\Delta V_I$	Line regulation	$V_I = V_O$+2.5 V to 12 V, I_O = 5 mA, T_J = +25°C			0.35	%
		$V_I = V_O$+2.5 V to 12 V, I_O = 5 mA, T_J = -55°C			0.4	
		$V_I = V_O$+2.5 V to 12 V, I_O = 5 mA, T_J = +125°C			0.4	
$\Delta V_O/\Delta V_O$	Load regulation	$V_I = V_O$+2.5 V, I_O = 5 to 400 mA, T_J = +25°C			0.3	%
		$V_I = V_O$+2.5 V, I_O = 5 to 400 mA, T_J = -55°C			0.5	
		$V_I = V_O$+2.5 V, I_O = 5 to 400 mA, T_J = +125°C			0.5	
		$V_I = V_O$+2.5 V, I_O = 5 mA to 1 A, T_J = +25°C			0.5	
		$V_I = V_O$+2.5 V, I_O = 5 mA to 1A, T_J = -55°C			0.6	
		$V_I = V_O$+2.5 V, I_O = 5 mA to 1A, T_J = +125°C			0.6	
Z_{OUT}	Output impedance	I_O = 100 mA DC and 20 mA rms		100		mΩ
I_q	Quiescent current	$V_I = V_O$+2.5 V, I_O = 5 mA, ON mode (+25°C)			6	mA
		$V_I = V_O$+2.5 V, I_O = 30 mA, ON mode (+25°C)			8	
		$V_I = V_O$+2.5 V, I_O = 300 mA, ON mode (+25°C)			25	
		$V_I = V_O$+2.5 V, I_O = 1 A, ON mode (+25°C)			60	
		$V_I = V_O$+2 V, V_{INH} = 2.4 V, OFF mode			1	
I_q	Quiescent current ON mode	$V_I = V_O$+2.5 V, I_O = 30 mA, (-55°C)			14	mA
		$V_I = V_O$+2.5 V, I_O = 300 mA, (-55°C)			40	
		$V_I = V_O$+2.5 V, I_O = 1 A, (-55°C)			100	
		$V_I = V_O$+2.5 V, I_O = 30 mA, (+125°C)			8	
		$V_I = V_O$+2.5 V, I_O = 300 mA, (+125°C)			20	
		$V_I = V_O$+2.5 V, I_O = 1 A, (+125°C)			40	

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_d	Dropout voltage	I_O = 400 mA, V_O = 2.5 to 9 V, (+25°C)			350	450	mV
		I_O = 400 mA, V_O = 2.5 to 9 V, (-55°C)			300	400	
		I_O = 400 mA, V_O = 2.5 to 9 V, (+125°C)			450	550	
		I_O = 1 A, V_O = 2.5 to 9 V, (+25°C)				650	
		I_O = 1 A, V_O = 2.5 to 9 V, (-55°C)				550	
		I_O = 1 A, V_O = 2.5 to 9 V, (+125°C)				800	
		I_O = 2 A, V_O = 2.5 to 9 V, (+25°C)			900		
		I_O = 2 A, V_O = 2.5 to 9 V, (+125°C)			950		
$V_{INH(ON)}$	Inhibit voltage	I_O = 5 mA, T_J = -55 to +125°C				0.8	V
$V_{INH(OFF)}$	Inhibit voltage	I_O = 5 mA, T_J = -55 to +125°C		2.4			
SVR	Supply voltage rejection (1)	$V_I = V_O + 2.5\ V \pm 0.5\ V$, V_O = 3 V I_O = 5 mA	f = 120 Hz	60	70		dB
			f = 33 kHz	30	40		
I_{SH}	Shutdown input current	V_{INH} = 5 V			15		µA
V_{OCM}	OCM pin voltage	Sinked I_{OCM} = 24 mA active low			0.38		V
t_{PLH} t_{PHL}	Inhibit propagation delay (1)	$V_I = V_O$ + 2.5V, V_{INH} = 2.4 V, I_O = 400 mA V_O = 3 V		ON-OFF		20	µs
				OFF-ON		100	µs
eN	Output noise voltage (1)	B = 10 Hz to 100 kHz, I_O = 5 mA to 2 A			40		µVrms

1. These values are guaranteed by design. For each application it is strongly recommended to comply with the maximum current limit of the package used.

Figure 3. Application diagram for remote sensing operation



5 Device description

The RHFL4913A adjustable voltage regulator contains a PNP type power element controlled by a signal resulting from an amplified comparison between the internal temperature-compensated band-gap and the fraction of the desired output voltage value obtained from an external resistor divider bridge. The device is protected by several functional blocks.

5.1 ADJ pin

The load output voltage feedback comes from an external resistor divider bridge mid-point connected to the ADJ pin (allowing all possible output voltage settings as per user requirements) established between load terminals.

5.2 Inhibit ON-OFF control

By setting the INHIBIT pin TTL high, the device switches off the output current and voltage. The device is ON when the INHIBIT pin is set low. Since the INHIBIT pin is pulled down internally, it can be left floating in cases where the inhibit function is not used.

5.3 Overtemperature protection

A temperature detector internally monitors the power element junction temperature. The device turns off when a temperature of approximately 175 °C is reached, returning to ON mode when back to approximately 135 °C. Combined with the other protection blocks, the device is protected from destructive junction temperature excursions in all load conditions. It should be noted that when the internal temperature detector reaches 175 °C, the active power element can be as high as 225 °C. Prolonged operation under these conditions far exceeds the maximum operating ratings and device reliability cannot be guaranteed.

5.4 Overcurrent protection

An internal non fold-back short circuit limitation is set with I_{SHORT} > 3.8 A (V_O is 0 V). This value can be decreased via an external resistor connected between the I_{SC} and V_I pins, with a typical value range of 10 kΩ to 200 kΩ. To maintain optimal V_O regulation, it is necessary to set I_{SHORT} 1.6 times greater than the maximum desired application I_O. When I_O reaches I_{SHORT} – 300 mA, the current limiter overrules the regulation, V_O starts to drop and the OCM flag is raised. When no current limitation adjustment is required, the I_{SC} pin must be left unbiased (as it is in 3 pin packages).

5.5 OCM pin

The OCM pin goes low when the current limit becomes active, otherwise $V_{OCM} = V_I$. It is buffered and can sink 10 mA. The OCM pin is internally pulled up by a 5 kΩ resistor.

5.6 Alternatives to the RHFL4913A

The adjustable RHFL4913A is recommended to replace all industry positive voltage regulators due to its exceptional radiation performance. To replace 3-terminal industry devices, the fixed voltage versions of the RHFL4913A should be used.

6 Application information

To adjust the output voltage, the R2 resistor must be connected between the V_O and ADJ pins. The R1 resistor must be connected between ADJ and ground. Resistor values can be derived from the following formula:

$V_O = V_{ADJ} (R1+ R2) / R1$

The V_{ADJ} is 1.23 V, controlled by the internal temperature-compensated band gap block.

The minimum output voltage is therefore 1.22 V and minimum input voltage is 3 V.

The RHFL4913A adjustable is functional as soon as the V_I - V_O voltage difference is slightly above the power element saturation voltage. The adjust pin to ground resistor value must not be greater than 10 kΩ, in order to keep the output feedback error below 0.2%. A minimum of 0.5 mA I_O must be set to ensure perfect no-load regulation. It is advisable to dissipate this current into the divider bridge resistor. All available V_I pins, as well as all available V_O pins, should always be externally interconnected, otherwise the stability and reliability of the device cannot be guaranteed. The inhibit function switches off the output current electronically, and therefore very quickly. According to Lenz's Law, external circuitry reacts with LdI/dt terms which can be of high amplitude in case somewhere a serial coil inductance exists. Large transient voltage would develop on both device terminals. It is advisable to protect the device with Schottky diodes to prevent negative voltage excursions. In the worst case, a 14 V Zener diode could protect the device input. The device has been designed for high stability and low dropout operation. Therefore, tantalum input and output capacitors with a minimum 1 µF are mandatory. Capacitor ESR range is from 0.01 Ω to over 20 Ω. This range is useful when ESR increases at low temperature. When large transient currents are expected, larger value capacitors are necessary.

In the case of high current operation with short circuit events expected, caution must be exercised with regard to capacitors. They must be connected as close as possible to the device terminals. As some tantalum capacitors may permanently fail when subjected to high charge-up surge currents, it is recommended to decouple them with 470 nF polyester capacitors.

Since the RHFL4913A adjustable voltage regulator is manufactured with very high speed bipolar technology (6 GHz f_T transistors), the PCB layout must be designed with exceptional care, with very low inductance and low mutually coupling lines. Otherwise, high frequency parasitic signals may be picked up by the device resulting in system self-oscillation. The benefit is an SVR performance extended to far higher frequencies.

6.1 Notes on the 16-pin hermetic package

The bottom section of the 16-pin package is metallized in order to allow the user to directly solder the RHFL4913A onto PCB, no heat sink needed for enhanced heat removal.

6.2 Remote sensing operation

A separate kelvin voltage sensing line provides the ADJ pin with exact load "high potential" information (see *Figure 3*). But variable remote load current consumption induces variable Iq current (Iq is roughly the I_O current divided by the h_{FE} of the internal PNP series power element) routed through the parasitic series line resistor RW2. To compensate for this

parasitic voltage, resistor RW1can be introduced to provide the necessary compensating voltage signal to the ADJUST pin.

6.3 FPGA power supply lines

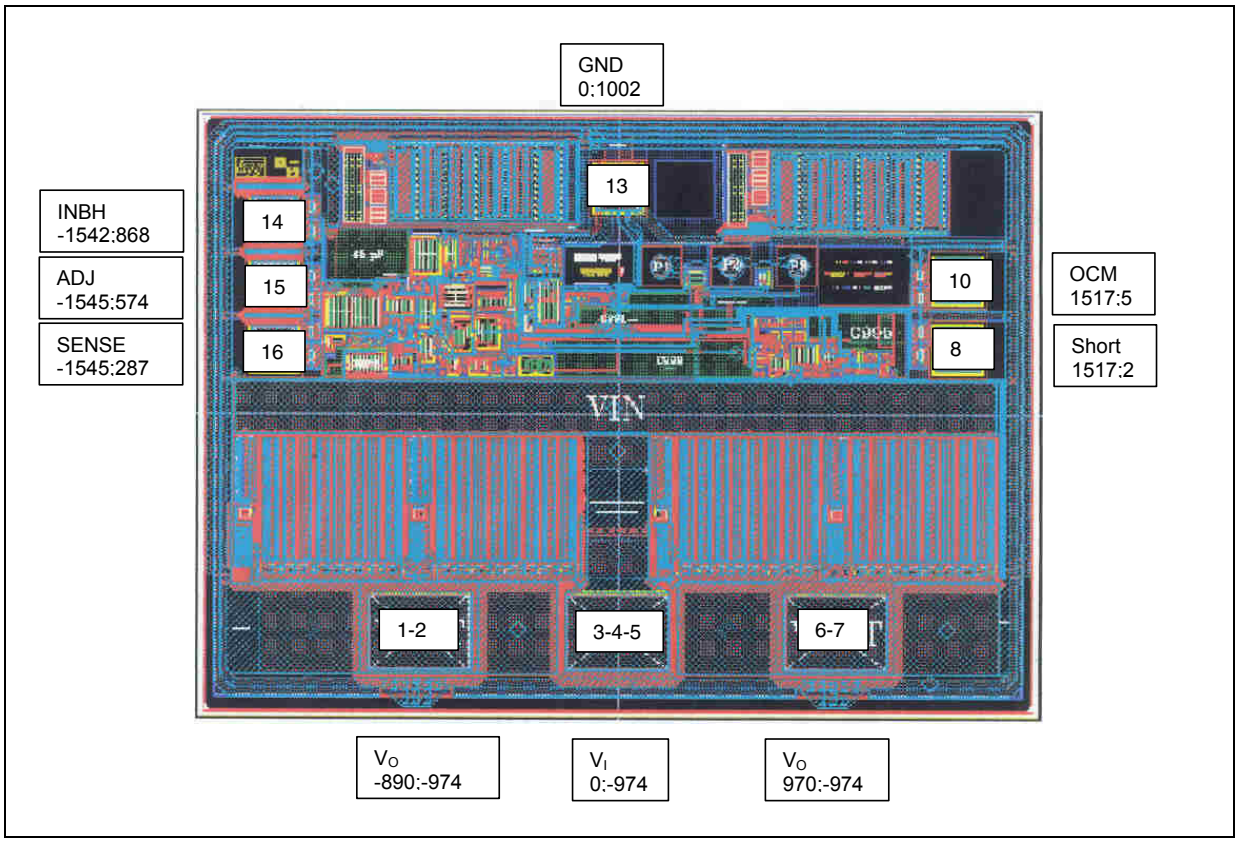
Because these devices are very sensitive to V_{DD} transients beyond a few % of their nominal supply voltage (usually 1.5 V), special attention must be given by supply lines designers to mitigate possible heavy ion L4913 disturbances. The worst case heavy ion effect can be summarized as: the L4913 internal control loop being cut (made open) or short-circuited for a sub-microsecond duration. During such an event, the L4913 die power element can either provide excessive current or current supply stoppage to the output (V_{OUT}) for a duration of about one microsecond, after which time the L4913 smoothly recovers to nominal operation. To mitigate these "transients", it is recommended to implement the L4913 PCB layout as follows:

- Minimizing series/parallel parasitic inductances of the PC path
- Using a low ESR 47 µF Tantalum V_{OUT} filtering capacitor with a 470 nF ceramic capacitor in parallel with the former (to reduce dynamic ESR)
- Inserting a 100-200 nH ferrite core on the V_{OUT}-to-tantalum capacitor wire

With this implementation, the ELDO simulated worst transient case shows no more than 90 mV deviation from the nominal line voltage value.

7 Die information

Figure 4. Die map



Note: Pad numbers reflect terminal numbers when placed in case FLAT-16.

7.1 Die bonding pad locations and electrical functions

Die physical dimensions:

Die size: 150 mils x 110 mils (3.81 mm by 2.79 mm)

Die thickness: 375 µm ± 25 µm (14.8 mils ± 1 mil)

Pad size: V_{IN}, V_{OUT} pads: 450 µm x 330 µm (17.7 mils by 13 mils)

Control pads: 184 µm x 184 µm (7.25 mils square)

Interface materials:

Top metallization: Al/Si/Cu, 1.05 µm ± 0.15 µm

Backside metallization: none

Glassivation:

Type: p. vapox + nitride

Thickness: 0.6 µm ± 0.1 µm + 0.6 µm ± 0.08 µm

Substrate: bare silicon

Assembly related information:

Substrate potential: floating recommended to be tied to ground

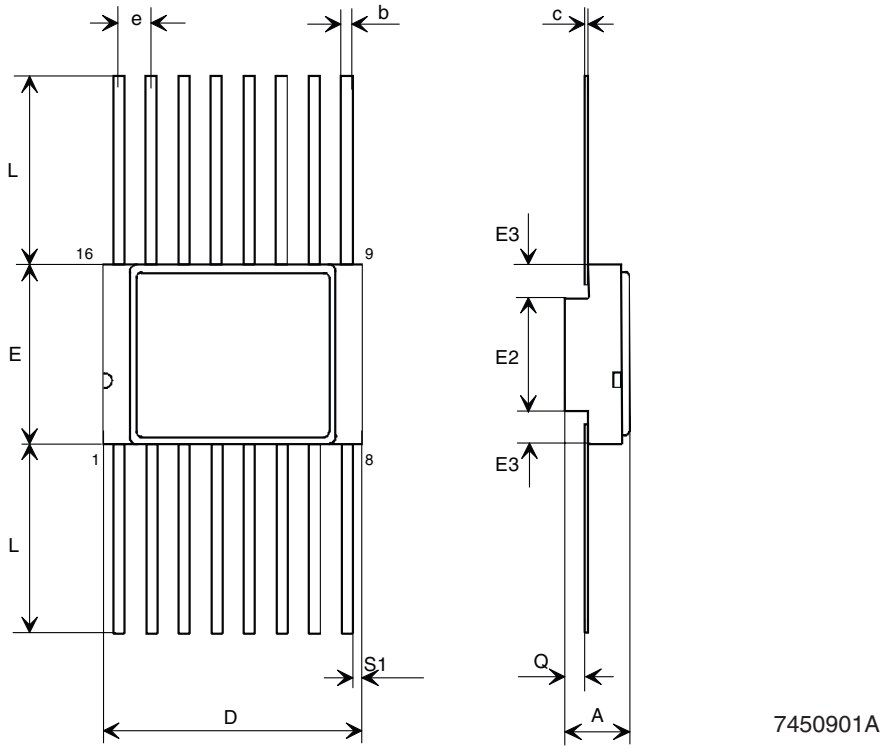
Special assembly instructions: "Sense" pad not used; not internally connected to any part of the IC. Can be connected to ground when space anti-static electricity rules apply.

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

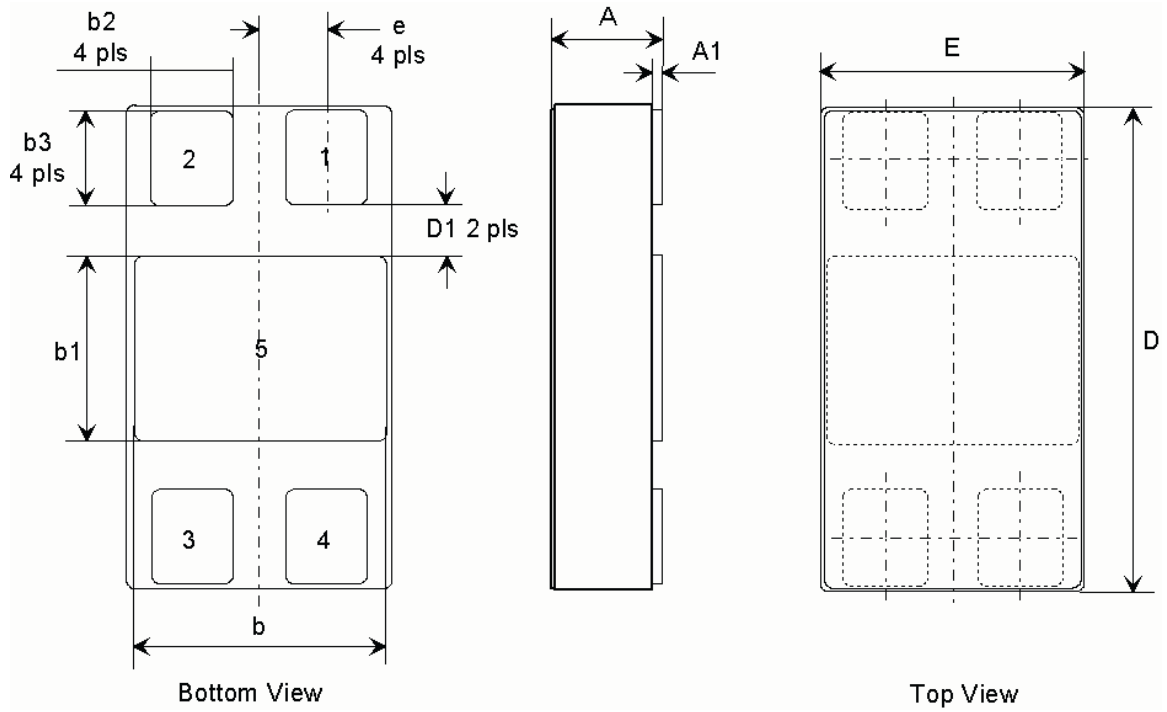
FLAT-16 (MIL-STD-1835) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.16		2.72	0.085		0.107
b		0.43			0.017	
c		0.13			0.005	
D		9.91			0.390	
E		6.91			0.272	
E2		4.32			0.170	
E3	0.76			0.030		
e		1.27			0.050	
L		6.72			0.265	
Q	0.66		1.14	0.026		0.045
S1	0.13			0.005		



SMD5C mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.84	3.00	3.15	0.112	0.118	0.124
A1	0.25	0.38	0.51	0.010	0.015	0.020
b	7.13	7.26	7.39	0.281	0.286	0.291
b1	4.95	5.08	5.21	0.195	0.200	0.205
b2	2.28	2.41	2.54	0.090	0.095	0.100
b3	2.92	3.05	3.18	0.115	0.120	0.125
D	13.71	13.84	13.97	0.540	0.545	0.550
D1	0.76			0.030		
E	7.39	7.52	7.65	0.291	0.296	0.301
e		1.91			0.075	



9 Packaging

The RHFL4913A adjustable voltage regulator is available in a high thermal dissipation 16-pin hermetic Flat package, the bottom flange of which is metallized to allow direct soldering to a heat sink (efficient thermal conductivity). The device is also available in the SMD5C hermetic ceramic package.

10 Ordering information

Table 5. Order codes

Die	FLAT-16	SMD5C	Terminal finish	Output voltage	Quality level
	RHFL4913KPA-01V	RHFL49143SCA-07V	Gold	Adj	QML-V
	RHFL4913KPA-02V		Solder	Adj	QML-V
	RHFL4913KPA1	RHFL4913SCA1	Gold	Adj	EM1
	RHFL4913KPA2	RHFL4913SCA2	Gold	Adj	EM2=EM1+48hours B.I.
L4913ADIE2V				Adj	QML-V die
L4913ADIES				Adj	EM1 die

Table 6. Part numbers - SMD equivalent

ST part number	SMD part number
RHFL4913KPA-01V	5962F0252401VXC
RHFL4913KPA-02V	5962F0252401VXA
RHFL4913SCA-07V	5962F0252403VUC
L4913ADIE2V	5962F0252401V9A

Table 7. Environmental characteristics

Parameter	Conditions	Value	Unit
Output voltage thermal drift	-55°C to +125°C	40	ppm/°C
Output voltage radiation drift	From 0 krad to 300 krad at 0.55 rad/s	8	ppm/krad
Output voltage radiation drift	From 0 krad to 300 krad, Mil Std 883E Method 1019.6	6	ppm/krad

11 Revision history

Table 8. Document revision history

Date	Revision	Changes
29-Oct-2004	3	New order codes added - Tables 4 and 5.
27-May-2005	4	Features, Tables 4, 5 and the Figure 1 has been updated. Add the Mechanical Data SOC-16.
08-Jun-2005	5	Mistake on Table 4 (Q.ty Level), Table 7 has been updated and add DIE Information.
30-Jan-2006	6	Added new package SMD5C and removed old package SOC-16.
26-Jan-2007	7	DIE Information and DIE Pad has been updated par. 6, pages 9 and 10.
23-Nov-2007	8	Pin information for the SMD5C package updated in *Table 1*; added section *6.3: FPGA power supply lines on page 11*. Minor text changes.
22-Sep-2008	9	Modified *Application information on page 10*.
17-Nov-2008	10	Modified *Table 6 on page 18*.
21-Jan-2010	11	Modified *Table 5 on page 18*.
18-Oct-2010	12	Modified *Section 6.1 on page 10*.
07-Feb-2011	13	Added: note *Table 1 on page 4*.
07-Dec-2011	14	Removed the note under *Table 1 on page 4* and added footnotes 1 and 2.

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