PM8803

High efficiency integrated IEEE 802.3at PoE-PD interface and PWM controller

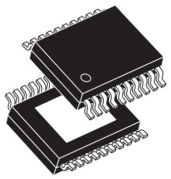
Data brief

Features

- IEEE 802.3at compliant PD interface
- Works with power supplied from Ethernet LAN cables or from local auxiliary sources
- Successful IEEE802.3at layer1 classification indicator
- Integrated 100 V, 0. 45 Ω, 1 A hot-swap MOSFET
- Accurate 140 mA typ. inrush current level
- Programmable classification current
- Support maintain power signature
- Programmable DC current limit up to 1 A
- Integrated high voltage start-up bias regulator
- Thermal shutdown protection
- Current mode pulse width modulator
- Programmable oscillator frequency
- 80% maximum duty cycle with internal slope compensation
- Support for flyback, forward, forward active clamp, flyback with synchronous rectification

Applications

- VoIP phones, WLAN AP
- WiMAX CPEs
- Security cameras
- PoE/PoE+ powered device appliances



HTSSOP20

Description

The PM8803 integrates a standard compliant Power over Ethernet (PoE) interface and a current mode PWM controller to simplify the design of the power supply sections of all powered devices.

The PoE/PoE+ interface incorporates all the functions required by the IEEE 802.3at including detection, classification, undervoltage lockout (UVLO) and inrush current limitation.

PM8803 specifically performs IEEE802.3at layer1 hardware classification scheme providing an indication of type 2 PSE successful detection to the rest of the system.

PM8803 has been designed to work with power either from the Ethernet cable or from an external power source such as wall adapter. Two possible connection are available, ensuring in one case prevalence of the auxiliary source wrt the PoE.

The DC/DC section of the PM8803 features a programmable oscillator frequency, an adjustable slope compensation, dual complementary low side drivers, programmable dead time and internal temperature sensor.

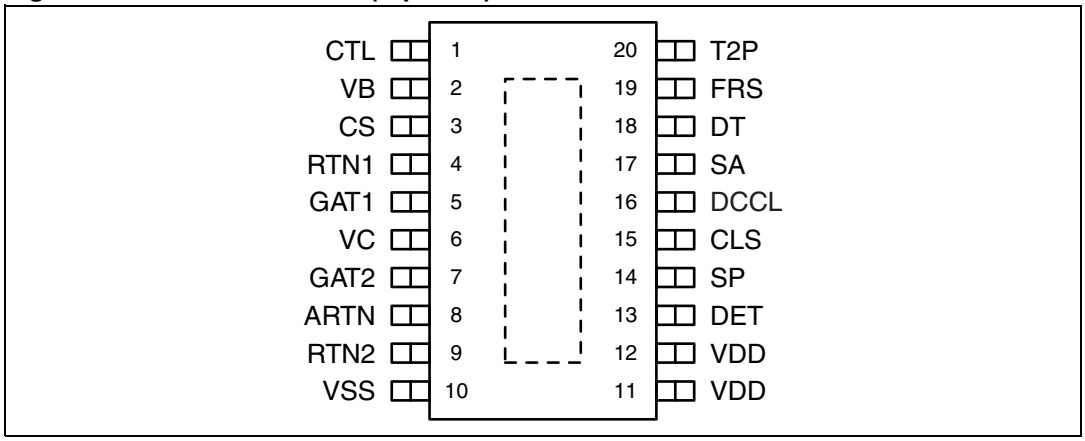
PM8803 targets high efficiency conversion at all load conditions supporting flyback, forward, forward active clamp and synchronous rectification.

Table 1. Device summary

Order codes	Package	Packing
PM8803	HTSSOP20	Tube
PM8803TR	HTSSOP20	Tape and Reel

1 Pins description and connection diagrams

Figure 1. Pins connection (top view)



1.1 Pin descriptions

Table 2. Pin description

Pin n°	Name	Function
1	CTL	Input of the pulse width modulator. CTL pull-up to VB is provided by an external resistor which may be used to bias an opto-coupler transistor.
2	VB	5V bias rail. This 10mA output; this reference voltage can be used to bias an opto-coupler transistor.
3	CS	Current sense input for current mode control and over-current protection. Current sensing is accomplished using a dedicated current sense comparator. If the CS pin voltage exceeds 0.5V the GAT1 pin switches low for cycle-by-cycle current limiting. CS is internally held low for 70ns after GAT1 switches high to blank leading edge current spikes.
4	RTN1	Power ground for the GAT1 driver. This pin must be connected to RTN2 and ARTN.
5	GAT1	Main gate drive output of the PWM controller. DC-DC converter gate driver output with 1A peak sink-source current capability. (5Ω typ MOSFETs).
6	VC	Output of the internal high voltage regulator. When the auxiliary transformer winding (if used) raises the voltage on this pin above the regulation set point, the internal regulator will shutdown, reducing the controller power dissipation. Connect to ground with a 1 µF typ capacitor.
7	GAT2	Secondary gate drive output. AUX gate driver output for active clamp or synchronous rectification designs. 1A peak sink-source current capability (5Ω typ MOSFETs).
8	ARTN	Analog PWM supply ground. RTN for sensitive analog circuitry including the SMPS current limit amplifier.

Table 2. Pin description (continued)

Pin n°	Name	Function
9	RTN2	Power ground for the secondary gate driver. This pin is also connected to the drain of the internal current limiting power MOSFET which closes VSS to the return path of the dc-dc converter. This pin must be connected to RTN1 and ARTN
10	VSS	System low potential input. Diode “OR” to the RJ45 connector and PSE's -48V supply, it is the more negative input potential.
11	VDD	System high potential input. The diode “OR” of several lines entering the PD, it is the most positive input potential.
12	VDD	System high potential input. The diode “OR” of several lines entering the PD, it is the most positive input potential.
13	DET	Detection resistor. Connect the signature resistance between DET pin and VDD. Current will flow through the resistor only during the detection phase. This pin is 100V rated with negligible resistance with respect to the external 25kΩ.
14	SP	Front auxiliary startup pin Pulling up this pin to the auxiliary source will change the internal UVLO settings and allow PD to be powered with voltage lower than nominal PoE voltages. Default Inrush and DC current protection are active. Use a resistor voltage divider from the auxiliary voltage to VSS to connect this low voltage rating pin
15	CLS	Classification resistor pin. Connect the classification programming resistor from this pin to VSS.
16	DCCL	DC current limit. A resistor between this pin and VSS will set the current limit for the interface section of PM8803. It can be set to exceed the IEEE802.3at current limit. Leave the pin open for standard IEEE 802.3at applications.
17	SA	Rear auxiliary startup pin. Pulling up this pin will give high priority to an auxiliary power source like an external wall adapter. Use a resistor voltage divider from the auxiliary voltage to ARTN to connect this low voltage rating pin.
18	DT	Delay time set. A resistor connected from this pin to ARTN sets the delay time between GAT1 and GAT2.
19	FRS	Switching frequency set. An external resistor connected from FRS to ARTN sets the oscillator frequency.
20	T2P	Layer 1 hardware classification OK. T2P open drain signal assertion happens when powered by a PSE performing 2-events classification. The T2P is an active low signal.
	EP	Exposed pad. Connect this to a board plane to improve heat dissipation; must be electrically connected to VSS.

2 Package mechanical data

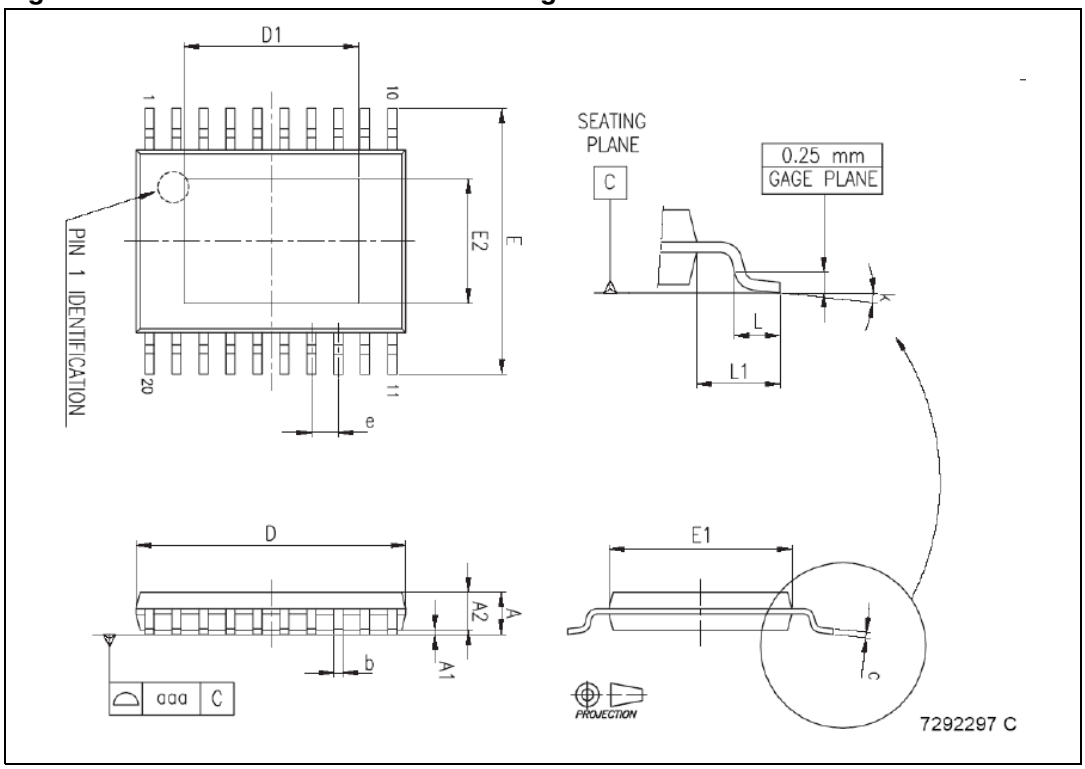
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 3. HTSSOP20 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.2
A1			0.15
A2	0.8	1	1.05
b	0.19		0.3
c	0.09		0.2
D (1)	6.4	6.5	6.6
D1 (2)	2.2		
E	6.2	6.4	6.6
E1 (3)	4.3	4.4	4.5
E2 (2)	1.5		
e		0.65	
L	0.45	0.6	0.75
L1		1	
k	0° min., 8° max.		
aaa			0.100

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
2. The size of exposed pad is variable depending of leadframe design pad size. End user should verify “D1” and “E2” dimensions for each device application.
3. Dimension “E1” does not include interlead flash or protrusions. Intelead flash or protrusions shall not exceed 0.25 mm per side.

Figure 2. HTSSOP20 mechanical drawing



3 Revision history

Table 4. Document revision history

Date	Revision	Changes
23-Nov-2009	1	Initial release

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