M95160-145

Automotive 16-Kbit serial SPI bus EEPROM with high-speed clock

Features

- Compatible with SPI bus serial interface (positive clock SPI modes)
- Extended operating temperature range:
  - Device grade 4: –40 °C to +145 °C
- Single supply voltage:
  - 2.5 V to 5.5 V
- High speed: 5 MHz
- Status Register
- Hardware protection of the Status Register
- Byte and page write (up to 32 bytes)
- Self-timed programming cycle
- Adjustable size read-only EEPROM area
- Enhanced ESD protection
- More than 1 million write cycles
- More than 40-year data retention
- Package
  - RoHS compliant and halogen-free (ECOPACK2®)

TSSOP8 (DW)
169 mil width

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1 Description

The M95160-145 is an EEPROM (Electrically Erasable PROgrammable Memory) accessed by a high-speed SPI bus.

The memory array is organized as 2048 × 8 bits.

The M95160-145 is the first EEPROM device in a TSSOP package qualified at 145 °C.

The M95160-145 device is designed to be compliant with the very high level of reliability defined by the Automotive standard AEC-Q100 grade 0.

Figure 1. Logic diagram

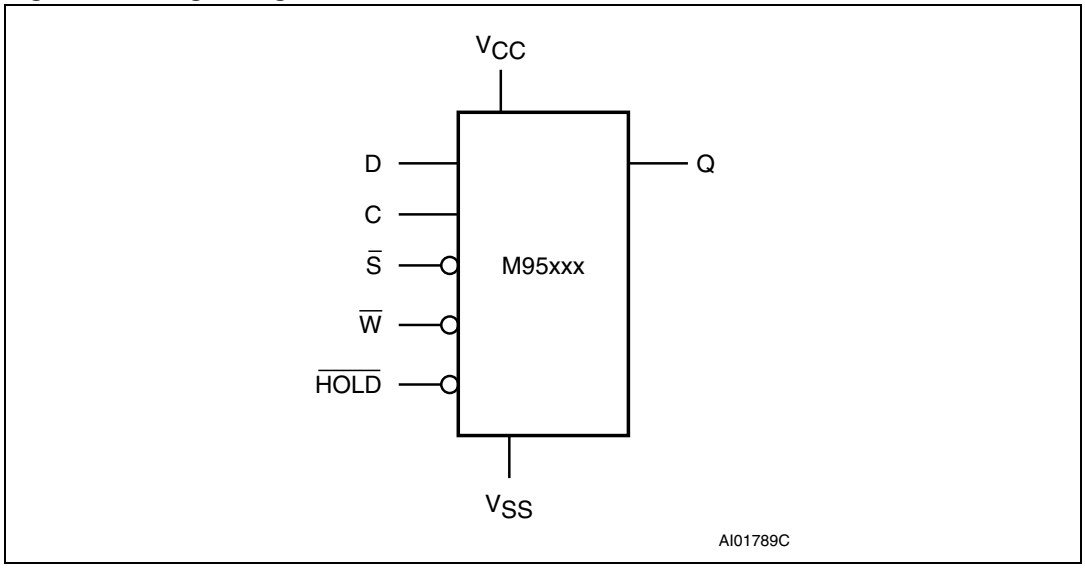
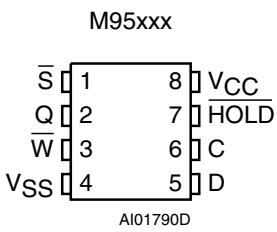


Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data input	Input
Q	Serial Data output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. TSSOP8-lead package connections (top view)



1. See *Package mechanical data* section for package dimensions, and how to identify pin-1.

2 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Table 10*. These signals are described next.

2.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Write cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

2.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either high or low, and must be stable during all write instructions.

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

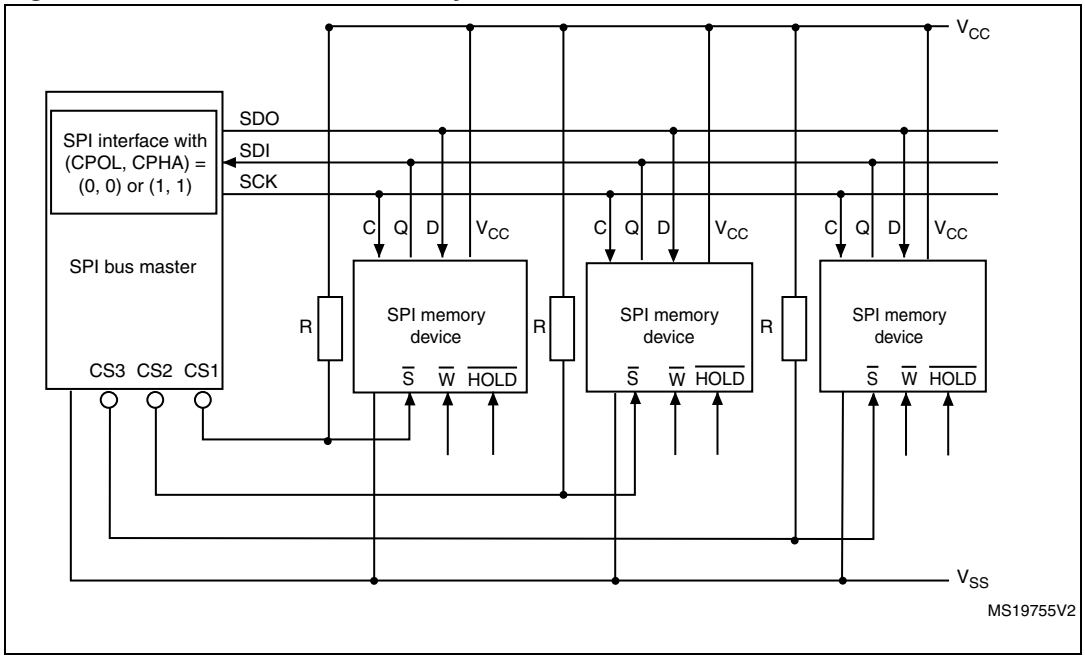
2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

3 Implementing devices on the SPI bus

Figure 3 shows an example of three devices, connected to the SPI bus master. Only one device is selected at a time, so that only the selected device drives the Serial Data output (Q) line. All the other devices outputs are then in high impedance.

Figure 3. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals must be driven high or low as appropriate.

A pull-up resistor connected on each $\overline{S}$ input (represented in *Figure 3*) ensures that each device is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state.

3.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

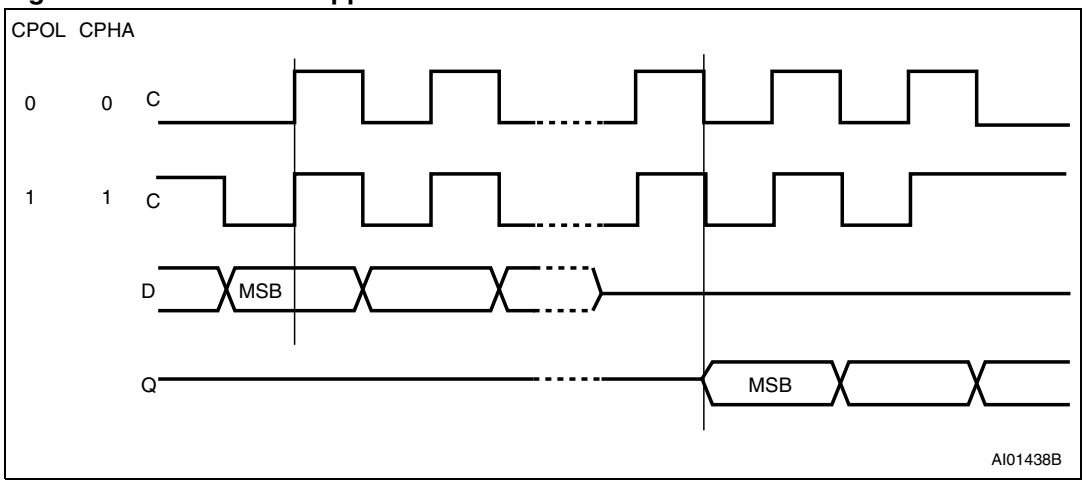
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 4*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 4. SPI modes supported



4 Operating features

4.1 Supply voltage (V_{CC})

4.1.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 8*). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

4.1.2 Device reset

In order to prevent inadvertent write operations during power-up, a power on reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches the internal reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 8*).

When V_{CC} passes over the POR threshold, the device is reset and in the following state:

- in Standby Power mode
- deselected (note that, to be executed, an instruction must be preceded by a falling edge on Chip Select ($\overline{S}$))
- Status Register value:
  - the Write Enable Latch (WEL) is reset to 0
  - Write In Progress (WIP) is reset to 0
  - The SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits)

When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode. The device must not be accessed until V_{CC} reaches a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range defined in *Table 8*.

4.1.3 Power-up conditions

When the power supply is turned on, V_{CC} rises continuously from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage, it is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see *Figure 3*).

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge-sensitive as well as level-sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 8* and the rise time must not vary faster than 1 V/µs.

4.1.4 Power-down

During power-down (continuous decrease of V_{CC} below the minimum V_{CC} operating voltage defined in *Table 8*), the device must be:

- deselected (Chip Select $\overline{S}$ should be allowed to follow the voltage applied on V_{CC})
- in Standby Power mode (there should not be any internal write cycle in progress).

4.2 Active Power and Standby Power modes

When Chip Select ($\overline{S}$) is low, the device is selected, and in the Active Power mode. The device consumes I_{CC}, as specified in *Table 10*.

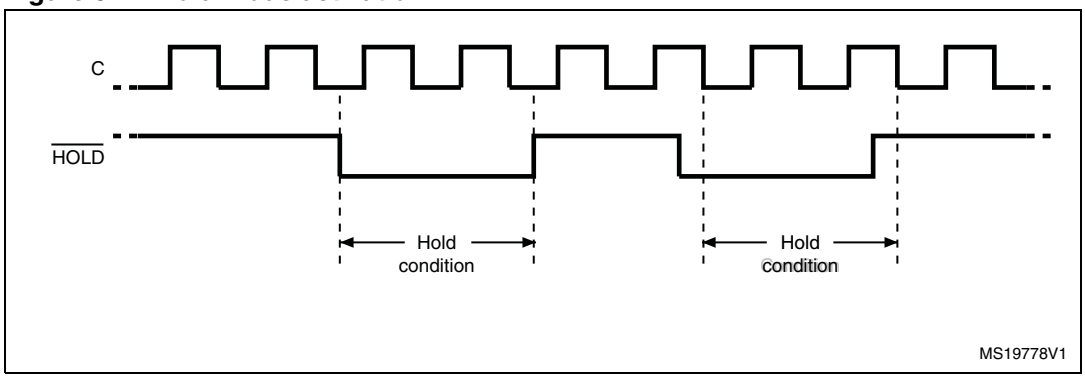
When Chip Select ($\overline{S}$) is high, the device is deselected. If a Write cycle is not currently in progress, the device then goes into the Standby Power mode, and the device consumption drops to I_{CC1}.

4.3 Hold condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

The Hold mode starts when the Hold (HOLD) signal is driven low and the Serial Clock (C) is low (as shown in *Figure 5*). During the Hold mode, the Serial Data output (Q) is high impedance, and Serial Data input (D) and Serial Clock (C) are Don't Care. The Hold mode ends when the Hold (HOLD) signal is driven high and the Serial Clock (C) is or becomes low.

Figure 5. Hold mode activation



Deselecting the device while it is in Hold mode resets the paused communication.

4.4 Status Register

Figure 6. shows the position of the Status Register in the control logic of the device. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See *Section 6.3: Read Status Register (RDSR)* for a detailed description of the Status Register bits

4.5 Data protection and protocol control

Non-volatile memory devices can be used in environments that are particularly noisy, and within applications that could experience problems if memory bytes are corrupted. Consequently, the device features the following data protection mechanisms:

- Write and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Write (WRITE) instruction completion
- The Block Protect (BP1, BP0) bits in the Status Register allow part of the memory to be configured as read-only.
- The Write Protect ($\overline{W}$) signal allows the Block Protect (BP1, BP0) bits of the Status Register to be protected.

For any instruction to be accepted, and executed, Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).

Two points need to be noted in the previous sentence:

- The “last bit of the instruction” can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The “next rising edge of Serial Clock (C)” might (or might not) be the next bus transaction for some other device on the SPI bus.

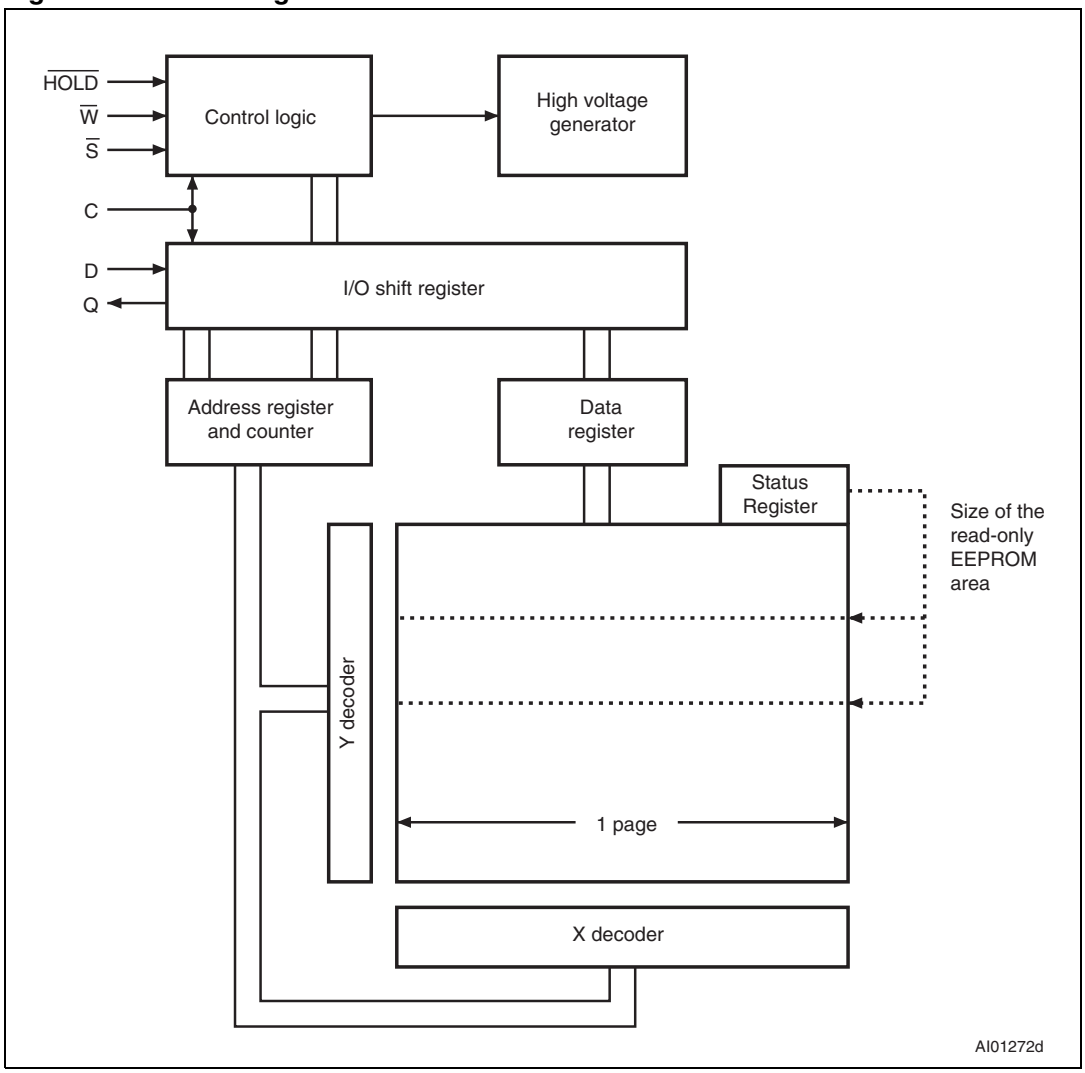
Table 2. Write-protected block size

Status Register bits		Protected block	Protected array addresses
BP1	BP0		
0	0	none	none
0	1	Upper quarter	0600h - 07FFh
1	0	Upper half	0400h - 07FFh
1	1	Whole memory	0000h - 07FFh

5 Memory organization

The memory is organized as shown in *Figure 6.*

Figure 6. Block diagram



6 Instructions

Each instruction starts with a single-byte code, as summarized in *Table 3.*

If an invalid instruction is sent (one not contained in *Table 3.*), the device automatically deselects itself.

Table 3. Instruction set

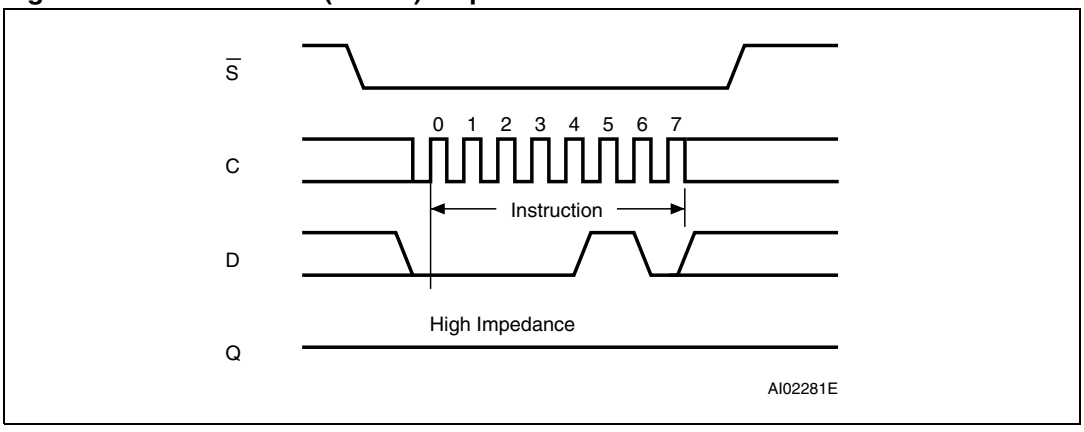
Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 7.*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 7. Write Enable (WREN) sequence



6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

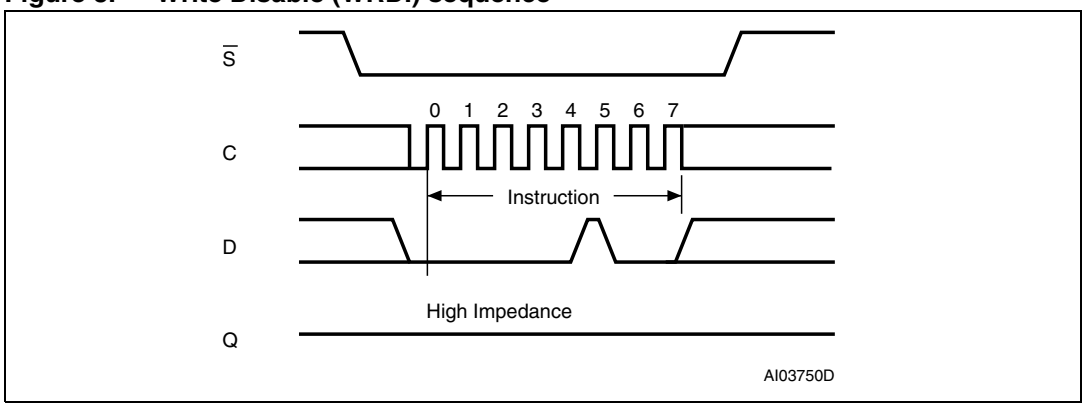
As shown in *Figure 8.*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

Figure 8. Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 9.*

The status and control bits of the Status Register are as follows:

6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 4.*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

6.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 4. Status Register format

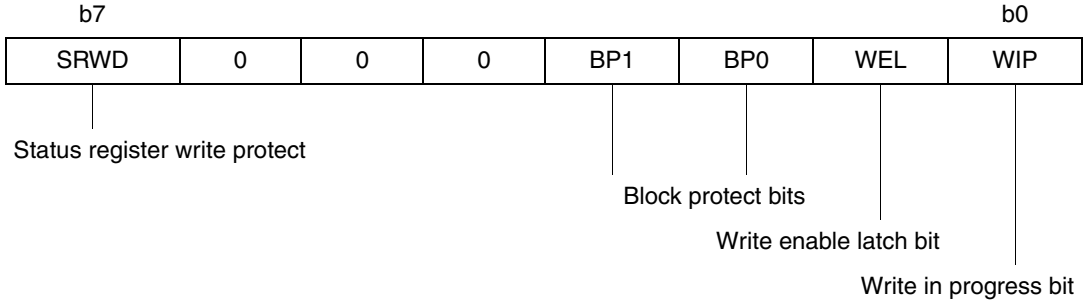
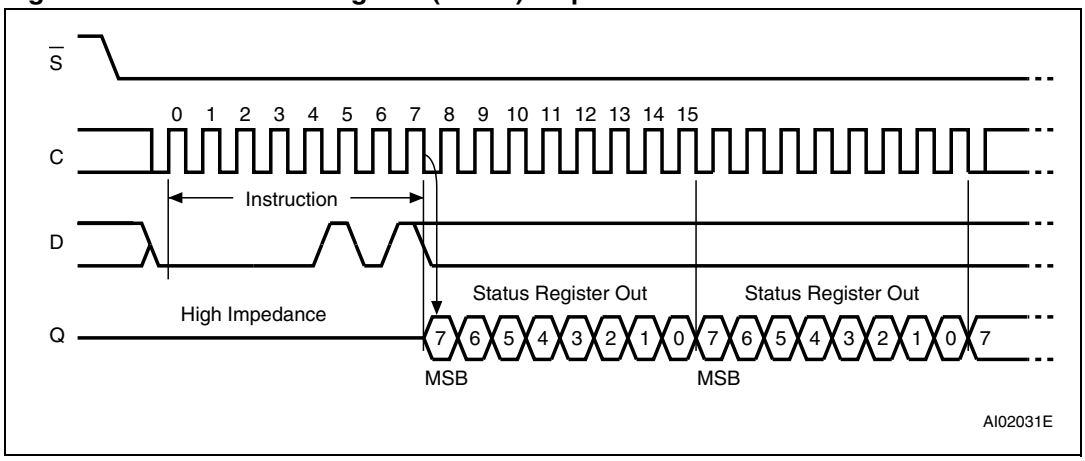


Figure 9. Read Status Register (RDSR) sequence



6.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must have been previously executed.

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) low, followed by the instruction code, the data byte on Serial Data input (D) and the Chip Select ($\overline{S}$) driven high. Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not executed.

Driving the Chip Select ($\overline{S}$) signal high at a byte boundary of the input data triggers the self-timed write cycle that takes t_W to complete (as specified in *Table 12*).

The instruction sequence is shown in *Figure 10*.

While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit: the WIP bit is 1 during the self-timed write cycle t_W, and is 0 when the write cycle is complete. The WEL bit (Write Enable Latch) is also reset at the end of the write cycle t_W.

The Write Status Register (WRSR) instruction allows the user to change the values of the BP1, BP0 bits and the SRWD bit:

- The Block Protect (BP1, BP0) bits define the size of the area that is to be treated as read only, as defined in *Table 5*.
- The SRWD bit (Status Register Write Disable bit), in accordance with the signal read on the Write Protect pin ($\overline{W}$), allows the user to set or reset the write protection mode of the Status Register itself. When in Write-protected mode, the Write Status Register (WRSR) instruction is not executed.

The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the t_W Write cycle.

The Write Status Register (WRSR) instruction has no effect on bits b6, b5, b4, b1, b0 of the Status Register. Bits b6, b5, b4 are always read as 0.

Table 5. Protection modes

$\overline{W}$ signal	SRWD bit	Mode	Write protection of the Status Register	Memory content	
				Protected area(1)	Unprotected area(1)
1	0	Software-protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit) The values in the BP1 and BP0 bits can be changed	Write-protected	Ready to accept Write instructions
0	0				
1	1				
0	1	Hardware-protected (HPM)	Status Register is Hardware write protected The values in the BP1 and BP0 bits cannot be changed	Write-protected	Ready to accept Write instructions

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register, as shown in *Table 4*.

The protection features of the device are summarized in *Table 2.*

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of whether Write Protect ($\overline{W}$) is driven high or low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect ($\overline{W}$):

- If Write Protect ($\overline{W}$) is driven high, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.
- If Write Protect ($\overline{W}$) is driven low, it is *not* possible to write to the Status Register *even* if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

- by setting the Status Register Write Disable (SRWD) bit after driving Write Protect ($\overline{W}$) low
- or by driving Write Protect ($\overline{W}$) low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered is to pull Write Protect ($\overline{W}$) high.

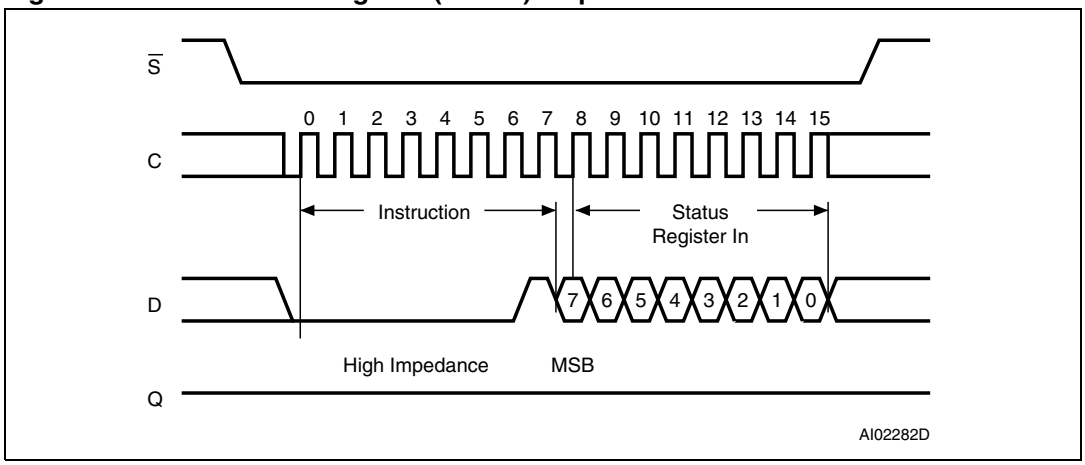
If Write Protect ($\overline{W}$) is permanently tied high, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the Block Protect (BP1, BP0) bits of the Status Register, can be used.

Table 6. Address range bits(1)

Device	M95160-145
Address bits	A10-A0

1. b15 to b11 are Don't Care.

Figure 10. Write Status Register (WRSR) sequence



6.5 Read from Memory Array (READ)

As shown in *Figure 11.*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

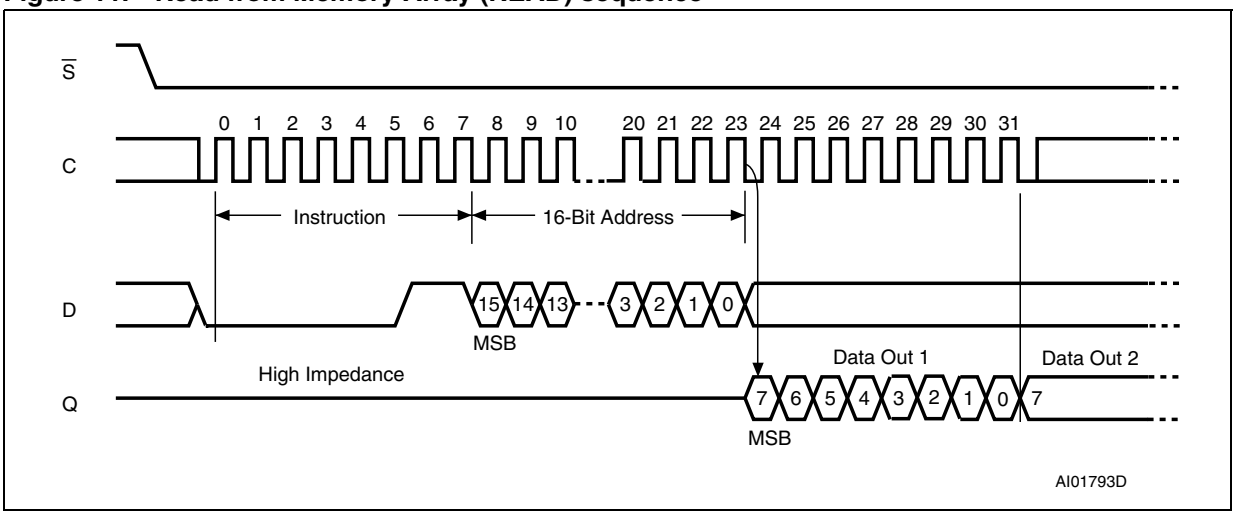
When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Figure 11. Read from Memory Array (READ) sequence



1. Depending on the memory size, as shown in *Table 6.*, the most significant address bits are Don't Care.

6.6 Write to Memory Array (WRITE)

As shown in *Figure 12.*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. The self-timed Write cycle, triggered by the Chip Select ($\overline{S}$) rising edge, continues for a period t_W (as specified in *Table 12*), at the end of which the Write in Progress (WIP) bit is reset to 0.

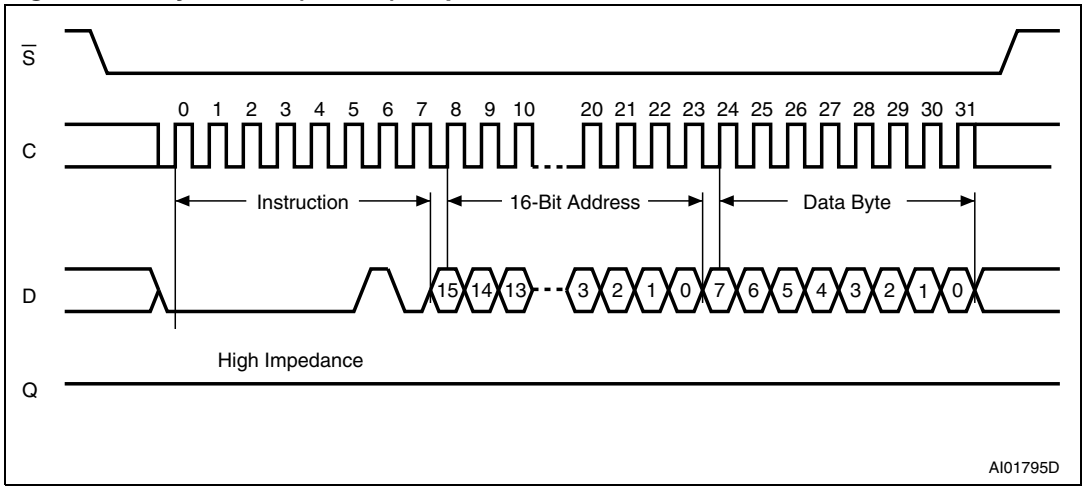
In the case of *Figure 12.*, Chip Select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. If, though, Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 13.*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size of these devices is 32 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

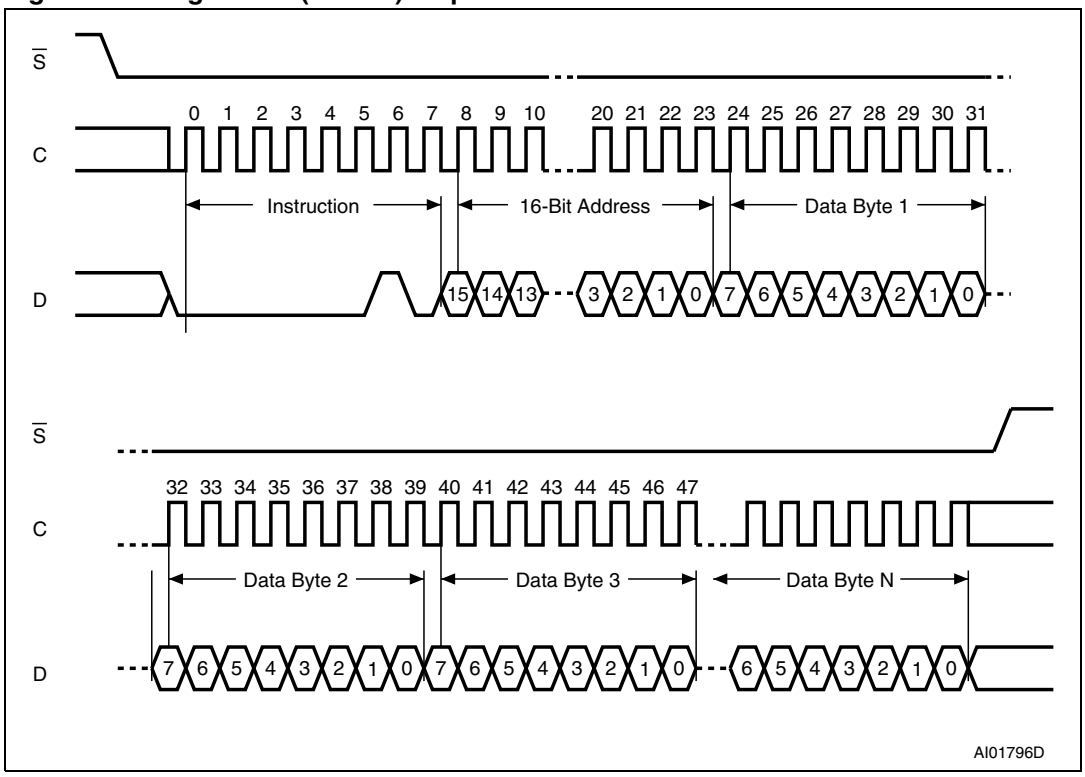
- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a Write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in)
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Figure 12. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 6.*, the most significant address bits are Don't Care.

Figure 13. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 6.*, the most significant address bits are Don't Care.

7 Delivery state

7.1 Initial delivery state

The device is delivered with the memory array set at all 1s (FFh). The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.

8 Absolute maximum ratings

Stressing the device outside the ratings listed in *Table 7* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	–65	150	°C
T_{AMR}	Ambient operating temperature	–40	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_O	Voltage on Q pin	–0.50	V_{CC}+0.6	V
V_I	Input voltage	–0.50	6.5	V
I_{OL}	DC output current (Q = 0)		5	mA
I_{OH}	DC output current (Q = 1)		–5	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body Model)(2)		4000	V

1. Compliant with JEDEC Std J-STD-020 (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU
2. Positive and negative pulses applied on pin pairs, in accordance with AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω, R2=500 Ω)

9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the dc and ac characteristics of the device. The parameters in the dc and ac characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 4)	–40	145	°C

Table 9. AC measurement conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_L	Load capacitance	30 or 100			pF
	Input rise and fall times			50	ns
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$			V
	Input and output(1) timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$			V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 14. AC measurement I/O waveform

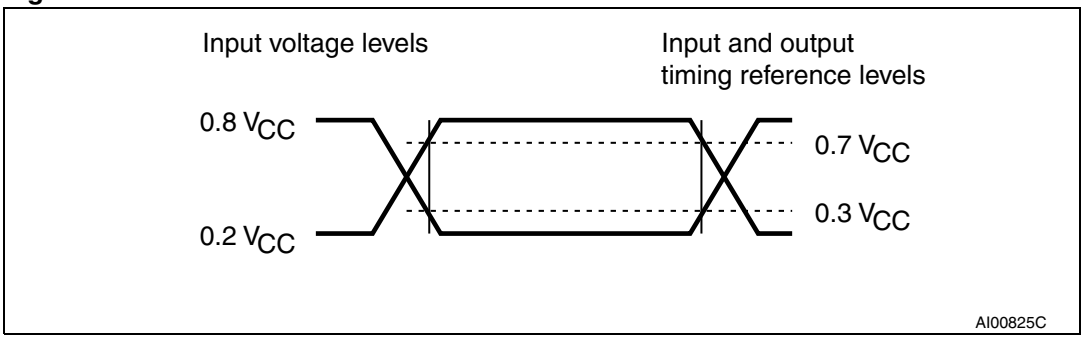


Table 10. Capacitance(1)

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (D)	V_{IN} = 0 V		8	pF
	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 5 MHz.

Table 11. DC characteristics(1)

Symbol	Parameter	Test conditions (in addition to those specified in *Table 8*, *Table 9* and *Table 10*)	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 2.5 V, Q = open		2	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 2.5 V, $V_{IN} = V_{SS}$ or V_{CC}		10	µA
		$\overline{S} = V_{CC}$, V_{CC} = 5.5 V, $V_{IN} = V_{SS}$ or V_{CC}		10	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}		V

1. Preliminary data.

Table 12. AC characteristics

Test conditions specified in *Table 8*, *Table 9* and *Table 10*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60		ns
t_{CHSL}		$\overline{S}$ not active hold time	60		ns
t_{CH}(1)	t_{CLH}	Clock high time	75		ns
t_{CL}(1)	t_{CLL}	Clock low time	75		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		1	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		1	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	20		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	60		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	60		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		80	ns
t_{CLQV}(3)	t_V	Clock low to output valid (C_L = 30 pF)		55	ns
		Clock low to output valid (C_L = 100 pF)		80	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		80	ns
t_{QHQL}(2)	t_{FO}	Output fall time		80	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		80	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		80	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max). See also *Note 3*.
2. Value guaranteed by characterization, not 100% tested in production.
3. t_{CLQV} must be compatible with t_{CL} (clock low time): if the SPI bus master offers a Read setup time t_{SU} = 0 ns, t_{CL} can be equal to (or greater than) t_{CLQV}; in all other cases, t_{CL} must be equal to (or greater than) $t_{CLQV}+t_{SU}$.

Figure 15. Serial input timing

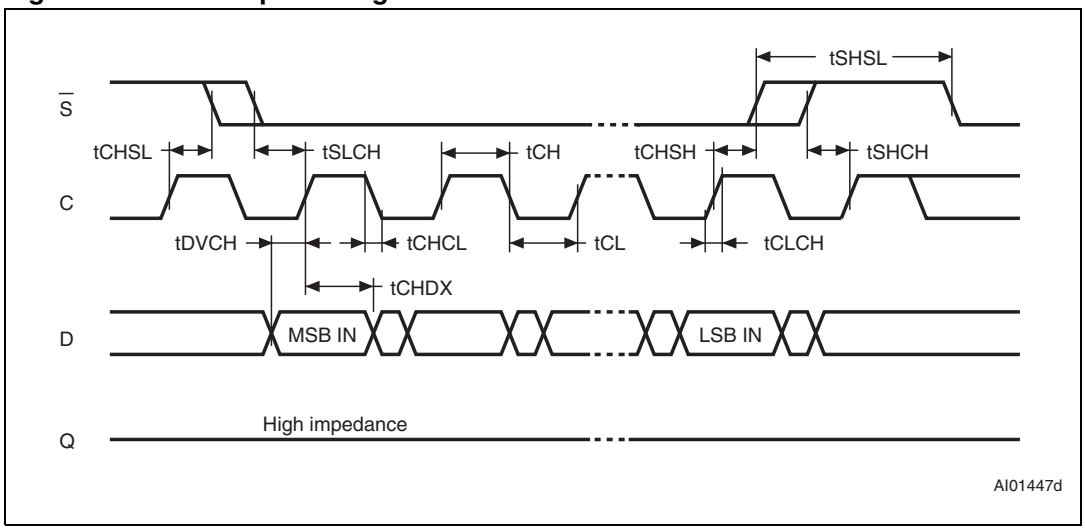


Figure 16. Hold timing

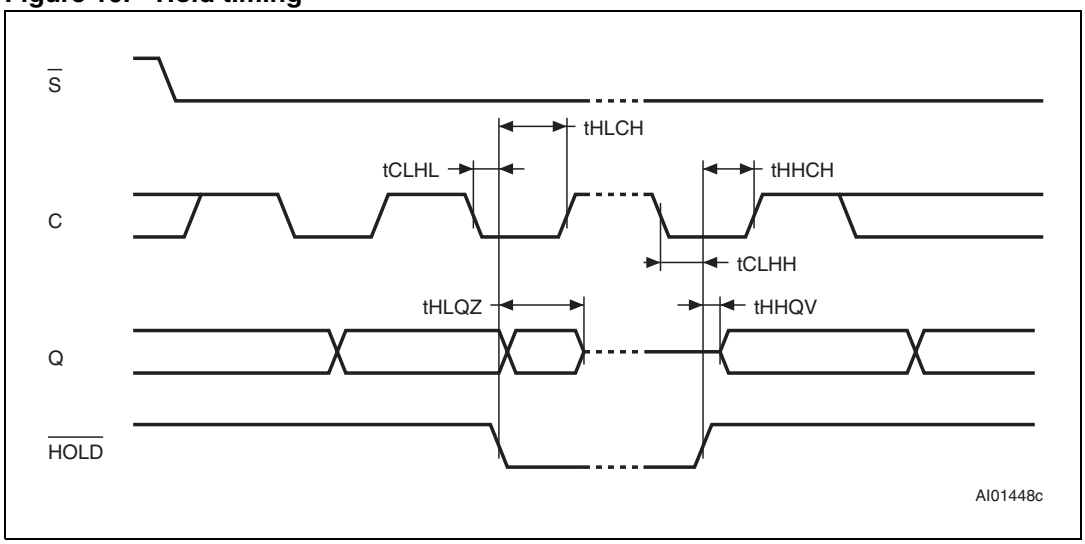
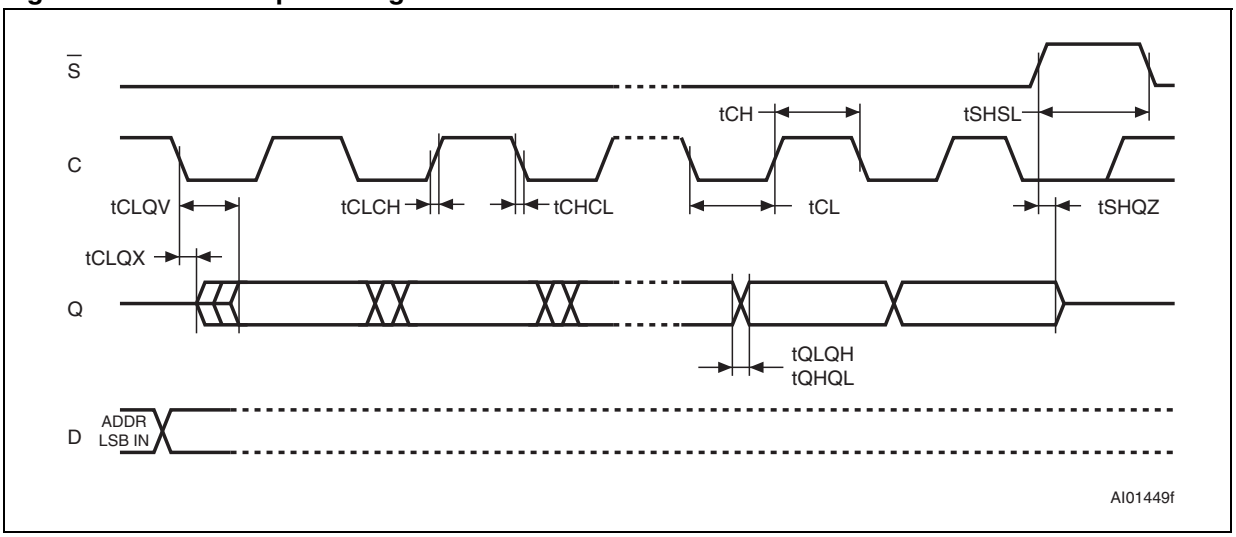


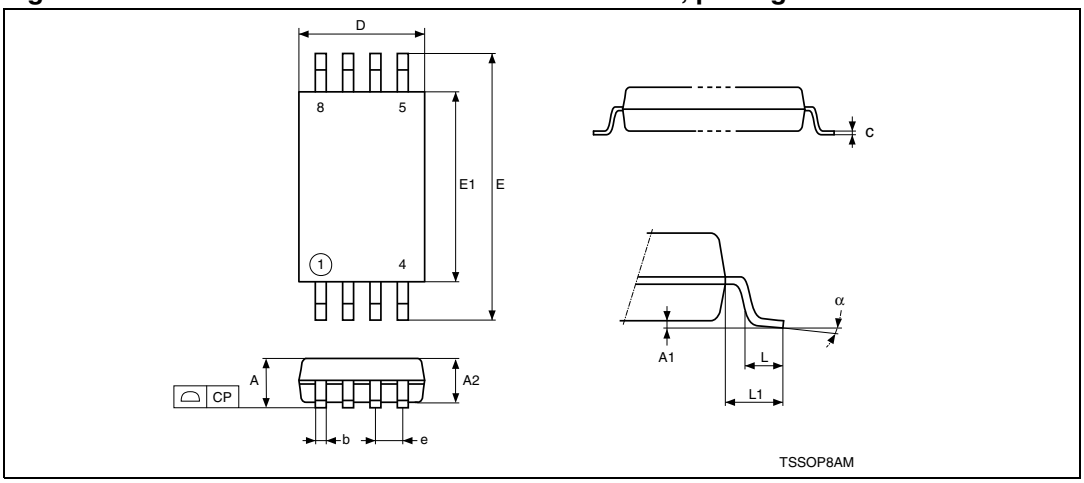
Figure 17. Serial output timing



10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 18. TSSOP8 – 8-lead thin shrink small outline, package outline



1. Drawing is not to scale.

Table 13. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.2			0.0472
A1		0.05	0.15		0.002	0.0059
A2	1	0.8	1.05	0.0394	0.0315	0.0413
b		0.19	0.3		0.0075	0.0118
c		0.09	0.2		0.0035	0.0079
CP			0.1			0.0039
D	3	2.9	3.1	0.1181	0.1142	0.122
e	0.65	-	-	0.0256	-	-
E	6.4	6.2	6.6	0.252	0.2441	0.2598
E1	4.4	4.3	4.5	0.1732	0.1693	0.1772
L	0.6	0.45	0.75	0.0236	0.0177	0.0295
L1	1			0.0394		
α		0°	8°		0°	8°
N (number of leads)	8			8		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

11 Part numbering

Table 14. Ordering information scheme

Example: M95160 – W DW 4 T P /SC

Device type
M95 = SPI serial access EEPROM

Device function
160 = 16 Kbit (2048 × 8)

Operating voltage
W = V_{CC} = 2.5 to 5.5 V

Package
DW = TSSOP8

Device grade
4 = Device tested with high reliability certified flow(1).
Automotive temperature range (–40 to 145 °C)

Option
blank = Standard packing
T = Tape and reel packing

Plating technology
G or P = ECOPACK2® (RoHS compliant and halogen-free)

Process
/SC = F6SP36%

1. The high reliability certified flow (HRCF) is described in quality note QNEE9801. Please ask your nearest ST sales office for a copy.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

12 Revision history

Table 15. Document revision history

Date	Revision	Changes
28-Nov-2011	1	Initial release.

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