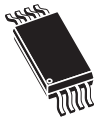
M24256-125

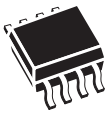
Automotive 256-Kbit serial I²C bus EEPROM

Features

- Compatible with all I²C bus modes:
  - 400 kHz Fast mode
  - 100 kHz Standard mode
- Memory array:
  - 256 Kbit (32 Kbytes) of EEPROM
  - Page size: 64 bytes
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Single supply voltage: 2.5 V to 5.5 V
- Operating temperature range: from -40 °C up to +125 °C
- Random and sequential Read modes
- Write protect of the whole memory array
- Enhanced ESD/Latch-Up protection
- More than 1 million Write cycles
- More than 40-year data retention
- Packages
  - RoHS compliant and halogen-free (ECOPACK®)



TSSOP8 (DW)
169 mil width



SO8 (MN)
150 mil width

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1 Description

The M24256 is a 256-Kbit I^2C-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 32 K × 8 bits.

This I^2C EEPROM can operate with a supply voltage from 2.5 V up to 5.5 V over an ambient temperature range of -40 °C / 125 °C.

The device is compliant with the Automotive standard AEC-Q100 grade 1.

Figure 1. Logic diagram

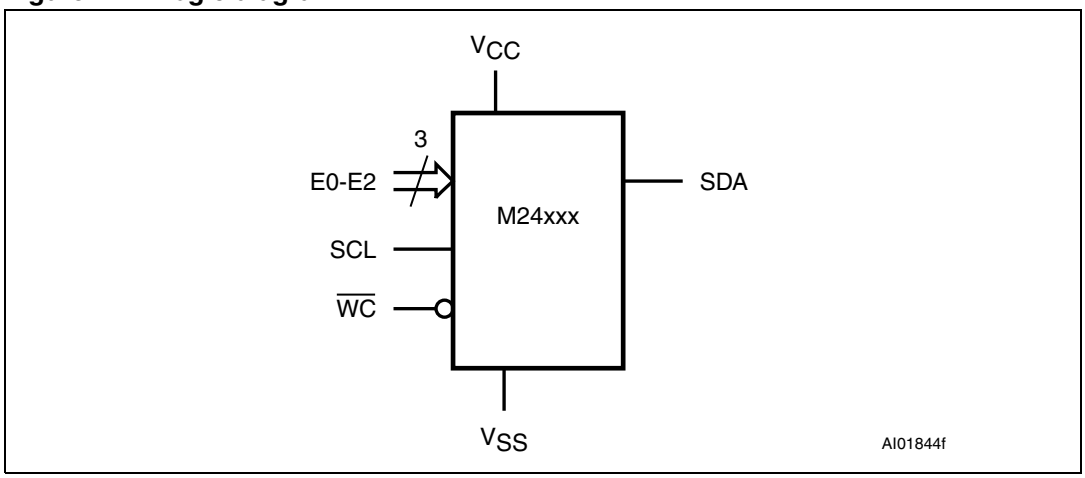
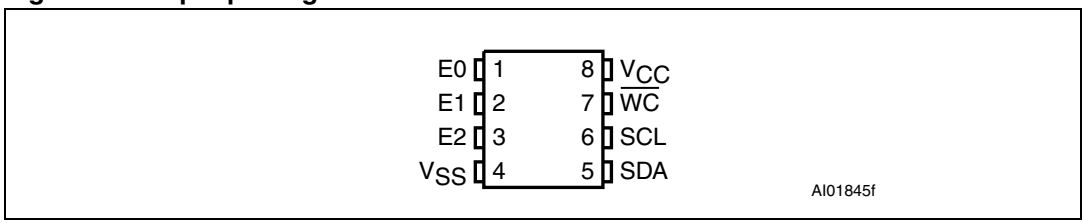


Table 1. Signal names

Signal name	Function	Direction
E2, E1, E0	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
WC	Write Control	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. 8-pin package connections



1. See *Section 9: Package mechanical data* for package dimensions, and how to identify pin 1.

2 Signal description

2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (*Figure 11* indicates how to calculate the value of the pull-up resistor). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

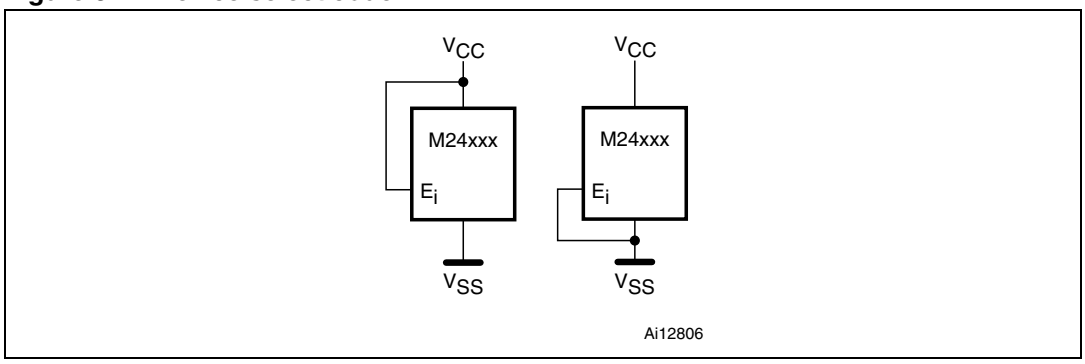
2.2 Serial Data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 11* indicates how to calculate the value of the pull-up resistor).

2.3 Chip Enable (E2, E1, E0)

(E2,E1,E0) input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code (see *Table 2*). These inputs must be tied to V_{CC} or V_{SS}, as shown in *Figure 3*. When not connected (left floating), these inputs are read as low (0).

Figure 3. Device select code



2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven high. Write operations are enabled when Write Control ($\overline{WC}$) is either driven low or left floating.

When Write Control ($\overline{WC}$) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in *Section 8: DC and AC parameters)*. In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters)* and the rise time must not vary faster than 1 V/µs.

2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see Operating conditions in *Section 8: DC and AC parameters*).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

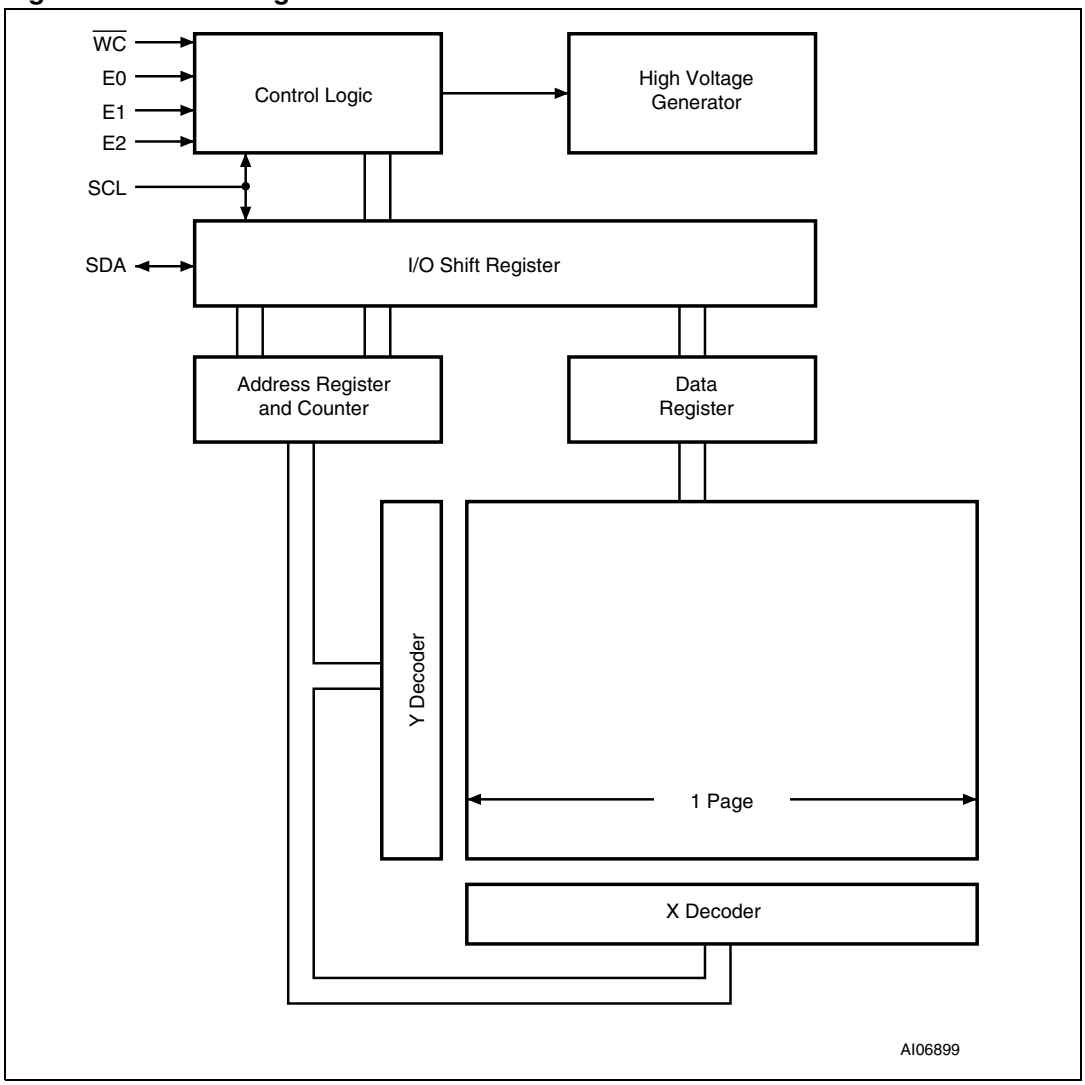
2.6.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that is there is no internal write cycle in progress).

3 Memory organization

The memory is organized as shown in *Figure 4*.

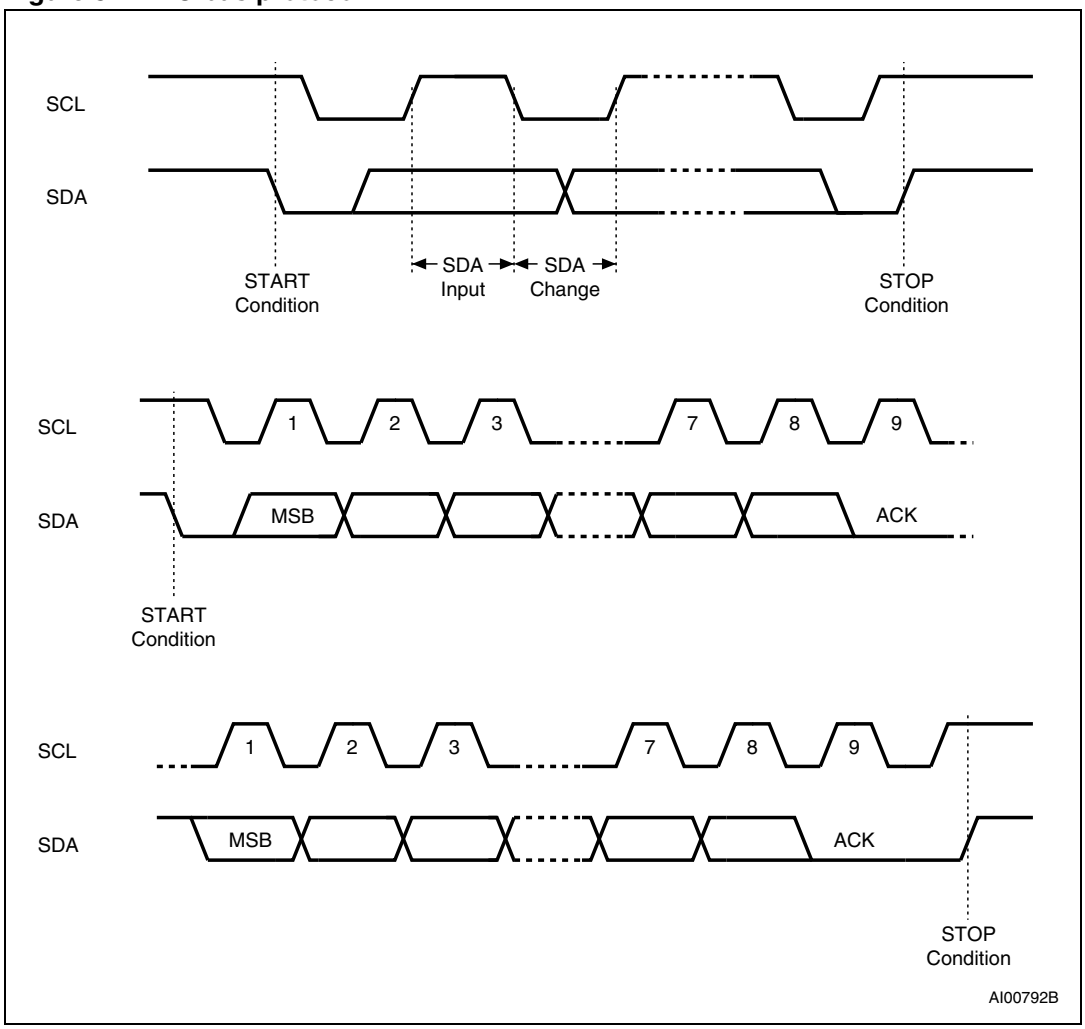
Figure 4. Block diagram



4 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 5*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 5. I^2C bus protocol



4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

4.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

4.4 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

4.5 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on Serial Data (SDA), most significant bit first).

Table 2. Device select code

Device type identifier(1)				Chip Enable address(2)			RW
b7	b6	b5	b4	b3	b2	b1	b0
1	0	1	0	E2	E1	E0	RW

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

The device select code consists of a 4-bit device type identifier 1010b, and a 3-bit Chip Enable address (E2, E1, E0). A device select code handling a value other than 1010b is not acknowledged by the device.

Up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on the Chip Enable (E2, E1, E0) inputs. When the device select code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E2, E1, E0) inputs.

The 8th bit is the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

Table 3. Operating modes

Mode	$\overline{\text{RW}}$ bit	$\overline{\text{WC}}$(1)	Bytes	Initial sequence
Current Address Read	1	X	1	Start, device select, $\overline{\text{RW}}$ = 1
Random Address Read	0	X	1	Start, device select, $\overline{\text{RW}}$ = 0, Address
	1	X		reStart, device select, $\overline{\text{RW}}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	Start, device select, $\overline{\text{RW}}$ = 0
Page Write	0	V_{IL}	≤ 64	Start, device select, $\overline{\text{RW}}$ = 0

1. X = V_{IH} or V_{IL}.

5 Instructions

5.1 Write operations

Following a Start condition the bus master sends a device select code with the R/$\overline{W}$ bit (R$\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 6*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Each byte location is defined by several address bits inside two address bytes. If the address bits are less than 16, the most significant bits (A15 and lower) are Don't Care. The most significant address byte (*Table 4*) is sent first, followed by the least significant address byte (*Table 5*).

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "10^{th} bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle t_W is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition and the successful completion of an internal Write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

If the Write Control input (WC) is driven High, the Write instruction is not executed and the accompanying data bytes are *not* acknowledged, as shown in *Figure 7*.

Table 4. Most significant address byte

A15	A14	A13	A12	A11	A10	A9	A8

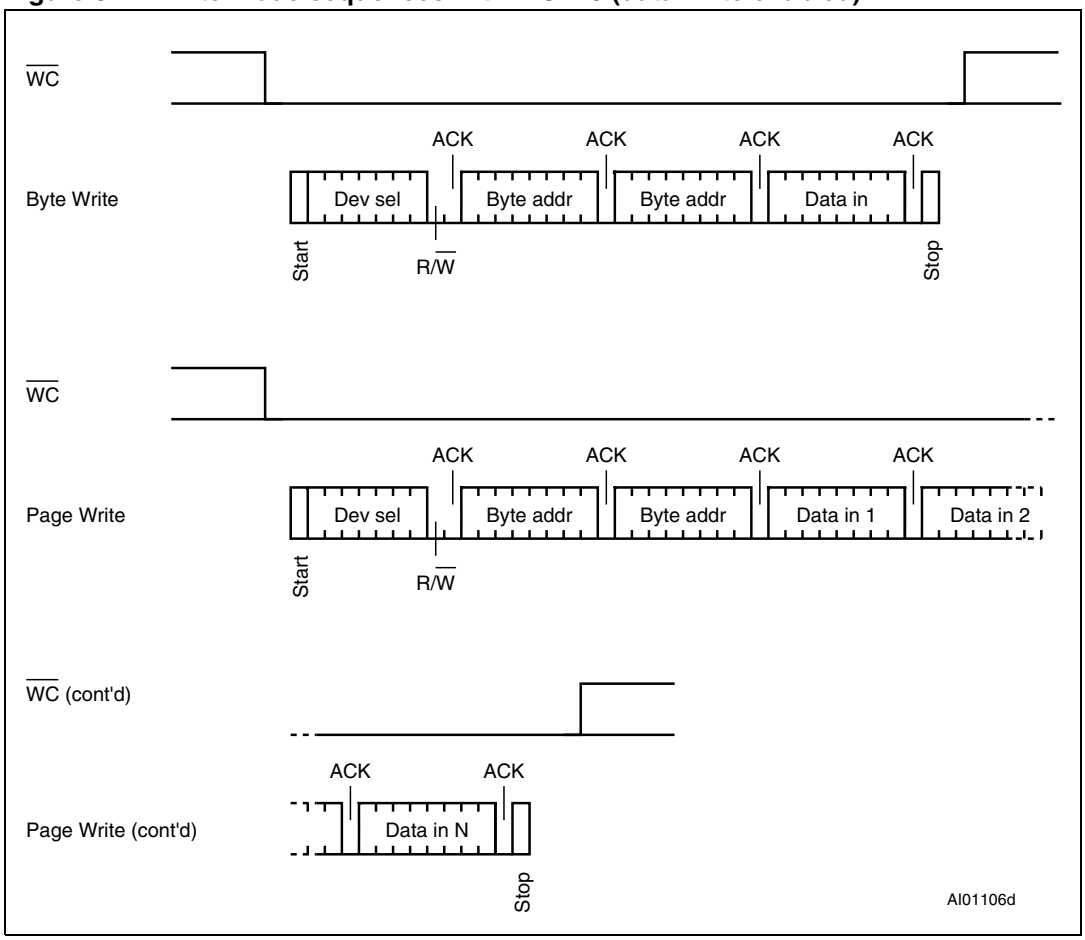
Table 5. Least significant address byte

A7	A6	A5	A4	A3	A2	A1	A0

5.1.1 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 6*.

Figure 6. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)

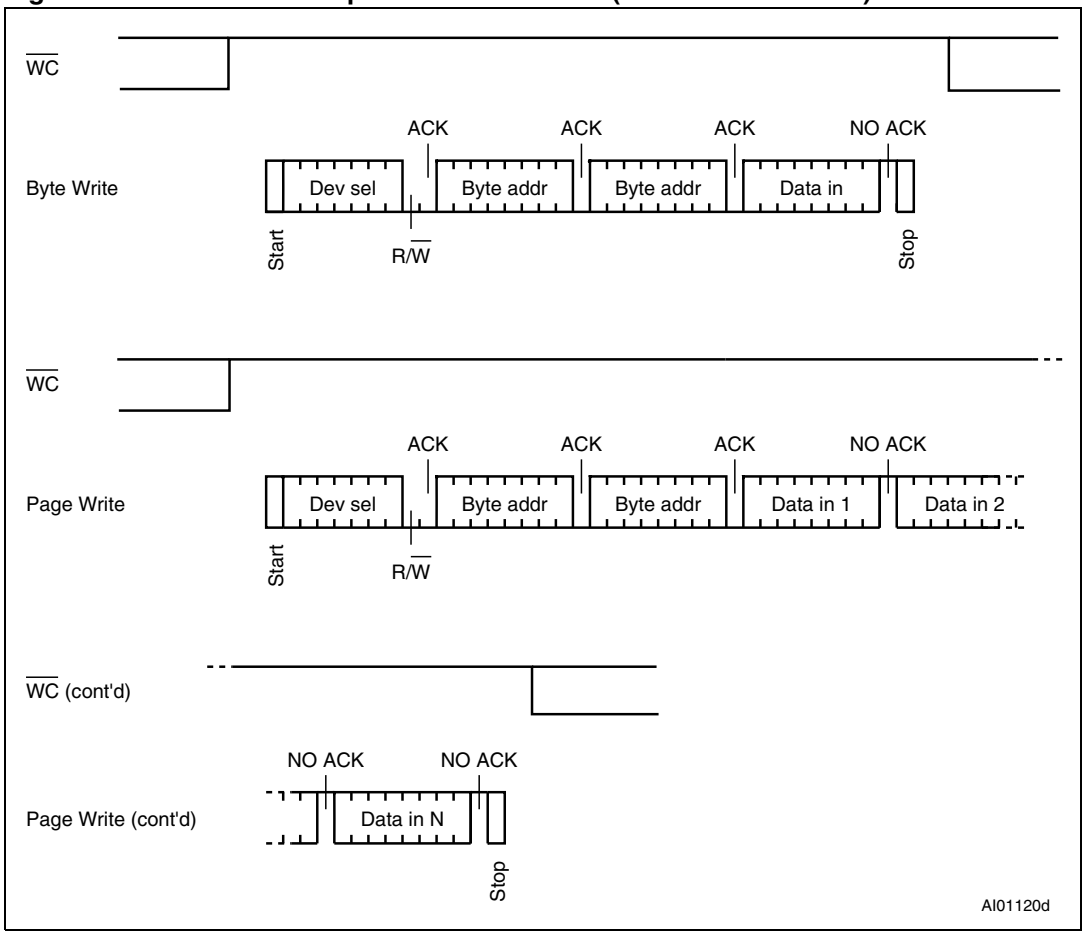


5.1.2 Page Write

The Page Write mode allows up to 64 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A14/A6, are the same. If more bytes are sent than will fit up to the end of the page, a condition known as “roll-over” occurs. In case of roll-over, the first bytes of the page are overwritten.

The bus master sends from 1 to 64 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is low. If Write Control ($\overline{WC}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck, as shown in *Figure 7*. After each byte is transferred, the internal byte address counter is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 7. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



5.1.3 ECC (Error Correction Code) and Write cycling

The device offers an ECC (error correction code) logic which compares each 4-byte group with 6 EEPROM bits of ECC. As a result, if a single bit out of 4 bytes of data happens to be erroneous during a read operation, the ECC detects it and replaces it by the correct value. The read reliability is therefore improved by the use of this feature.

Note however that even if a single byte has to be written, 4 bytes are internally modified (plus the ECC bits), that is, the addressed byte is cycled together with the three other bytes making up the group[(a)]. It is therefore recommended to write by groups of 4 bytes in order to benefit from the larger amount of write cycles.

The maximum number of write cycles is qualified at 1 million (1 000 000) write cycles, using a cycling routine that writes to the device by multiples of 4-byte groups.

a. The group of 4 bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.

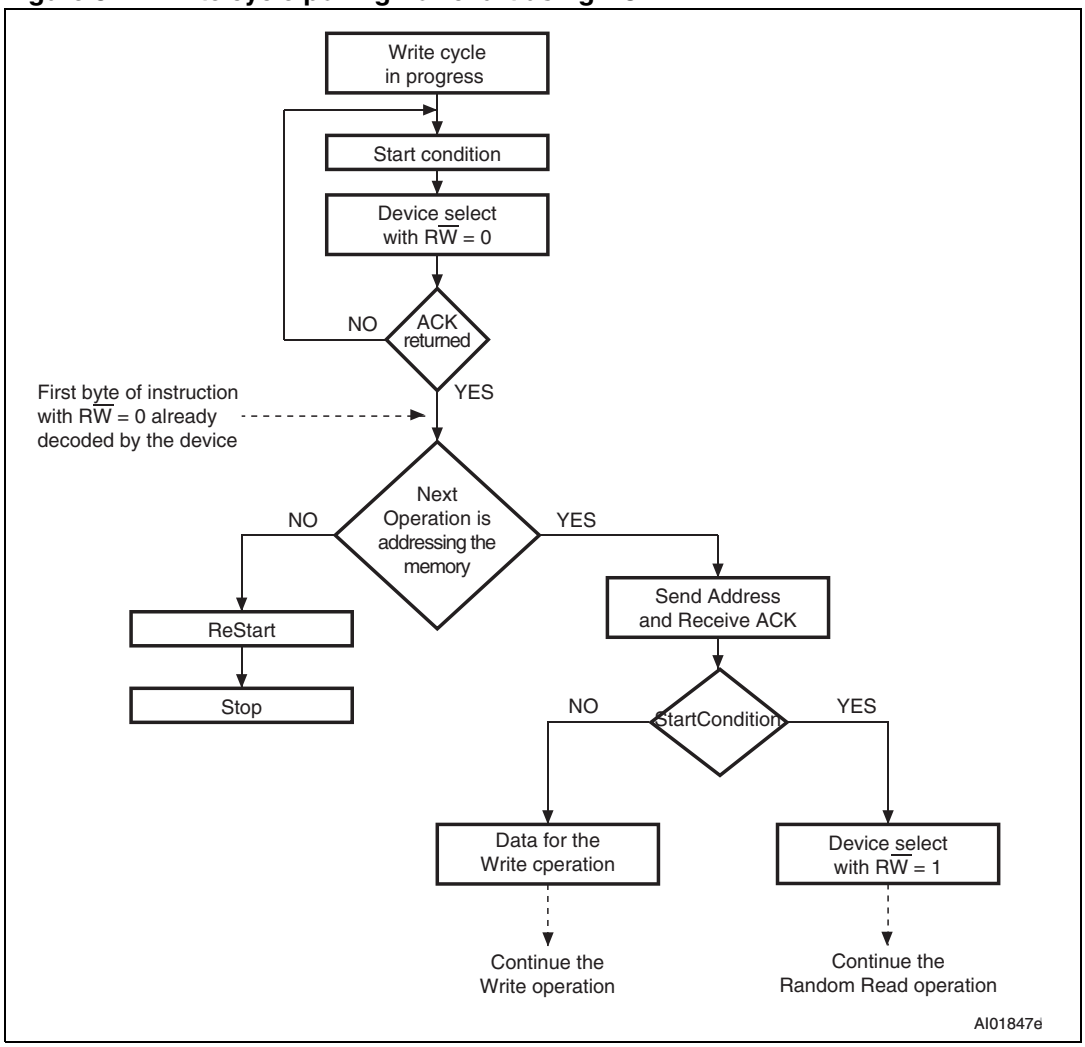
5.1.4 Minimizing Write delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in AC characteristics tables in *Section 8: DC and AC parameters*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 8*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 8. Write cycle polling flowchart using ACK

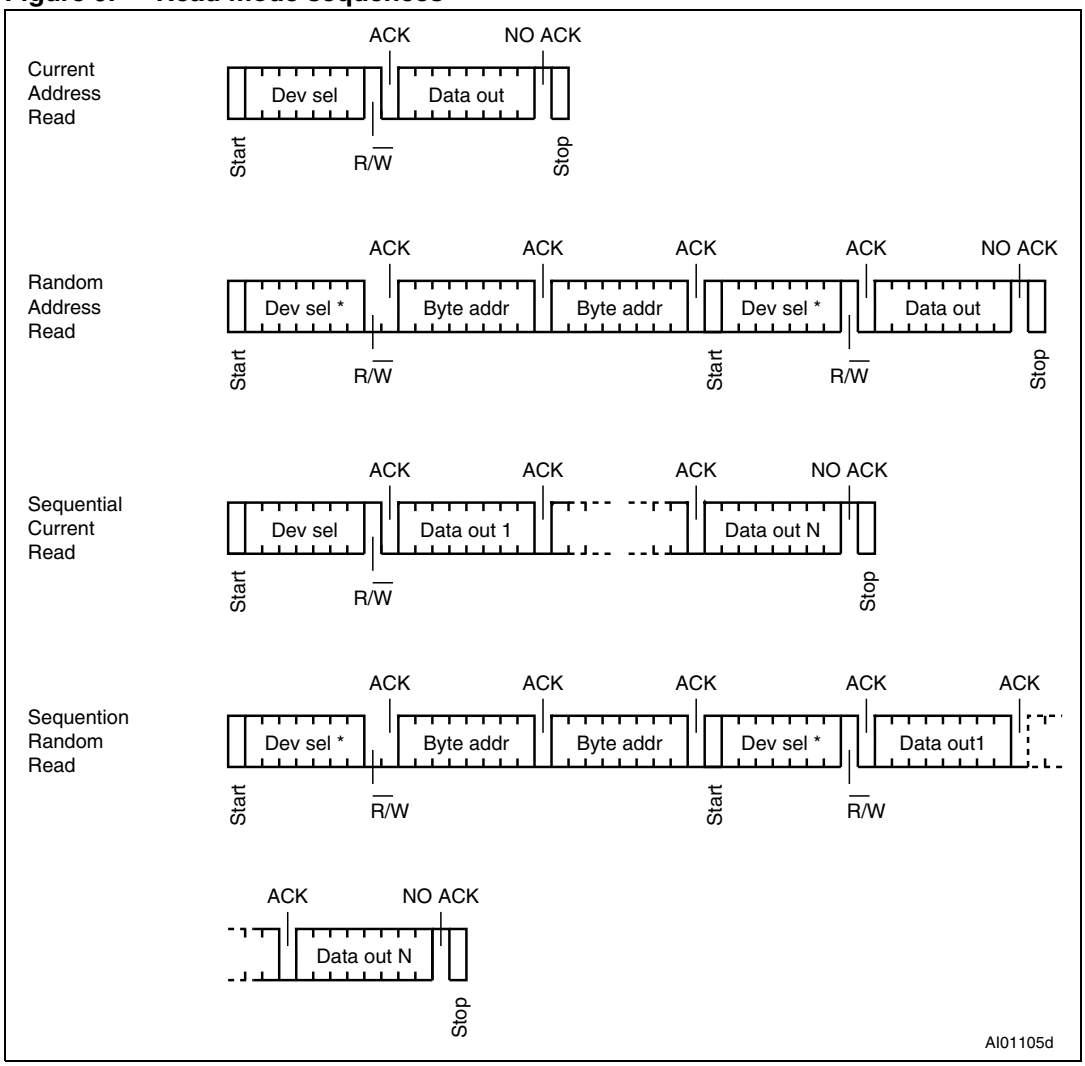


5.2 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device's internal address counter is incremented by one, to point to the next byte address.

Figure 9. Read mode sequences



5.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 9*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the $\overline{RW}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 9*, *without* acknowledging the byte.

5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 9*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

5.2.4 Acknowledge in Read mode

For all Read instructions, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) low during this time, the device terminates the data transfer and switches to its Standby mode.

6 Initial delivery state

The device is delivered with all the memory array bits set to 1 (each byte contains FFh).

7 Maximum rating

Stressing the device outside the ratings listed in *Table 6* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
V_{IO}	Input or output range	–0.50	6.5	V
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body model)(2)	-	3000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. Positive and negative pulses applied on pin pairs, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω, R2=500 Ω)

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 7. Operating conditions (voltage range W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	125	°C

Table 8. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	100		pF
	SCL input rise/fall time, SDA input fall time		50	ns
	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 10. AC measurement I/O waveform

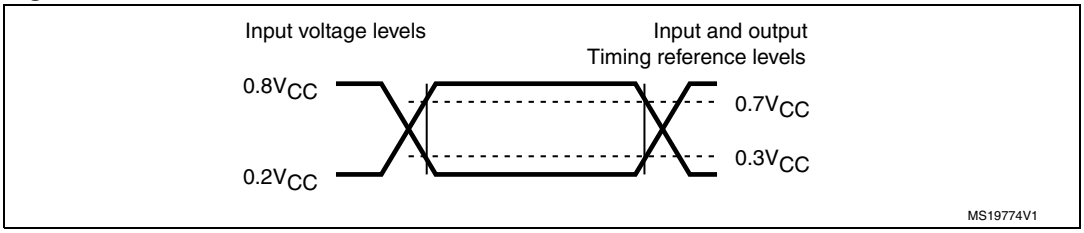


Table 9. Input parameters

Symbol	Parameter[1]	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)			8	pF
C_{IN}	Input capacitance (other pins)			6	pF
Z_L	Input impedance (E2, E1, E0, $\overline{WC}$)[2]	$V_{IN} < 0.3\ V_{CC}$	30		kΩ
Z_H		$V_{IN} > 0.7\ V_{CC}$	500		kΩ

1. Characterized only, not tested in production.
2. E2, E1, E0 input impedance when the memory is selected (after a Start condition).

Table 10. Memory cell characteristics

Symbol	Parameter	Test condition	Min.	Max.	Unit
N_{cycle}	Endurance	TA = 25 °C, 2.5 V < V_{cc} < 5.5 V	1,000,000	-	Write cycle

Note: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please refer to AN2014.

Table 11. DC characteristics (voltage range W, device grade 3)

Symbol	Parameter	Test conditions (see *Table 8* and *Table 10*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E0, E1, E2)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	f_c = 400 kHz (rise/fall time < 50 ns)		2	mA
I_{CC0}	Supply current (Write)	During t_W, 2.5 V < V_{CC} < 5.5 V		5(1)	mA
I_{CC1}	Standby supply current	Device not selected(2), $V_{IN} = V_{SS}$ or V_{CC}		5	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)		0.7 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$, E0, E1, E2)		0.7 V_{CC}	V_{CC}+0.6	
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V		0.4	V

1. Characterized value, not tested in production.
2. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle tW (tW is triggered by the correct decoding of a Write instruction).

Table 12. 400 kHz AC characteristics

Symbol	Alt.	Parameter[1]	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300		ns
t_{QL1QL2}[2]	t_F	SDA (out) fall time	20[3]	120	ns
t_{XH1XH2}	t_R	Input signal rise time	(4)	(4)	ns
t_{XL1XL2}	t_F	Input signal fall time	(4)	(4)	ns
t_{DXCX}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}[5]	t_{DH}	Data out hold time	100	-	ns
t_{CLQV}[6]	t_{AA}	Clock low to next data valid (access time)		900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS}[2]		Pulse width ignored (input filter on SCL and SDA) - single glitch	-	80	ns

1. Test conditions (in addition to those specified under Operating conditions and AC test measurement conditions in *Section 8: DC and AC parameters*).
2. Characterized only, not tested in production.
3. With C_L = 10 pF.
4. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.
5. The min value for t_{CLQX} (Data out hold time) of the M24xxx devices offers a safe timing to bridge the undefined region of the falling edge SCL.
6. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in *Figure 11*.

Figure 11. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 400 kHz

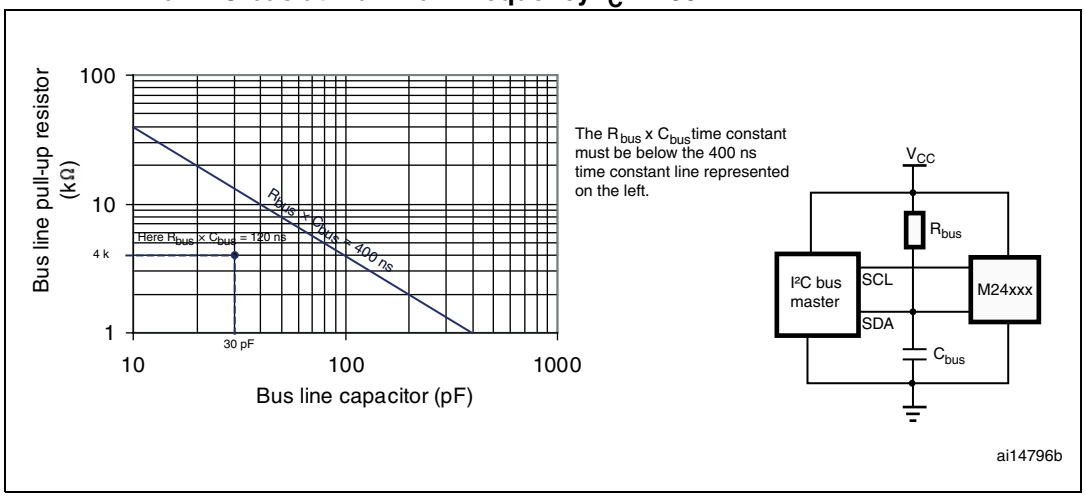
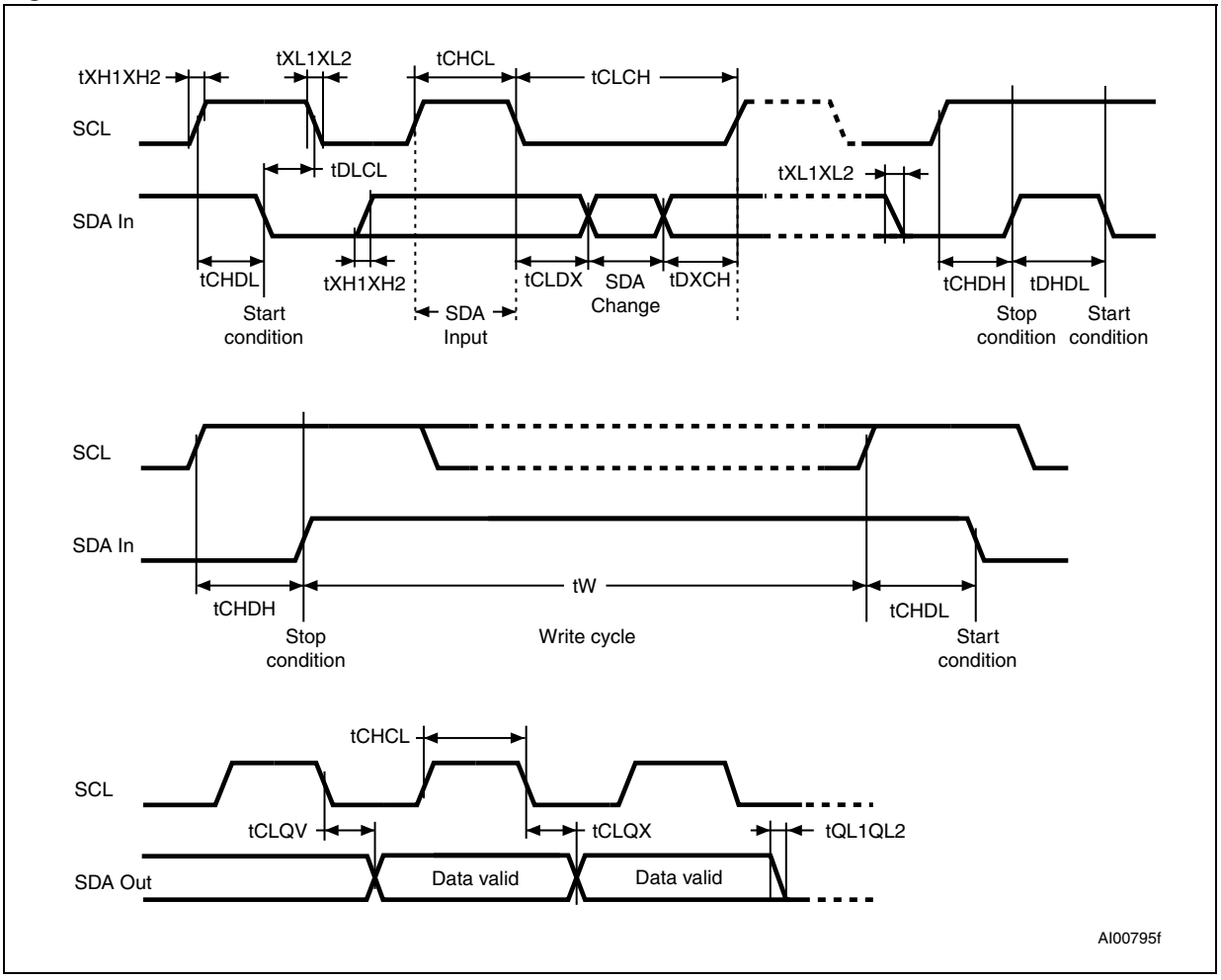


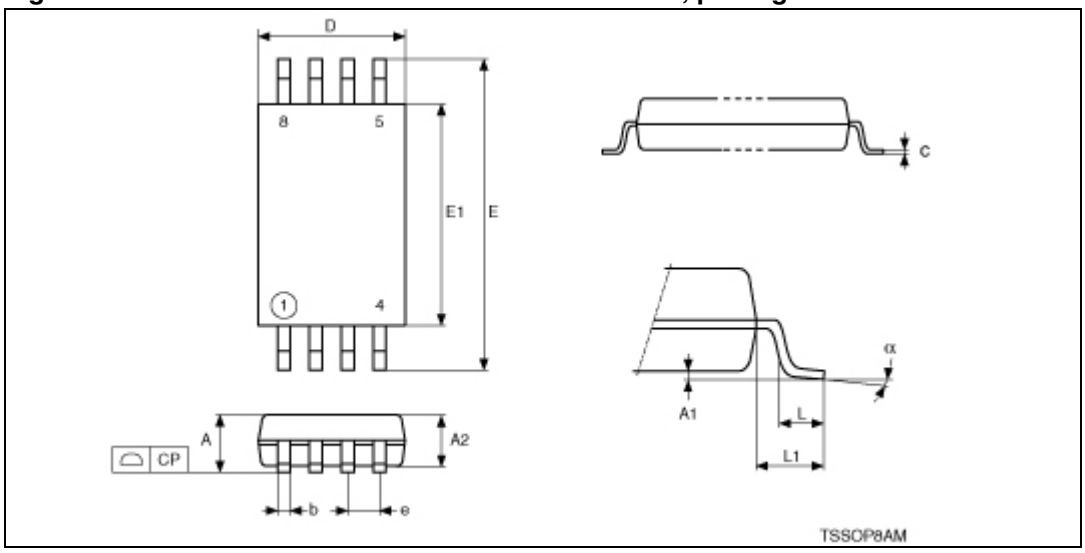
Figure 12. AC waveforms



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 13. TSSOP8 – 8-lead thin shrink small outline, package outline



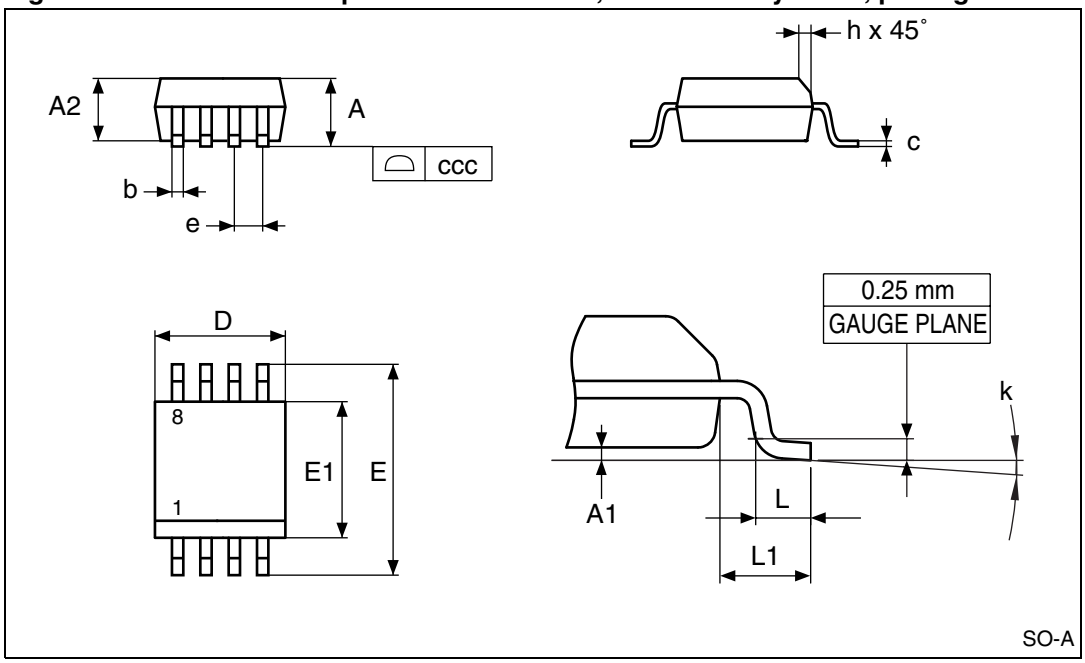
1. Drawing is not to scale.

Table 13. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches(1)		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 14. SO8N – 8 lead plastic small outline, 150 mils body width, package outline



1. Drawing is not to scale.

Table 14. SO8N – 8 lead plastic small outline, 150 mils body width, package data

Symbol	millimeters			inches (1)		
	Typ	Min	Max	Typ	Min	Max
A			1.750			0.0689
A1		0.100	0.250		0.0039	0.0098
A2		1.250			0.0492	
b		0.280	0.480		0.0110	0.0189
c		0.170	0.230		0.0067	0.0091
ccc			0.100			0.0039
D	4.900	4.800	5.000	0.1929	0.1890	0.1969
E	6.000	5.800	6.200	0.2362	0.2283	0.2441
E1	3.900	3.800	4.000	0.1535	0.1496	0.1575
e	1.270			0.0500		
h		0.250	0.500		0.0098	0.0197
k		0°	8°		0°	8°
L		0.400	1.270		0.0157	0.0500
L1	1.040			0.0409		

1.

10 Part numbering

Table 15. Ordering information scheme

Example: M24256 W MN 3 T P /AB

Device type

M24 = I^2C serial access EEPROM

Device function

256 = 256 Kbit (32 K x 8 bit)

Operating voltage

W = V_{CC} = 2.5 V to 5.5 V

Package

MN = SO8 (150 mil width)(1)

DW = TSSOP8 (169 mil width)(1)

Device grade

3 = Device tested with high-reliability certified flow over -40 to 125 °C

Option

blank = standard packing

T = Tape and reel packing

Plating technology

P = ECOPACK® (RoHS compliant)

Process

/AB = Manufacturing technology code

1. RoHS-compliant and halogen-free (ECOPACK2®)

For a list of available options (speed, package, etc.) or for further information on any aspect of the devices, please contact your nearest ST sales office.

11 Revision history

Table 16. Document revision history

Date	Revision	Changes
22-Feb-2012	1	Initial release.

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