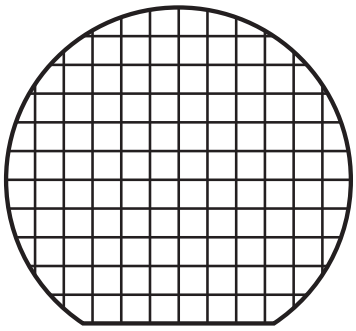
LRIS64K

64 Kbit EEPROM tag IC at 13.56 MHz with 64-bit UID and password based on ISO/IEC 15693 and ISO/IEC 18000-3 Mode 1

Features

- Based on ISO/IEC 15693 and ISO/IEC 18000-3 mode 1 standards
- 13.56 MHz ±7 kHz carrier frequency
- To tag: 10% or 100% ASK modulation using 1/4 (26 Kbit/s) or 1/256 (1.6 Kbit/s) pulse position coding
- From tag: load modulation using Manchester coding with 423 kHz and 484 kHz subcarriers in low (6.6 Kbit/s) or high (26 Kbit/s) data rate mode. Supports the 53 Kbit/s data rate with Fast commands
- Internal tuning capacitor (27.5 pF)
- More than 1 million write cycles
- More than 40-year data retention
- 64 Kbit EEPROM organized into 2048 blocks of 32 bits
- 64-bit unique identifier (UID)
- Multipassword protection
- Read Block & Write (32-bit blocks)
- Write time: 5.75 ms including the internal verify



Wafer (SBN18)

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1 Description

The LRIS64K is a contactless memory powered by the received carrier electromagnetic wave, which follows the ISO/IEC 15693 and ISO/IEC 18000-3 mode 1 recommendation for radio-frequency power and signal interface. It is a 64 Kbit electrically erasable programmable memory (EEPROM). The memory is organized as 64 sectors divided into 32 blocks of 32 bits.

The LRIS64K is accessed via the 13.56 MHz carrier electromagnetic wave, on which incoming data are demodulated from the received signal amplitude modulation (ASK: amplitude shift keying). The received ASK wave is 10% or 100% modulated with a data rate of 1.6 Kbit/s using the 1/256 pulse coding mode, or a data rate of 26 Kbit/s using the 1/4 pulse coding mode. Outgoing data are generated by the LRIS64K load variation using Manchester coding with one or two subcarrier frequencies at 423 kHz and 484 kHz. Data are transferred from the LRIS64K at 6.6 Kbit/s in low data rate mode and 26 Kbit/s in high data rate mode. The LRIS64K supports the 53 Kbit/s data rate in high data rate mode with a single subcarrier frequency of 423 kHz.

The LRIS64K also features a unique 32-bit multi-password protection scheme.

Figure 1. Pad connection

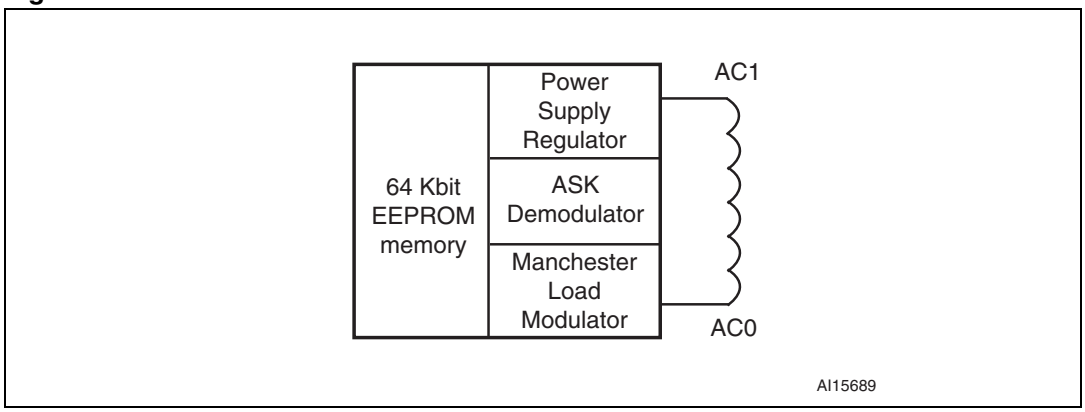


Table 1. Signal names

Signal name	Function	Direction
AC0	Antenna coil	I/O
AC1	Antenna coil	I/O

2 User memory organization

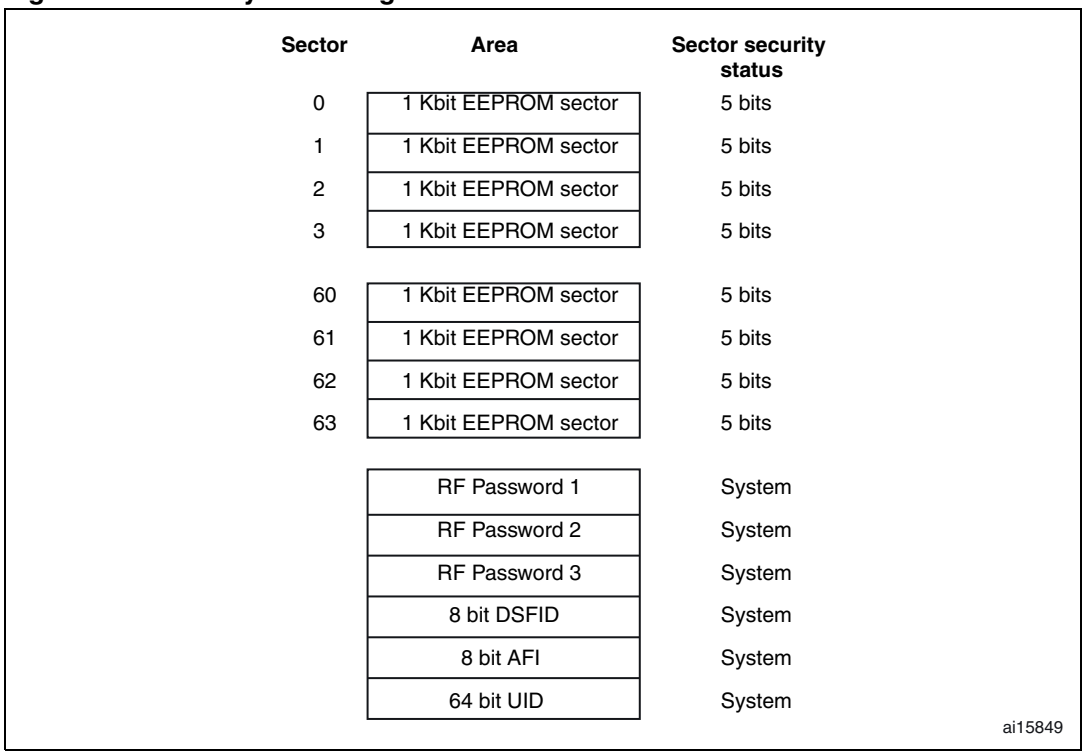
The LRIS64K is divided into 64 sectors of 32 blocks of 32 bits as shown in *Table 2*. *Figure 2* shows the memory sector organization. Each sector can be individually read- and/or write-protected using a specific password command. Read and write operations are possible if the addressed data are not in a protected sector.

The LRIS64K also has a 64-bit block that is used to store the 64-bit unique identifier (UID). The UID is compliant with the ISO/IEC 15963 description, and its value is used during the anticollision sequence (Inventory). This block is not accessible by the user and its value is written by ST on the production line.

The LRIS64K includes an AFI register that stores the application family identifier, and a DSFID register that stores the data storage family identifier used in the anticollision algorithm.

The LRIS64K has three additional 32-bit blocks that store the RF password codes.

Figure 2. Memory sector organization



Sector details

The LRIS64K user memory is divided into 64 sectors. Each sector contains 1024 bits. The protection scheme is described in *Section 3: System memory area*.

A sector provides 32 blocks of 32 bits. Each read and write access are done by block. Read and write block accesses are controlled by a Sector Security Status byte that defines the access rights to all the 32 blocks contained in the sector. If the sector is not protected, a Write command updates the complete 32 bits of the selected block.

Table 2. Sector details

Sector number	RF block address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
0	0	user	user	user	user
	1	user	user	user	user
	2	user	user	user	user
	3	user	user	user	user
	4	user	user	user	user
	5	user	user	user	user
	6	user	user	user	user
	7	user	user	user	user
	8	user	user	user	user
	9	user	user	user	user
	10	user	user	user	user
	11	user	user	user	user
	12	user	user	user	user
	13	user	user	user	user
	14	user	user	user	user
	15	user	user	user	user
	16	user	user	user	user
	17	user	user	user	user
	18	user	user	user	user
	19	user	user	user	user
	20	user	user	user	user
	21	user	user	user	user
	22	user	user	user	user
	23	user	user	user	user
	24	user	user	user	user
	25	user	user	user	user
	26	user	user	user	user
	27	user	user	user	user
	28	user	user	user	user
	29	user	user	user	user
	30	user	user	user	user
	31	user	user	user	user

Table 2. Sector details (continued)

Sector number	RF block address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
1	32	user	user	user	user
	33	user	user	user	user
	34	user	user	user	user
	35	user	user	user	user
	36	user	user	user	user
	37	user	user	user	user
	38	user	user	user	user
	39	user	user	user	user
	...	...	...	...	...
...	...	...	...	...	...
63	2016	user	user	user	user
	2017	user	user	user	user
	2018	user	user	user	user
	2019	user	user	user	user
	2020	user	user	user	user
	2021	user	user	user	user
	2022	user	user	user	user
	2023	user	user	user	user
	2024	user	user	user	user
	2025	user	user	user	user
	2026	user	user	user	user
	2027	user	user	user	user
	2028	user	user	user	user
	2029	user	user	user	user
	2030	user	user	user	user
	2031	user	user	user	user
	2032	user	user	user	user
	2033	user	user	user	user
	2034	user	user	user	user
	2035	user	user	user	user
	2036	user	user	user	user
	2037	user	user	user	user
	2038	user	user	user	user
	2039	user	user	user	user

Table 2. Sector details (continued)

Sector number	RF block address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
63 continued	2040	user	user	user	user
	2041	user	user	user	user
	2042	user	user	user	user
	2043	user	user	user	user
	2044	user	user	user	user
	2045	user	user	user	user
	2046	user	user	user	user
	2047	user	user	user	user

3 System memory area

3.1 LRIS64K RF block security

The LRIS64K provides a special protection mechanism based on passwords. Each memory sector of the LRIS64K can be individually protected by one out of three available passwords, and each sector can also have Read/Write access conditions set.

Each memory sector of the LRIS64K is assigned with a Sector security status byte including a Sector Lock bit, two Password Control bits and two Read/Write protection bits as shown in *Table 4*. *Table 3* describes the organization of the Sector security status byte which can be read using the Read Single Block and Read Multiple Block commands with the Option_flag set to '1'.

On delivery, the default value of the SSS bytes is reset to 00h.

Table 3. Sector security status byte area

RF address	Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
0	SSS 3	SSS 2	SSS 1	SSS 0
128	SSS 7	SSS 6	SSS 5	SSS 4
256	SSS 11	SSS 10	SSS 9	SSS 8
384	SSS 15	SSS 14	SSS 13	SSS 12
512	SSS 19	SSS 18	SSS 17	SSS 16
640	SSS 23	SSS 22	SSS 21	SSS 20
768	SSS 27	SSS 26	SSS 25	SSS 24
896	SSS 31	SSS 30	SSS 29	SSS 28
1024	SSS 35	SSS 34	SSS 33	SSS 32
1152	SSS 39	SSS 38	SSS 37	SSS 36
1280	SSS 43	SSS 42	SSS 41	SSS 40
1408	SSS 47	SSS 46	SSS 45	SSS 44
1536	SSS 51	SSS 50	SSS 49	SSS 48
1664	SSS 55	SSS 54	SSS 53	SSS 52
1792	SSS 59	SSS 58	SSS 57	SSS 56
1920	SSS 63	SSS 62	SSS 61	SSS 60

Table 4. Sector security status byte organization

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	0	0	Password Control bits		Read / Write protection bits		Sector Lock

When the Sector Lock bit is set to '1', for instance by issuing a Lock-sector Password command, the 2 Read/Write protection bits (b_1, b_2) are used to set the Read/Write access of the sector as described in *Table 5*.

Table 5. Read / Write protection bit setting

Sector Lock	b_2, b_1	Sector access when password presented		Sector access when password not presented	
0	xx	Read	Write	Read	Write
1	00	Read	Write	Read	No Write
1	01	Read	Write	Read	Write
1	10	Read	Write	No Read	No Write
1	11	Read	No Write	No Read	No Write

The next 2 bits of the Sector security status byte (b_3, b_4) are the Password Control bits. The value these two bits is used to link a password to the sector as defined in *Table 6*.

Table 6. Password Control bits

b_4, b_3	Password
00	The sector is not protected by a Password
01	The sector is protected by the Password 1
10	The sector is protected by the Password 2
11	The sector is protected by the Password 3

The LRIS64K password protection is organized around a dedicated set of commands plus a system area of three password blocks where the password values are stored. This system area is described in *Table 7*.

Table 7. Password system area

Add	0 7	8 15	16 23	24 31
1	Password 1			
2	Password 2			
3	Password 3			

The dedicated password commands are:

- **Write-sector Password**

  The Write-sector Password command is used to write a 32-bit block into the password system area. This command must be used to update password values. After the write cycle, the new password value is automatically activated. It is possible to modify a password value after issuing a valid Present-sector Password command.
  On delivery, the three default password values are set to 0000 0000h and are activated.

- **Lock-sector Password**

  The Lock-sector Password command is used to set the Sector security status byte of the selected sector. Bits b_4 to b_1 of the Sector security status byte are affected by the

Lock-sector Password command. The Sector Lock bit, b_0, is set to '1' automatically. After issuing a Lock-sector Password command, the protection settings of the selected sector are activated. The protection of a locked block cannot be changed. A Lock-sector Password command sent to a locked sector returns an error code.

- **Present-sector Password**

  The Present-sector Password command is used to present one of the three passwords to the LRIS64K in order to modify the access rights of all the memory sectors linked to that password (*Table 5*) including the password itself. If the presented password is correct, the access rights remain activated until the tag is powered off or until a new Present-sector Password command is issued. If the presented password value is not correct, all the access rights of all the memory sectors are deactivated.

3.2 Example of the LRIS64K security protection

Table 8 and *Table 9* show the sector security protections before and after a valid Present-sector Password command. *Table 8* shows the sector access rights of an LRIS64K after power-up. After a valid Present-sector Password command with password 1, the memory sector access is changed as shown in *Table 9*.

Table 8. Sector security protection after power-up

Sector address				Sector security status byte					
				$b_7b_6b_5$	b_4	b_3	b_2	b_1	b_0
0	Protection: Standard	Read	No Write	xxx	0	0	0	0	1
1	Protection: Pswd 1	Read	No Write	xxx	0	1	0	0	1
2	Protection: Pswd 1	Read	Write	xxx	0	1	0	1	1
3	Protection: Pswd 1	No Read	No Write	xxx	0	1	1	0	1
4	Protection: Pswd 1	No Read	No Write	xxx	0	1	1	1	1

Table 9. Sector security protection after a valid presentation of password 1

Sector address				Sector security status byte					
				$b_7b_6b_5$	b_4	b_3	b_2	b_1	b_0
0	Protection: Standard	Read	No Write	xxx	0	0	0	0	1
1	Protection: Pswd 1	Read	Write	xxx	0	1	0	0	1
2	Protection: Pswd 1	Read	Write	xxx	0	1	0	1	1
3	Protection: Pswd 1	Read	Write	xxx	0	1	1	0	1
4	Protection: Pswd 1	Read	No Write	xxx	0	1	1	1	1

4 Initial delivery state

The device is delivered with the following factory settings:

- All bits in the memory array are set to 1 (each byte contains FFh).
- The default value of the SSS bytes is reset to 00h.
- The three default password values are set to 0000 0000h and are activated.

System parameters are set to:

- (E0 02 xx xx xx xx xx xx)h for UID
- (03 07 FF)h for Memory Size
- 00h for AFI
- 00h for DSFID

5 Commands

The LRIS64K supports the following commands:

- ***Inventory***, used to perform the anticollision sequence.
- ***Stay Quiet***, used to put the LRIS64K in quiet mode, where it does not respond to any inventory command.
- ***Select***, used to select the LRIS64K. After this command, the LRIS64K processes all Read/Write commands with Select_flag set.
- ***Reset To Ready***, used to put the LRIS64K in the ready state.
- ***Read Block***, used to output the 32 bits of the selected block and its locking status.
- ***Write Block***, used to write the 32-bit value in the selected block, provided that it is not locked.
- ***Read Multiple Blocks***, used to read the selected blocks and send back their value.
- ***Write AFI***, used to write the 8-bit value in the AFI register.
- ***Lock AFI***, used to lock the AFI register.
- ***Write DSFID***, used to write the 8-bit value in the DSFID register.
- ***Lock DSFID***, used to lock the DSFID register.
- ***Get System Info***, used to provide the system information value
- ***Get Multiple Block Security Status***, used to send the security status of the selected block.
- ***Initiate***, used to trigger the tag response to the Inventory Initiated sequence.
- ***Inventory Initiated***, used to perform the anticollision sequence triggered by the Initiate command.
- ***Write-sector Password***, used to write the 32 bits of the selected password.
- ***Lock-sector Password***, used to write the Sector security status bits of the selected sector.
- ***Present-sector Password***, enables the user to present a password to unprotect the user blocks linked to this password.
- ***Fast Initiate***, used to trigger the tag response to the Inventory Initiated sequence.
- ***Fast Inventory Initiated***, used to perform the anticollision sequence triggered by the Initiate command.
- ***Fast Read Single Block***, used to output the 32 bits of the selected block and its locking status.
- ***Fast Read Multiple Blocks***, used to read the selected blocks and send back their value.

5.1 Initial dialogue for vicinity cards

The dialog between the vicinity coupling device (VCD) and the vicinity integrated circuit Card or VICC (LRIS64K) takes place as follows:

- activation of the LRIS64K by the RF operating field of the VCD.
- transmission of a command by the VCD.
- transmission of a response by the LRIS64K.

These operations use the RF power transfer and communication signal interface described below (see *Power transfer*, *Frequency* and *Operating field*). This technique is called RTF (Reader Talk First).

5.1.1 Power transfer

Power is transferred to the LRIS64K by radio frequency at 13.56 MHz via coupling antennas in the LRIS64K and the VCD. The RF operating field of the VCD is transformed on the LRIS64K antenna to an AC Voltage which is rectified, filtered and internally regulated. The amplitude modulation (ASK) on this received signal is demodulated by the ASK demodulator.

5.1.2 Frequency

The ISO/IEC 15693 standard defines the carrier frequency (f_C) of the operating field as 13.56 MHz ±7 kHz.

5.1.3 Operating field

The LRIS64K operates continuously between H_{min} and H_{max}.

- The minimum operating field is H_{min} and has a value of 150 mA/m rms.
- The maximum operating field is H_{max} and has a value of 5 A/m rms.

A VCD shall generate a field of at least H_{min} and not exceeding H_{max} in the operating volume.

6 Communication signal from VCD to LRIS64K

Communications between the VCD and the LRIS64K takes place using the modulation principle of ASK (Amplitude Shift Keying). Two modulation indexes are used, 10% and 100%. The LRIS64K decodes both. The VCD determines which index is used.

The modulation index is defined as [a – b]/[a + b] where a is the peak signal amplitude and b, the minimum signal amplitude of the carrier frequency.

Depending on the choice made by the VCD, a “pause” will be created as described in *Figure 3* and *Figure 4*.

The LRIS64K is operational for any degree of modulation index from between 10% and 30%.

Figure 3. 100% modulation waveform

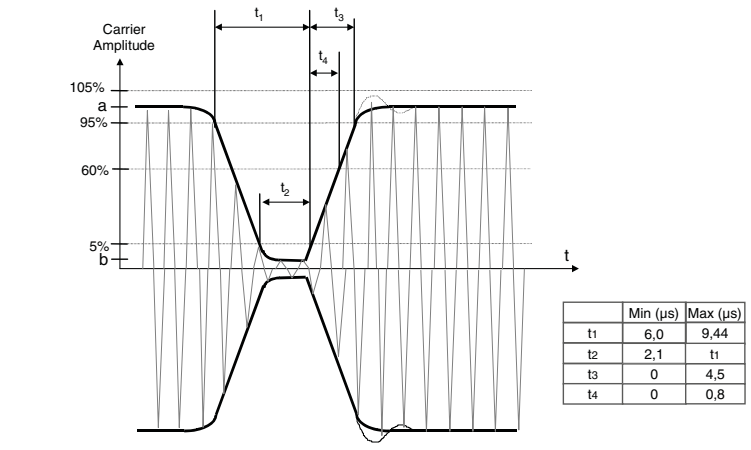
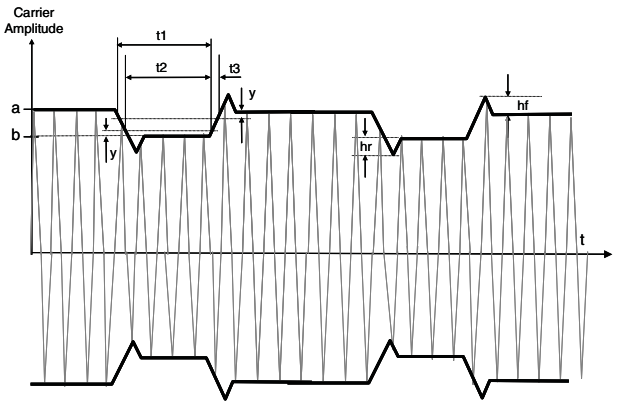


Table 10. 10% modulation parameters

Symbol	Parameter definition	Value
hr	0.1 x (a – b)	Max
hf	0.1 x (a – b)	Max

Figure 4. 10% modulation waveform



	Min	Max
t1	6,0 µs	9,44 µs
t2	3,0 µs	t1
t3	0	4,5 µs
Modulation Index	10%	30%

y	0,05 (a-b)
hf, hr	0,1 (a-b) max

The VICC shall be operational for any value of modulation index between 10 % and 30 %.

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7 Data rate and data coding

The data coding implemented in the LRIS64K uses pulse position modulation. Both data coding modes that are described in the ISO/IEC15693 are supported by the LRIS64K. The selection is made by the VCD and indicated to the LRIS64K within the start of frame (SOF).

7.1 Data coding mode: 1 out of 256

The value of one single byte is represented by the position of one pause. The position of the pause on 1 of 256 successive time periods of 18.88 µs (256/f_C), determines the value of the byte. In this case the transmission of one byte takes 4.833 ms and the resulting data rate is 1.65 kbits/s (f_C/8192).

Figure 5 illustrates this pulse position modulation technique. In this figure, data E1h (225 decimal) is sent by the VCD to the LRIS64K.

The pause occurs during the second half of the position of the time period that determines the value, as shown in *Figure 6*.

A pause during the first period transmits the data value 00h. A pause during the last period transmit the data value FFh (255 decimal).

Figure 5. 1 out of 256 coding mode

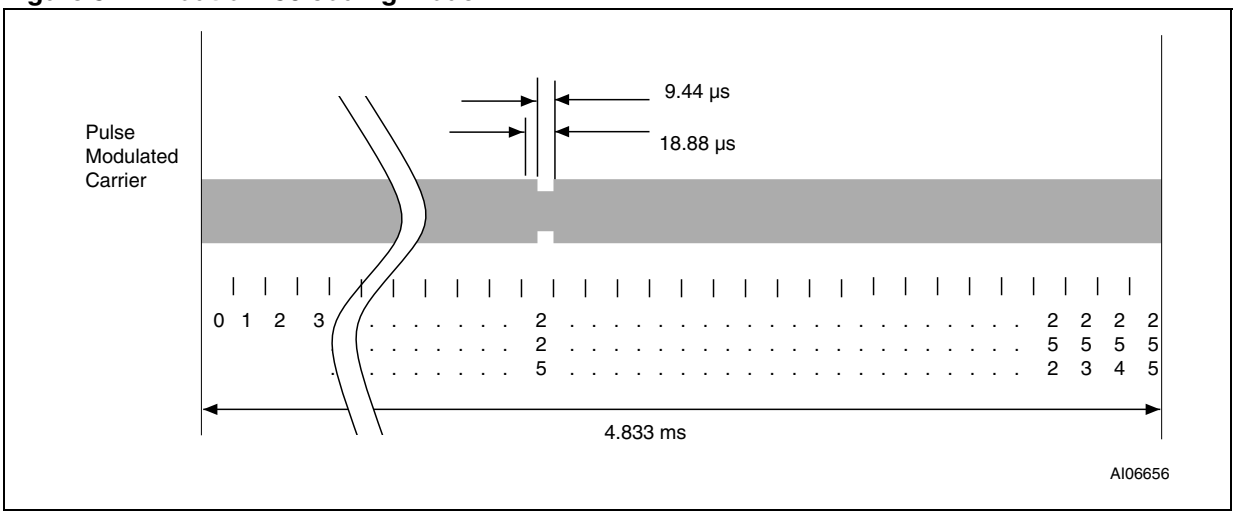
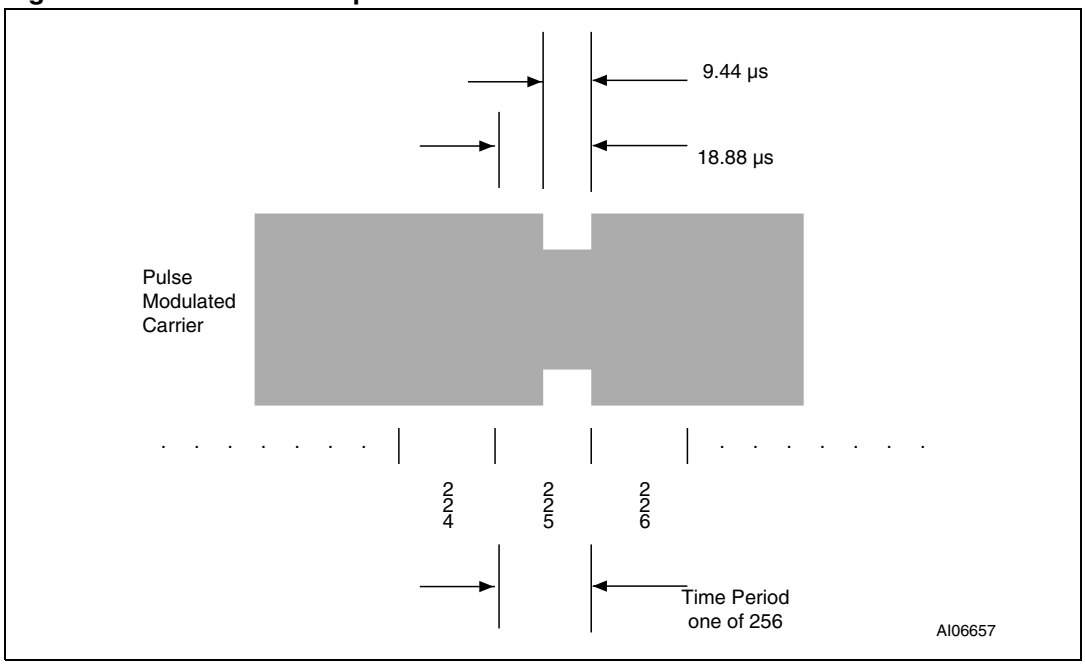


Figure 6. Detail of a time period



7.2 Data coding mode: 1 out of 4

The value of 2 bits is represented by the position of one pause. The position of the pause on 1 of 4 successive time periods of 18.88 µs ($256/f_C$), determines the value of the 2 bits. Four successive pairs of bits form a byte, where the least significant pair of bits is transmitted first.

In this case the transmission of one byte takes 302.08 µs and the resulting data rate is 26.48 Kbits/s ($f_C/512$). *Figure 7* illustrates the 1 out of 4 pulse position technique and coding. *Figure 8* shows the transmission of E1h (225d - 1110 0001b) by the VCD.

Figure 7. 1 out of 4 coding mode

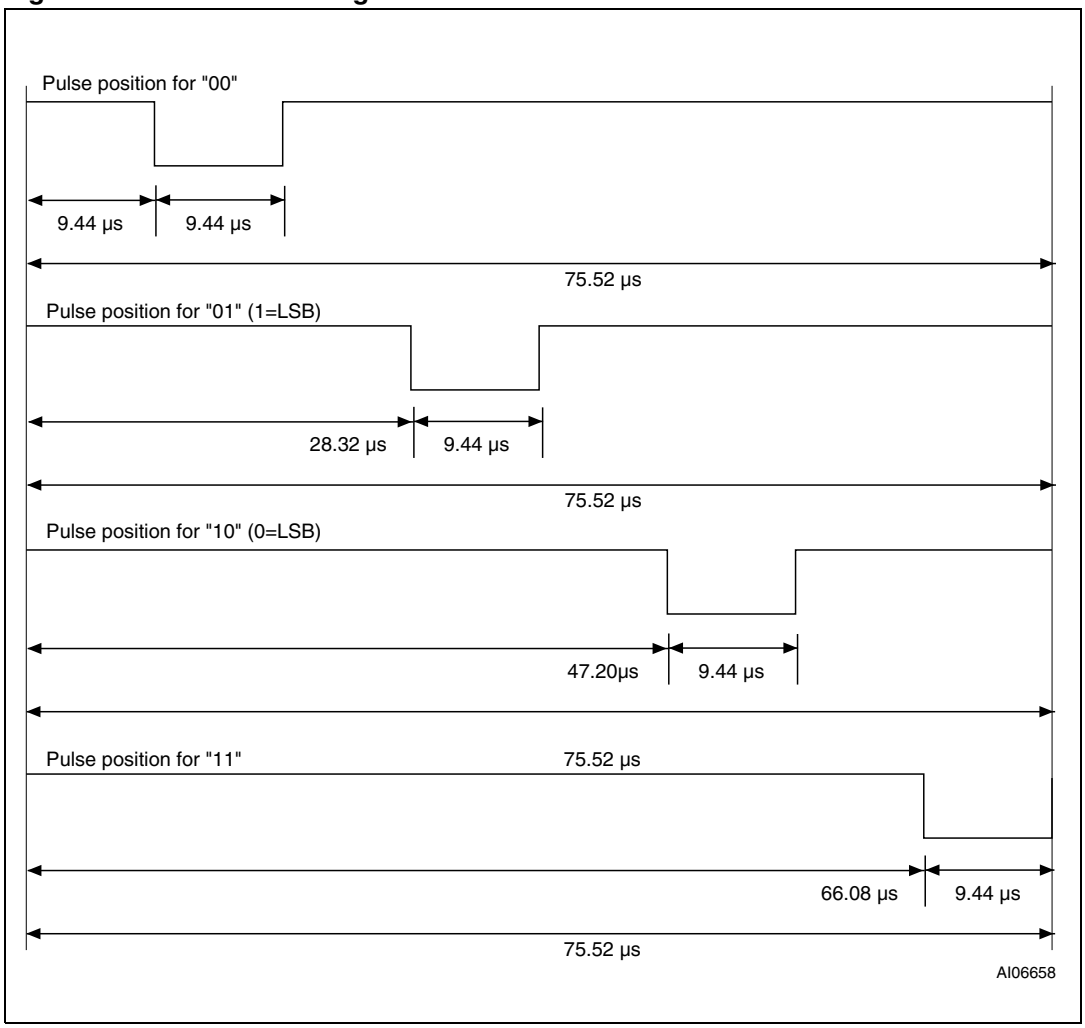
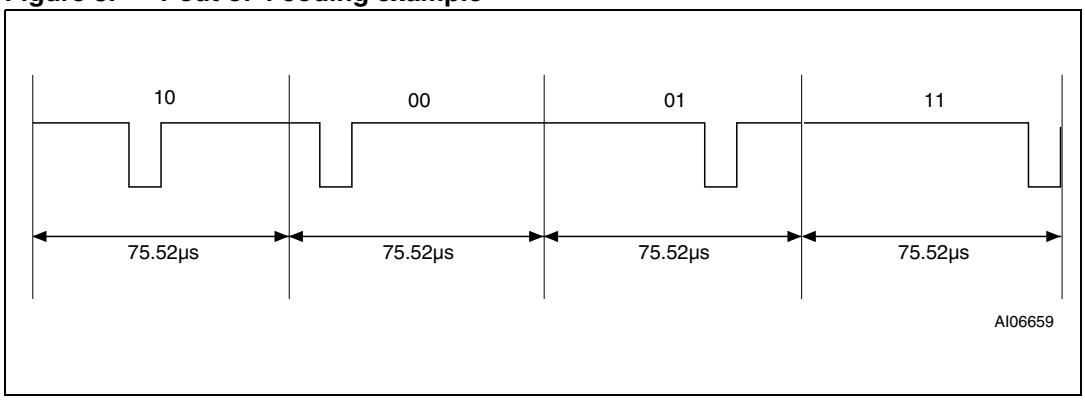


Figure 8. 1 out of 4 coding example



7.3 VCD to LRIS64K frames

Frames are delimited by a start of frame (SOF) and an end of frame (EOF). They are implemented using code violation. Unused options are reserved for future use.

The LRIS64K is ready to receive a new command frame from the VCD 311.5 µs (t_2) after sending a response frame to the VCD.

The LRIS64K takes a power-up time of 0.1 ms after being activated by the powering field. After this delay, the LRIS64K is ready to receive a command frame from the VCD.

7.4 Start of frame (SOF)

The SOF defines the data coding mode the VCD is to use for the following command frame. The SOF sequence described in *Figure 9* selects the 1 out of 256 data coding mode. The SOF sequence described in *Figure 10* selects the 1 out of 4 data coding mode. The EOF sequence for either coding mode is described in *Figure 11*.

Figure 9. SOF to select 1 out of 256 data coding mode

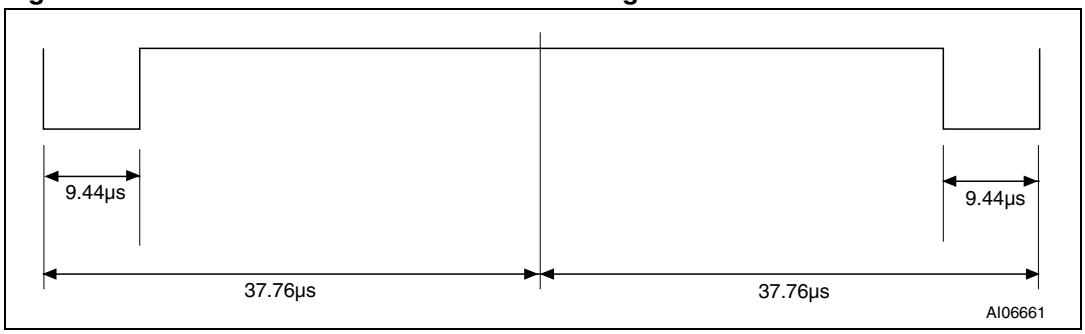


Figure 10. SOF to select 1 out of 4 data coding mode

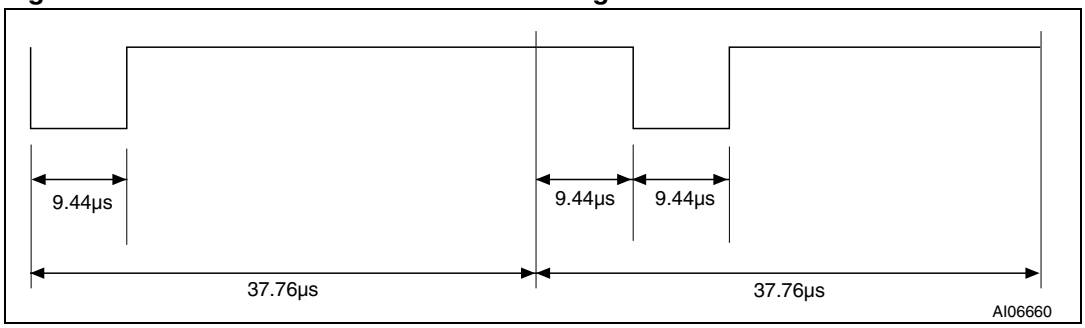
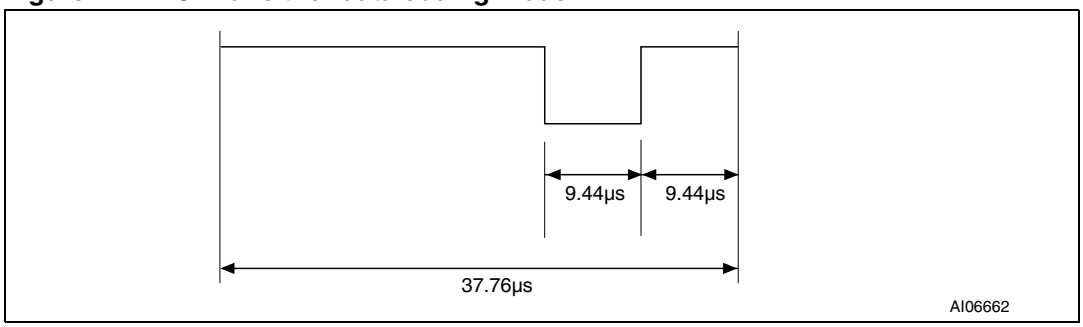


Figure 11. EOF for either data coding mode



8 Communications signal from LRIS64K to VCD

The LRIS64K has several modes defined for some parameters, owing to which it can operate in different noise environments and meet different application requirements.

8.1 Load modulation

The LRIS64K is capable of communication to the VCD via an inductive coupling area whereby the carrier is loaded to generate a subcarrier with frequency f_S. The subcarrier is generated by switching a load in the LRIS64K.

The load-modulated amplitude received on the VCD antenna must be of at least 10mV when measured as described in the test methods defined in International Standard ISO/IEC10373-7.

8.2 Subcarrier

The LRIS64K supports the one-subcarrier and two-subcarrier response formats. These formats are selected by the VCD using the first bit in the protocol header. When one subcarrier is used, the frequency f_{S1} of the subcarrier load modulation is 423.75 kHz (f_C/32). When two subcarriers are used, the frequency f_{S1} is 423.75 kHz (f_C/32), and frequency f_{S2} is 484.28 kHz (f_C/28). When using the two-subcarrier mode, the LRIS64K generates a continuous phase relationship between f_{S1} and f_{S2}.

8.3 Data rates

The LRIS64K can respond using the low or the high data rate format. The selection of the data rate is made by the VCD using the second bit in the protocol header. It also supports the x2 mode available on all the Fast commands. *Table 11* shows the different data rates produced by the LRIS64K using the different response format combinations.

Table 11. Response data rates

Data rate		One subcarrier	Two subcarriers
Low	Standard commands	6.62 Kbit/s (f_c/2048)	6.67 Kbit/s (f_c/2032)
	Fast commands	13.24 Kbit/s (f_c/1024)	not applicable
High	Standard commands	26.48 Kbit/s (f_c/512)	26.69 Kbit/s (f_c/508)
	Fast commands	52.97 Kbit/s (f_c/256)	not applicable

9 Bit representation and coding

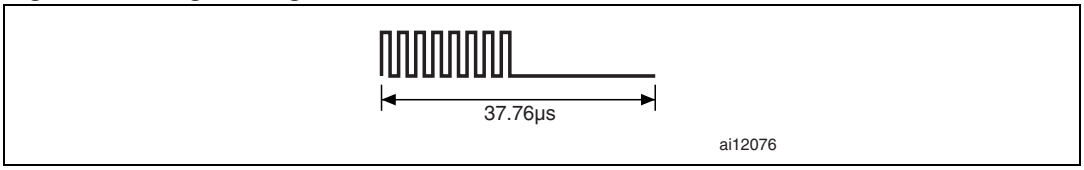
Data bits are encoded using Manchester coding, according to the following schemes. For the low data rate, same subcarrier frequency or frequencies is/are used, in this case the number of pulses is multiplied by 4 and all times will increase by this factor. For the Fast commands using one subcarrier, all pulse numbers and times are divided by 2.

9.1 Bit coding using one subcarrier

9.1.1 High data rate

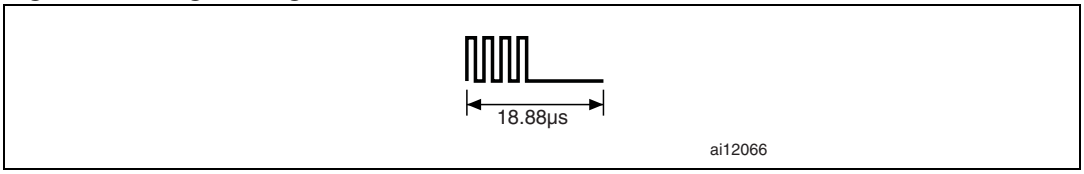
A logic 0 starts with 8 pulses at 423.75 kHz ($f_C/32$) followed by an unmodulated time of 18.88 µs as shown in *Figure 12*.

Figure 12. Logic 0, high data rate, one subcarriers



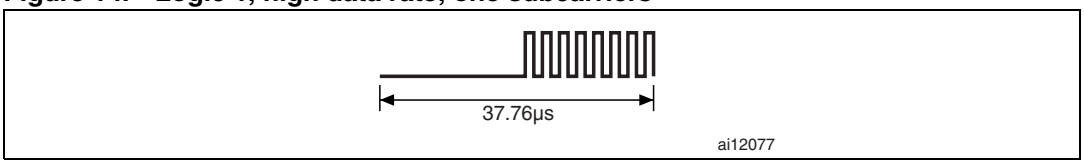
For the fast commands, a logic 0 starts with 4 pulses at 423.75 kHz ($f_C/32$) followed by an unmodulated time of 9.44 µs as shown in *Figure 13*.

Figure 13. Logic 0, high data rate, one subcarriers x2



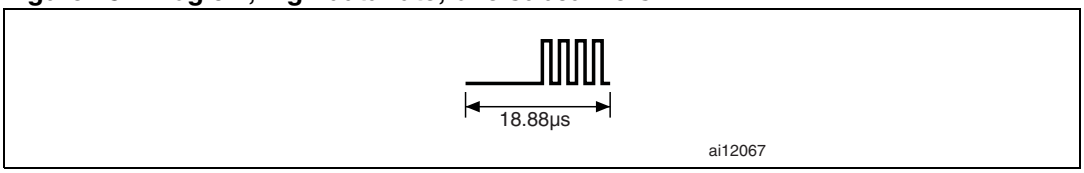
A logic 1 starts with an unmodulated time of 18.88 µs followed by 8 pulses at 423.75 kHz ($f_C/32$) as shown in *Figure 14*.

Figure 14. Logic 1, high data rate, one subcarriers



For the Fast commands, a logic 1 starts with an unmodulated time of 9.44 µs followed by 4 pulses of 423.75 kHz ($f_C/32$) as shown in *Figure 15*.

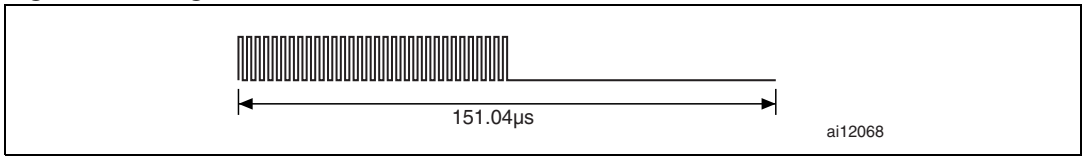
Figure 15. Logic 1, high data rate, one subcarriers x2



9.1.2 Low data rate

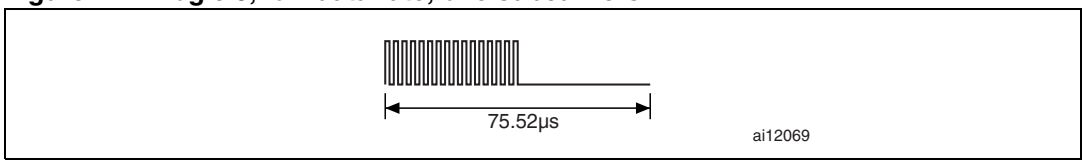
A logic 0 starts with 32 pulses at 423.75 kHz (f_C/32) followed by an unmodulated time of 75.52 µs as shown in *Figure 16*.

Figure 16. Logic 0, low data rate, one subcarriers



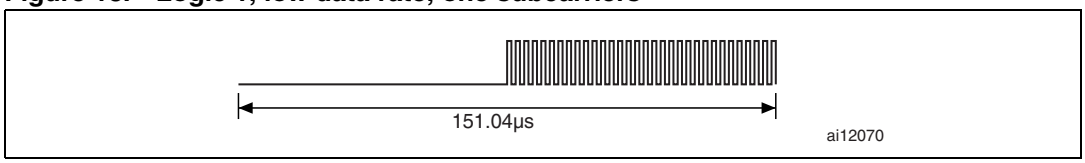
For the Fast commands, a logic 0 starts with 16 pulses at 423.75 kHz (f_C/32) followed by an unmodulated time of 37.76 µs as shown in *Figure 17*.

Figure 17. Logic 0, low data rate, one subcarriers x2



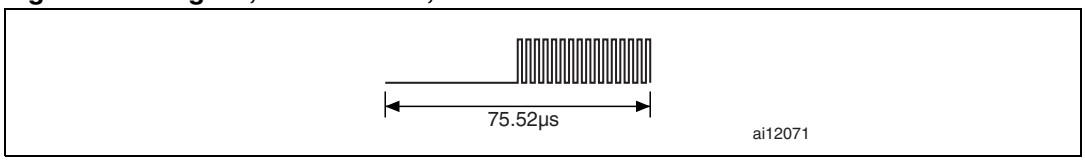
A logic 1 starts with an unmodulated time of 75.52 µs followed by 32 pulses at 423.75 kHz (f_C/32) as shown in *Figure 18*.

Figure 18. Logic 1, low data rate, one subcarriers



For the Fast commands, a logic 1 starts with an unmodulated time of 37.76 µs followed by 16 pulses at 423.75 kHz (f_C/32) as shown in *Figure 18*.

Figure 19. Logic 1, low data rate, one subcarriers x2

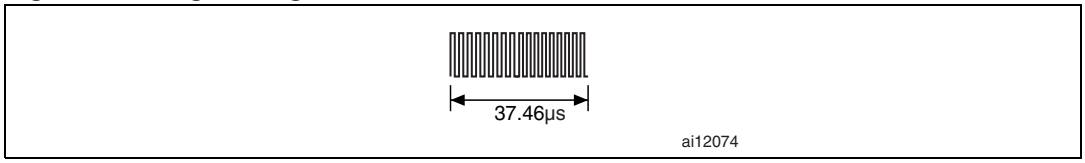


9.2 Bit coding using two subcarriers

9.3 High data rate

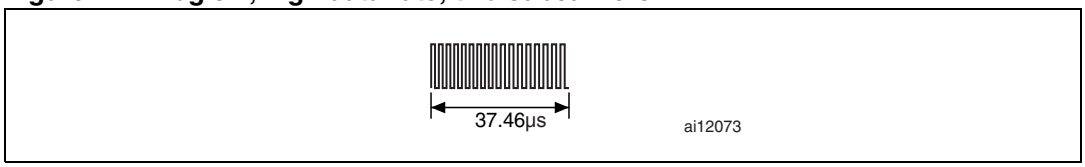
A logic 0 starts with 8 pulses at 423.75 kHz ($f_C/32$) followed by 9 pulses at 484.28 kHz ($f_C/28$) as shown in *Figure 20*. For the Fast commands, the x2 mode is not available.

Figure 20. Logic 0, high data rate, two subcarriers



A logic 1 starts with 9 pulses at 484.28 kHz ($f_C/28$) followed by 8 pulses at 423.75 kHz ($f_C/32$) as shown in *Figure 21*. For the Fast commands, the x2 mode is not available.

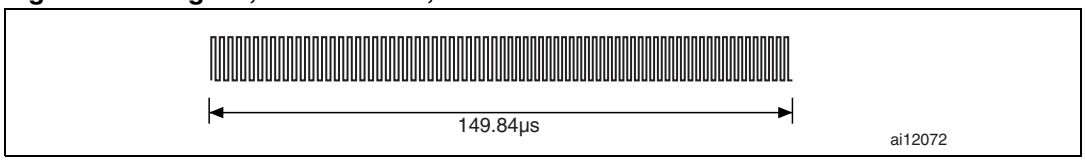
Figure 21. Logic 1, high data rate, two subcarriers



9.4 Low data rate

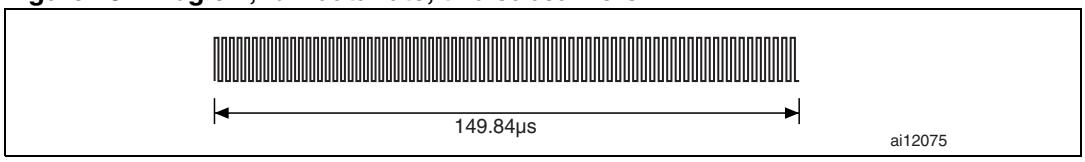
A logic 0 starts with 32 pulses at 423.75 kHz ($f_C/32$) followed by 36 pulses at 484.28 kHz ($f_C/28$) as shown in *Figure 22*. For the Fast commands, the x2 mode is not available.

Figure 22. Logic 0, low data rate, two subcarriers



A logic 1 starts with 36 pulses at 484.28 kHz ($f_C/28$) followed by 32 pulses at 423.75 kHz ($f_C/32$) as shown in *Figure 23*. For the Fast commands, the x2 mode is not available.

Figure 23. Logic 1, low data rate, two subcarriers



10 LRIS64K to VCD frames

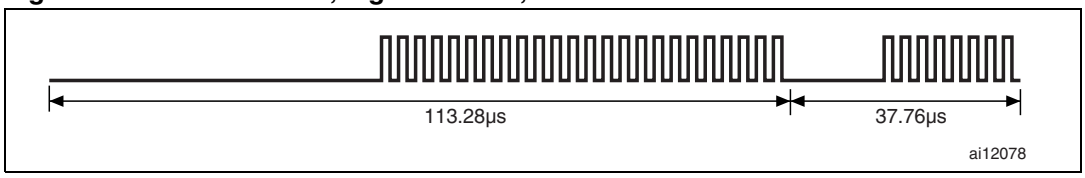
Frames are delimited by an SOF and an EOF. They are implemented using code violation. Unused options are reserved for future use. For the low data rate, the same subcarrier frequency or frequencies is/are used. In this case the number of pulses is multiplied by 4. For the Fast commands using one subcarrier, all pulse numbers and times are divided by 2.

10.1 SOF when using one subcarrier

10.2 High data rate

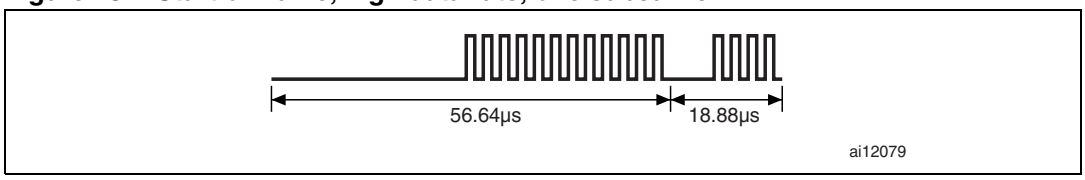
The SOF includes an unmodulated time of 56.64 µs, followed by 24 pulses at 423.75 kHz ($f_C/32$), and a logic 1 that consists of an unmodulated time of 18.88 µs followed by 8 pulses at 423.75 kHz as shown in *Figure 24*.

Figure 24. Start of frame, high data rate, one subcarrier



For the Fast commands, the SOF comprises an unmodulated time of 28.32 µs, followed by 12 pulses at 423.75 kHz ($f_C/32$), and a logic 1 that consists of an unmodulated time of 9.44µs followed by 4 pulses at 423.75 kHz as shown in *Figure 25*.

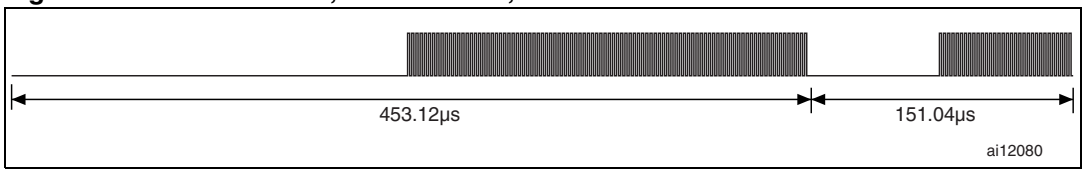
Figure 25. Start of frame, high data rate, one subcarrier x2



10.3 Low data rate

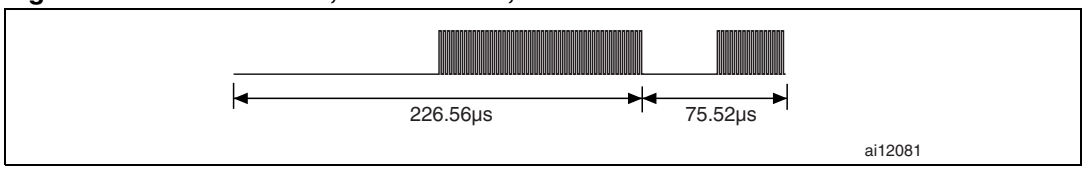
The SOF comprises an unmodulated time of 226.56 µs, followed by 96 pulses at 423.75 kHz ($f_C/32$), and a logic 1 that consists of an unmodulated time of 75.52 µs followed by 32 pulses at 423.75 kHz as shown in *Figure 26*.

Figure 26. Start of frame, low data rate, one subcarrier



For the Fast commands, the SOF comprises an unmodulated time of 113.28 µs, followed by 48 pulses at 423.75 kHz (f_C/32), and a logic 1 that includes an unmodulated time of 37.76 µs followed by 16 pulses at 423.75 kHz as shown in *Figure 27*.

Figure 27. Start of frame, low data rate, one subcarrier x2



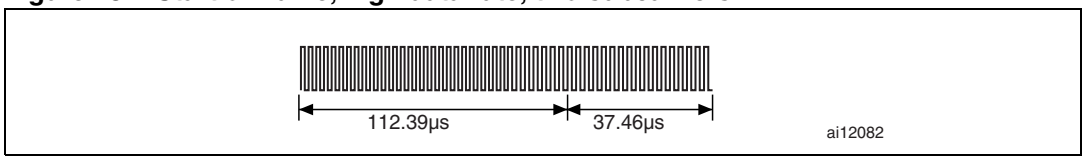
10.4 SOF when using two subcarriers

10.5 High data rate

The SOF comprises 27 pulses at 484.28 kHz (f_C/28), followed by 24 pulses at 423.75 kHz (f_C/32), and a logic 1 that includes 9 pulses at 484.28 kHz followed by 8 pulses at 423.75 kHz as shown in *Figure 28*.

For the Fast commands, the x2 mode is not available.

Figure 28. Start of frame, high data rate, two subcarriers

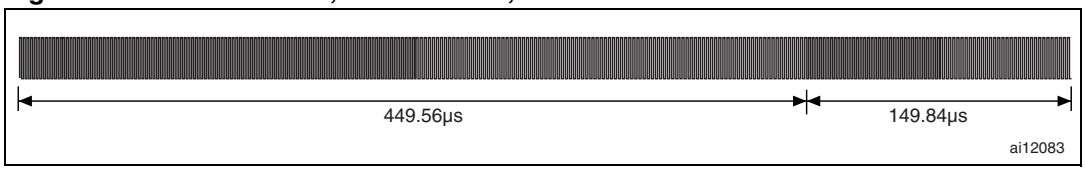


10.6 Low data rate

The SOF comprises 108 pulses at 484.28 kHz (f_C/28), followed by 96 pulses at 423.75 kHz (f_C/32), and a logic 1 that includes 36 pulses at 484.28 kHz followed by 32 pulses at 423.75 kHz as shown in *Figure 29*.

For the Fast commands, the x2 mode is not available.

Figure 29. Start of frame, low data rate, two subcarriers

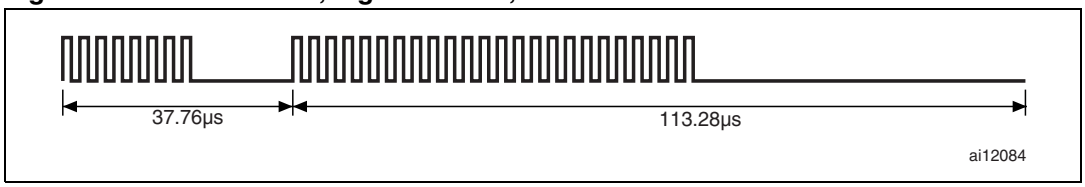


10.7 EOF when using one subcarrier

10.8 High data rate

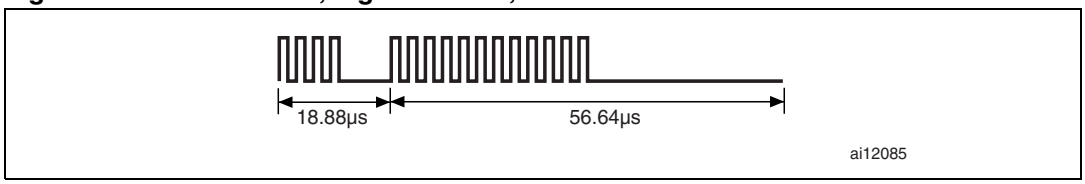
The EOF comprises a logic 0 that includes 8 pulses at 423.75 kHz and an unmodulated time of 18.88 µs, followed by 24 pulses at 423.75 kHz (f_C/32), and by an unmodulated time of 56.64 µs as shown in *Figure 30*.

Figure 30. End of frame, high data rate, one subcarriers



For the Fast commands, the EOF comprises a logic 0 that includes 4 pulses at 423.75 kHz and an unmodulated time of 9.44 µs, followed by 12 pulses at 423.75 kHz (f_C/32) and an unmodulated time of 37.76 µs as shown in *Figure 31*.

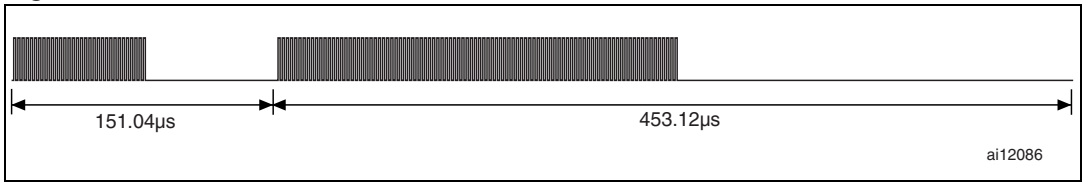
Figure 31. End of frame, high data rate, one subcarriers x2



10.9 Low data rate

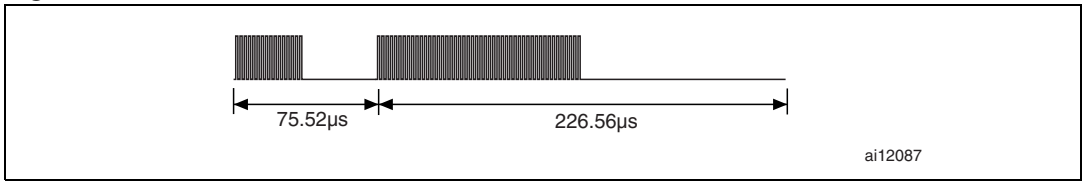
The EOF comprises a logic 0 that includes 32 pulses at 423.75 kHz and an unmodulated time of 75.52 µs, followed by 96 pulses at 423.75 kHz (f_C/32) and an unmodulated time of 226.56 µs as shown in *Figure 32*.

Figure 32. End of frame, low data rate, one subcarriers



For the Fast commands, the EOF comprises a logic 0 that includes 16 pulses at 423.75 kHz and an unmodulated time of 37.76 µs, followed by 48 pulses at 423.75 kHz (f_C/32) and an unmodulated time of 113.28 µs as shown in *Figure 33*.

Figure 33. End of frame, low data rate, one subcarriers x2



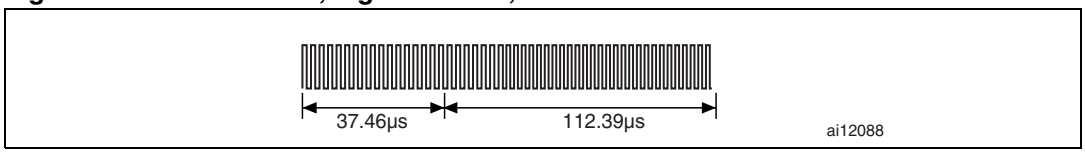
10.10 EOF when using two subcarriers

10.11 High data rate

The EOF comprises a logic 0 that includes 8 pulses at 423.75 kHz and 9 pulses at 484.28 kHz, followed by 24 pulses at 423.75 kHz (f_C/32) and 27 pulses at 484.28 kHz (f_C/28) as shown in *Figure 34*.

For the Fast commands, the x2 mode is not available.

Figure 34. End of frame, high data rate, two subcarriers

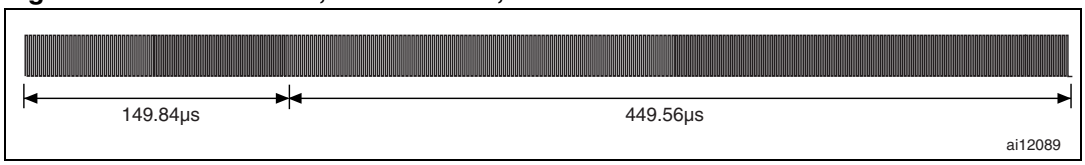


10.12 Low data rate

The EOF comprises a logic 0 that includes 32 pulses at 423.75 kHz and 36 pulses at 484.28 kHz, followed by 96 pulses at 423.75 kHz (f_C/32) and 108 pulses at 484.28 kHz (f_C/28) as shown in *Figure 35*.

For the Fast commands, the x2 mode is not available.

Figure 35. End of frame, low data rate, two subcarriers



11 Unique identifier (UID)

The LRIS64K is uniquely identified by a 64-bit Unique Identifier (UID). This UID complies with ISO/IEC 15963 and ISO/IEC 7816-6. The UID is a read-only code and comprises:

- 8 MSBs with a value of E0h
- The IC Manufacturer code of ST 02h, on 8 bits (ISO/IEC 7816-6/AM1)
- a Unique Serial Number on 48 bits

Table 12. UID format

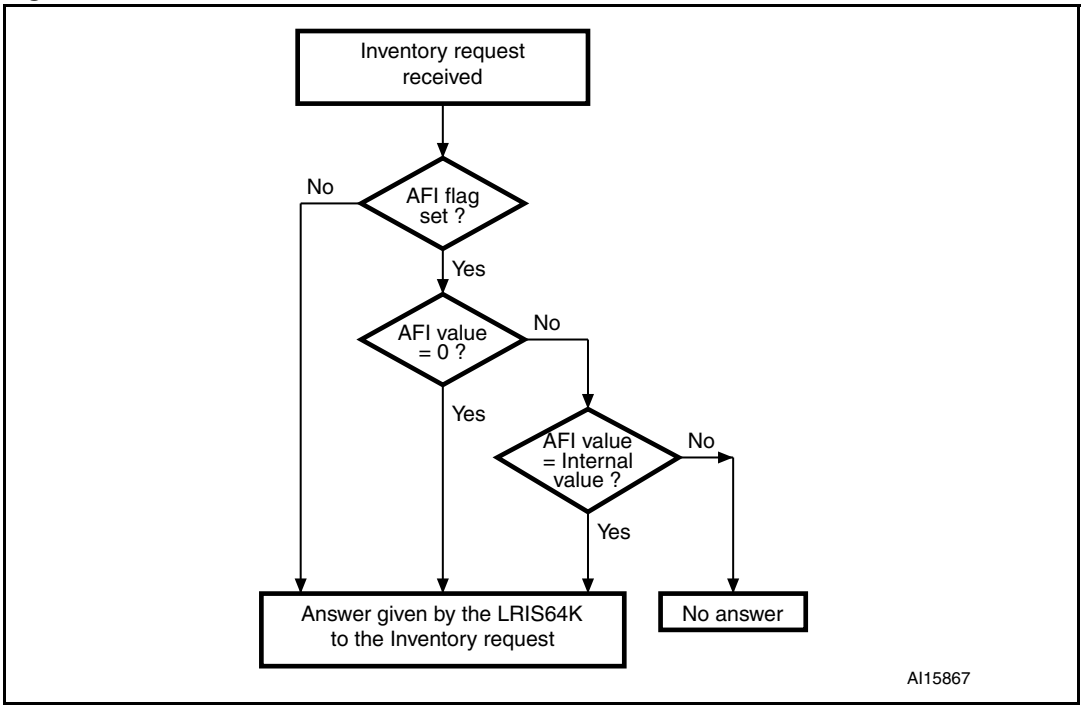
MSB		LSB
63 56	55 48	47 0
0xE0	0x02	Unique serial number

With the UID each LRIS64K can be addressed uniquely and individually during the anticollision loop and for one-to-one exchanges between a VCD and an LRIS64K.

12 Application family identifier (AFI)

The AFI (application family identifier) represents the type of application targeted by the VCD and is used to identify, among all the LRIS64Ks present, only the LRIS64Ks that meet the required application criteria.

Figure 36. LRIS64K decision tree for AFI



The AFI is programmed by the LRIS64K issuer (or purchaser) in the AFI register. Once programmed and Locked, it can no longer be modified.

The most significant nibble of the AFI is used to code one specific or all application families.

The least significant nibble of the AFI is used to code one specific or all application subfamilies. Subfamily codes different from 0 are proprietary.

(See ISO/IEC 15693-3 documentation)

13 Data storage format identifier (DSFID)

The data storage format identifier indicates how the data is structured in the LRIS64K memory. The logical organization of data can be known instantly using the DSFID. It can be programmed and locked using the Write DSFID and Lock DSFID commands.

13.1 CRC

The CRC used in the LRIS64K is calculated as per the definition in ISO/IEC 13239. The initial register contents are all ones: “FFFF”.

The two-byte CRC are appended to each request and response, within each frame, before the EOF. The CRC is calculated on all the bytes after the SOF up to the CRC field.

Upon reception of a request from the VCD, the LRIS64K verifies that the CRC value is valid. If it is invalid, the LRIS64K discards the frame and does not answer to the VCD.

Upon reception of a Response from the LRIS64K, it is recommended that the VCD verifies whether the CRC value is valid. If it is invalid, actions to be performed are left to the discretion of the VCD designer.

The CRC is transmitted least significant byte first. Each byte is transmitted least significant bit first.

Table 13. CRC transmission rules

LSByte		MSByte	
LSBit	MSBit	LSBit	MSBit
CRC 16 (8 bits)		CRC 16 (8 bits)	

14 LRIS64K protocol description

The transmission protocol (or simply protocol) defines the mechanism used to exchange instructions and data between the VCD and the LRIS64K, in both directions. It is based on the concept of “VCD talks first”.

This means that an LRIS64K will not start transmitting unless it has received and properly decoded an instruction sent by the VCD. The protocol is based on an exchange of:

- a request from the VCD to the LRIS64K
- a response from the LRIS64K to the VCD

Each request and each response are contained in a frame. The frame delimiters (SOF, EOF) are described in *Section 10: LRIS64K to VCD frames*.

Each request consists of:

- a request SOF (see *Figure 9* and *Figure 10*)
- flags
- a command code
- parameters, depending on the command
- application data
- a 2-byte CRC
- a request EOF (see *Figure 11*)

Each response consists of:

- an answer SOF (see *Figure 24* to *Figure 29*)
- flags
- parameters, depending on the command
- application data
- a 2-byte CRC
- an answer EOF (see *Figure 30* to *Figure 35*)

The protocol is bit-oriented. The number of bits transmitted in a frame is a multiple of eight (8), that is an integer number of bytes.

A single-byte field is transmitted least significant bit (LSBit) first. A multiple-byte field is transmitted least significant byte (LSByte) first, each byte is transmitted least significant bit (LSBit) first.

The setting of the flags indicates the presence of the optional fields. When the flag is set (to one), the field is present. When the flag is reset (to zero), the field is absent.

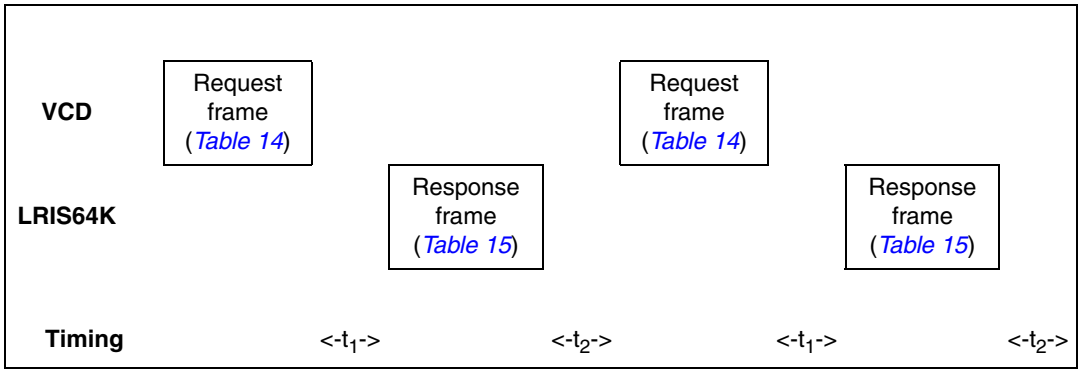
Table 14. VCD request frame format

Request SOF	Request_flags	Command code	Parameters	Data	2-byte CRC	Request EOF

Table 15. LRIS64K Response frame format

Response SOF	Response_flags	Parameters	Data	2-byte CRC	Response EOF

Figure 37. LRIS64K protocol timing



15 LRIS64K states

An LRIS64K can be in one of 4 states:

- Power-off
- Ready
- Quiet
- Selected

Transitions between these states are specified in *Figure 38: LRIS64K state transition diagram* and *Table 16: LRIS64K response depending on Request_flags*.

15.1 Power-off state

The LRIS64K is in the Power-off state when it does not receive enough energy from the VCD.

15.2 Ready state

The LRIS64K is in the Ready state when it receives enough energy from the VCD. When in the Ready state, the LRIS64K answers any request where the Select_flag is not set.

15.3 Quiet state

When in the Quiet state, the LRIS64K answers any request except for Inventory requests with the Address_flag set.

15.4 Selected state

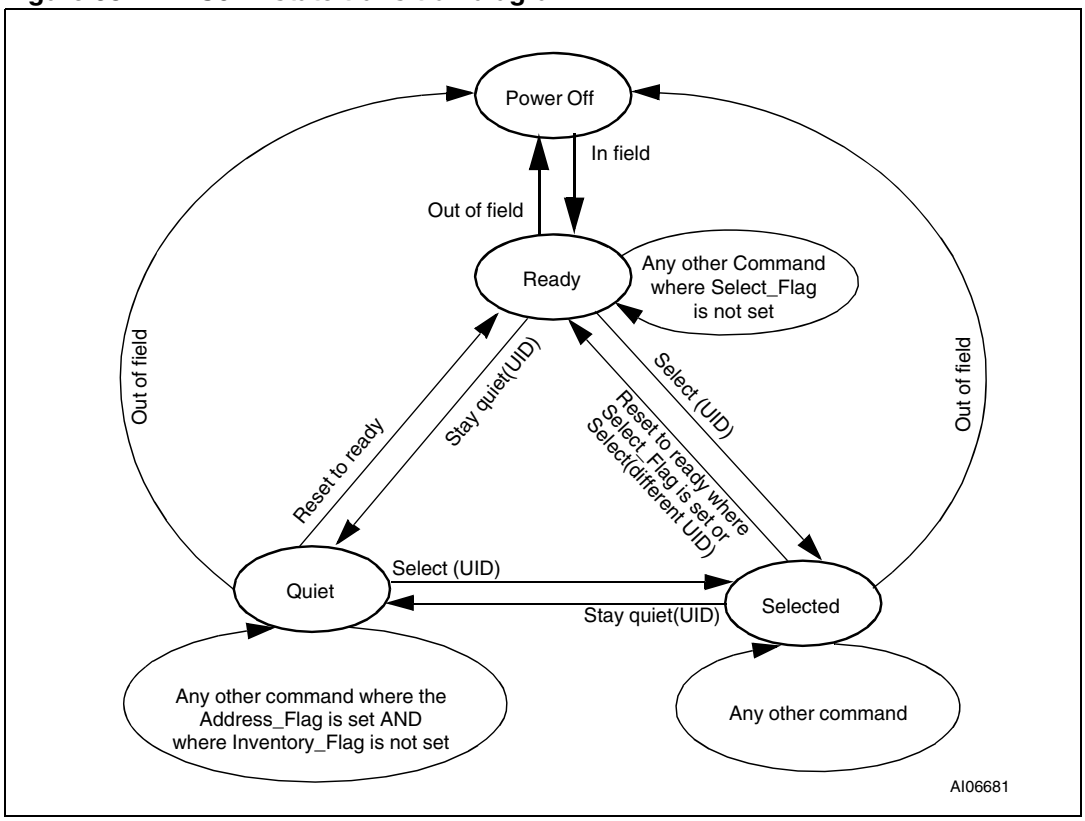
In the Selected state, the LRIS64K answers any request in all modes (see *Section 16: Modes*):

- Request in Select mode with the Select_flag set
- Request in Addressed mode if the UID matches
- Request in Non-Addressed mode as it is the mode for general requests

Table 16. LRIS64K response depending on Request_flags

Flags	Address_flag		Select_flag	
	1 Addressed	0 Non addressed	1 Selected	0 Non selected
LRIS64K in Ready or Selected state (Devices in Quiet state do not answer)		X		X
LRIS64K in Selected state		X	X	
LRIS64K in Ready, Quiet or Selected state (the device which matches the UID)	X			X
Error (03h)	X		X	

Figure 38. LRIS64K state transition diagram



1. The intention of the state transition method is that only one LRIS64K should be in the selected state at a time.

16 Modes

The term “mode” refers to the mechanism used in a request to specify the set of LRIS64Ks that will answer the request.

16.1 Addressed mode

When the Address_flag is set to 1 (Addressed mode), the request contains the Unique ID (UID) of the addressed LRIS64K.

Any LRIS64K that receives a request with the Address_flag set to 1 compares the received Unique ID to its own. If it matches, then the LRIS64K executes the request (if possible) and returns a response to the VCD as specified in the command description.

If the UID does not match, then it remains silent.

16.2 Non-addressed mode (general request)

When the Address_flag is cleared to 0 (Non-Addressed mode), the request does not contain a Unique ID. Any LRIS64K receiving a request with the Address_flag cleared to 0 executes it and returns a response to the VCD as specified in the command description.

16.3 Select mode

When the Select_flag is set to 1 (Select mode), the request does not contain an LRIS64K Unique ID. The LRIS64K in the Selected state that receives a request with the Select_flag set to 1 executes it and returns a response to the VCD as specified in the command description.

Only LRIS64Ks in the Selected state answer a request where the Select_flag set to 1.

The system design ensures in theory that only one LRIS64K can be in the Select state at a time.

17 Request format

The request consists of:

- an SOF
- flags
- a command code
- parameters and data
- a CRC
- an EOF

Table 17. General request format

SOF	Request_flags	Command code	Parameters	Data	CRC	EOF

17.1 Request flags

In a request, the “flags” field specifies the actions to be performed by the LRIS64K and whether corresponding fields are present or not.

The flags field consists of eight bits. The bit 3 (Inventory_flag) of the request flag defines the contents of the 4 MSBs (bits 5 to 8). When bit 3 is reset (0), bits 5 to 8 define the LRIS64K selection criteria. When bit 3 is set (1), bits 5 to 8 define the LRIS64K Inventory parameters.

Table 18. Definition of request flags 1 to 4

Bit No	Flag	Level	Description
Bit 1	Subcarrier_flag(1)	0	A single subcarrier frequency is used by the LRIS64K
		1	Two subcarrier are used by the LRIS64K
Bit 2	Data_rate_flag(2)	0	Low data rate is used
		1	High data rate is used
Bit 3	Inventory_flag	0	The meaning of flags 5 to 8 is described in *Table 19*
		1	The meaning of flags 5 to 8 is described in *Table 20*
Bit 4	Protocol_extension_flag	0	No Protocol format extension
		1	Protocol format extension

1. Subcarrier_flag refers to the LRIS64K-to-VCD communication.
2. Data_rate_flag refers to the LRIS64K-to-VCD communication

Table 19. Request flags 5 to 8 when Bit 3 = 0

Bit No	Flag	Level	Description
Bit 5	Select flag(1)	0	Request is executed by any LRIS64K according to the setting of Address_flag
		1	Request is executed only by the LRIS64K in Selected state
Bit 6	Address flag(1)	0	Request is not addressed. UID field is not present. The request is executed by all LRIS64Ks.
		1	Request is addressed. UID field is present. The request is executed only by the LRIS64K whose UID matches the UID specified in the request.
Bit 7	Option flag	0	Option not activated.
		1	Option activated.
Bit 8	RFU	0	

1. If the Select_flag is set to 1, the Address_flag is set to 0 and the UID field is not present in the request.

Table 20. Request flags 5 to 8 when Bit 3 = 1

Bit No	Flag	Level	Description
Bit 5	AFI flag	0	AFI field is not present
		1	AFI field is present
Bit 6	Nb_slots flag	0	16 slots
		1	1 slot
Bit 7	Option flag	0	
Bit 8	RFU	0	

18 Response format

The response consists of:

- an SOF
- flags
- parameters and data
- a CRC
- an EOF

Table 21. General response format

SOF	Response_flags	Parameters	Data	CRC	EOF

18.1 Response flags

In a response, the flags indicate how actions have been performed by the LRIS64K and whether corresponding fields are present or not. The response flags consist of eight bits.

Table 22. Definitions of response flags 1 to 8

Bit No	Flag	Level	Description
Bit 1	Error_flag	0	No error
		1	Error detected. Error code is in the "Error" field.
Bit 2	RFU	0	
Bit 3	RFU	0	
Bit 4	Extension flag	0	No extension
Bit 5	RFU	0	
Bit 6	RFU	0	
Bit 7	RFU	0	
Bit 8	RFU	0	

18.2 Response error code

If the Error_flag is set by the LRIS64K in the response, the Error code field is present and provides information about the error that occurred.

Error codes not specified in *Table 23* are reserved for future use.

Table 23. Response error code definition

Error code	Meaning
02h	The command is not recognized, for example a format error occurred
03h	The option is not supported
0Fh	Error with no information given
10h	The specified block is not available
11h	The specified block is already locked and thus cannot be locked again
12h	The specified block is locked and its contents cannot be changed.
13h	The specified block was not successfully programmed
14h	The specified block was not successfully locked
15h	The specified block is read-protected

19 Anticollision

The purpose of the anticollision sequence is to inventory the LRIS64Ks present in the VCD field using their unique ID (UID).

The VCD is the master of communications with one or several LRIS64Ks. It initiates LRIS64K communication by issuing the Inventory request.

The LRIS64K sends its response in the determined slot or does not respond.

19.1 Request parameters

When issuing the Inventory Command, the VCD:

- sets the Nb_slots_flag as desired
- adds the mask length and the mask value after the command field
- The mask length is the number of significant bits of the mask value.
- The mask value is contained in an integer number of bytes. The mask length indicates the number of significant bits. LSB is transmitted first
- If the mask length is not a multiple of 8 (bits), as many 0-bits as required will be added to the mask value MSB so that the mask value is contained in an integer number of bytes
- The next field starts at the next byte boundary.

Table 24. Inventory request format

MSB SOF	Request _flags	Command	Optional AFI(1)	Mask length	Mask value	CRC	LSB EOF
	8 bits	8 bits	8 bits	8 bits	0 to 8 bytes	16 bits	

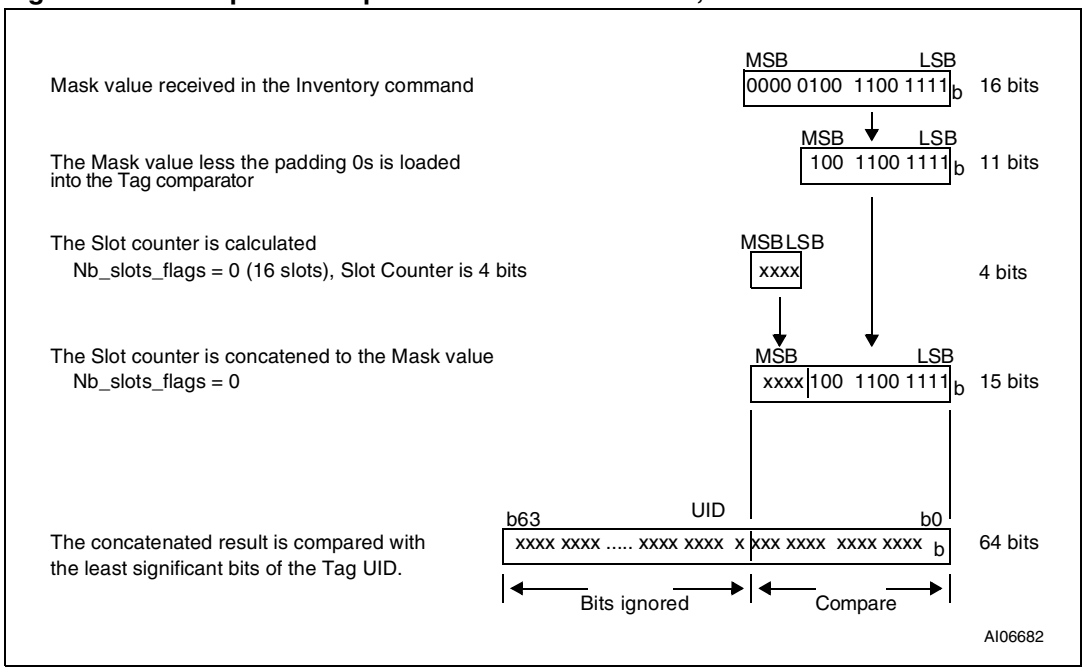
1. Gray means that the field is optional.

In the example of the *Table 25* and *Figure 39*, the mask length is 11 bits. Five 0-bits are added to the mask value MSB. The 11-bit Mask and the current slot number are compared to the UID.

Table 25. Example of the addition of 0-bits to an 11-bit mask value

(b_{15}) MSB	LSB (b_0)
0000 0	100 1100 1111
0-bits added	11-bit mask value

Figure 39. Principle of comparison between the mask, the slot number and the UID



The AFI field is present if the AFI_flag is set.

The pulse is generated according to the definition of the EOF in ISO/IEC 15693-2.

The first slot starts immediately after the reception of the request EOF. To switch to the next slot, the VCD sends an EOF.

The following rules and restrictions apply:

- if no LRIS64K answer is detected, the VCD may switch to the next slot by sending an EOF,
- if one or more LRIS64K answers are detected, the VCD waits until the complete frame has been received before sending an EOF for switching to the next slot.

20 Request processing by the LRIS64K

Upon reception of a valid request, the LRIS64K performs the following algorithm:

- NbS is the total number of slots (1 or 16)
- SN is the current slot number (0 to 15)
- LSB (value, n) function returns the n Less Significant Bits of value
- MSB (value, n) function returns the n Most Significant Bits of value
- “&” is the concatenation operator
- Slot_Frame is either an SOF or an EOF

```
SN = 0
if (Nb_slots_flag)
   then NbS = 1
        SN_length = 0
        endif
   else NbS = 16
        SN_length = 4
        endif

label1:
if LSB(UID, SN_length + Mask_length) =
  LSB(SN,SN_length)&LSB(Mask,Mask_length)
   then answer to inventory request
        endif

wait (Slot_Frame)

if Slot_Frame = SOF
   then Stop Anticollision
        decode/process request
        exit
        endif

if Slot_Frame = EOF
   if SN < NbS-1
     then SN = SN + 1
          goto label1
          exit
          endif
   endif
```

21 Explanation of the possible cases

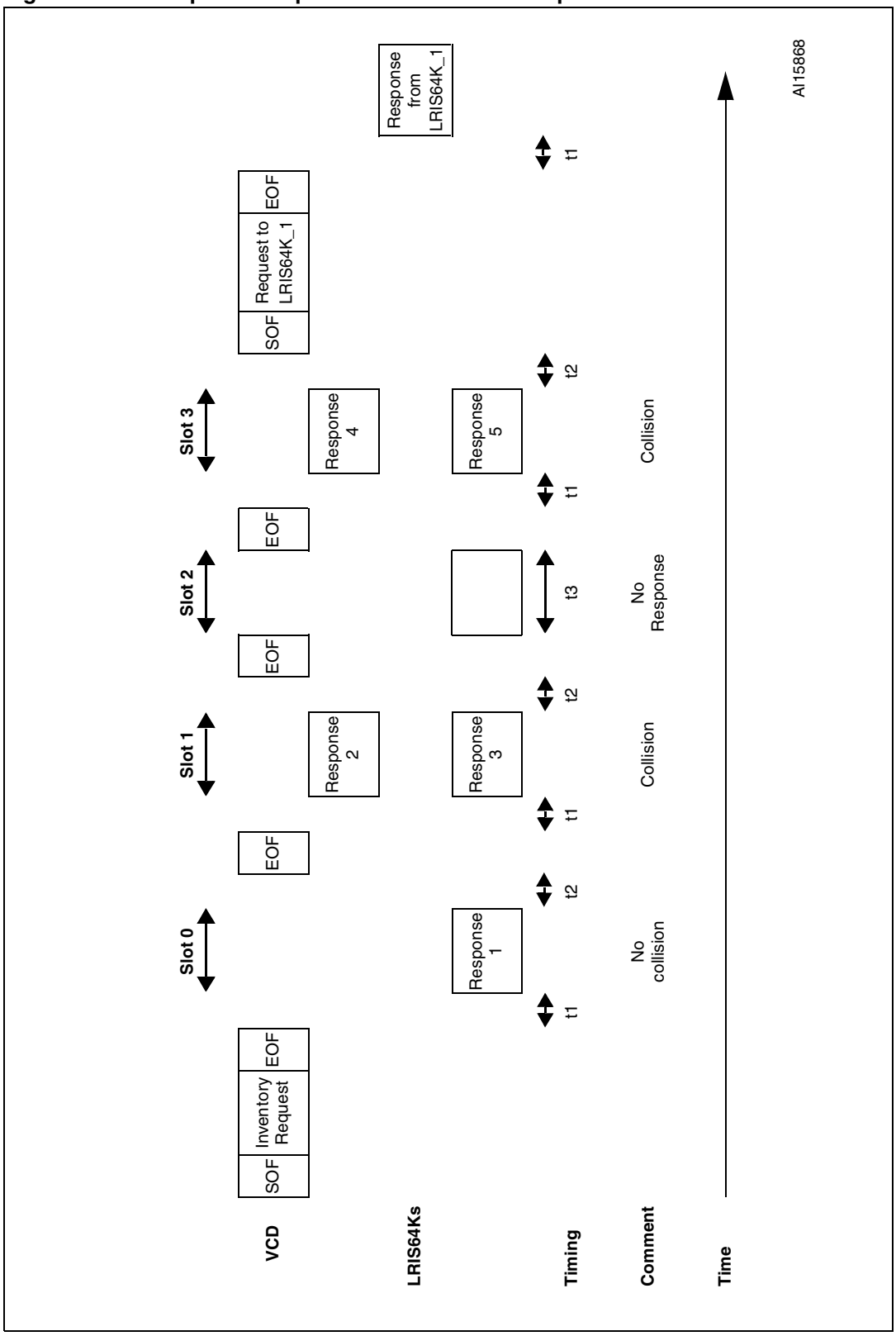
Figure 40 summarizes the main possible cases that can occur during an anticollision sequence when the slot number is 16.

The different steps are:

- The VCD sends an Inventory request, in a frame terminated by an EOF. The number of slots is 16.
- LRIS64K_1 transmits its response in Slot 0. It is the only one to do so, therefore no collision occurs and its UID is received and registered by the VCD;
- The VCD sends an EOF in order to switch to the next slot.
- In slot 1, two LRIS64Ks, LRIS64K_2 and LRIS64K_3 transmit a response, thus generating a collision. The VCD records the event and remembers that a collision was detected in Slot 1.
- The VCD sends an EOF in order to switch to the next slot.
- In Slot 2, no LRIS64K transmits a response. Therefore the VCD does not detect any LRIS64K SOF and decides to switch to the next slot by sending an EOF.
- In slot 3, there is another collision caused by responses from LRIS64K_4 and LRIS64K_5
- The VCD then decides to send a request (for instance a Read Block) to LRIS64K_1 whose UID has already been correctly received.
- All LRIS64Ks detect an SOF and exit the anticollision sequence. They process this request and since the request is addressed to LRIS64K_1, only LRIS64K_1 transmits a response.
- All LRIS64Ks are ready to receive another request. If it is an Inventory command, the slot numbering sequence restarts from 0.

Note: The decision to interrupt the anticollision sequence is made by the VCD. It could have continued to send EOFs until Slot 16 and only then sent the request to LRIS64K_1.

Figure 40. Description of a possible anticollision sequence



22 Inventory Initiated command

The LRIS64K provides a special feature to improve the inventory time response of moving tags using the Initiate_flag value. This flag, controlled by the Initiate command, allows tags to answer to Inventory Initiated commands.

For applications in which multiple tags are moving in front of a reader, it is possible to miss tags using the standard inventory command. The reason is that the inventory sequence has to be performed on a global tree search. For example, a tag with a particular UID value may have to wait the run of a long tree search before being inventoried. If the delay is too long, the tag may be out of the field before it has been detected.

Using the Initiate command, the inventory sequence is optimized. When multiple tags are moving in front of a reader, the ones which are within the reader field will be initiated by the Initiate command. In this case, a small batch of tags will answer to the Inventory Initiated command which will optimize the time necessary to identify all the tags. When finished, the reader has to issue a new Initiate command in order to initiate a new small batch of tags which are new inside the reader field.

It is also possible to reduce the inventory sequence time using the Fast Initiate and Fast Inventory Initiated commands. These commands allow the LRIS64Ks to increase their response data rate by a factor of 2, up to 53 Kbit/s.

23 Timing definition

23.1 t_1: LRIS64K response delay

Upon detection of the rising edge of the EOF received from the VCD, the LRIS64K waits for a time t_{1nom} before transmitting its response to a VCD request or before switching to the next slot during an inventory process. Values of t_1 are given in *Table 26*. The EOF is defined in *Figure 11 on page 26*.

23.2 t_2: VCD new request delay

t_2 is the time after which the VCD may send an EOF to switch to the next slot when one or more LRIS64K responses have been received during an Inventory command. It starts from the reception of the EOF from the LRIS64Ks.

The EOF sent by the VCD may be either 10% or 100% modulated regardless of the modulation index used for transmitting the VCD request to the LRIS64K.

t_2 is also the time after which the VCD may send a new request to the LRIS64K as described in *Table 37: LRIS64K protocol timing*.

Values of t_2 are given in *Table 26*.

23.3 t_3: VCD new request delay in the absence of a response from the LRIS64K

t_3 is the time after which the VCD may send an EOF to switch to the next slot when no LRIS64K response has been received.

The EOF sent by the VCD may be either 10% or 100% modulated regardless of the modulation index used for transmitting the VCD request to the LRIS64K.

From the time the VCD has generated the rising edge of an EOF:

- If this EOF is 100% modulated, the VCD waits a time at least equal to t_{3min} before sending a new EOF.
- If this EOF is 10% modulated, the VCD waits a time at least equal to the sum of t_{3min} + the LRIS64K nominal response time (which depends on the LRIS64K data rate and subcarrier modulation mode) before sending a new EOF.

Table 26. Timing values(1)

	Minimum (min) values	Nominal (nom) values	Maximum (max) values
t_1	318.6 µs	320.9 µs	323.3 µs
t_2	309.2 µs	No t_{nom}	No t_{max}
t_3	t_{1max}(2) + t_{SOF}(3)	No t_{nom}	No t_{max}

1. *The tolerance of specific timings is ± 32/f_C.*
2. t_{1max} does not apply for write alike requests. Timing conditions for write alike requests are defined in the command description.
3. t_{SOF} is the time taken by the LRIS64K to transmit an SOF to the VCD. t_{SOF} depends on the current data rate: High data rate or Low data rate.

24 Commands codes

The LRIS64K supports the commands described in this section. Their codes are given in *Table 27*.

Table 27. Command codes

Command code standard	Function
01h	Inventory
02h	Stay Quiet
20h	Read Single Block
21h	Write Single Block
23h	Read Multiple Block
25h	Select
26h	Reset to Ready
27h	Write AFI
28h	Lock AFI
29h	Write DSFID
2Ah	Lock DSFID
2Bh	Get System Info

Command code custom	Function
2Ch	Get Multiple Block Security Status
B1h	Write-sector Password
B2h	Lock-sector Password
B3h	Present-sector Password
C0h	Fast Read Single Block
C1h	Fast Inventory Initiated
C2h	Fast Initiate
C3h	Fast Read Multiple Block
D1h	Inventory Initiated
D2h	Initiate

24.1 Inventory

When receiving the Inventory request, the LRIS64K runs the anticollision sequence. The Inventory_flag is set to 1. The meaning of flags 5 to 8 is shown in *Table 20: Request flags 5 to 8 when Bit 3 = 1*.

The request contains:

- the flags,
- the Inventory command code (see *Table 27: Command codes*)
- the AFI if the AFI flag is set
- the mask length
- the mask value
- the CRC

The LRIS64K does not generate any answer in case of error.

Table 28. Inventory request format

Request SOF	Request_flags	Inventory	Optional AFI(1)	Mask length	Mask value	CRC16	Request EOF
	8 bits	01h	8 bits	8 bits	0 - 64 bits	16 bits	

1. Gray means that the field is optional.

The response contains:

- the flags
- the Unique ID

Table 29. Inventory response format

Response SOF	Response_ flags	DSFID	UID	CRC16	Response EOF
	8 bits	8 bits	64 bits	16 bits	

During an Inventory process, if the VCD does not receive an RF LRIS64K response, it waits a time t_3 before sending an EOF to switch to the next slot. t_3 starts from the rising edge of the request EOF sent by the VCD.

- If the VCD sends a 100% modulated EOF, the minimum value of t_3 is:
  $t_3min = 4384/f_C$ (323.3µs) + t_{SOF}
- If the VCD sends a 10% modulated EOF, the minimum value of t_3 is:
  $t_3min = 4384/f_C$ (323.3µs) + t_{NRT}

where:

- t_{SOF} is the time required by the LRIS64K to transmit an SOF to the VCD
- t_{NRT} is the nominal response time of the LRIS64K

t_{NRT} and t_{SOF} are dependent on the LRIS64K-to-VCD data rate and subcarrier modulation mode.

24.2 Stay Quiet

Command code = 0x02

On receiving the Stay Quiet command, the LRIS64K enters the Quiet State if no error occurs, and does NOT send back a response. There is NO response to the Stay Quiet command even if an error occurs.

When in the Quiet state:

- the LRIS64K does not process any request if the Inventory_flag is set,
- the LRIS64K processes any Addressed request

The LRIS64K exits the Quiet State when:

- it is reset (power off),
- receiving a Select request. It then goes to the Selected state,
- receiving a Reset to Ready request. It then goes to the Ready state.

Table 30. Stay Quiet request format

Request SOF	Request flags	Stay Quiet	UID	CRC16	Request EOF
	8 bits	02h	64 bits	16 bits	

The Stay Quiet command must always be executed in Addressed mode (Select_flag is reset to 0 and Address_flag is set to 1).

Figure 41. Stay Quiet frame exchange between VCD and LRIS64K

24.3 Read Single Block

On receiving the Read Single Block command, the LRIS64K reads the requested block and sends back its 32-bit value in the response. The Protocol_extention_flag should be set to 1 for the LRIS64K to operate correctly. If the Protocol_extention_flag is at 0, the LRIS64K answers with an error code. The Option_flag is supported.

Table 31. Read Single Block request format

Request SOF	Request_ flags	Read Single Block	UID(1)	Block number	CRC16	Request EOF
	8 bits	20h	64 bits	16 bits	16 bits	

1. Gray means that the field is optional.

Request parameters:

- Option_flag
- UID (optional)
- Block number

Table 32. Read Single Block response format when Error_flag is NOT set

Response SOF	Response_ flags	Sector security status(1)	Data	CRC16	Response EOF
	8 bits	8 bits	32 bits	16 bits	

1. Gray means that the field is optional.

Response parameters:

- Sector security status if Option_flag is set (see *Table 33: Sector security status*)
- 4 bytes of block data

Table 33. Sector security status

b_7 b_6 b_5 b_4 b_3	b_2	b_1	b_0
Reserved for future use. All at 0	password control bits	Read / Write protection bits	0: Current sector not locked 1: Current sector locked

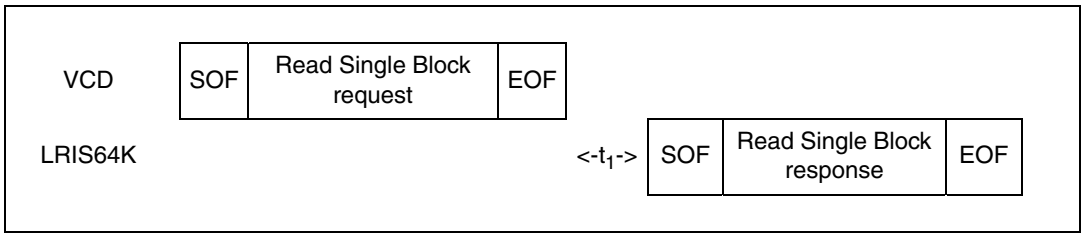
Table 34. Read Single Block response format when Error_flag is set

Response SOF	Response_ flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 10h: the specified block is not available
  - 15h: the specified block is read-protected

Figure 42. Read Single Block frame exchange between VCD and LRIS64K



24.4 Write Single Block

On receiving the Write Single Block command, the LRIS64K writes the data contained in the request to the requested block and reports whether the write operation was successful in the response. The Protocol_extention_flag should be set to 1 for the LRIS64K to operate correctly. If the Protocol_extention_flag is at 0, the LRIS64K answers with an error code. The Option_flag is supported.

During write cycle W_t, there should be no modulation (neither 100% nor 10%). Otherwise, the LRIS64K may not program correctly the data into the memory. The W_t time is equal to $t_{1nom} + 18 \times 302$ µs.

Table 35. Write Single Block request format

Request SOF	Request_ flags	Write Single Block	UID(1)	Block number	Data	CRC16	Request EOF
	8 bits	21h	64 bits	16 bits	32 bits	16 bits	

1. Gray means that the field is optional.

Request parameters:

- UID (optional)
- Block number
- Data

Table 36. Write Single Block response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
	8 bits	16 bits	

Response parameter:

- No parameter. The response is send back after the writing cycle.

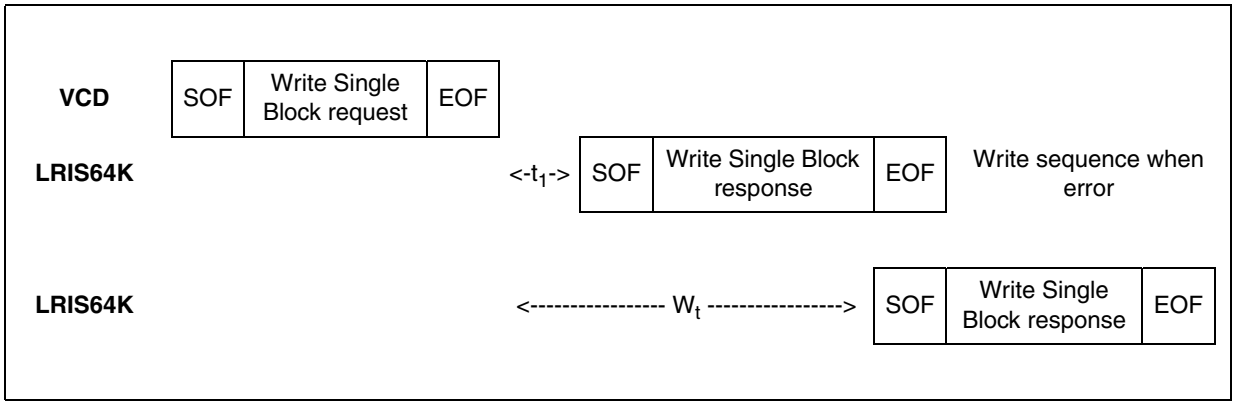
Table 37. Write Single Block response format when Error_flag is set

Response SOF	Response_ flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 10h: the specified block is not available
  - 12h: the specified block is locked and its contents cannot be changed.
  - 13h: the specified block was not successfully programmed

Figure 43. Write Single Block frame exchange between VCD and LRIS64K



24.5 Read Multiple Block

When receiving the Read Multiple Block command, the LRIS64K reads the selected blocks and sends back their value in multiples of 32 bits in the response. The blocks are numbered from '00h to '7FFh' in the request and the value is minus one (–1) in the field. For example, if the “number of blocks” field contains the value 06h, 7 blocks are read. The maximum number of blocks is fixed at 32 assuming that they are all located in the same sector. If the number of blocks overlaps sectors, the LRIS64K returns an error code.
The Protocol_extention_flag should be set to 1 for the LRIS64K to operate correctly. If the Protocol_extention_flag is at 0, the LRIS64K answers with an error code.
The Option_flag is supported.

Table 38. Read Multiple Block request format

Request SOF	Request_ flags	Read Multiple Block	UID(1)	First block number	Number of blocks	CRC16	Request EOF
	8 bits	23h	64 bits	16 bits	8 bits	16 bits	

1. Gray means that the field is optional.

Request parameters:

- Option_flag
- UID (optional)
- First block number
- Number of blocks

Table 39. Read Multiple Block response format when Error_flag is NOT set

Response SOF	Response_ flags	Sector security status(1)	Data	CRC16	Response EOF
	8 bits	8 bits(2)	32 bits(2)	16 bits	

1. Gray means that the field is optional.
2. Repeated as needed.

Response parameters:

- Sector security status if Option_flag is set (see *Table 40: Sector security status*)
- N blocks of data

Table 40. Sector security status

b_7 b_6 b_5 b_4 b_3	b_2	b_1	b_0
Reserved for future use. All at 0	password control bits	Read / Write protection bits	0: Current sector not locked 1: Current sector locked

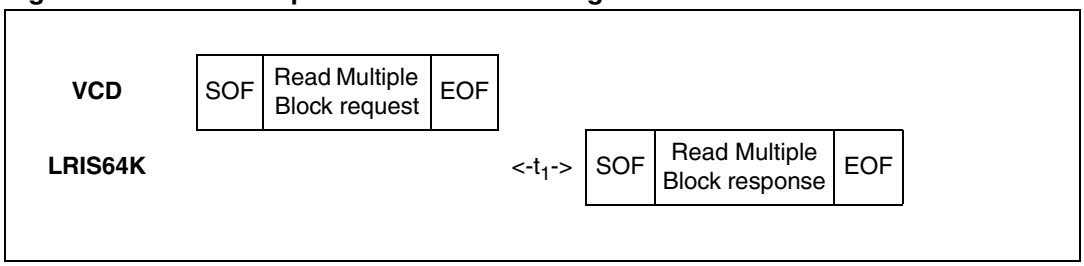
Table 41. Read Multiple Block response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 10h: the specified block is not available
  - 15h: the specified block is read-protected

Figure 44. Read Multiple Block frame exchange between VCD and LRIS64K



24.6 Select

When receiving the Select command:

- if the UID is equal to its own UID, the LRIS64K enters or stays in the Selected state and sends a response.
- if the UID does not match its own, the selected LRIS64K returns to the Ready state and does not send a response.

The LRIS64K answers an error code only if the UID is equal to its own UID. If not, no response is generated. If an error occurs, the LRIS64K remains in its current state.

Table 42. Select request format

Request SOF	Request_ flags	Select	UID	CRC16	Request EOF
	8 bits	25h	64 bits	16 bits	

Request parameter:

- UID

Table 43. Select Block response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
	8 bits	16 bits	

Response parameter:

- No parameter.

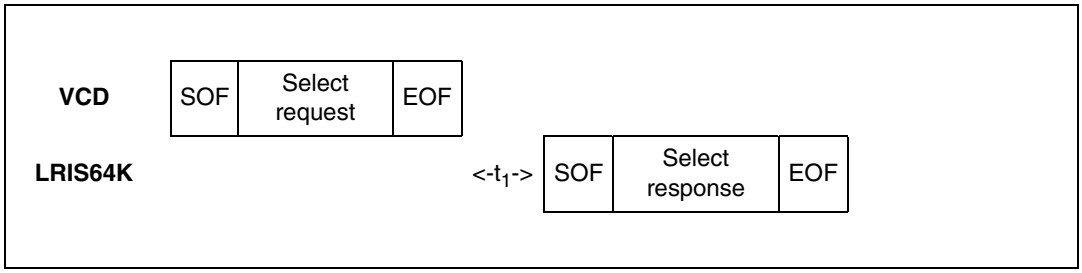
Table 44. Select response format when Error_flag is set

Response SOF	Response_ flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported
  - 0Fh: error with no information given

Figure 45. Select frame exchange between VCD and LRIS64K



24.7 Reset to Ready

On receiving a Reset to Ready command, the LRIS64K returns to the Ready state if no error occurs. In the Addressed mode, the LRIS64K answers an error code only if the UID is equal to its own UID. If not, no response is generated.

Table 45. Reset to Ready request format

Request SOF	Request_ flags	Reset to Ready	UID(1)	CRC16	Request EOF
	8 bits	26h	64 bits	16 bits	

1. Gray means that the field is optional.

Request parameter:

- UID (optional)

Table 46. Reset to Ready response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
	8 bits	16 bits	

Response parameter:

- No parameter

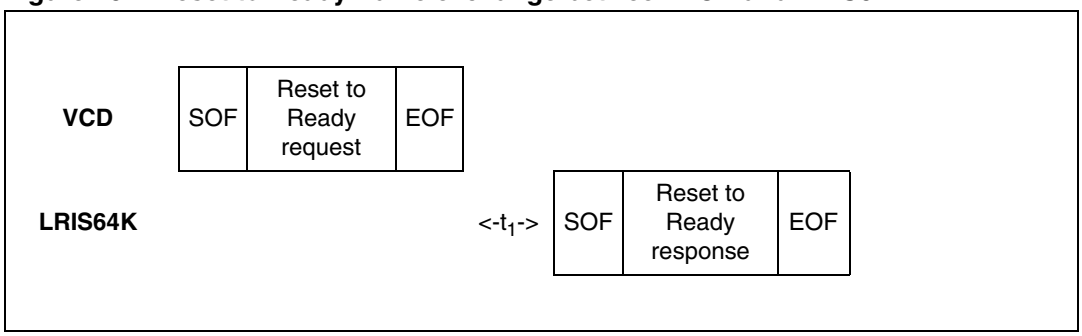
Table 47. Reset to ready response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported
  - 0Fh: error with no information given

Figure 46. Reset to Ready frame exchange between VCD and LRIS64K



24.8 Write AFI

On receiving the Write AFI request, the LRIS64K programs the 8-bit AFI value to its memory. The Option_flag is supported.

During write cycle W_t, there should be no modulation (neither 100% nor 10%). Otherwise, the LRIS64K may not write correctly the AFI value into the memory. The W_t time is equal to t_{1nom} + 18 × 302 µs.

Table 48. Write AFI request format

Request SOF	Request _flags	Write AFI	UID(1)	AFI	CRC16	Request EOF
	8 bits	27h	64 bits	8 bits	16 bits	

1. Gray means that the field is optional.

Request parameter:

- UID (optional)
- AFI

Table 49. Write AFI response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
	8 bits	16 bits	

Response parameter:

- No parameter.

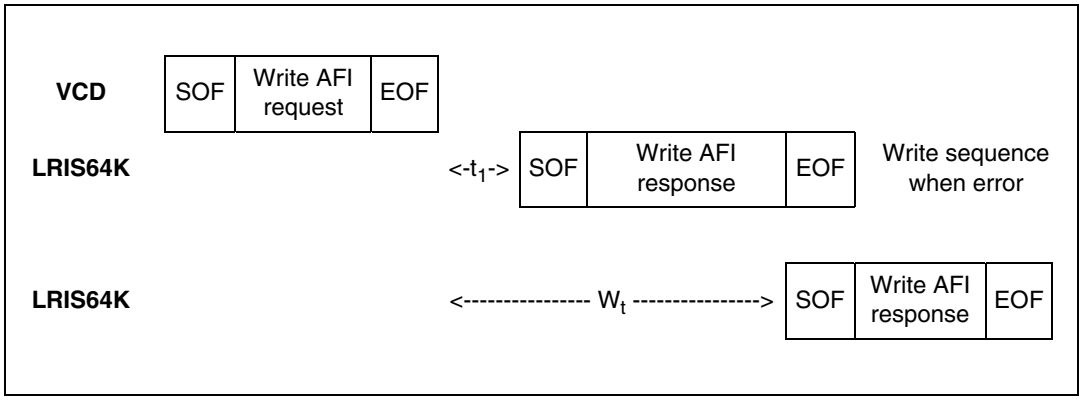
Table 50. Write AFI response format when Error_flag is set

Response SOF	Response_ flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 12h: the specified block is locked and its contents cannot be changed.
  - 13h: the specified block was not successfully programmed

Figure 47. Write AFI frame exchange between VCD and LRIS64K



24.9 Lock AFI

On receiving the Lock AFI request, the LRIS64K locks the AFI value permanently. The Option_flag is supported.

During write cycle W_t, there should be no modulation (neither 100% nor 10%). Otherwise, the LRIS64K may not Lock correctly the AFI value in memory. The W_t time is equal to t_{1nom} + 18 × 302 µs.

Table 51. Lock AFI request format

Request SOF	Request_ flags	Lock AFI	UID(1)	CRC16	Request EOF
	8 bits	28h	64 bits	16 bits	

1. Gray means that the field is optional.

Request parameter:

- UID (optional)

Table 52. Lock AFI response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
	8 bits	16 bits	

Response parameter:

- No parameter

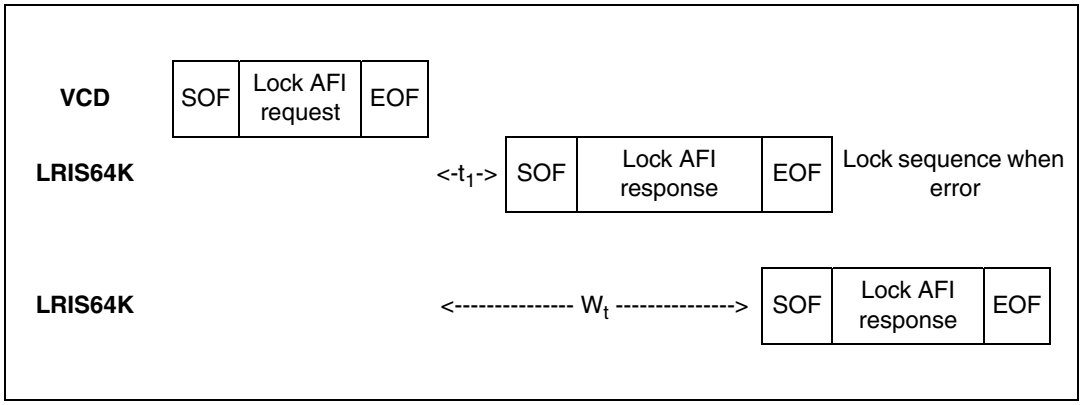
Table 53. Lock AFI response format when Error_flag is set

Response SOF	Response_ flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 11h: the specified block is already locked and thus cannot be locked again
  - 14h: the specified block was not successfully locked

Figure 48. Lock AFI frame exchange between VCD and LRIS64K



24.10 Write DSFID

On receiving the Write DSFID request, the LRIS64K programs the 8-bit DSFID value to its memory. The Option_flag is supported.

During write cycle W_t, there should be no modulation (neither 100% nor 10%). Otherwise, the LRIS64K may not write correctly the DSFID value in memory. The W_t time is equal to $t_{1nom} + 18 \times 302$ µs.

Table 54. Write DSFID request format

Request SOF	Request_ flags	Write DSFID	UID(1)	DSFID	CRC16	Request EOF
	8 bits	29h	64 bits	8 bits	16 bits	

1. Gray means that the field is optional.

Request parameter:

- UID (optional)
- DSFID

Table 55. Write DSFID response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
	8 bits	16 bits	

Response parameter:

- No parameter

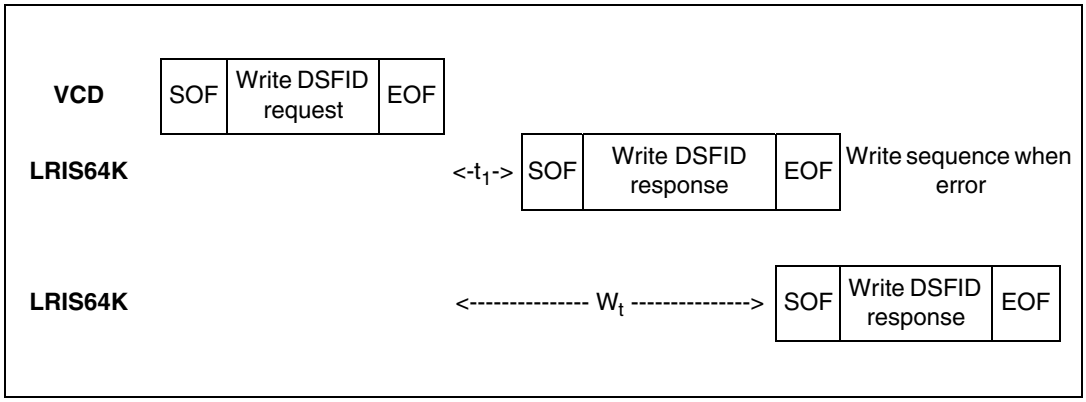
Table 56. Write DSFID response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 12h: the specified block is locked and its contents cannot be changed.
  - 13h: the specified block was not successfully programmed

Figure 49. Write DSFID frame exchange between VCD and LRIS64K



24.11 Lock DSFID

On receiving the Lock DSFID request, the LRIS64K locks the DSFID value permanently. The Option_flag is supported.

During write cycle W_t, there should be no modulation (neither 100% nor 10%). Otherwise, the LRIS64K may not lock correctly the DSFID value in memory. The W_t time is equal to t_{1nom} + 18 × 302 µs.

Table 57. Lock DSFID request format

Request SOF	Request_ flags	Lock DSFID	UID(1)	CRC16	Request EOF
	8 bits	2Ah	64 bits	16 bits	

1. Gray means that the field is optional.

Request parameter:

- UID (optional)

Table 58. Lock DSFID response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
	8 bits	16 bits	

Response parameter:

- No parameter.

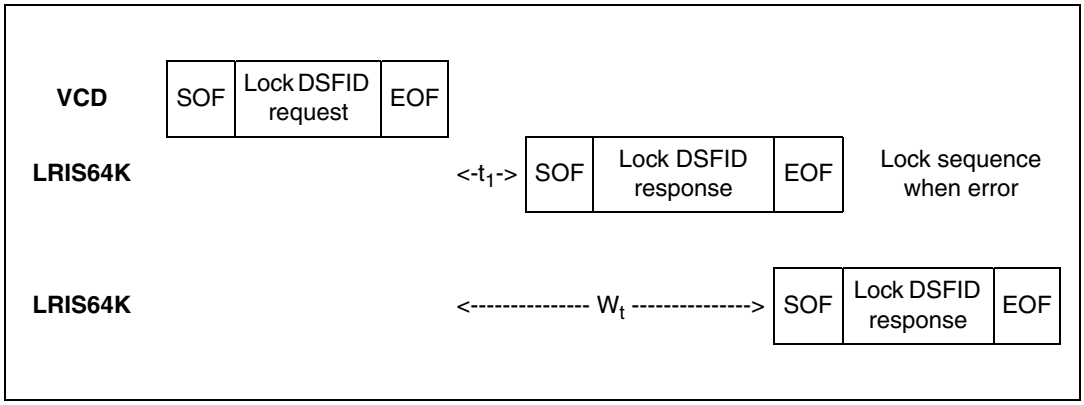
Table 59. Lock DSFID response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 11h: the specified block is already locked and thus cannot be locked again
  - 14h: the specified block was not successfully locked

Figure 50. Lock DSFID frame exchange between VCD and LRIS64K



24.12 Get System Info

When receiving the Get System Info command, the LRIS64K sends back its information data in the response.The Option_flag is supported and must be reset to 0. The Get System Info can be issued in both Addressed and Non Addressed modes.
The Protocol_extention_flag should be set to 1 for the LRIS64K to operate correctly. If the Protocol_extention_flag is at 0, the LRIS64K answers with an error code.

Table 60. Get System Info request format

Request SOF	Request _flags	Get System Info	UID(1)	CRC16	Request EOF
	8 bits	2Bh	64 bits	16 bits	

1. Gray means that the field is optional.

Request parameter:

- UID (optional)

Table 61. Get System Info response format when Error_flag is NOT set

Response SOF	Response _flags	Information flags	UID	DSFID	AFI	Memory size	IC reference	CRC16	Response EOF
	00h	0Fh	64 bits	8 bits	8 bits	0307FFh	44h	16 bits	

Response parameters:

- Information flags set to 0Fh. DSFID, AFI, Memory Size and IC reference fields are present
- UID code on 64 bits
- DSFID value
- AFI value
- Memory size. The LRIS64K provides 2048 blocks (07FFh) of 4 byte (03h)
- IC reference. Only the 6 MSB are significant.

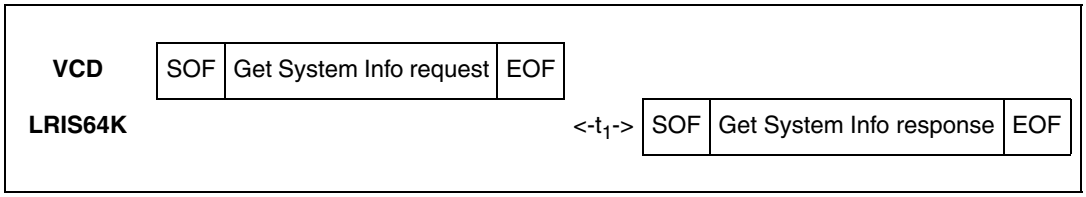
Table 62. Get System Info response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
	01h	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set:
  - 03h: Option not supported
  - 0Fh: other error

Figure 51. Get System Info frame exchange between VCD and LRIS64K



24.13 Get Multiple Block Security Status

When receiving the Get Multiple Block Security Status command, the LRIS64K sends back the sector security status. The blocks are numbered from '00h to '07FFh' in the request and the value is minus one (–1) in the field. For example, a value of '06' in the “Number of blocks” field requests to return the security status of 7 blocks.

The Protocol_extention_flag should be set to 1 for the LRIS64K to operate correctly. If the Protocol_extention_flag is at 0, the LRIS64K answers with an error code.

During the LRIS64K response, if the internal block address counter reaches 07FFh, it rolls over to 0000h and the Sector Security Status bytes for that location are sent back to the reader.

Table 63. Get Multiple Block Security Status request format

Request SOF	Request _flags	Get Multiple Block Security Status	UID(1)	First block number	Number of blocks	CRC16	Request EOF
	8 bits	2Ch	64 bits	16 bits	16 bits	16 bits	

1. Gray means that the field is optional.

Request parameter:

- UID (optional)
- First block number
- Number of blocks

Table 64. Get Multiple Block Security Status response format when Error_flag is NOT set

Response SOF	Response_ flags	Sector security status	CRC16	Response EOF
	8 bits	8 bits(1)	16 bits	

1. Repeated as needed.

Response parameters:

- Sector security status (see *Table 65: Sector security status*)

Table 65. Sector security status

b_7 b_6 b_5	b_4 b_3	b_2 b_1	b_0
Reserved for future use. All at 0	password control bits	Read / Write protection bits	0: Current sector not locked 1: Current sector locked

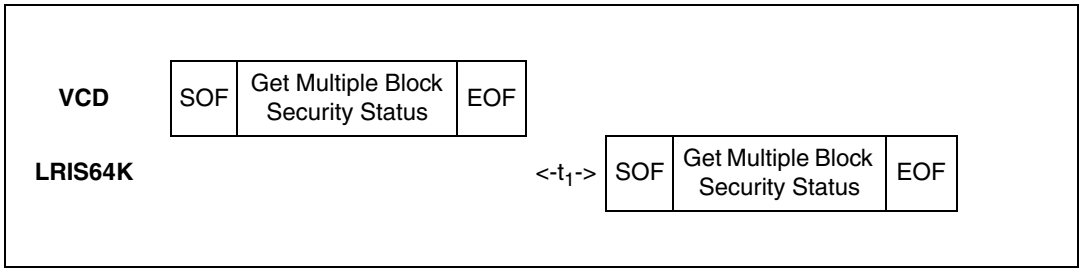
Table 66. Get Multiple Block Security Status response format when Error_flag is set

Response SOF	Response_ flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set:
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 10h: the specified block is not available

Figure 52. Get Multiple Block Security Status frame exchange between VCD and LRIS64K



24.14 Write-sector Password

On receiving the Write-sector Password command, the LRIS64K uses the data contained in the request to write the password and reports whether the operation was successful in the response. The Option_flag is supported.

During write cycle time W_t, there must be no modulation at all (neither 100% nor 10%). Otherwise, the LRIS64K may not correctly program the data into the memory. The W_t time is equal to t_{1nom} + 18 × 302 µs. After a successful write, the new value of the selected password is automatically activated. It is not required to present the new password value until LRIS64K power-down.

Table 67. Write-sector Password request format

Request SOF	Request _flags	Write-sector Password	IC Mfg code	UID(1)	Password number	Data	CRC16	Request EOF
	8 bits	B1h	02h	64 bits	8 bits	32 bits	16 bits	

1. Gray means that the field is optional.

Request parameter:

- UID (optional)
- Password number (01h = Pswd1, 02h = Pswd2, 03h = Pswd3, other = Error)
- Data

Table 68. Write-sector Password response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
	8 bits	16 bits	

Response parameter:

- 32-bit password value. The response is sent back after the write cycle.

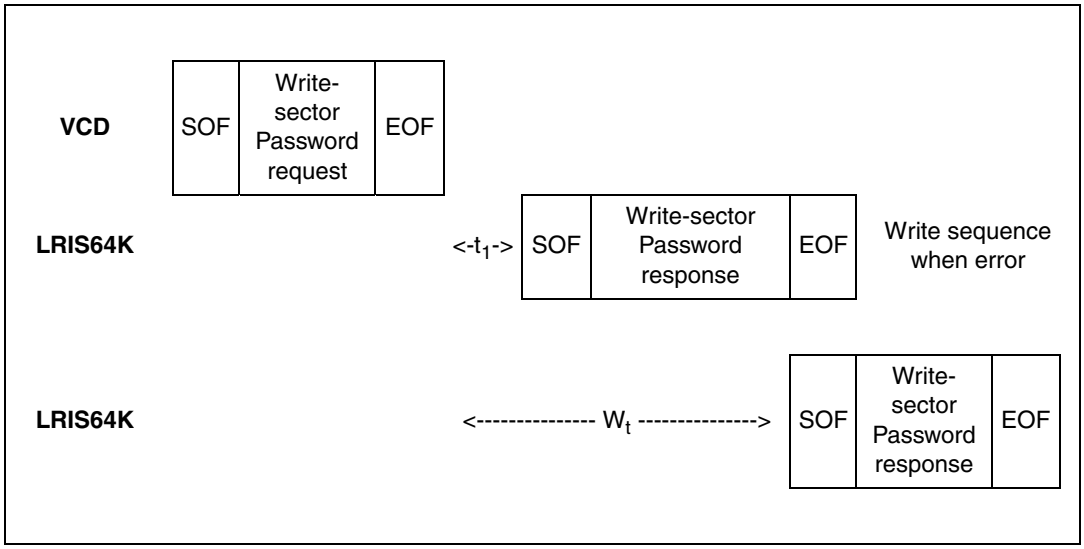
Table 69. Write-sector Password response format when Error_flag is set

Response SOF	Response_ flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set:
  - 02h: the command is not recognized, for example: a format error occurred
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 10h: the specified block is not available
  - 12h: the specified block is locked and its contents cannot be changed.
  - 13h: the specified block was not successfully programmed

Figure 53. Write-sector Password frame exchange between VCD and LRIS64K



24.15 Lock-sector Password

On receiving the Lock-sector Password command, the LRIS64K sets the access rights and permanently locks the selected sector. The Option_flag is supported.

A sector is selected by giving the address of one of its blocks in the Lock-sector Password request (Sector number field). For example, addresses 0 to 31 are used to select sector 0 and addresses 32 to 63 are used to select sector 1. Care must be taken when issuing the Lock-sector Password command as all the blocks belonging to the same sector are automatically locked by a single command.

The Protocol_extention_flag should be set to 1 for the LRIS64K to operate correctly. If the Protocol_extention_flag is at 0, the LRIS64K answers with an error code.

During write cycle W_t, there should be no modulation (neither 100% nor 10%) otherwise, the LRIS64K may not correctly lock the memory block.
The W_t time is equal to t_{1nom} + 18 × 302 µs.

Table 70. Lock-sector Password request format

Request SOF	Request _flags	Lock-sector Password	IC Mfg code	UID(1)	Sector number	Sector security status	CRC16	Request EOF
	8 bits	B2h	02h	64 bits	16 bits	8 bits	16 bits	

1. Gray means that the field is optional.

Request parameters:

- (optional) UID
- Sector number
- Sector security status (refer to *Table 71*)

Table 71. Sector security status

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	0	0	password control bits		Read / Write protection bits		1

Table 72. Lock-sector Password response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
	8 bits	16 bits	

Response parameter:

- No parameter.

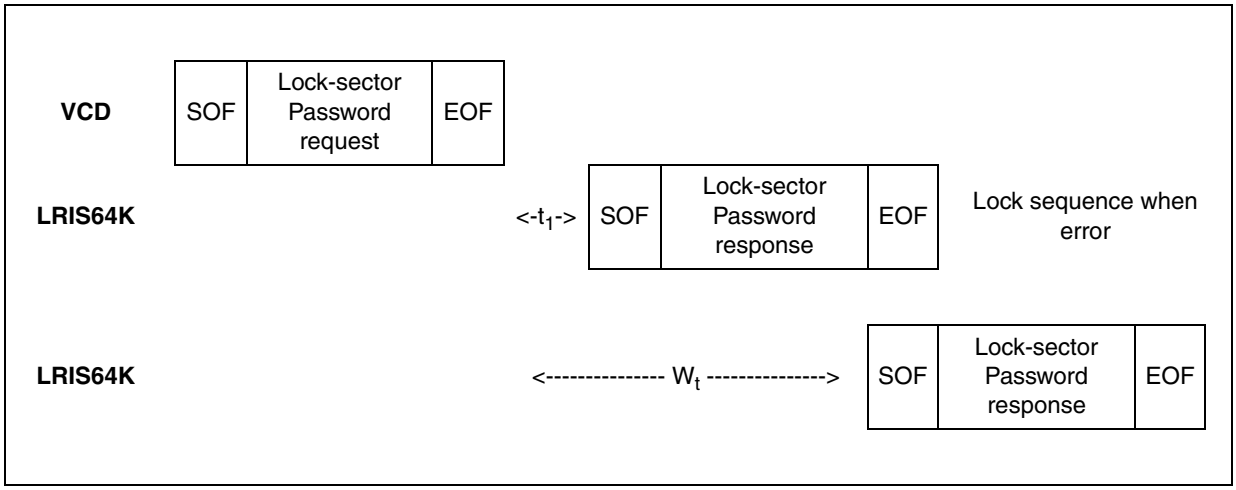
Table 73. Lock-sector Password response format when Error_flag is set

Response SOF	Response_ flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set:
  - 02h: the command is not recognized, for example: a format error occurred
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 10h: the specified block is not available
  - 11h: the specified block is already locked and thus cannot be locked again
  - 14h: the specified block was not successfully locked

Figure 54. Lock-sector Password frame exchange between VCD and LRIS64K



24.16 Present-sector Password

On receiving the Present-sector Password command, the LRIS64K compares the requested password with the data contained in the request and reports whether the operation has been successful in the response. The Option_flag is supported.
During the W_t comparison cycle time, there should be no modulation (neither 100% nor 10%) otherwise, the LRIS64K Password value may not be correctly compared.
The W_t time is equal to t_{1nom} + 18 × 302 µs.
After a successful command, the access to all the memory blocks linked to the password is changed as described in *Section 3.1: LRIS64K RF block security*.

Table 74. Present-sector Password request format

Request SOF	Request _flags	Present-sector Password	IC Mfg code	UID(1)	Password number	Data	CRC16	Request EOF
	8 bits	B3h	02h	64 bits	8 bits	32 bits	16 bits	

1. Gray means that the field is optional.

Request parameter:

- UID (optional)
- Password Number (0x01 = Pswd1, 0x02 = Pswd2, 0x03 = Pswd3, other = Error)
- Data

Table 75. Present-sector Password response format when Error_flag is NOT set

Response SOF	Response_flags	CRC16	Response EOF
	8 bits	16 bits	

Response parameter:

- No parameter. The response is send back after the writing cycle

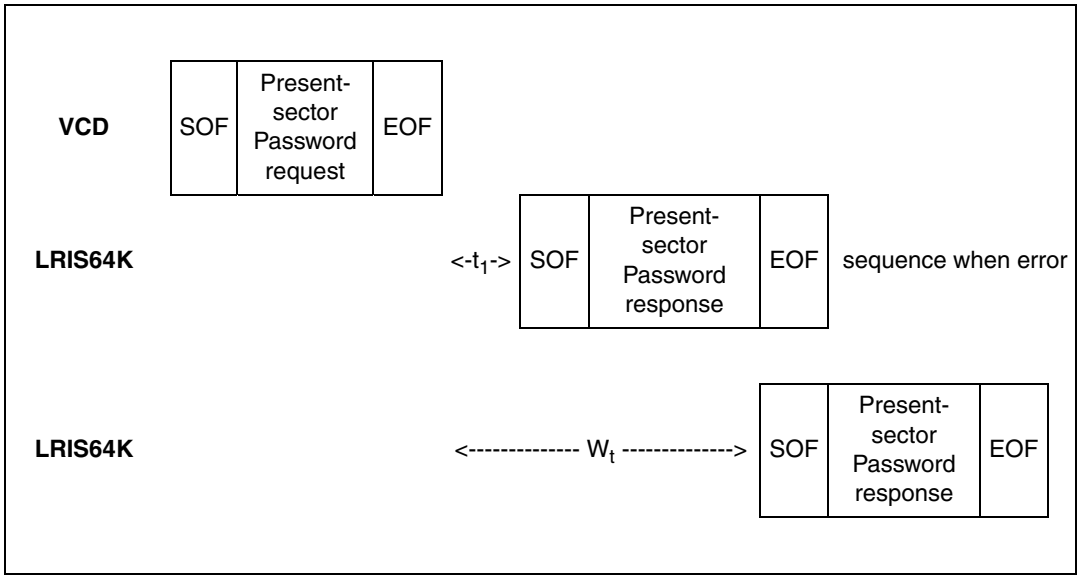
Table 76. Present-sector Password response format when Error_flag is set

Response SOF	Response_ flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set:
  - 02h: the command is not recognized, for example: a format error occurred
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 10h: the specified block is not available

Figure 55. Present-sector Password frame exchange between VCD and LRIS64K



24.17 Fast Read Single Block

On receiving the Fast Read Single Block command, the LRIS64K reads the requested block and sends back its 32-bit value in the response. The Option_flag is supported. The data rate of the response is multiplied by 2.

The Protocol_extention_flag should be set to 1 for the LRIS64K to operate correctly. If the Protocol_extention_flag is at 0, the LRIS64K answers with an error code.

Table 77. Fast Read Single Block request format

Request SOF	Request_ flags	Fast Read Single Block	IC Mfg code	UID(1)	Block number	CRC16	Request EOF
	8 bits	C0h	02h	64 bits	16 bits	16 bits	

1. Gray means that the field is optional.

Request parameters:

- Option_flag
- UID (optional)
- Block number

Table 78. Fast Read Single Block response format when Error_flag is NOT set

Response SOF	Response _flags	Sector security status(1)	Data	CRC16	Response EOF
	8 bits	8 bits	32 bits	16 bits	

1. Gray means that the field is optional.

Response parameters:

- Sector security status if Option_flag is set (see *Table 79*)
- 4 bytes of block data

Table 79. Sector security status

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Reserved for future used. All at 0			password control bits		Read / Write protection bits		0: Current sector not locked 1: Current sector locked

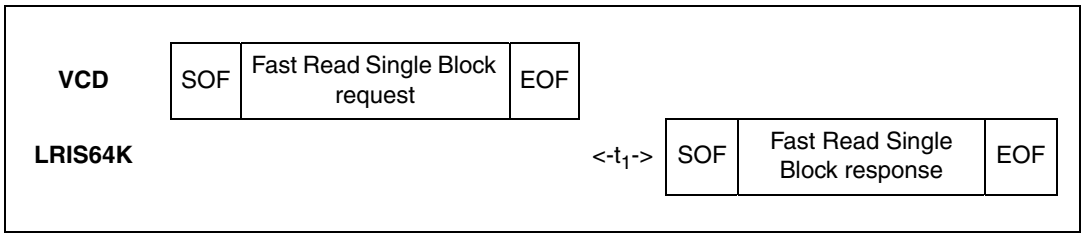
Table 80. Fast Read Single Block response format when Error_flag is set

Response SOF	Response_ flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set:
  - 02h: the command is not recognized, for example: a format error occurred
  - 03h: the option is not supported
  - 0Fh: error with no information given
  - 10h: the specified block is not available
  - 15h: the specified block is read protected

Figure 56. Fast Read Single Block frame exchange between VCD and LRIS64K



24.18 Fast Inventory Initiated

Before receiving the Fast Inventory Initiated command, the LRIS64K must have received an Initiate or a Fast Initiate command in order to set the Initiate_ flag. If not, the LRIS64K does not answer to the Fast Inventory Initiated command.
On receiving the Fast Inventory Initiated request, the LRIS64K runs the anticollision sequence. The Inventory_flag must be set to 1. The meaning of flags 5 to 8 is shown in *Table 20: Request flags 5 to 8 when Bit 3 = 1*. The data rate of the response is multiplied by 2.

The request contains:

- the flags,
- the Inventory command code
- the AFI if the AFI flag is set
- the mask length
- the mask value
- the CRC

The LRIS64K does not generate any answer in case of error.

Table 81. Fast Inventory Initiated request format

Request SOF	Request _flags	Fast Inventory Initiated	IC Mfg code	Optional AFI(1)	Mask length	Mask value	CRC16	Request EOF
	8 bits	C1h	02h	8 bits	8 bits	0 - 64 bits	16 bits	

1. Gray means that the field is optional.

The Response contains:

- the flags
- the Unique ID

Table 82. Fast Inventory Initiated response format

Response SOF	Response _flags	DSFID	UID	CRC16	Response EOF
	8 bits	8 bits	64 bits	16 bits	

During an Inventory process, if the VCD does not receive an RF LRIS64K response, it waits a time t_3 before sending an EOF to switch to the next slot. t_3 starts from the rising edge of the request EOF sent by the VCD.

- If the VCD sends a 100% modulated EOF, the minimum value of t_3 is:
  $t_3 min = 4384/f_C$ (323.3µs) + t_{SOF}
- If the VCD sends a 10% modulated EOF, the minimum value of t_3 is:
  $t_3 min = 4384/f_C$ (323.3µs) + t_{NRT}

where:

- t_{SOF} is the time required by the LRIS64K to transmit an SOF to the VCD
- t_{NRT} is the nominal response time of the LRIS64K

t_{NRT} and t_{SOF} are dependent on the LRIS64K-to-VCD data rate and subcarrier modulation mode.

24.19 Fast Initiate

On receiving the Fast Initiate command, the LRIS64K will set the internal Initiate_flag and send back a response only if it is in the Ready state. The command has to be issued in the Non Addressed mode only (Select_flag is reset to 0 and Address_flag is reset to 0). If an error occurs, the LRIS64K does not generate any answer. The Initiate_flag is reset after a power off of the LRIS64K. The data rate of the response is multiplied by 2.

The request contains:

- No data

Table 83. Fast Initiate request format

Request SOF	Request_flags	Fast Initiate	IC Mfg Code	CRC16	Request EOF
	8 bits	C2h	02h	16 bits	

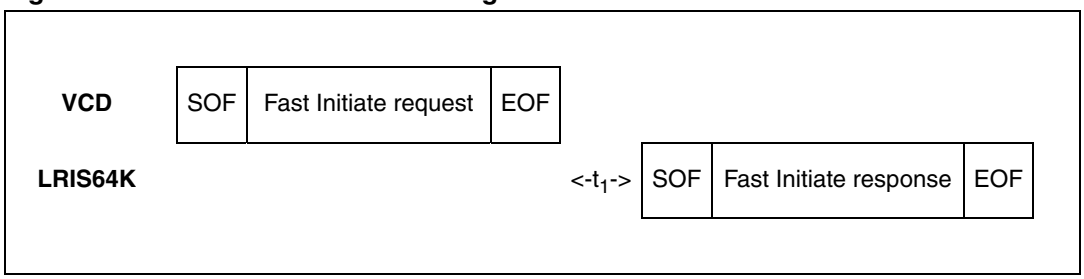
The response contains:

- the flags
- the Unique ID

Table 84. Fast Initiate response format

Response SOF	Response _flags	DSFID	UID	CRC16	Response EOF
	8 bits	8 bits	64 bits	16 bits	

Figure 57. Fast Initiate frame exchange between VCD and LRIS64K



24.20 Fast Read Multiple Block

On receiving the Fast Read Multiple Block command, the LRIS64K reads the selected blocks and sends back their value in multiples of 32 bits in the response. The blocks are numbered from '00h to '7FFh' in the request and the value is minus one (–1) in the field. For example, if the “number of blocks” field contains the value 06h, 7 blocks are read. The maximum number of blocks is fixed to 32 assuming that they are all located in the same sector. If the number of blocks overlaps sectors, the LRIS64K returns an error code.

The Protocol_extention_flag should be set to 1 for the LRIS64K to operate correctly. If the Protocol_extention_flag is at 0, the LRIS64K answers with an error code.

The Option_flag is supported. The data rate of the response is multiplied by 2.

Table 85. Fast Read Multiple Block request format

Request SOF	Request_ flags	Fast Read Multiple Block	IC Mfg code	UID(1)	First block number	Number of blocks	CRC16	Request EOF
	8 bits	C3h	02h	64 bits	16 bits	8 bits	16 bits	

1. Gray means that the field is optional.

Request parameters:

- Option_flag
- UID (Optional)
- First block number
- Number of blocks

Table 86. Fast Read Multiple Block response format when Error_flag is NOT set

Response SOF	Response_ flags	Sector security status(1)	Data	CRC16	Response EOF
	8 bits	8 bits(2)	32 bits(2)	16 bits	

1. Gray means that the field is optional.
2. Repeated as needed.

Response parameters:

- Sector security status if Option_flag is set (see *Table 87: Sector security status if Option_flag is set*)
- N block of data

Table 87. Sector security status if Option_flag is set

b_7 b_6 b_5 b_4 b_3	b_2	b_1	b_0
Reserved for future use. All at 0	password control bits	Read / Write protection bits	0: Current sector not locked 1: Current sector locked

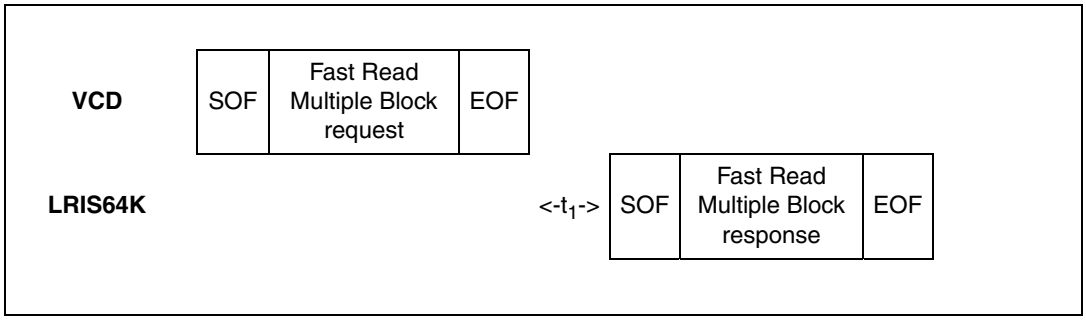
Table 88. Fast Read Multiple Block response format when Error_flag is set

Response SOF	Response_flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Response parameter:

- Error code as Error_flag is set:
  - 0Fh: other error
  - 10h: block address not available

Figure 58. Fast Read Multiple Block frame exchange between VCD and LRIS64K



24.21 Inventory Initiated

Before receiving the Inventory Initiated command, the LRIS64K must have received an Initiate or a Fast Initiate command in order to set the Initiate_ flag. If not, the LRIS64K does not answer to the Inventory Initiated command.

On receiving the Inventory Initiated request, the LRIS64K runs the anticollision sequence. The Inventory_flag must be set to 1. The meaning of flags 5 to 8 is given in *Table 20: Request flags 5 to 8 when Bit 3 = 1*.

The request contains:

- the flags,
- the Inventory Command code
- the AFI if the AFI flag is set
- the mask length
- the mask value
- the CRC

The LRIS64K does not generate any answer in case of error.

Table 89. Inventory Initiated request format

Request SOF	Request _flags	Inventory Initiated	IC Mfg code	Optional AFI	Mask length	Mask value	CRC16	Request EOF
	8 bits	D1h	02h	8 bits	8 bits	0 - 64 bits	16 bits	

The response contains:

- the flags
- the Unique ID

Table 90. Inventory Initiated response format

Response SOF	Response _flags	DSFID	UID	CRC16	Response EOF
	8 bits	8 bits	64 bits	16 bits	

During an Inventory process, if the VCD does not receive an RF LRIS64K response, it waits a time t_3 before sending an EOF to switch to the next slot. t_3 starts from the rising edge of the request EOF sent by the VCD.

- If the VCD sends a 100% modulated EOF, the minimum value of t_3 is:
  $t_3 min = 4384/f_C$ (323.3µs) + t_{SOF}
- If the VCD sends a 10% modulated EOF, the minimum value of t_3 is:
  $t_3 min = 4384/f_C$ (323.3µs) + t_{NRT}

where:

- t_{SOF} is the time required by the LRIS64K to transmit an SOF to the VCD
- t_{NRT} is the nominal response time of the LRIS64K

t_{NRT} and t_{SOF} are dependent on the LRIS64K-to-VCD data rate and subcarrier modulation mode.

24.22 Initiate

On receiving the Initiate command, the LRIS64K will set the internal Initiate_flag and send back a response only if it is in the ready state. The command has to be issued in the Non Addressed mode only (Select_flag is reset to 0 and Address_flag is reset to 0). If an error occurs, the LRIS64K does not generate any answer. The Initiate_flag is reset after a power off of the LRIS64K.

The request contains:

- No data

Table 91. Initiate request format

Request SOF	Request_flags	Initiate	IC Mfg code	CRC16	Request EOF
	8 bits	D2h	02h	16 bits	

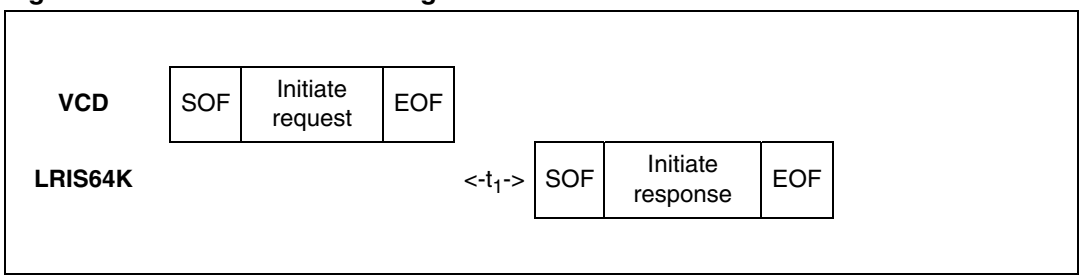
The response contains:

- the flags
- the Unique ID

Table 92. Initiate Initiated response format

Response SOF	Response _flags	DSFID	UID	CRC16	Response EOF
	8 bits	8 bits	64 bits	16 bits	

Figure 59. Initiate frame exchange between VCD and LRIS64K



25 Maximum rating

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 93. Absolute maximum ratings

Symbol	Parameter		Min.	Max.	Unit
T_{STG}	Storage conditions	Sawn Bumped Wafer (kept in its antistatic bag)	15	25	°C
t_{STG}	Storage time			6	months
I_{CC}	Supply current on AC0 / AC1		–20	20	mA
V_{MAX}	Input voltage on AC0 / AC1		–7	7	V
V_{ESD}	Electrostatic discharge voltage	AC0 - AC1 (HBM)(1)	–800	800	V
		AC0 - AC1 (MM)	–100	100	V

1. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114A, C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

26 RF DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device in RF mode. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 94. RF AC characteristics(1) (2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{CC}	External RF signal frequency		13.553	13.56	13.567	MHz
H_ISO	Operating field according to ISO	T_A = 0 °C to 50 °C	150		5000	mA/m
H_Extended	Operating field in extended temperature range	T_A = –40 °C to 85 °C	150		3500	mA/m
$MI_{CARRIER}$	10% carrier modulation index(3) (4) MI=(A-B)/(A+B)	150 mA/m > H_ISO > 1000 mA/m	15		30	%
		H_ISO > 1000 mA/m	10		30	
t_{RFR}, t_{RFF}	10% rise and fall time		0.5		3.0	µs
t_{RFSBL}	10% minimum pulse width for bit		7.1		9.44	µs
$MI_{CARRIER}$	100% carrier modulation index	MI=(A-B)/(A+B)	95		100	%
t_{RFR}, t_{RFF}	100% rise and fall time		0.5		3.5	µs
t_{RFSBL}	100% minimum pulse width for bit		7.1		9.44	µs
t_{JIT}	Bit pulse jitter		-2		+2	µs
$t_{MIN\ CD}$	Minimum time from carrier generation to first data	From H-field min		0.1	1	ms
f_{SH}	Subcarrier frequency high	$f_{CC}/32$		423.75		kHz
f_{SL}	Subcarrier frequency low	$f_{CC}/28$		484.28		kHz
t_1	Time for LRIS64K response	$4224/f_S$	318.6	320.9	323.3	µs
t_2	Time between commands	$4224/f_S$	309	311.5	314	µs
W_t	RF write time (including internal Verify)			5.75		ms

1. T_A = –40 to 85 °C.
2. All timing measurements were performed between 0 °C and 50 °C on a reference antenna with the following characteristics:
   External size: 75 mm x 48 mm
   Number of turns: 5
   Width of conductor: 0.5 mm
   Space between 2 conductors: 0.3 mm
   Value of the tuning capacitor in SO8: 27.5 pF (LRIS64K)
   Value of the coil: 5 µH
   Tuning frequency: 13.56 MHz.
3. Characterized only, not 100% tested
4. 15% (or more) carrier modulation index offers a better signal/noise ratio and therefore a wider operating range with a better noise immunity

Table 95. RF DC characteristics(1)

Symbol	Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Limited voltage					2.0	V
V_{BACK}	Backscattered level as defined by ISO test		ISO/IEC 10373-7	10			mV
I_{CC}	Supply current	Read	V_{CC} = 2.0 V			50	µA
		Write	V_{CC} = 2.0 V			150	µA
C_{TUN}	Internal tuning capacitor(2)		f = 13.56 MHz	24.8	27.5	30.2	pF

1. T_A = –40 to 85 °C.
2. Characterised only, at room temperature only, measured at $V_{AC0-AC1}$ = 0.5 V peak.

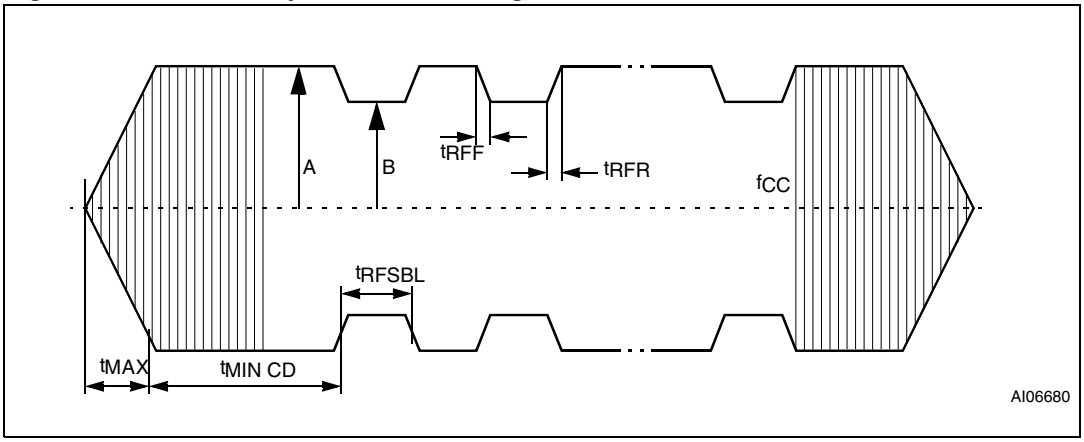
Table 96. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	–40	85	°C

Figure 60 shows an ASK modulated signal, from the VCD to the LRIS64K. The test condition for the AC/DC parameters are:

- Close coupling condition with tester antenna (1mm)
- LRIS64K performance measured at the tag antenna

Figure 60. LRIS64K synchronous timing, transmit and receive



27 Part numbering

Table 97. Ordering information scheme

Example: LRIS64K - SBN18/ 2

Device type

LRIS64K (long-range tag with 64 Kbit EEPROM)

Package

SBN18 = 180 µm ± 15 µm bumped and sawn wafer on 8-inch frame

Tuning capacitance

2= 27.5 pF

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Appendix A Anticollision algorithm

The following pseudocode describes how anticollision could be implemented on the VCD, using recursivity.

A.1 Algorithm for pulsed slots

```
function push (mask, address); pushes on private stack
function pop (mask, address); pops from private stack
function pulse_next_pause; generates a power pulse
function store(LRIS64K_UID); stores LRIS64K_UID

function poll_loop (sub_address_size as integer)
  pop (mask, address)
  mask = address & mask; generates new mask
           ; send the request
  mode = anticollision
  send_Request (Request_cmd, mode, mask length, mask value)
  for sub_address = 0 to (2^sub_address_size - 1)
    pulse_next_pause
    if no_collision_is_detected ; LRIS64K is inventoried
      then
        store (LRIS64K_UID)
      else ; remember a collision was detected
        push(mask,address)
      endif
    next sub_address

  if stack_not_empty ; if some collisions have been detected and
    then   ; not yet processed, the function calls itself
      poll_loop (sub_address_size); recursively to process the
last stored collision
    endif
end poll_loop

main_cycle:
  mask = null
  address = null
  push (mask, address)
  poll_loop(sub_address_size)
end_main_cycle
```

Appendix B CRC

B.1 CRC error detection method

The cyclic redundancy check (CRC) is calculated on all data contained in a message, from the start of the flags through to the end of Data. The CRC is used from VCD to LRIS64K and from LRIS64K to VCD.

Table 98. CRC definition

CRC definition					
CRC type	**Length**	**Polynomial**	**Direction**	**Preset**	**Residue**
ISO/IEC 13239	16 bits	$X^{16} + X^{12} + X^5 + 1 = 8408h$	Backward	FFFFh	F0B8h

To add extra protection against shifting errors, a further transformation on the calculated CRC is made. The One's Complement of the calculated CRC is the value attached to the message for transmission.

To check received messages the 2 CRC bytes are often also included in the re-calculation, for ease of use. In this case, the expected value for the generated CRC is the residue F0B8h.

B.2 CRC calculation example

This example in C language illustrates one method of calculating the CRC on a given set of bytes comprising a message.

C-example to calculate or check the CRC16 according to ISO/IEC 13239

```
#define  POLYNOMIAL0x8408//  x^16 + x^12 + x^5 + 1
#define  PRESET_VALUE0xFFFF
#define  CHECK_VALUE0xF0B8

#define  NUMBER_OF_BYTES4// Example: 4 data bytes
#define  CALC_CRC1
#define  CHECK_CRC0

void main()
{
  unsigned int  current_crc_value;
  unsigned char array_of_databytes[NUMBER_OF_BYTES + 2] = {1, 2, 3,
4, 0x91, 0x39};
  int           number_of_databytes = NUMBER_OF_BYTES;
  int           calculate_or_check_crc;
  int           i, j;
  calculate_or_check_crc = CALC_CRC;
// calculate_or_check_crc = CHECK_CRC;// This could be an other
example
  if (calculate_or_check_crc == CALC_CRC)
  {
```

```
        number_of_databytes = NUMBER_OF_BYTES;
    }
    else    // check CRC
    {
        number_of_databytes = NUMBER_OF_BYTES + 2;
    }

    current_crc_value = PRESET_VALUE;

    for (i = 0; i < number_of_databytes; i++)
    {
        current_crc_value = current_crc_value ^ ((unsigned
int)array_of_databytes[i]);

        for (j = 0; j < 8; j++)
        {
            if (current_crc_value & 0x0001)
            {
                current_crc_value = (current_crc_value >> 1) ^
POLYNOMIAL;
            }
            else
            {
                current_crc_value = (current_crc_value >> 1);
            }
        }
    }

    if (calculate_or_check_crc == CALC_CRC)
    {
        current_crc_value = ~current_crc_value;

        printf ("Generated CRC is 0x%04X\n", current_crc_value);

        // current_crc_value is now ready to be appended to the data
stream
        // (first LSByte, then MSByte)
    }
    else   // check CRC
    {
        if (current_crc_value == CHECK_VALUE)
        {
            printf ("Checked CRC is ok (0x%04X)\n",
current_crc_value);
        }
        else
        {
            printf ("Checked CRC is NOT ok (0x%04X)\n",
current_crc_value);
        }
    }
}
```

Appendix C Application family identifier (AFI)

The AFI (application family identifier) represents the type of application targeted by the VCD and is used to extract from all the LRIS64K present only the LRIS64K meeting the required application criteria.

It is programmed by the LRIS64K issuer (the purchaser of the LRIS64K). Once locked, it cannot be modified.

The most significant nibble of the AFI is used to code one specific or all application families, as defined in *Table 99*.

The least significant nibble of the AFI is used to code one specific or all application subfamilies. Subfamily codes different from 0 are proprietary.

Table 99. AFI coding(1)

AFI Most significant nibble	AFI Least significant nibble	Meaning VICCs respond from	Examples / Note
'0'	'0'	All families and subfamilies	No applicative preselection
'X'	'0	'All subfamilies of family X	Wide applicative preselection
'X	''Y'	Only the Yth subfamily of family X	
'0'	'Y'	Proprietary subfamily Y only	
'1	''0', 'Y'	Transport	Mass transit, bus, airline, etc.
'2	''0', 'Y'	Financial	IEP, banking, retail, etc.
'3	''0', 'Y'	Identification	Access control, etc.
'4	''0', 'Y'	Telecommunication	Public telephony, GSM, etc.
'5'	'0', 'Y'	Medical	
'6	''0', 'Y'	Multimedia	Internet services, etc.
'7	''0', 'Y'	Gaming	
8	''0', 'Y'	Data storage	Portable files, etc.
'9	''0', 'Y'	Item management	
'A	''0', 'Y'	Express parcels	
'B	''0', 'Y'	Postal services	
'C	''0', 'Y'	Airline bags	
'D	''0', 'Y'	RFU	
'E	''0', 'Y'	RFU	
'F'	'0', 'Y'	RFU	

1. X = '1' to 'F', Y = '1' to 'F'

Revision history

Table 100. Document revision history

Date	Revision	Changes
26-Jan-2009	1	Initial release.
05-Feb-2009	2	TSSOP8 package removed. Wafer silhouette added *on page 1*.
13-Feb-2009	3	Device programming time corrected.
02-Apr-2009	4	Revision history corrected (revision 3 added). Figure 2: UFDFPN8 connections corrected.
16-Jul-2009	5	Document status promoted from Target specification to Preliminary data. V_{ESD} modified in *Table 93: Absolute maximum ratings*.
17-Sep-2009	6	V_{ESD} modified in *Table 93: Absolute maximum ratings*.
25-Aug-2010	7	Updated *Features on page 1*. Removed all references to packages. Removed Figure 2: UFDFPN8 connections. Updated *Section 4: Initial delivery state on page 18*. Updated *Figure 3*, *Figure 4*, *Table 94*, and *Table 95*. Updated storage time (t_{STG}) in *Table 93: Absolute maximum ratings on page 91*.
05-Oct-2010	8	Document classification changed to public. Updated DSFID value in *Section 4: Initial delivery state*
08-Nov-2010	9	Updated document status from preliminary status to public.
19-Sep-2011	10	Modified *Section 1: Description* Updated disclaimer on last page.
27-Oct-2011	11	Updated footnote (2) of *Table 94: RF AC characteristics*.

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