L99MD01

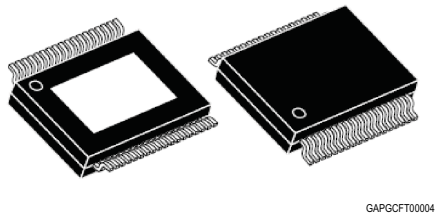
Octal half-bridge driver with SPI control for automotive application

Features

- 8 half bridges
- R_{ON} = typ. 0.9 Ω (HS), 0.64 Ω (LS) @ T_j = 25 °C
- Current limit of each output at min. 0.8 A
- Intrinsic DC/DC step up converter driving an external MOSFET
- PWM mode option for all half bridges for hold current
- Internal PWM generation
- Two current monitor outputs
- SPI interface for data communication
- Temperature warning
- All outputs overtemperature protected
- All outputs short circuit protected
- V_{CC} supply voltage 3.0 to 5.3 V
- Very low current consumption in standby mode typ. 5 µA
- V_S operating range compliant: 6 V – 18 V

Applications

- Stepper motor driver and / or DC
- Intended to drive HVAC flaps



PowerSSO-36

Description

The L99MD01 is an octal half-bridge driver for automotive applications.

The device is intended to drive DC and/or stepper motors. Using the boost converter it's possible to drive 4 stepper motors simultaneously. Without boost converter the system is able to run 3 stepper motors in sequential mode or 2 stepper motors simultaneously. The octal half bridge configuration allows also to drive 4 DC-motors simultaneously and 7 DC-motors sequentially.

The integrated 24 bit standard Serial Peripheral Interface (SPI) controls all outputs and provides diagnostic information: normal operation, open-load in on-state, overcurrent, temperature warning and overtemperature.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	L99MD01XP	L99MD01XPTR

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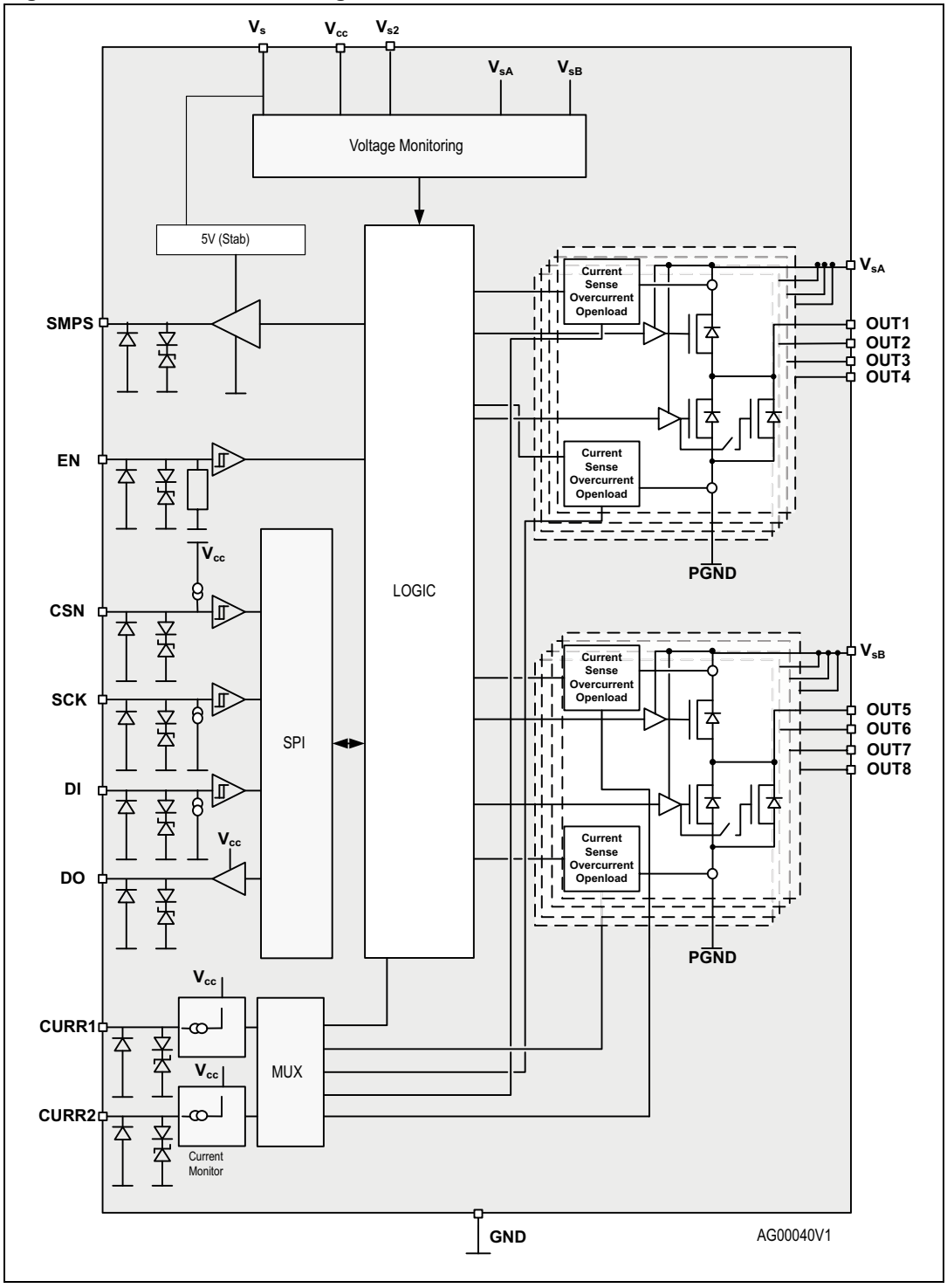
1 Block diagram

Figure 1. Detailed block diagram

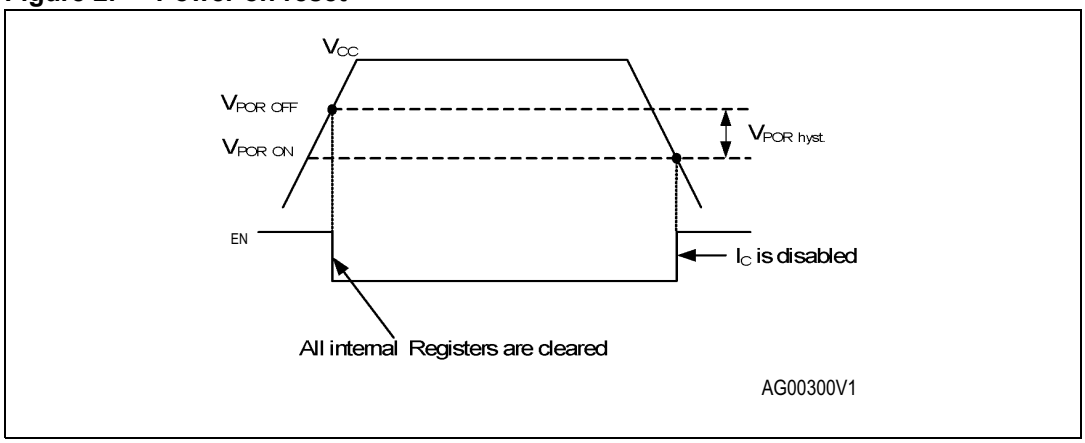


2 Detailed description

2.1 Power supply: V_{CC}

The supply voltage V_{CC} (3.3 V / 5 V) supplies the whole device. In case of power-on (V_{CC} increases from undervoltage to $V_{POR\ OFF}$ = 2.75 V, typical) the circuit is initialized by an internally generated power-on-reset (POR). If the voltage V_{CC} decreases under the minimum threshold ($V_{POR\ ON}$ = 2.55 V, typical), the outputs are switched off in 3-state (high impedance). The status registers are cleared and the control registers are reset to their default.

Figure 2. Power on reset



2.2 Power supply: V_{SA}, V_{SB}

Each V_{SA} and V_{SB} supplies 4 half bridges independently.

V_{SA} → Out 1 to Out 4

V_{SB} → Out 5 to Out 8

2.3 Standby mode

The standby mode of the L99MD01 is activated by EN pin to low. The inputs and outputs are switched off. The status registers are cleared and the control registers are reset to their default values.

In the standby mode the current consumption is typ. 5 µA.

2.4 PWM mode

The PWM Mode is intended to generate a hold current for stepper motors.

PWM frequency typ. 100 Hz.

Duty cycle (SPI 2bit): 15 %, 30 %, 45 % and 60 %.

Each half-bridge is independently addressable (SPI 8bit).

2.5 SMPS Switched Mode Power Supply

External MOSFET

Spread spectrum technique:

- Wobble oscillator, programmable by SPI (1.95 K / 3.9 K / 7.8 K / 15.6 KHz).
- Frequency modulation programmable by SPI (0 / 5 / 10 / 20%).

V_{S2} level concept:

- Microcontroller measuring pulse of SMPS frequency (dependent on internal oscillator frequency).
  Due to the Oscillator frequency of L99MD01 the µC can calculate the on/off counts to program the SMPS frequency and duty cycle.
- Microcontroller sending by SPI SMPS 6-bit on counter value, microcontroller sending by SPI SMPS 6-bit off counter value.
  Basing on the on and off counter value the duty cycle and the SMPS frequency can be programmed.

The V_{S2} voltage is strongly related to the duty cycle of SMPS.

2.6 Current monitor

The current monitor output sources a current image at the current monitor output which has a programmable ratio (1/250, 1/500, 1/750, 1/1000) of the instantaneous current of the selected half bridge (high-side or low-side). Via SPI it can be programmed which of the outputs are multiplexed to the current monitor output.

The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open or overload condition. For example this can be used to detect the motor state (starting, free-running, stalled).

2.7 Inductive loads

Each half bridge is built by an internally connected high-side and a low-side power DMOS transistor. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs.

2.8 Diagnostic functions

All diagnostic functions (over/open-load, temperature warning and thermal shutdown, over/undervoltage) are internally filtered and the condition has to be valid for at least 32 µs (open-load: typ. 2 ms, respectively) before the corresponding status bit in the status registers is set. The filters are used to improve the noise immunity of the device. Open-load and temperature warning function are intended for information purpose and not changes the state of the output drivers. On contrary, the overload and thermal shutdown condition disables the corresponding driver (overload) or all drivers (thermal shutdown), respectively. The microcontroller has to clear the overcurrent status bit to reactivate the corresponding driver.

2.9 Temperature warning and thermal shutdown

If the junction temperature rises above $T_{j\ TW\ ON}$ a temperature warning flag is set and is detectable via the SPI. If the junction temperature increases above the second threshold $T_{j\ SD\ ON}$, the thermal shutdown bit is set and power DMOS transistors of all output stages are switched off to protect the device. Temperature warning flag and thermal shutdown bits are latched. In order to reactivate the output stages, the junction temperature must decrease below $T_{j\ SD\ ON}$ and the thermal shutdown bit has to be cleared by the microcontroller.

2.10 V_S, V_{S2}, V_{SA}, V_{SB} monitoring

V_S undervoltage: Status bit is set. All outputs and SMPS are switched off.
The microcontroller needs to clear the status bits to reactivate the drivers and SMPS.

V_S overvoltage: Status bit is set. All outputs are switched off (default).
The microcontroller needs to clear the status bits to reactivate the drivers Can be deactivated via SPI.

V_{SA} undervoltage: Status bit is set. Out 1 to Out 8 are switched off.
The microcontroller needs to clear the status bits to reactivate the drivers.

V_{SB} undervoltage: Status bit is set. Out 1 to Out 8 are switched off.
The microcontroller needs to clear the status bits to reactivate the drivers.

V_{S2} undervoltage: Status bit is set. Only if SPMS is active.
The microcontroller needs to clear the status bits to reactivate SMPS

V_{S2} overvoltage: Status bit is set. SMPS is switched off (default).
The microcontroller needs to clear the status bits to reactivate SMPS. If the VS2 recovery bit is set, and the VS2 voltage falls below the threshold, the SMPS goes in active mode and the status bit is cleared.

Table 2. V_S, V_{S2}, V_{SA}, V_{SB} monitoring

	'typ	SMPS	Out x
V_S undervoltage	5.7 V	Status + off	Status + off
V_S overvoltage	22.0 V	X	Status + (off or mask)
V_{SA} undervoltage	5.7 V	X	Status + off
V_{SB} undervoltage	5.7 V	X	Status + off
V_{S2} undervoltage	V_S + 1.5V	Status	X
V_{S2} overvoltage	35.0 V	Status + (off or (off+ recovery))	

2.11 Open-load detection

The open-load detection monitors the load current in each activated output stage. If the load current is below the open-load detection threshold for at least 2 ms (t_{dOL}) the corresponding

open load bit is set in the status register. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3 ms) can be used to test the open-load status without changing the mechanical/electrical state of the loads.

2.12 Overload detection

In case of an overcurrent condition, a flag is set in the corresponding status register. If the overcurrent signal is valid for at least t_{ISC} = 32 µs, the overcurrent flag is set and the corresponding switch is switched off to reduce the power dissipation and to protect the integrated circuit. The microcontroller has to clear the status bit to reactivate the corresponding driver.

2.13 Cross-current protection

The device is cross-current protected by an internal delay time. If one driver (LS or HS) is turned-off the activation of the other driver of the same half bridge are automatically delayed by the cross-current protection time. After the cross-current protection time is expired the slew-rate limited switch-off phase of the driver is changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behavior it is always guaranteed that the previously activated driver is totally turned-off before the opposite driver starts to conduct. If wrong SPI commands try to turn-on both driver (LS and HS) simultaneously, the high-side and the low-side are (or stay) deactivated (3-state).

3 Pin definitions and functions

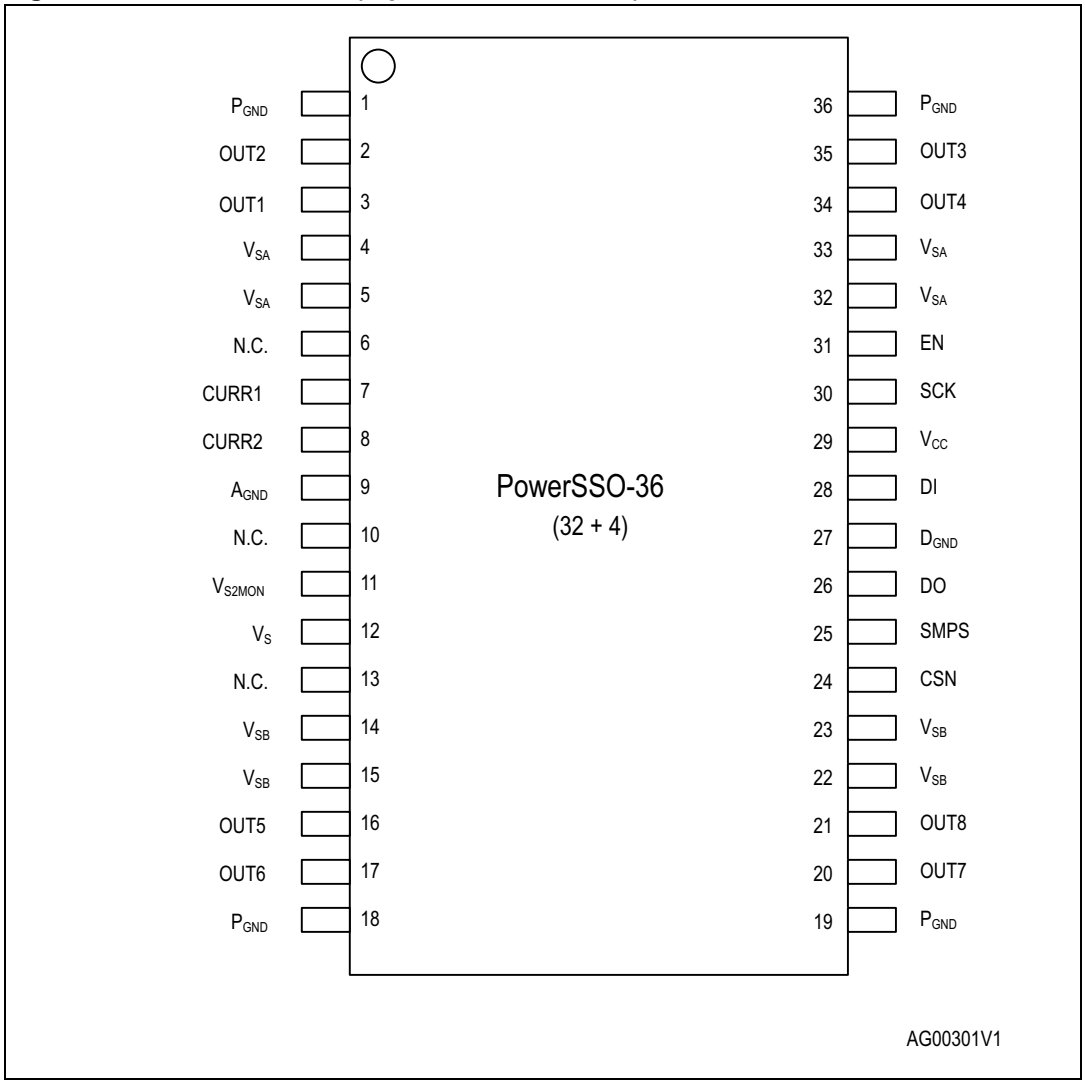
Table 3. Pin description

Pin	Symbol	Function
1, 18, 19, 36	P_{GND}	Power ground: reference potential
9	A_{GND}	Analog ground: reference potential
27	D_{GND}	Digital ground: reference potential
6, 10, 13	N.C.	Not connected
		Exposed pad: reference potential connected to PGND
2, 3, 16, 17, 20, 21, 34, 35	OUT 1 - 8	Half bridge-output: the output is built by a high-side and a low-side switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V_{Sx}, low-side driver from PGND to output).
29	V_{CC}	Logic voltage supply 3.3 V / 5 V For this input a ceramic capacitor as close as possible to AGND is recommended
4, 5, 32, 33	V_{SA}	Power supply voltage for OUT 1 to 4 (external reverse protection required): For this input a ceramic capacitor as close as possible to PGND is recommended. Important: for the capability of driving the full current at the outputs all pins of V_{SA} must be externally connected!
14, 15, 22, 23	V_{SB}	Power supply voltage for OUT 5 to 8 (external reverse protection required): For this input a ceramic capacitor as close as possible to PGND is recommended. Important: for the capability of driving the full current at the outputs all pins of V_{SA} must be externally connected!
11	V_{S2MON}	V_{S2} monitoring
12	V_S	V_S supply and monitoring
25	SMPS	SMPS gate driver. For overcurrent and overvoltage protection a external resistor is recommended
7, 8	CURR1 / 2	Current monitor 1 / 2
31	EN	Enable the L99MD01
28	DI	SPI data in: the input requires CMOS logic levels and receives serial data from the microcontroller. The data is a 24 bit control word and the most significant bit (MSB) is transferred first.
26	DO	SPI data out: the diagnosis data is available via the SPI and this 3-state output. The output remains in 3-state, if the chip is not selected by the input CSN (CSN = high)

Table 3. Pin description (continued)

Pin	Symbol	Function
24	CSN	SPI CSN chip select: this input is active low and requires CMOS logic levels. The serial data transfer between the L99MD01 and micro controller is enabled by pulling the input CSN to low level.
30	SCK	SPI serial clock input: this input controls the internal shift register of the SPI and requires CMOS logic levels.

Figure 3. Pin connection (top view- not in scale)



4 Electrical specifications

4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0,3…28	V
	Single pulse t_{max} < 400 ms	40	V
V_{S2} V_{SA} V_{SB}	DC supply voltage	-0,3…38	V
	Single pulse t_{max} < 400 ms	40	V
V_{CC}	Stabilized supply voltage, logic supply	-0.3 to 5.5	V
EN DI DO SCK CSN	Digital input / output voltage	-0.3 to V_{CC} + 0.3	V
CURR1/2	Current monitor output	-0.3 to V_{CC} + 0.3	
OUT 1-8	Output current capability	±2	A
SMPS	SMPS is not overcurrent protected, external resistor can be used for protection and EMC optimizations		

Note: All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit!

4.2 ESD protection

Table 5. ESD protection

Parameter	Value	Unit
All pins	±2(1)	kV
Output Pins: OUT1 – 8, V_S, V_{SA}, V_{SB}, V_{S2},	±4(2)	kV

1. HBM according to EIA/JESD22-A114-E.
2. HBM with all unzapped pins grounded.

4.3 Thermal data

Table 6. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	operating junction temperature	-40 to 150	°C

Table 7. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{jTW\ ON}$	temperature warning threshold junction temperature	T_j increasing	-	-	150	°C
$T_{jSD\ ON}$	thermal shutdown threshold junction temperature	T_j increasing	-	-	170	°C

4.4 Electrical characteristics

V_S = 6 to 18 V, V_{CC} = 3.0 to 5.3 V, T_j = -40 to 150 °C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 8. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SA}/ V_{SB}	operating supply voltage range		6		38	V
I_S	V_{SA} / V_{SB} DC supply current	V_{Sx} = 13 V, V_{CC} = 5.0 V EN = high Outputs floating		0.5	2	mA
I_{VS}	V_S supply current	V_S = 13 V, V_{CC} = 5 V EN = high SMPS output off		1.5	4	mA
		V_S = 13 V, V_{CC} = 5 V EN = high SMPS load = 2 nF, 200 kHz, duty 50 %		4.2	7	mA
I_{VS2}	V_{S2} DC current	V_{S2} =26 V, V_{CC} = 5.0 V EN = high		300	600	µA
I_{VSX}	V_{Sx} (V_S, V_{SA}, V_{SB}, V_{S2}) quiescent supply current	V_{Sx} = 13 V, V_{CC} = 5 V EN = low T_j = -40, 25 °C Outputs floating		3	10	µA
		T_j = 130 °C; TBV		6	20	µA
V_{CC}	operating supply voltage range		3,0		5,3	V

Table 8. Supply (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{CC}	V_{CC} DC supply current	V_{Sx} = 13 V, V_{CC} = 5.0 V EN = high		1	3	mA
	V_{CC} quiescent supply current	V_S = 13 V, V_{CC} = 5.0 V CSN = V_{CC} EN = low Outputs floating		5	20	µA

Table 9. Overvoltage and undervoltage detection

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{POR\ OFF}$	power-on-reset threshold	V_{CC} increasing			3.0	V
$V_{POR\ ON}$	power-on-reset threshold	V_{CC} decreasing	2.3			V
$V_{POR\ hyst}$	power-on-reset hysteresis	$V_{POR\ OFF}$ - $V_{POR\ ON}$		0.2		V
$V_{SUV\ OFF}$	V_S UV-threshold voltage	V_S increasing	6.0		6.7	V
$V_{SUV\ ON}$	V_S UV-threshold voltage	V_S decreasing	5.4		6	V
$V_{SUV\ hyst}$	V_S UV-hysteresis	$V_{SUV\ OFF}$ - $V_{SUV\ ON}$	0.35	0.5		V
$V_{SAUV\ OFF}$	V_{SA} UV-threshold voltage	V_{SA} increasing	5.95		6.7	V
$V_{SAUV\ ON}$	V_{SA} UV-threshold voltage	V_{SA} decreasing	5.4		6	V
$V_{SAUV\ hyst}$	V_{SA} UV-hysteresis	$V_{SAUV\ OFF}$ - $V_{SAUV\ ON}$	0.35	0.5		V
$V_{SBUV\ OFF}$	V_{SB} UV-threshold voltage	V_{SB} increasing	5.95		6.7	V
$V_{SBUV\ ON}$	V_{SB} UV-threshold voltage	V_{SB} decreasing	5.4		6	V
$V_{SBUV\ hyst}$	V_{SB} UV-hysteresis	$V_{SBUV\ OFF}$ - $V_{SBUV\ ON}$	0.35	0.5		V
$V_{SOV\ ON}$	V_S OV-threshold voltage	V_S increasing			24	V
$V_{SOV\ OFF}$	V_S OV-threshold voltage	V_S decreasing	18			V
$V_{SOV\ hyst}$	V_S OV-hysteresis	$V_{SOV\ ON}$ - $V_{SOV\ OFF}$	0.75	1		V
$V_{S2UV\ OFF}$	V_{S2} UV-threshold voltage	V_{S2} increasing			V_S+5	V
$V_{S2UV\ ON}$	V_{S2} UV-threshold voltage	V_{S2} decreasing	V_S+1			V
$V_{S2UV\ hyst}$	V_{S2} UV-hysteresis	$V_{S2UV\ OFF}$ - $V_{S2UV\ ON}$	0.55	0.8	1.15	V
$V_{S2OV\ ON}$	V_{S2} OV-threshold voltage	V_S increasing			38	V
$V_{S2OV\ OFF}$	V_{S2} OV-threshold voltage	V_S decreasing	32			V
$V_{S2OV\ hyst}$	V_{S2} OV-hysteresis	$V_{S2OV\ ON}$ - $V_{S2OV\ OFF}$	0.75	1		V

Table 10. Switches

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$r_{ON\ HS\ 1-8}$	On resistance V_{SA} / V_{SB} to OUT 1-8	T_j = 25 °C, I_{OUT1-8} = -0.25 A		900	1200	mΩ
		T_j = 125 °C, I_{OUT1-8} = -0.25 A		1300	1800	mΩ
$r_{ONLSHC\ 1-8}$	On resistance OUT 1-8 to GND in HC mode	T_j = 25 °C, HC=1 I_{OUT1-8} = 0.25 A		700	1000	mΩ
		T_j = 125 °C, HC=1 I_{OUT1-8} = 0.25 A		1000	1500	mΩ
$r_{ONLSLC\ 1-8}$	On resistance OUT 1-8 to GND in LC mode	T_j = 25 °C, HC=0 I_{OUT1-8} = 0.125 A		1200	1800	mΩ
		T_j = 125 °C, HC=0 I_{OUT1-8} = 0.125 A		2000	2800	mΩ
$I_{SCHS1-8}$	HS overcurrent protection	V_S = 13.5 V	0.8		1.4	A
$I_{SCLSHC1-8}$	LS overcurrent protection in HC mode	V_S = 13.5 V, HC = 1	0.8		1.4	A
$I_{SCLSLC1-8}$	LS overcurrent protection in LC mode	V_S = 13.5 V, HC = 0	0.4		0.7	A
$t_{d\ ON1-8\ H}$	Output delay time, HS switch on	V_S = 13.5 V, R_{load} = 52 Ω	10	25	80	µs
$t_{d\ OFF1-8\ H}$	Output delay time, HS switch off	V_S = 13.5 V, R_{load} = 52 Ω	50	100	300	µs
$t_{d\ ON1-8\ L}$	Output delay time, LS switch on	V_S = 13.5 V, R_{load} = 52 Ω	5	15	80	µs
$t_{d\ OFF1-8\ L}$	Output delay time, LS switch off	V_S = 13.5 V, R_{load} = 52 Ω	50	100	300	µs
$t_{D\ LH}/t_{D\ HL}$	Cross current protection time		20	200	400	µs
I_{QLH}	Switched-off output current HS OUT 1-8	V_{OUT1-8} = 0 V	-2			µA
I_{QLL}	Switched-off output current LS OUT 1-8	V_{OUT1-8} = V_S			2	µA
$I_{OLDHS1-8}$	Open-load detection current HS OUT 1-8	T_j = -40 °C	8	30	60	mA
		T_j = 25 °C to 125 °C	10	30	60	mA
$I_{OLDLSHC1-8}$	Open-load detection current LS OUT 1-8 in HC mode	HC bit set to 1; T_j = -40 °C	4.5	30	65	mA
		HC bit set to 1; T_j = 25 °C to 125 °C	8	30	60	mA
$I_{OLDLSLC1-8}$	Open-load detection current LS OUT 1-8 in LC mode	HC bit set to 0; T_j = -40 °C	1.8	15	35	mA
		HC bit set to 0; T_j = 25 °C to 125 °C	4	15	30	mA
t_{dOL}	Minimum duration of open-load condition to set the status bit		500	2000	3000	µs
t_{ISC}	Minimum duration of overcurrent condition to switch off the driver		10	32	100	µs
dV_{OUT1-8}/dt	Slew rate of OUT 1-8	V_S = 13.5 V, R_{load} = 52 Ω	0.1	0.25	0.5	V/µs

Figure 4. Output turn-on/off delays and slew rates

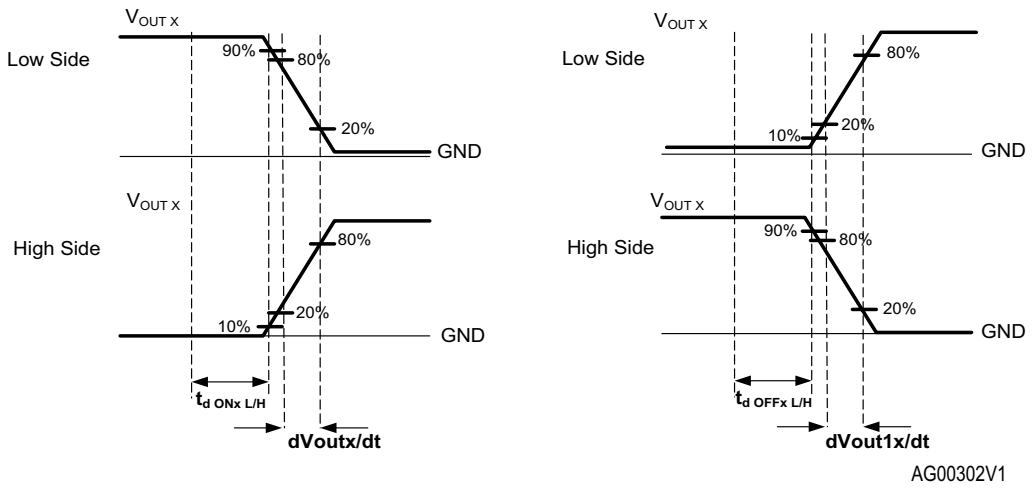


Table 11. Current monitor output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{CURR1/2}$	Functional voltage range	V_{CC} = 5 V	0		V_{CC} - 1	V
$I_{CURRHSLS250}$	HS/LS current monitor output ratio: $I_{CURR1/2}$ / $I_{OUT\ 1-8}$	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; prog. via SPI, I_{max} = 800 mA, HC = 1		1/250		-
$I_{CURRHSLS500}$	HS/LS current monitor output ratio: $I_{CURR1/2}$ / $I_{OUT\ 1-8}$	0 V ≤ $V_{CURR1/2}$ ≤V_{CC} - 1 V, V_{CC} = 5 V; prog. via SPI, I_{max} = 800 mA, HC = 1		1/500		-
$I_{CURRHSLS750}$	HS/LS current monitor output ratio: $I_{CURR1/2}$ / $I_{OUT\ 1-8}$	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; prog. via SPI, I_{max} = 800 mA, HC = 1		1/750		-
$I_{CURRHSLS1000}$	HS/LS current monitor output ratio: $I_{CURR1/2}$ / $I_{OUT\ 1-8}$	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; prog. via SPI, I_{max} = 800 mA, HC = 1		1/1000		-
$I_{CURRLSLC125}$	LS current monitor output ratio in LC mode: $I_{CURR1/2}$ / $I_{OUT\ 1-8}$	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; prog. via SPI, HC = 0; I_{max} = 400 mA		1/125		-
$I_{CURRLSLC250}$	LS current monitor output ratio in LC mode: $I_{CURRLSLC1/2}$ / $I_{OUT\ 1-8}$	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; prog. via SPI, HC = 0; I_{max} = 400 mA		1/250		-
$I_{CURRLSLC375}$	LS current monitor output ratio in LC mode: $I_{CURR1/2}$ / $I_{OUT\ 1-8}$	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; prog. via SPI, HC = 0; I_{max} = 400 mA		1/375		-
$I_{CURRLSLC500}$	LS current monitor output ratio in LC mode: $I_{CURR1/2}$ / $I_{OUT\ 1-8}$	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; prog. via SPI, HC = 0; I_{max} = 400 mA		1/500		-

Table 11. Current monitor output (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{CURRHS1/2\ acc}$	HS current monitor accuracy	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; $I_{OUT\ 1\text{-}8\ max}$ = 0.8 A (FS = full scale= 800 mA*current ratio); T_j = -40 °C		4% + 1%FS	10% + 3%FS	-
		0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; $I_{OUT\ 1\text{-}8\ max}$ = 0.8 A; (FS = full scale= 800 mA*current ratio); T_j = 25 °C to 125 °C		4% + 1%FS	8% + 2%FS	
$I_{CURRLSHC1/2\ acc}$	LS current monitor accuracy in HC mode	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; 0.4 A ≤ $I_{OUT1\text{-}8}$ ≤ 0.8 A (FS = full scale= 800 mA*current ratio)		4% + 1%FS	10% + 3%FS	-
$I_{CURRLSLC1/2\ acc}$	LS current monitor accuracy in LC mode	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; $I_{OUT\ 1\text{-}8\ max}$ = 0.4 A (FS = full scale= 800 mA*current ratio)		4% + 1%FS	10% + 3%FS	-

Table 12. Current monitor dynamic characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d\text{-}CM}$	Output to current monitor delay time	I_{OUT} from 100 mA to 200 mA; $t_{d\text{-}CM}$ measured from 50 % I_{OUT} to 50 % ICM	—	2	—	µs

Table 13. SMPS switched mode power supply gate driver output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SMPSHI}	SMPS output voltage high	V_S = 8 V, I_{SMPS} = -10 mA	4.5	5.5	6.5	V
V_{SMPL}	SMPS output voltage low	V_S = 8 V, I_{SMPS} = 10 mA			100	mV
t_{SMPSH}	Output rise time	V_S = 13.5 V, Cout = 2 nF		110	160	ns
t_{SMPSL}	Output fall time	V_S = 13.5 V, Cout = 2 nF		110	160	ns
$t_{dONSMPS}$	Output delay time, switch to high	V_S = 13.5 V, Cout = 2 nF		110	160	ns
$t_{dOFFSMPS}$	Output delay time, switch to low	V_S = 13.5 V, Cout = 2 nF		30	100	ns
$t_{dON\text{-}OFFSMPS}$	Output delay time difference ON/OFF	V_S = 13.5 V, Cout = 2 nF		80	120	ns
R_{SMPS}	Pull down resistor, SMPS		23	50	100	kΩ

Figure 5. SMPS timings

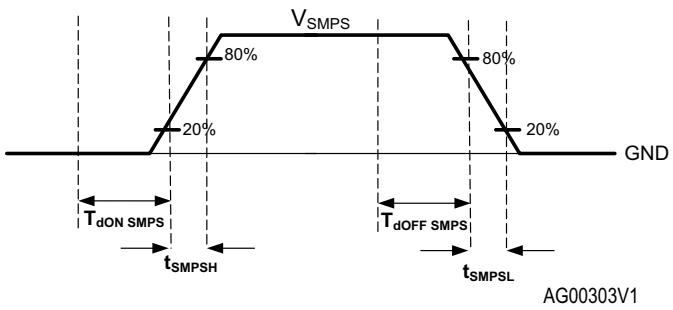


Table 14. Oscillator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{CLK}	Internal clock frequency		2.8	4	5.2	MHz

4.4.1 SPI electrical characteristics

V_S = 6 to 18 V, V_{CC} = 3.0 to 5.3 V, T_j = -40 to 150 °C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 15. DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SDI, SCK, CSN, EN						
V_{IL}	Input low voltage				$0.3V_{CC}$	V
V_{IH}	Input high voltage		$0.7V_{CC}$			V
$I_{CSN\ in}$	Pull up current at input CSN	V_{CSN} = 1.5 V; V_{CC} = 5 V	8	20	40	µA
$I_{SCK\ in}$	Pull down current at input SCK	V_{SCK} = 1.5 V; V_{CC} = 5 V	10	25	50	µA
$I_{DI\ in}$	Pull down current at input DI	V_{DI} = 1.5 V; V_{CC} = 5 V	10	25	50	µA
$R_{EN\ in}$	Pull down resistor at input EN	V_{EN} = 1.5 V; V_{CC} = 5 V	25	50	115	kΩ
SDO						
V_{OL}	Output low voltage	I_{out} = 2 mA		0.2	0.4	V

Table 15. DC characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	I_{out} = +2 mA	V_{CC} - 0.4	V_{CC} - 0.2		V
I_{DOLK}	3-state leakage current	$V_{CSN} = V_{CC}$, 0 V < V_{CC}	-10		10	µA

Table 16. AC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SDO, SDI, SCK, CSN, EN						
C_{OUT}(1)	Output capacitance (SDO)	V_{OUT} = 0 V to 5 V	—	—	10	pF
C_{IN}(1)	Input capacitance (SDI)	V_{IN} = 0 V to 5 V	—	—	10	pF
	Input capacitance (other pins)	V_{IN} = 0 V to 5 V	—	—	10	pF

1. Guaranteed by design

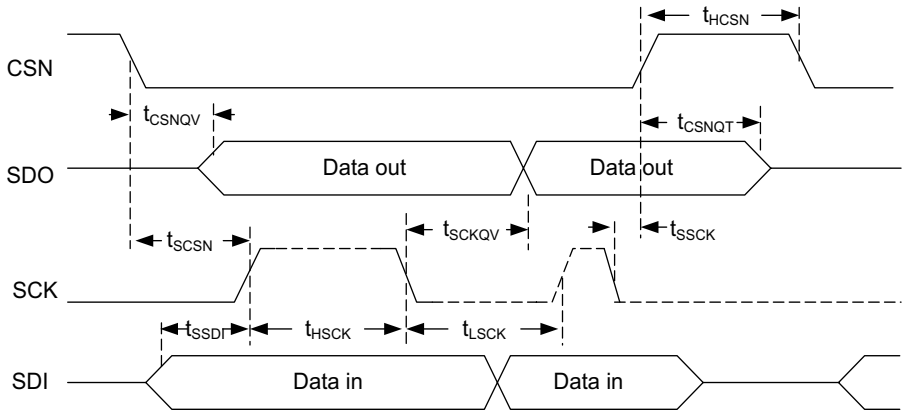
Table 17. Dynamic characteristics(1)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{EN}	EN high setup time				100	µs
t_{SCSN}	CSN setup time before SCK rising		400			ns
t_{HCSN}	CSN high time		2			µs
t_{CSNQV}	CSN falling until SDO valid	C_{out} = 100 pF			100	ns
t_{CSNQT}	CSN rising until SDO 3-state	C_{out} = 100 pF			150	ns
t_{SSCK}	SCK setup time before CSN rising		50			ns
t_{SSDI}	SDI setup time before SCK rising		40			ns
t_{HSCK}	SCK high time		200			ns
t_{LSCK}	SCK low time		200			ns
t_{SCKQV}	SCK falling until SDO valid	C_{out} = 100 pF			150	ns
t_{QLQH}	Output rise time	C_{out} = 100 pF, 20 % - 80 % x V_{CC}			110	ns
t_{QHQL}	Output fall time	C_{out} = 100 pF, 80 % - 20 % x V_{CC}			110	ns
f_{SPI}	SPI frequency				1	MHz

1. See *Section 4.4.2: SPI timing parameter definition*.

4.4.2 SPI timing parameter definition

Figure 6. SPI timing



t_{CSNQV} : CSN falling until SDO valid
t_{CSNQT} : CSN rising until SDO tristate
t_{SCKQV} : SCK rising until SDO valid
t_{SCSN} : CSN setup time before SCK rising
t_{SSDI} : SDI setup time before SCK rising
t_{HSCK} : minimum SCK high time
t_{LSCK} : minimum SCK low time
t_{HCSN} : minimum CSN high time
t_{SSCK} : SCK setup time before NCS rising

AG00304V1

5 Functional description of the SPI

5.1 Signal description

5.1.1 Serial clock (SCK)

This input signal provides the timing of the serial interface. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCK). Data on Serial Data Out (SDO) is shifted out at the falling edge of Serial Clock (see *Figure 7*).

The SPI can be driven by a microcontroller with its SPI peripherals running in following mode: CPOL=0 and CPHA=0 (see *Figure 7*).

5.1.2 Serial data input (SDI)

This input is used to transfer data serially into the device. It receives the data to be written. Values are latched on the rising edge of Serial Clock (SCK).

Serial data output (SDO)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK). SDO also reflects the status of the <Global Error Flag> (Bit 7 of the <Global Status Register>) while CSN is low and no clock signal is present.

Chip select not (CSN)

When this input signal is High, the device is deselected and Serial Data Output (SDO) is high impedance (3-state). Driving this input low enables the communication. The communication must start and stop on a low level of Serial Clock (SCK).

Figure 7. Clock polarity and clock phase

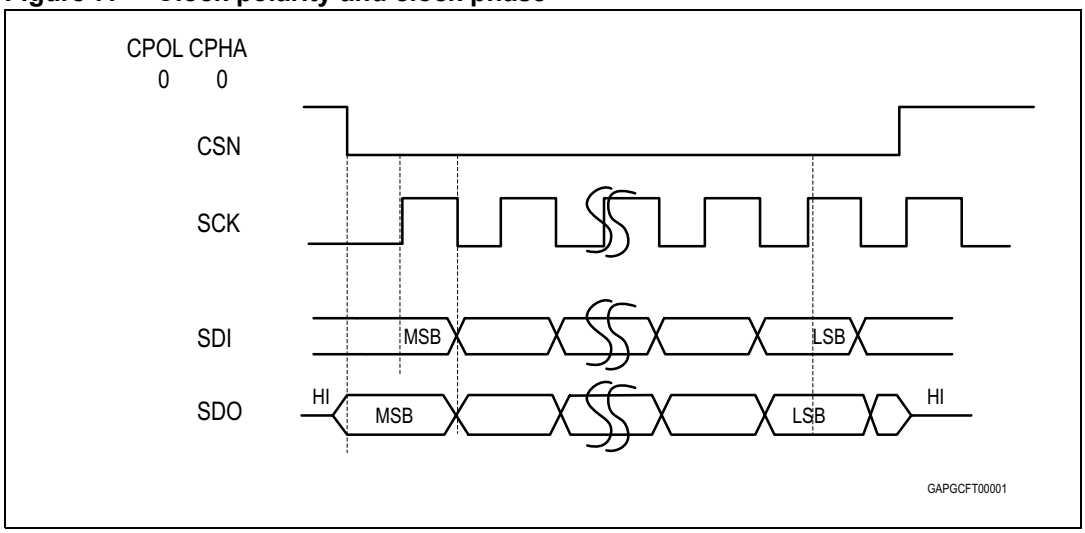
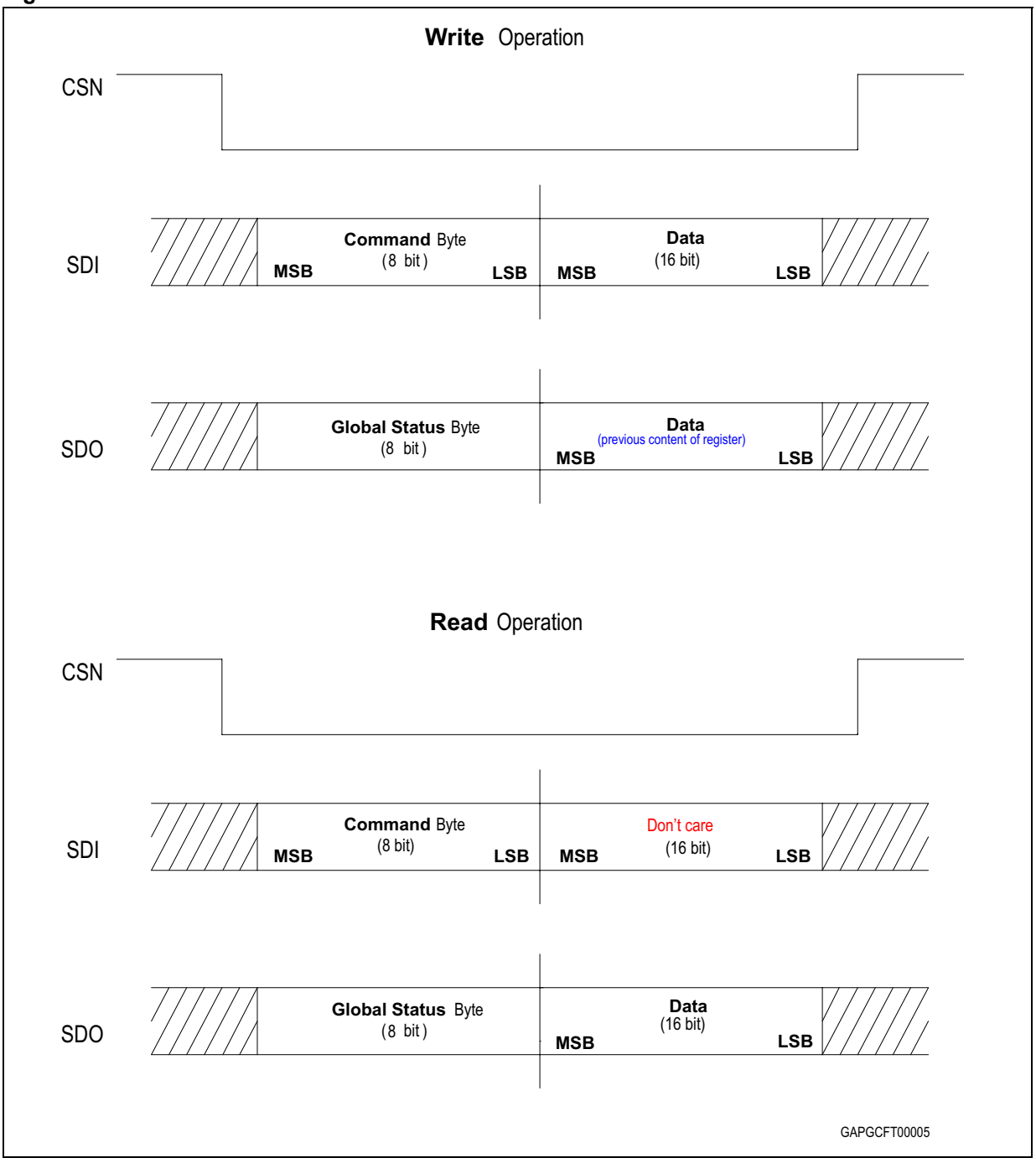


Figure 8. SPI frame structure



5.2 SPI communication flow

5.2.1 General description

The proposed SPI communication is based on a standard SPI interface structure using CSN (Chip Select Not), SDI (Serial Data In), SDO (Serial Data Out/Error) and SCK (Serial Clock) signal lines. Maximum SPI frequency is 1 MHz.

At the beginning of each communication the master reads the <SPI-frame-ID> register (ROM address 3EH) of the slave device. This 8-bit register indicates the SPI frame length (24-bit for the L99MD01) and the availability of additional features.

Each communication frame consists of an instruction byte which is followed by 2 data bytes (see *Figure 8*).

The data returned on SDO within the same frame always starts with the <Global Status> register. It provides general status information about the device. It is followed by 2bytes (i. e. 'In-frame-response', *Figure 8*).

For write cycles the *<Global Status>* register is followed by the previous content of the addressed register.

For read cycles the <Global Status> register is followed by the content of the addressed register.

Table 18. Command byte (8 bit)

	Operating code		Address					
Bit	23	22	21	20	19	18	17	16
Name	OC1	OC0	A5	A4	A3	A2	A1	A0

Table 19. Data byte

	Data byte 1								Data byte 0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

5.2.2 Command byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Read>, <Write>, <Read and Clear Status>, <Read Device Information>) and a 6 bit address.

Table 20. Operating code definition

OC1	OC0	Meaning
0	0	<Write mode>
0	1	<Read mode>
1	0	<Read and clear status>
1	1	<Read device information>

The <Write Mode> and <Read Mode> operations allow access to the RAM of the device, i. e. write to control registers or read status information.

A <Read and Clear Status> operation addressed to a device specific status register reads back and subsequently clear this status register. A <Read and Clear Status> operation with address 3FH clears all status registers at a time and reads back the <Configuration> register.

A <Read and Clear Status> operation addressed to an unused RAM address register is identical to a <Read Mode> operation (in case of unused RAM address, the second byte is equal to 00H).

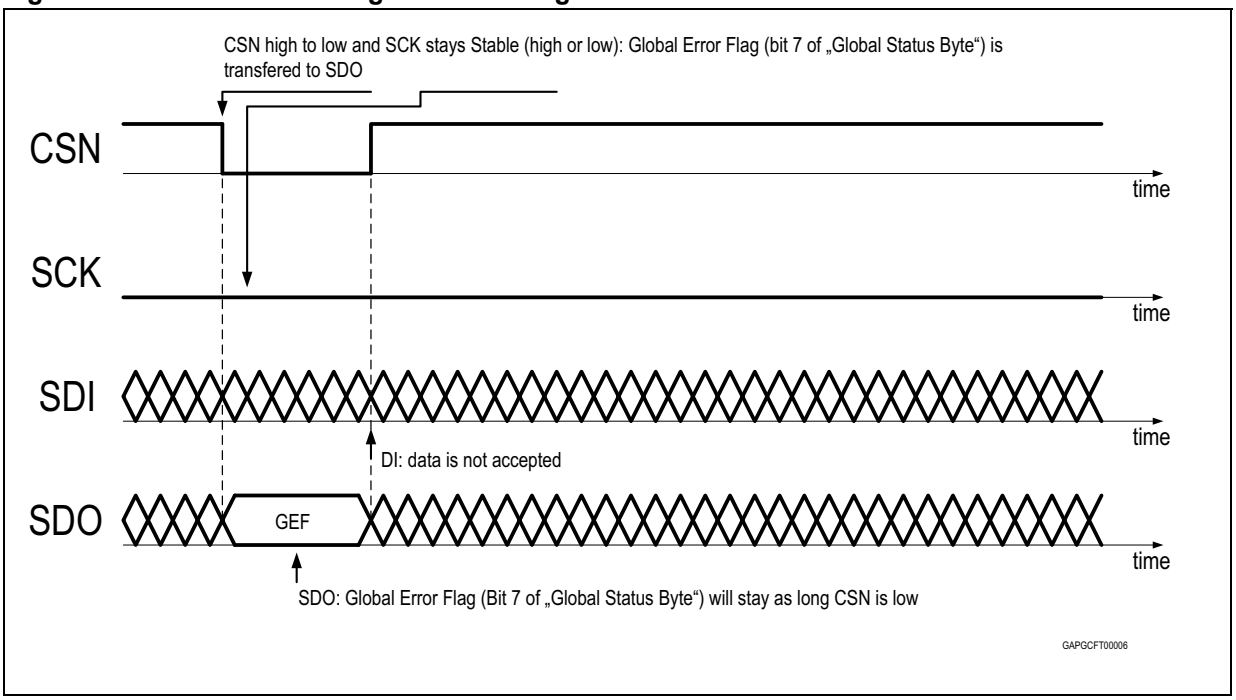
<Read Device Information> allows access to the ROM area which contains device related information such as the product family, product name, silicon version and register width.

Table 21. Global status byte

<table>
<tr><th>Bit</th><th>Description</th><th>Polarity</th><th>Comment</th></tr>
<tr><td>0</td><td>Software reset or under/overvoltage</td><td>Active high</td><td>Depends on bit 5 of <Global Status Byte>:<table><tr><th>Bit 5</th><th>Bit 0</th></tr><tr><td>0</td><td>Set if software reset (SDI stuck at 1 or 0)</td></tr><tr><td>1</td><td>Logical OR of the under- / overvoltage status bits</td></tr></table></td></tr>
<tr><td>1</td><td>Overcurrent detected</td><td>Active high</td><td>Set by any overcurrent event</td></tr>
<tr><td>2</td><td>Open-load detected</td><td>Active high</td><td>Set by any open-load event</td></tr>
<tr><td>3</td><td>Temp warning</td><td>Active high</td><td></td></tr>
<tr><td>4</td><td>Thermal shutdown / chip overload</td><td>Active high</td><td></td></tr>
<tr><td>5</td><td>Not (chip reset or communication error)</td><td>Active low</td><td>Activated by all internal reset events that change device state or configuration registers (e. g. software reset, V_{CC} under-voltage, etc.). The bit is set after a valid communication with any register. This bit is initially ‘0’ and is set to ‘1’ by a valid SPI communication</td></tr>
<tr><td>6</td><td>Communication Error</td><td>Active high</td><td>Bit is set if the number of clock cycles during CSN = low does not match with the specified frame width or if an invalid bus condition is detected (SDI stuck at 1 or 0).</td></tr>
<tr><td>7</td><td>Global Error Flag</td><td>Active high</td><td>Logic OR combination of all failures in the <Global Status Byte>.</td></tr>
</table>

The *<Global Error Flag>* is generated by an OR-combination of all failure events of the device (i.e. bit 0 to bit 6 of the *<Global Status Byte>*.

Figure 9. Indication of the global error flag on SDO when CSN is low and SCK is stable.



The bit 0 of the <*Global Status Byte*> is a combination of an under/overvoltage warning and a software warning: If the bit 5 is one (this is the standard after a correct SPI communication), bit 0 is the logical OR of all under- and overvoltage status bits.

On the other hand, if there has been an SPI communication error or a chip reset (bit 5 is zero), then bit 0 gives a better indication about the SPI error: An SDI stuck-at error leads to a software reset and sets bit 0, while a clock pulse error only sets the communication error bit, clears bit 5 and clears also bit 0. This leads to the following table of possible states (assuming there is no under/overvoltage, overcurrent, openload or thermal error):

Table 22. Reset

State	Description	Global status
EN = 0 (power on reset)	All registers reset Outputs switched off (3-state)	1000 0000
Clock cycles != 24	Ignore frame No reset	1100 0000
SDI always 0	Software reset Outputs switched off	1100 0001
SDI always 1	Software reset Outputs switched off	1100 0001

Writing to the selected data input register is only enabled if exactly one frame length is transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame, the complete frame is ignored and a SPI frame error is signaled in the Global Status register. This safety function is implemented to avoid an unwanted activation of output stages by a wrong communication frame.

For read operations, the *<communication error>* bit in the *<Global Status Byte>* is set, but the register to be read is still transferred to the SDO pin. If the number of clock cycles is smaller than the frame width, the data at SDO are truncated. If the number of clock cycles is larger than the frame width, the data at SDO are filled with '0' bits.

Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

Note: As the frame width is 24 bits, an initial Read of <SPI-frame-ID> using a 16 bits communication sets the <communication Error bit> of the <Global Status Byte>. A subsequent correct length transaction is necessary to correct this bit.

5.3 Write operation

OC0, OC1: operating code (00 for 'write' mode)

The write operation starts with a command byte followed by 2 data bytes.

For write cycles the *<Global Status>* register is followed by the previous content of the addressed register.

The RAM memory area consists of 16 bit registers. All unused RAM addresses are read as '0'.

Failures are indicated by activating the corresponding bit of the <Global Status> register.

Note: RAM address 00H is unused. An attempt to access this address is recognized as a communication line error ('Data-in stuck to GND') and all internal registers are cleared (software reset).

5.4 Read operation

OC0, OC1: operating code (01 for 'read' mode)

The read operation starts with a command byte followed by 2 data bytes. The content of the data bytes is 'don't care'. The content of the addressed register is shifted out at SDO within the same frame ('in-frame response').

The returned data byte represents the content of the register to be read.

Failures are indicated by activating the corresponding bit of the <Global Status> register.

5.5 Read and clear status operation

OC0, OC1: operating code (10 for 'read and clear status' mode)

The 'Read and Clear Status' operation starts with a command byte followed by 2 data bytes. The content of the data bytes is 'don't care'. The content of the addressed status register is transferred to SDO within the same frame ('in-frame response') and is subsequently cleared.

A 'Read and Clear Status' operation with address 3FH clears all Status registers simultaneously.

A <Read and Clear Status> operation addressed to an unused RAM address is identical to a <Read Mode> operation (in case of unused RAM address, the second byte is equal to 00H).

The returned data byte represents the content of the register to be read.

Failures are indicated by activating the corresponding bit of the <Global Status> register.

5.6 Read device information

OC0, OC1: operating code (11 for ‘read device information mode).

The device information is stored at the ROM In the ROM memory area, the first 8 bits are used. All unused ROM addresses are read as ‘0’.

Note: ROM address 3FH is unused. An attempt to access this address is recognized as a communication line error (‘Data-in stuck to V_{CC}’) all internal registers are cleared (software reset).

6 SPI control and status register

Table 23. RAM memory map

Address	Name	Access	Content
01h	Control register 1	Read/write	Output switch on/off
02h	Control register 2	Read/write	SMPS driver configuration
03h	Control register 3	Read/write	Low-side high current mode V_S configuration SMPS configuration
04h	Control register 4	Read/write	Current multiplexer
05h	Control register 5	Read/write	PWM
06h	Control register 6	Read/write	Open-load
10h	Status register 0	Read only	Overcurrent
11h	Status register 1	Read only	Open-load
12h	Status register 2	Read only	TSD Over/undervoltage

Table 24. ROM memory map (access with OC0 and OC1 set to '1')

Address	Name	Access	Content
00h	ID Header	Read only	43h (device class ASSP, 2 additional information bytes)
01h	Version	Read only	00h (engineering samples) (ST-SPI)
02h	ProducCode1	Read only	3Eh (62 ST_SPI)
03h	ProducCode2	Read only	4Eh (N ST_SPI)
3Dh	Fuses	Read only	Fuse data 9 - 0
3Eh	SPI-Frame ID	Read only	02h SPI-Frame-ID Register (24 Bit ST_SPI)

6.1 Control status register

Default reset value is 0, all unused bits read 0, unused bits have to be set to 0

Table 25. Control status register

Address	Access	Data byte 1								Data byte 0							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
01h	R/W	HS8	LS8	HS7	LS7	HS6	LS6	HS5	LS5	HS4	LS4	HS3	LS3	HS2	LS2	HS1	LS1
		Output switch on/off															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
02h	R/W	0	0	ON	ON	ON	ON	ON	ON	0	0	OFF	OFF	OFF	OFF	OFF	OFF
		On/off cycles counter for SMPS driver (OFF must be > 3dec.)															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
03h	R/W	HC8	HC7	HC6	HC5	HC4	HC3	HC2	HC1	0	V_S OV warn/ shutdown	V_{S2} reco.	Wob	Wob	Freq dev.	Freq dev.	Rnd/ lin
		Low-side high current (reset value = 1)											**SMPS configuration**				
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
04h	R/W	OUTx to CURR2	OUTx to CURR2	OUTx to CURR2	OUTx to CURR2	OUTx to CURR1	OUTx to CURR1	OUTx to CURR1	OUTx to CURR1	0	0	0	0	2K- fact	2K-fact	1K-fact	1K-fact
				Current multiplexer													
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
05h	R/W	0	0	0	0	0	0	PWM duty		OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1
		PWM															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
06h	R/W	0	0	0	0	0	0	0	0	disable OL8	disable OL7	disable OL6	disable OL5	disable OL4	disable OL3	disable OL2	disable OL1
		Open-load															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10h	R	HS8	LS8	HS7	LS7	HS6	LS6	HS5	LS5	HS4	LS4	HS3	LS3	HS2	LS2	HS1	LS1
		Status overcurrent															

Table 25. Control status register (continued)

Address	Access	Data byte 1								Data byte 0							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11h	R	0	0	0	0	0	0	0	0	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1
		Status open-load															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
12h	R	0	0	0	0	0	0	0	0	TSD	TSD warn	V_{S2} UV	V_{S2} OV	V_S UV	V_S OV	V_{SB} UV	V_{SA} UV
		Status TSD; over/ undervoltage															

Table 26. Control register 1

Bit	Control register 1 (read/write); address 01h	
	Name	**Comment**
15	OUT8 – HS on/off	If a bit is set, the selected output driver is switched on. If the corresponding PWM enable bit is set the driver is PWMed. If the bits of HS- and LS-driver of the same half bridge are set, the HS- and the LS-driver is deactivated.
14	OUT8 – LS on/off	
13	OUT7 – HS on/off	
12	OUT7 – LS on/off	
11	OUT6 – HS on/off	
10	OUT6 – LS on/off	
9	OUT5 – HS on/off	
8	OUT5 – LS on/off	
7	OUT4 – HS on/off	
6	OUT4 – LS on/off	
5	OUT3 – HS on/off	
4	OUT3 – LS on/off	
3	OUT2 – HS on/off	
2	OUT2 – LS on/off	
1	OUT1 – HS on/off	
0	OUT1 – LS on/off	

Table 27. Control register 2

Bit	Control register 2 (read/write); address 02h	
	Name	Comment
SMPS frequency and duty cycle.		
15	-	
14	-	
13	SMPS on cycles bit 5	Number of ON cycles for SMPS driver, binary coded. Cycles are based on the internal oscillator If all bits are set to “1” the SMPS output is high for 63 clock cycles.
12	SMPS on cycles bit 4	
11	SMPS on cycles bit 3	
10	SMPS on cycles bit 2	
9	SMPS on cycles bit 1	
8	SMPS on cycles bit 0	
7	-	
6	-	
5	SMPS off cycles bit 5	Number of OFF cycles for SMPS driver, binary coded. Cycles are based on the internal Oscillator. If OFF is set to values 3 the SMPS driver is switched off. If all bits are set to “1” the SMPS output is low for 63 clock cycles.
4	SMPS off cycles bit 4	
3	SMPS off cycles bit 3	
2	SMPS off cycles bit 2	
1	SMPS off cycles bit 1	
0	SMPS off cycles bit 0	

Table 28. Control register 3

Bit	Control register 3 (read/write); address 03h	
	Name	Comment
15	High current LS 8	High current mode of low-side switch “0”: The selected low-side switch is in low current mode. The overcurrent and open-load thresholds are reduced by ½. The selected current monitor ratio is doubled. “1” (default setting) the selected low-side switch is in high current mode
14	High current LS 7	
13	High current LS 6	
12	High current LS 5	
11	High current LS 4	
10	High current LS 3	
9	High current LS 2	
8	High current LS 1	
7	-	
6	V_S OV shutdown/warn	In case of V_S overvoltage “0”: all outputs are switched off + status bit set “1”: only status bit is set

Table 28. Control register 3 (continued)

Bit	Control register 3 (read/write); address 03h	
	Name	Comment
5	V_{S2} recovery	V_{S2} recovery mode: “0”: no recovery after V_{S2} overvoltage “1”: If the V_{S2} voltage falls below the threshold after a V_{S2} overvoltage condition, the SMPS goes again in active mode and the status bit is cleared
SMPS configuration		
4	Wobble bit 1	Wobble defines the modulation frequency deviation of the internal oscillator, definition see *Table 29*.
3	Wobble bit 0	
2	Frequency deviation bit 1	Frequency deviation of the internal oscillator, definition see *Table 30*
1	Frequency deviation bit 0	
0	Rnd/Lin	Random/linear mode: “0”: the oscillator is changed in linear mode like a triangle. “1”: the oscillator frequency is distributed randomly.

Table 29. Wobble

Bit 4	Bit 3	Wobble
0	0	1.95 KHz
0	1	3.9 KHz
1	0	7.8 KHz
1	1	15.6 KHz

Table 30. Frequency deviation

Bit 2	Bit 1	Frequency deviation
0	0	0 %
0	1	5 %
1	0	10 %
1	1	20 %

Table 31. Control register 4

Bit	Control register 4 (read/write); address 04h									
	Name	Comment								
15	OUTx to CURR2 bit 2	Bit setting	111	110	101	100	011	010	001	000
14	OUTx to CURR2 bit 1	To CURR2	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1
13	OUTx to CURR2 bit 0									
12	Enable CURR2	Enable the current monitor output 2								
11	OUTx to CURR1 bit 2	Bit setting	111	110	101	100	011	010	001	000
10	OUTx to CURR1 bit 1	To CURR1	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1
9	OUTx to CURR1 bit 0									
8	Enable CURR1	Enable the current monitor output 1								
7	-									
6	-									
5	-									
4	-									
3	CURR2 K-factor	Current monitor ratio I_{OUTx}/I_{CURR} If the high current bit (register 03h) is set to 0 the ratio for the low-side is the double of the programmed one.								
2	CURR2 K-factor									
1	CURR1 K-factor									
0	CURR1 K-factor									

Table 32. Ratio for CURR2

Bit3	Bit2	Ratio for CURR2
0	0	1/1000
0	1	1/750
1	0	1/500
1	1	1/250

Table 33. Ratio for CURR1

Bit1	Bit0	Ratio for CURR1
0	0	1/1000
0	1	1/750
1	0	1/500
1	1	1/250

Table 34. Control register 5

<table>
<tr><th rowspan="2">Bit</th><th colspan="2">Control register 5 (read/write); address 05h</th></tr>
<tr><th>Name</th><th>Comment</th></tr>
<tr><td>15</td><td>-</td><td></td></tr>
<tr><td>14</td><td>-</td><td></td></tr>
<tr><td>13</td><td>-</td><td rowspan="5"></td></tr>
<tr><td>12</td><td>-</td></tr>
<tr><td>11</td><td>-</td></tr>
<tr><td>10</td><td>-</td></tr>
<tr><td>9</td><td>PWM duty bit 1</td></tr>
<tr><td>8</td><td>PWM duty bit 0</td><td></td></tr>
<tr><td>7</td><td>PWM to OUT 8</td><td rowspan="8">PWM enable
“0”: PWM disabled for this output
“1”: If the corresponding enable bit is set and the PWM bit is set to “1” the programmed output is PWM’ed with typical 100 Hz</td></tr>
<tr><td>6</td><td>PWM to OUT 7</td></tr>
<tr><td>5</td><td>PWM to OUT 6</td></tr>
<tr><td>4</td><td>PWM to OUT 5</td></tr>
<tr><td>3</td><td>PWM to OUT 4</td></tr>
<tr><td>2</td><td>PWM to OUT 3</td></tr>
<tr><td>1</td><td>PWM to OUT 2</td></tr>
<tr><td>0</td><td>PWM to OUT 1</td></tr>
</table>

Bit 9	Bit 8	PWM duty cycle
0	0	15 %
0	1	30 %
1	0	45 %
1	1	60 %

Table 35. Control register 6

Bit	Control register 6 (read/write); address 06h	
	Name	Comment
15	-	
14	-	
13	-	
12	-	
11	-	
10	-	
9	-	
8	-	
7	Disable OL OUT8	Disable the open-load measurement “0”: open-load is signaled via the corresponding bit in status register 2 and the global error byte “1”: in case of an open-load, no register changes. Also the global error register not changes.
6	Disable OL OUT7	
5	Disable OL OUT6	
4	Disable OL OUT5	
3	Disable OL OUT4	
2	Disable OL OUT3	
1	Disable OL OUT2	
0	Disable OL OUT1	

Table 36. Status register 0

Bit	Status register 0 (read only); address 10h	
	Name	Comment
15	HS8	Overcurrent error detected, driver is deactivated
14	LS8	
13	HS7	
12	LS7	
11	HS6	
10	LS6	
9	HS5	
8	LS5	
7	HS4	
6	LS4	
5	HS3	
4	LS3	
3	HS2	
2	LS2	
1	HS1	
0	LS1	

Table 37. Status register 1

Bit	Status register 1 (read only); address 11h	
	Name	Comment
15-8	-	-
7	Open-load Out8	Open-load detected, information only No changes if the corresponding disable OL bit (Control register 6) is set
6	Open-load Out7	
5	Open-load Out6	
4	Open-load Out5	
3	Open-load Out4	
2	Open-load Out3	
1	Open-load Out2	
0	Open-load Out1	

Table 38. Status register 2

Bit	Status register 2 (read only); address 12h	
	Name	Comment
15-8	-	-
7	TSD	Overtemperature detected: all the drivers are switched off
6	TSD warning	Overtemperature warning level detected, information only
5	V_{S2} UV	V_{S2} undervoltage
4	V_{S2} OV	V_{S2} overvoltage
3	V_S UV	V_S undervoltage
2	V_S OV	V_S overvoltage
1	V_{SB} UV	V_{SB} undervoltage
0	V_{SA} UV	V_{SA} undervoltage

7 Application examples

Figure 10. Driving 4 bipolar stepper motors simultaneously

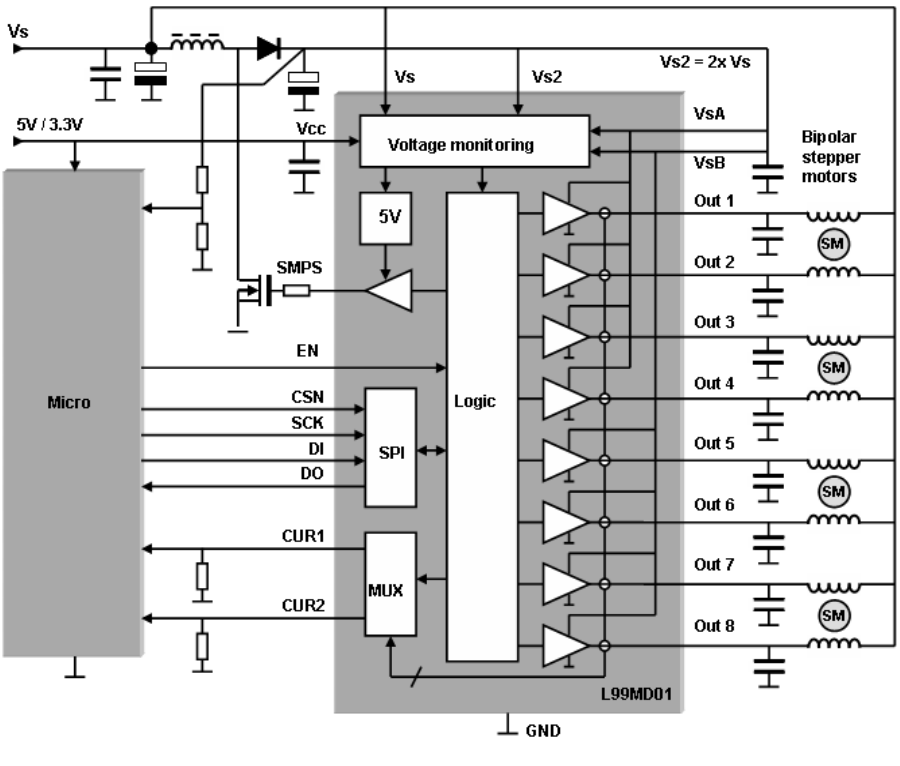


Figure 11. Driving 2 bipolar stepper motors simultaneously and 3 DC-motors sequentially

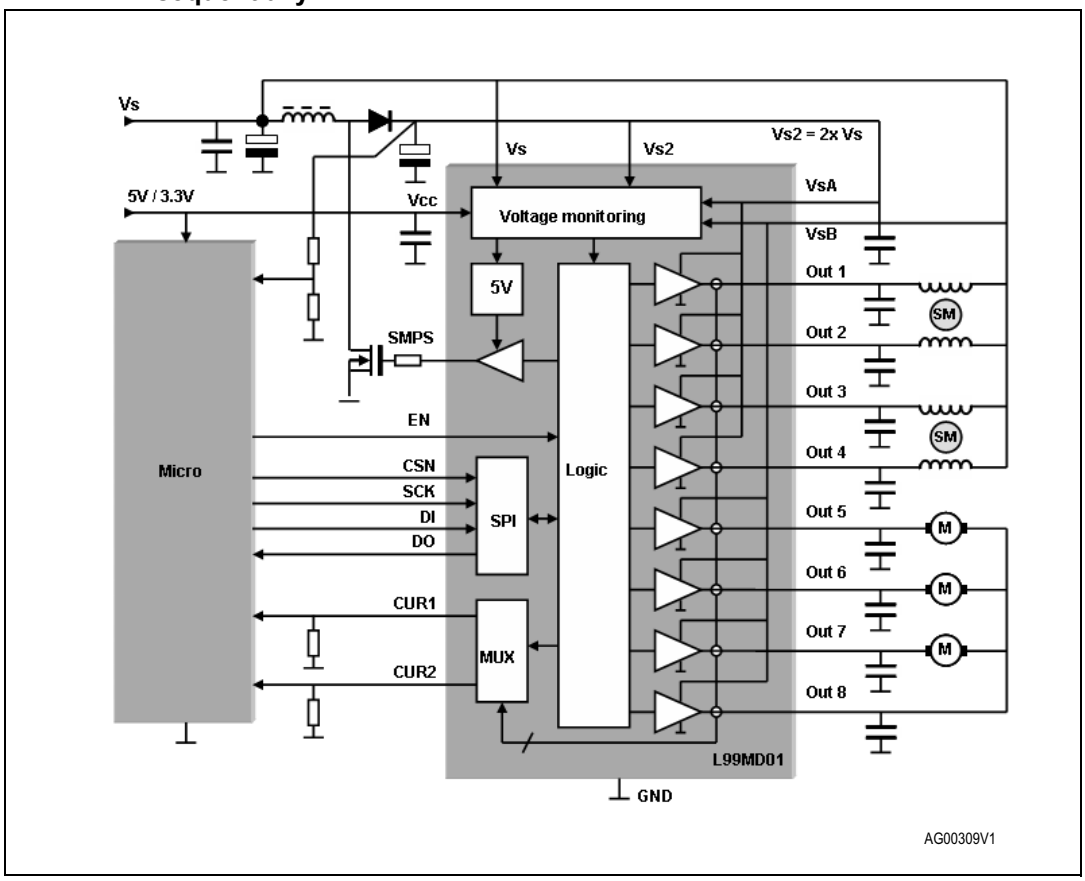


Figure 12. Driving 2 bipolar stepper motors simultaneously

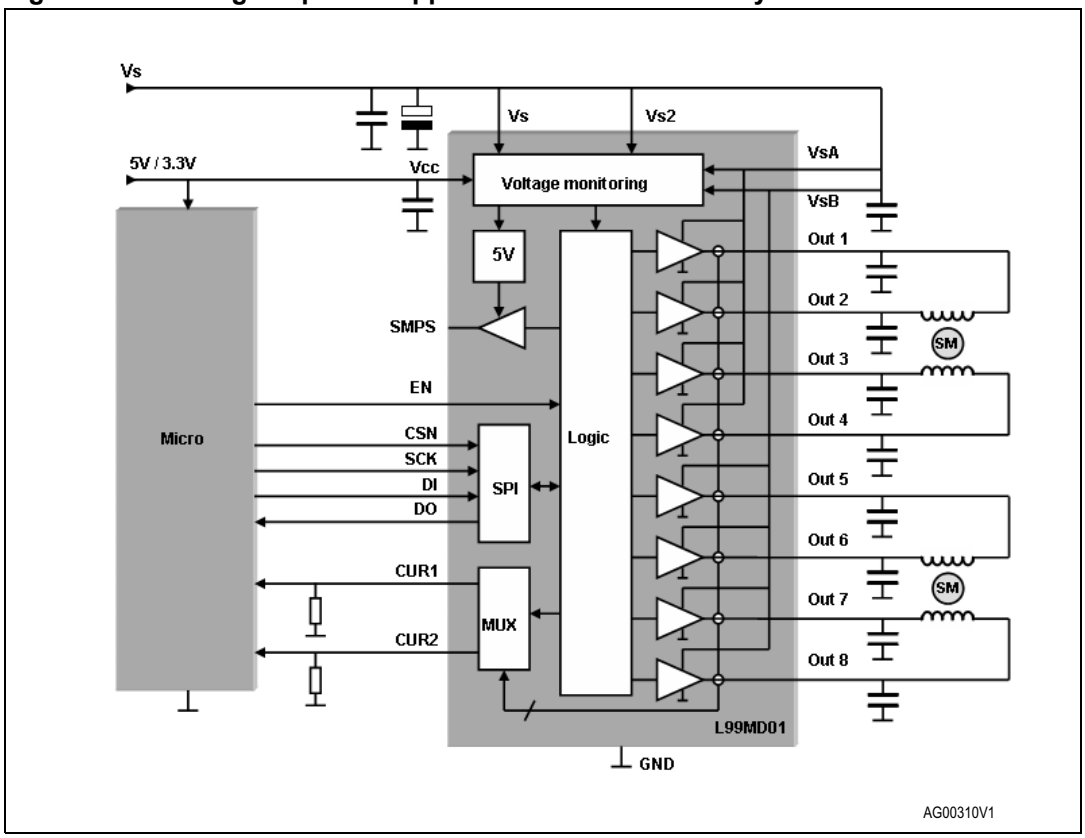


Figure 13. Driving 1 bipolar stepper motor and 2 DC-motors simultaneously

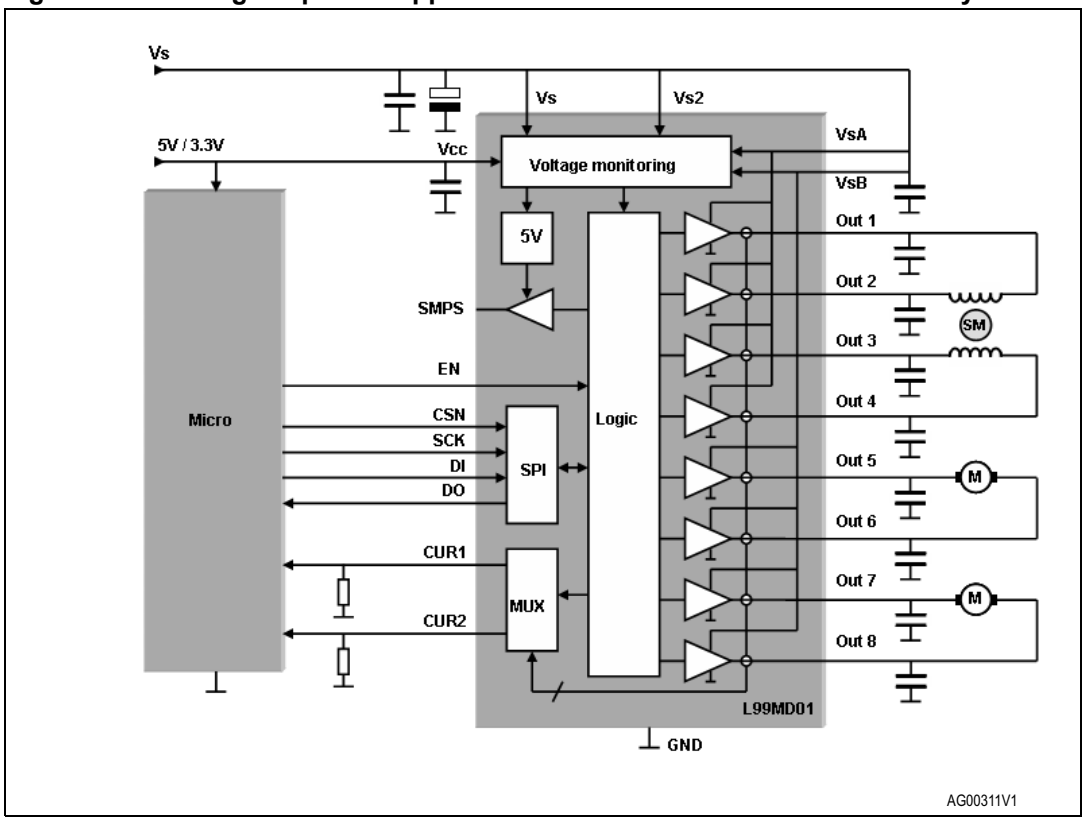


Figure 14. Driving 3 bipolar stepper motors sequentially

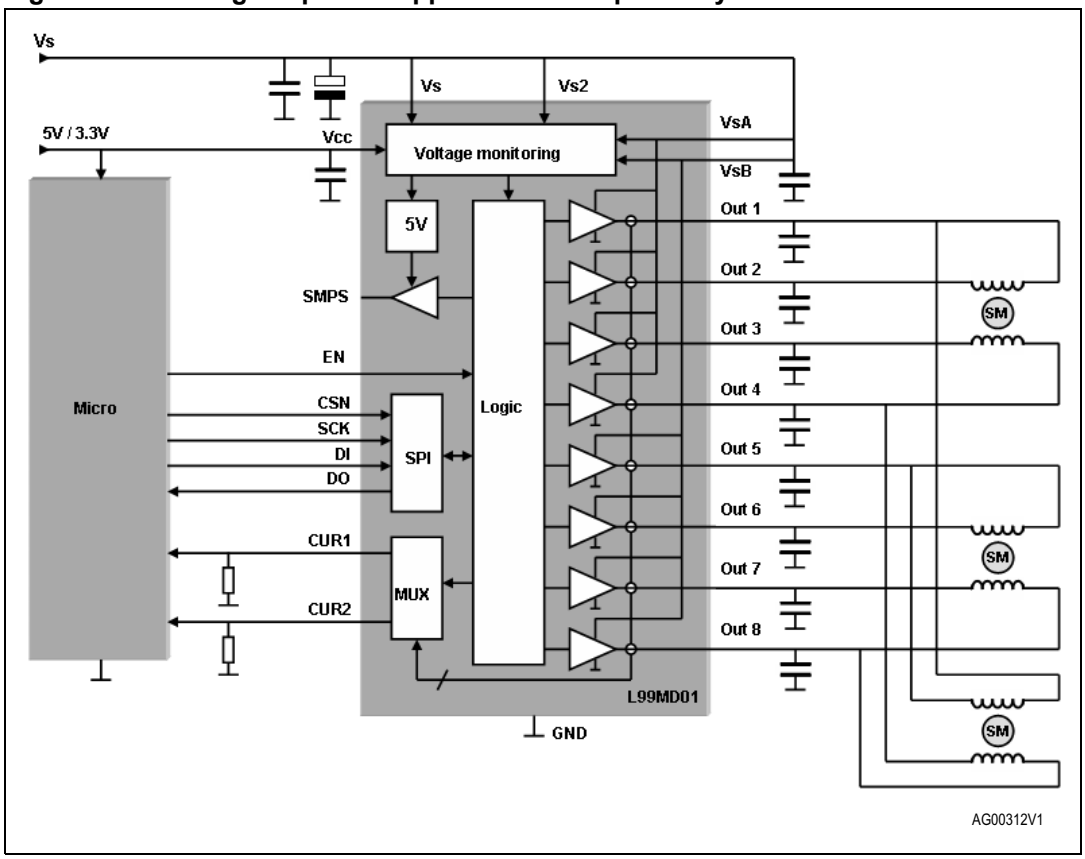


Figure 15. Driving 4 DC-motors simultaneously

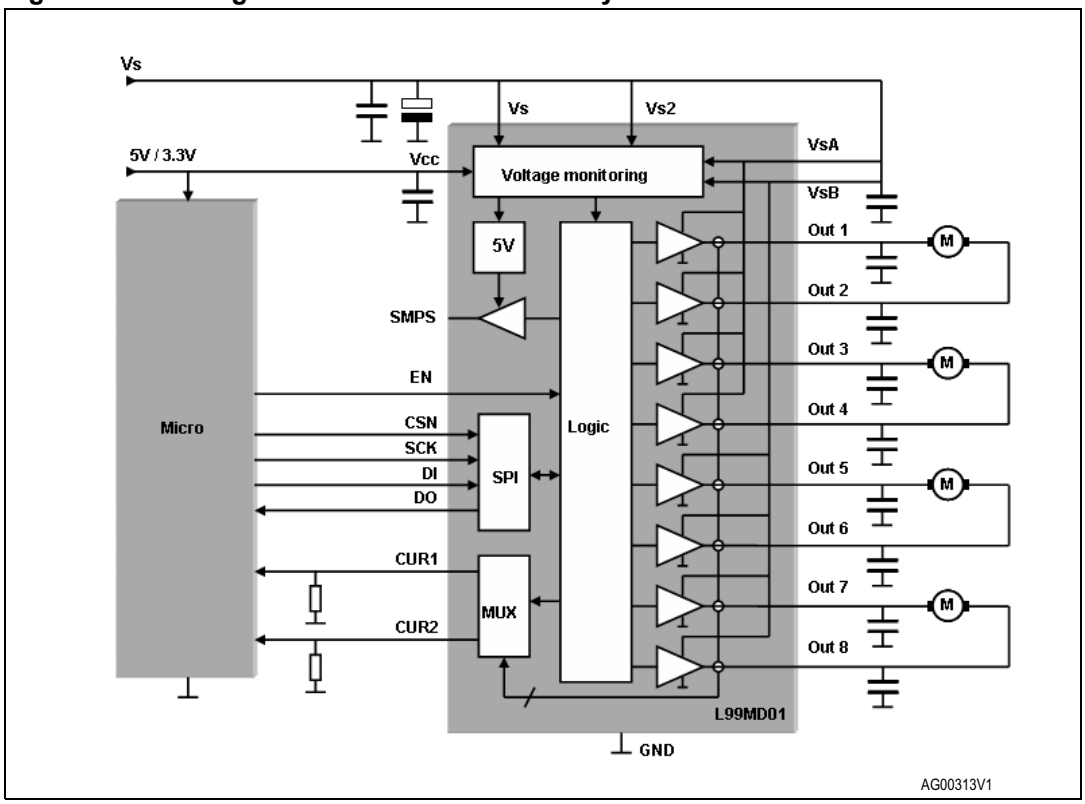


Figure 16. Driving 3 DC-motors simultaneously and 2 DC-motors sequentially

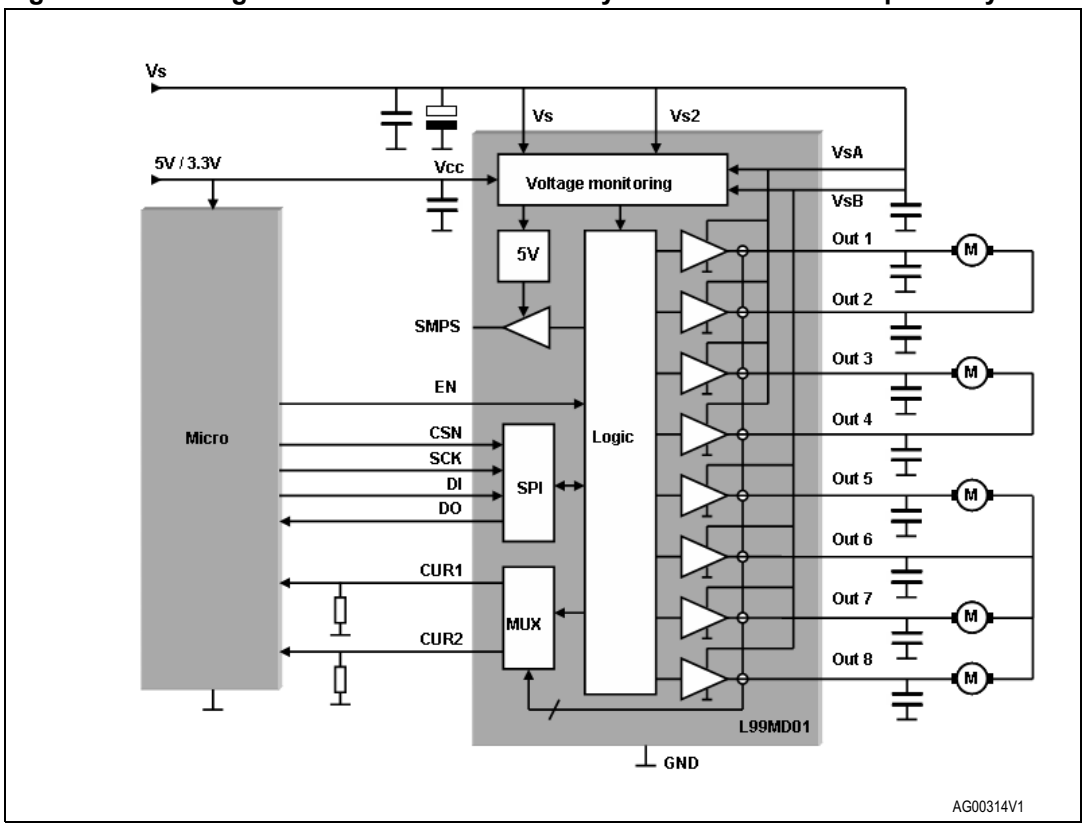


Figure 17. Driving 7 DC-motors sequentially

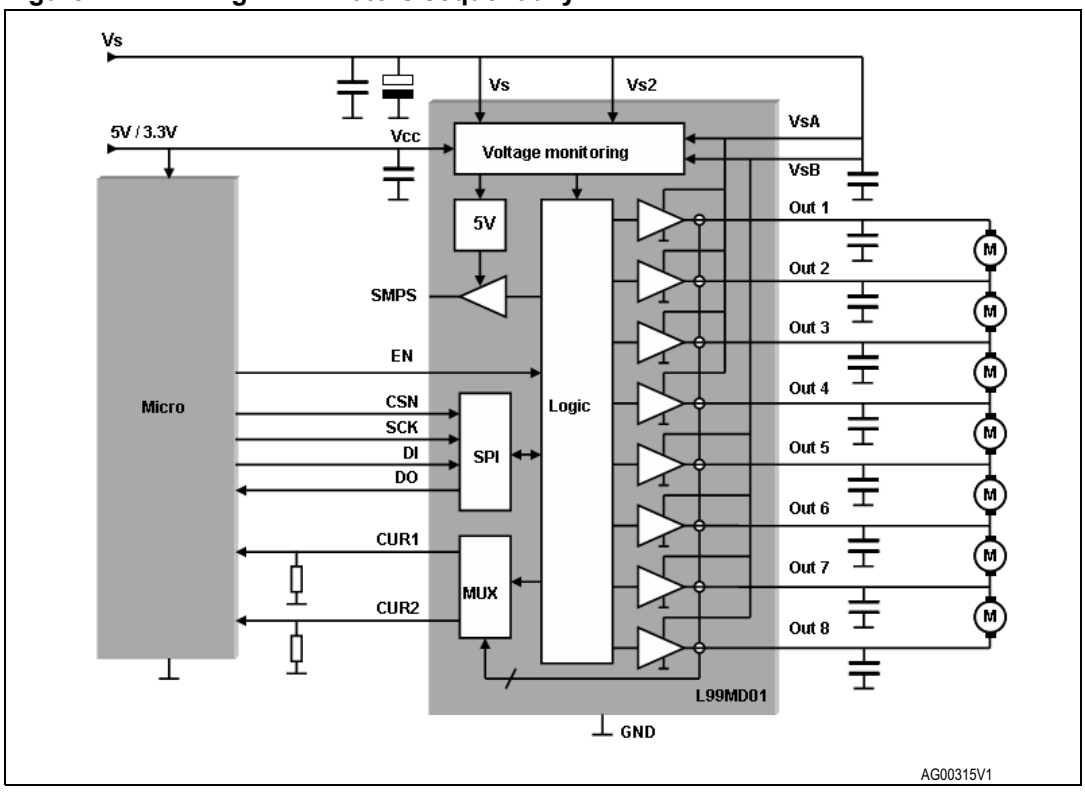


Figure 18. Driving simultaneously 4 unipolar winded stepper motors in bipolar mode

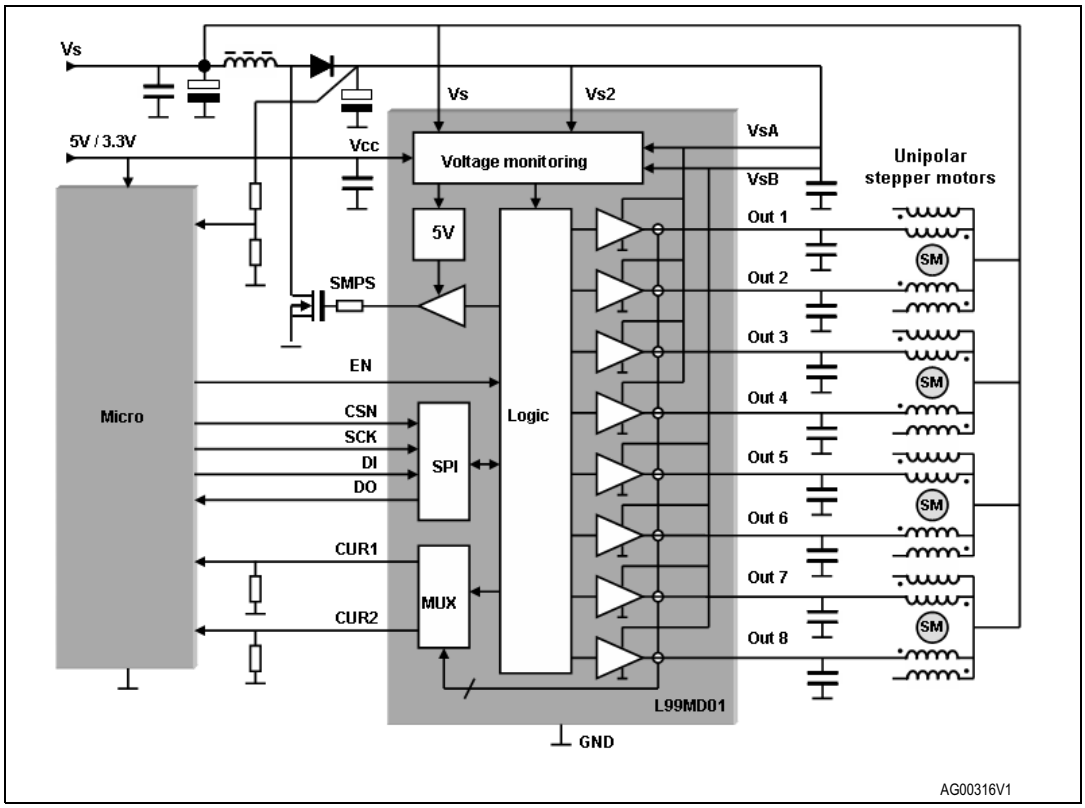
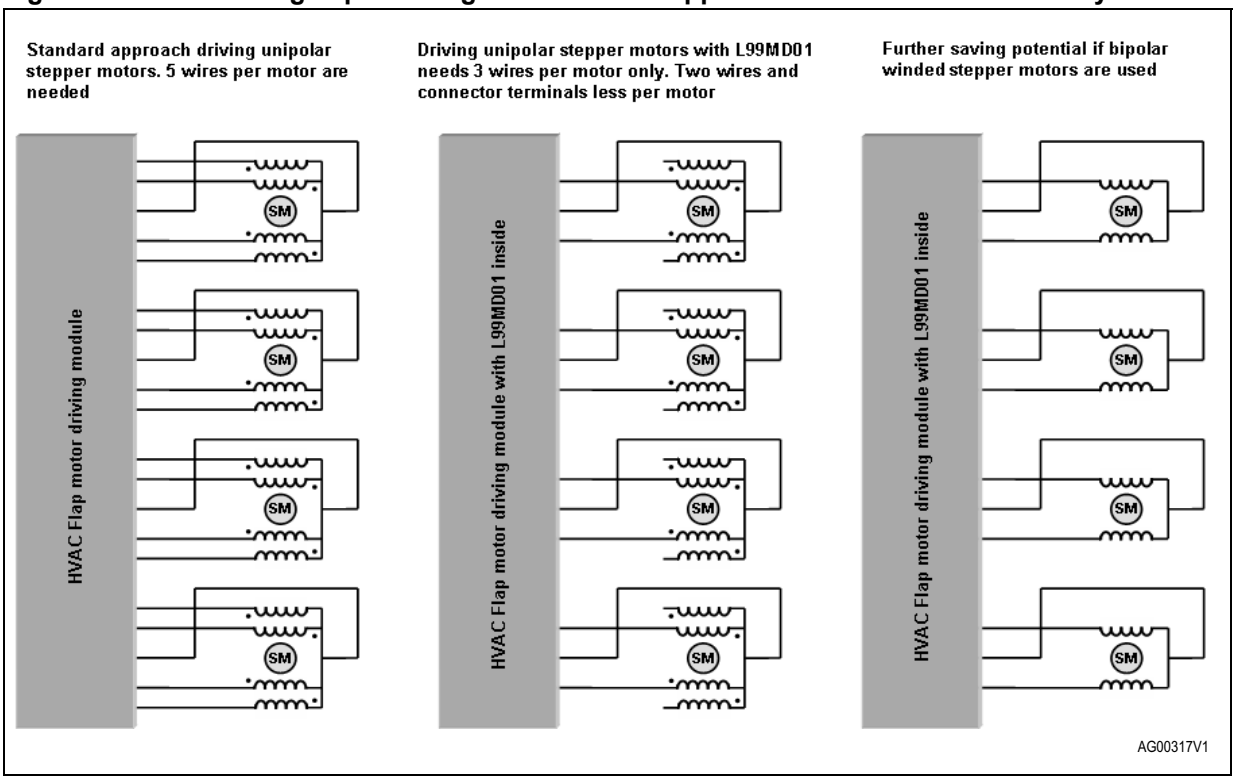


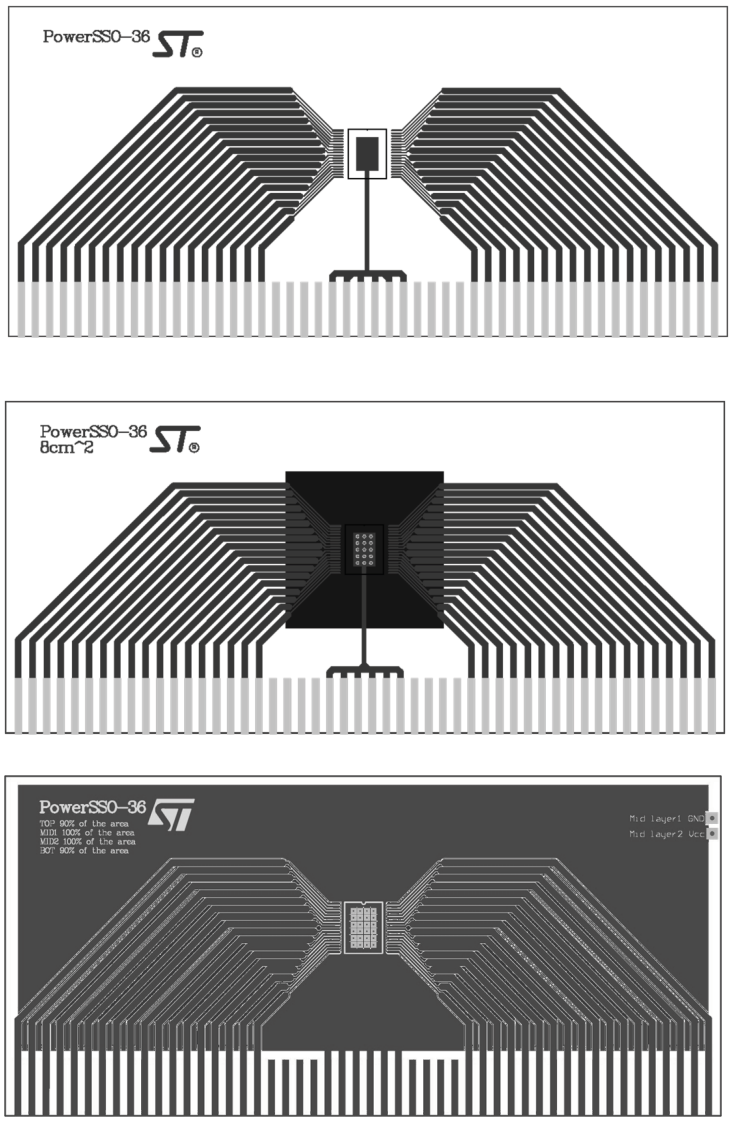
Figure 19. Cost saving impact using L99MD01 as stepper motor driver inside HVAC systems



8 Package and PCB thermal data

8.1 PowerSSO-36 thermal data

Figure 20. PowerSSO-36 PC board



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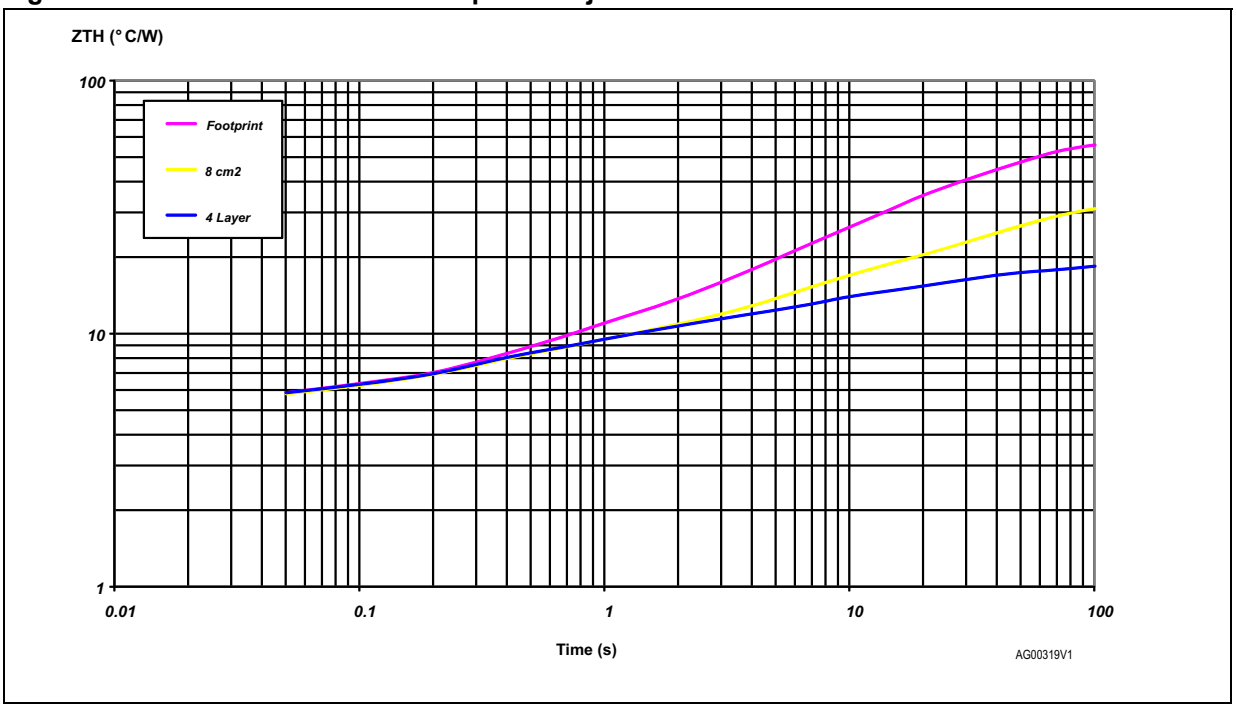
Note:
Board finish thickness 1.6 mm +/- 10%; Board double layer and four layers; Board dimension 129 mm x 60 mm;
Board Material FR4; Cu thickness 0.070 mm (outer layers); Cu thickness 0.035mm (inner layers);
Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/-0.08 mm; Cu thickness on vias 0.025 mm;
Footprint dimension 4.1 mm x 6.5 mm

Figure 21. PowerSSO-36 thermal impedance junction ambient



9 Package information

9.1 ECOPACK® package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

9.2 PowerSSO-36™ mechanical data

Figure 22. PowerSSO-36™ package dimensions

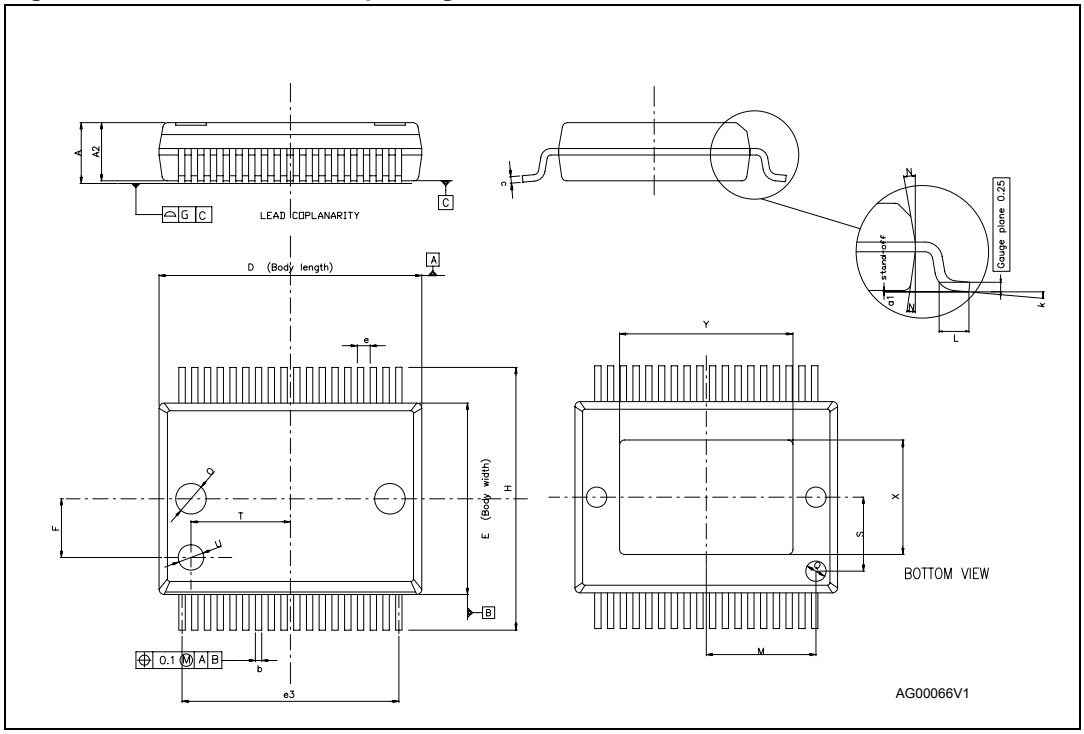


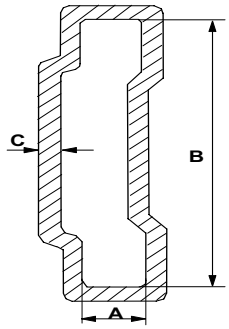
Table 39. PowerSSO-36 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15	-	2.45
A2	2.15	-	2.35
a1	0	-	0.1
b	0.18	-	0.36
c	0.23	-	0.32
D(1)	10.10	-	10.50
E	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
F	-	2.3	-
G	-	-	0.1
G1	-	-	0.06
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
M	-	4.3	-
N	-	-	10°
O	-	1.2	-
Q	-	0.8	-
S	-	2.9	-
T	-	3.65	-
U	-	1	-
X	4.3	-	5.2
Y	6.9	-	7.5

1. “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side (0.006”).

9.3 Packing information

Figure 23. PowerSSO-36 tube shipment (no suffix)



Base Q.ty	49
Bulk Q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

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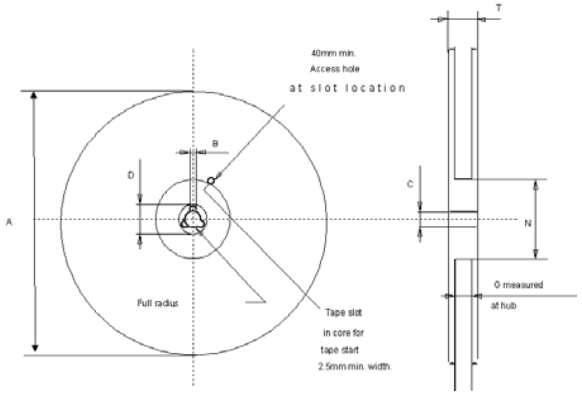
Figure 24. PowerSSO-36 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

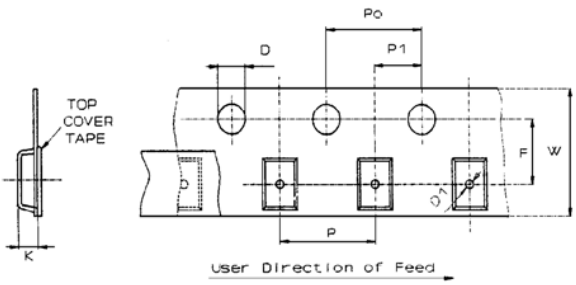
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	100
T (max)	30.4

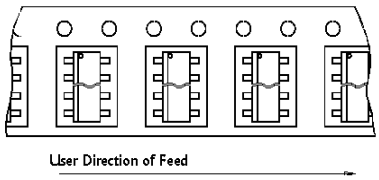
TAPE DIMENSIONS

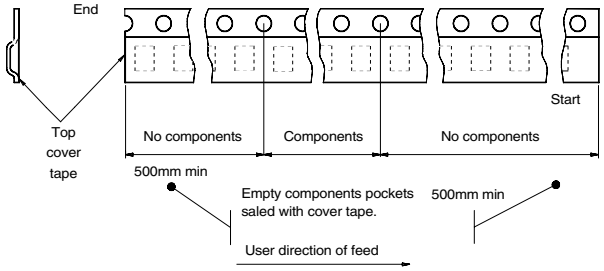
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







GAPGCFT00003

10 Revision history

Table 40. Document revision history

Date	Revision	Changes
22-Mar-2010	1	Initial release.
17-May-2010	2	Updated *Features* list. Removed Block diagram Updated following tables: – *Table 1: Device summary* – *Table 3: Pin description* – *Table 11: Current monitor output* Updated *Section 2.3: Standby mode*, *Section 2.5: SMPS Switched Mode Power Supply* and *Section 2.10: V_S, V_{S2}, V_{SA}, V_{SB} monitoring*. *Section 9.2: PowerSSO-36™ mechanical data*: – Updated *Figure 22: PowerSSO-36™ package dimensions* – Updated *Table 39: PowerSSO-36 mechanical data*
24-Jan-2011	3	Updated *Features* list Updated *Figure 2: Power on reset* *Table 8: Supply*: – I_{VS}: updated maximum value – I_{VSX}: updated test condition *Table 9: Overvoltage and undervoltage detection*: – $V_{SUV\ OFF}$, $V_{SAUV\ OFF}$, $V_{SBUV\ OFF}$: updated maximum value – $V_{SUV\ hyst}$, $V_{SAUV\ hyst}$, $V_{SBUV\ OFF}$, $V_{SBUV\ hyst}$, $V_{SOV\ hyst}$, $V_{S2OV\ hyst}$: updated minimum value *Table 10: Switches*: – $r_{ONLSLC\ 1\text{-}8}$: updated maximum value – I_{QLH}, I_{QLL}: updated minimum, typical and maximum values – $I_{OLDHS1\text{-}8}$, $I_{OLDLSHC1\text{-}8}$, $I_{OLDLSLC1\text{-}8}$: updated test condition, minimum and maximum values *Table 11: Current monitor output*: – $I_{CURRHS1/2\ acc}$: updated test condition and maximum value – $I_{CURRLSHC1/2\ acc}$, $I_{CURRLSLC1/2\ acc}$: updated maximum value Added *Table 12: Current monitor dynamic characteristics* *Table 13: SMPS switched mode power supply gate driver output*: R_{SMPS}: updated minimun and maximum values Updated *Section 2.9: Temperature warning and thermal shutdown* Added *Chapter 8: Package and PCB thermal data*
23-Feb-2011	4	Updated tables *Table 12: Current monitor dynamic characteristics*

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