



**L6388**

## HIGH-VOLTAGE HIGH AND LOW SIDE DRIVER

### 1 FEATURES

- HIGH VOLTAGE RAIL UP TO 600 V
- $dV/dt$  IMMUNITY  $\pm 50$  V/nsec IN FULL TEMPERATURE RANGE
- DRIVER CURRENT CAPABILITY: 400 mA SOURCE, 650 mA SINK
- SWITCHING TIMES 70/40 nsec RISE/FALL WITH 1nF LOAD
- 3.3V, 5V, 15V CMOS/TTL INPUTS COMPARATORS WITH HYSTERESIS AND PULL DOWN
- INTERNAL BOOTSTRAP DIODE
- OUTPUTS IN PHASE WITH INPUTS
- DEAD TIME AND INTERLOCKING FUNCTION

### 2 DESCRIPTION

The L6388 is an high-voltage device, manufactured with the BCD"OFF-LINE" technology.

**Figure 1. Package**



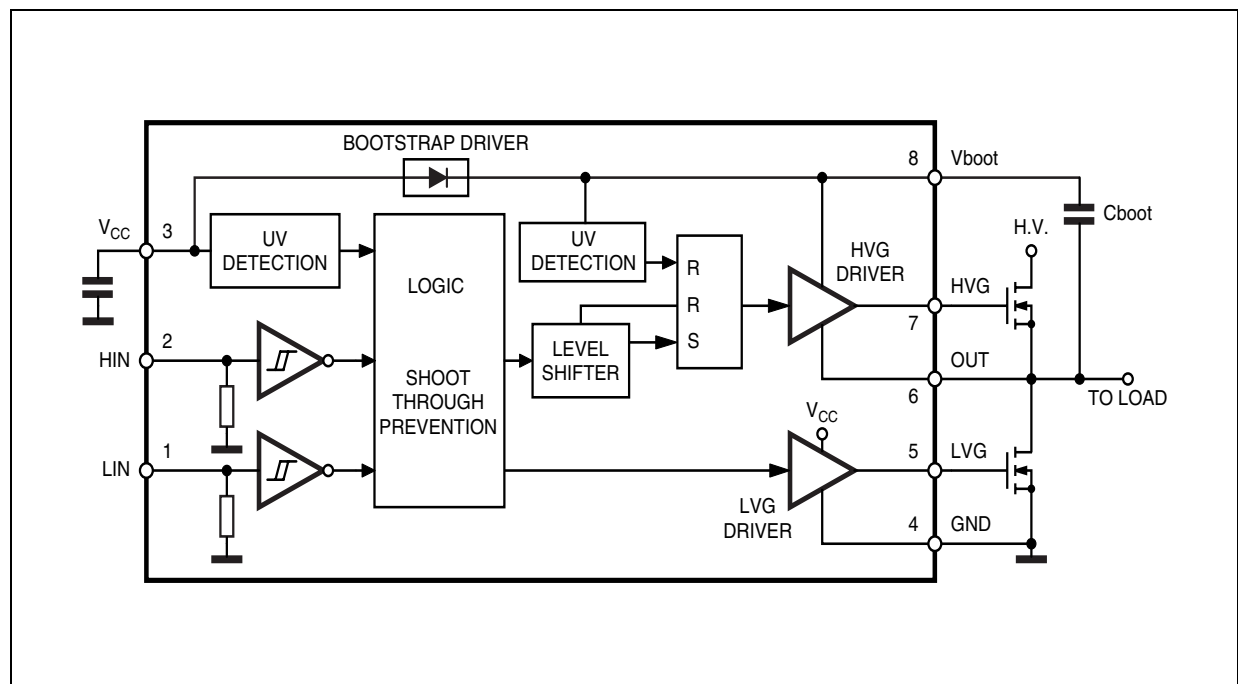
**Table 1. Order Codes**

Part Number	Package
L6388	DIP8
L6388D	SO8
L6388D013TR	SO8 in Tape & Reel

It has a Driver structure that enables to drive independent referenced N Channel Power MOS or IGBT. The Upper (Floating) Section is enabled to work with voltage Rail up to 600V.

The Logic Inputs are CMOS/TTL compatible for ease of interfacing with controlling devices.

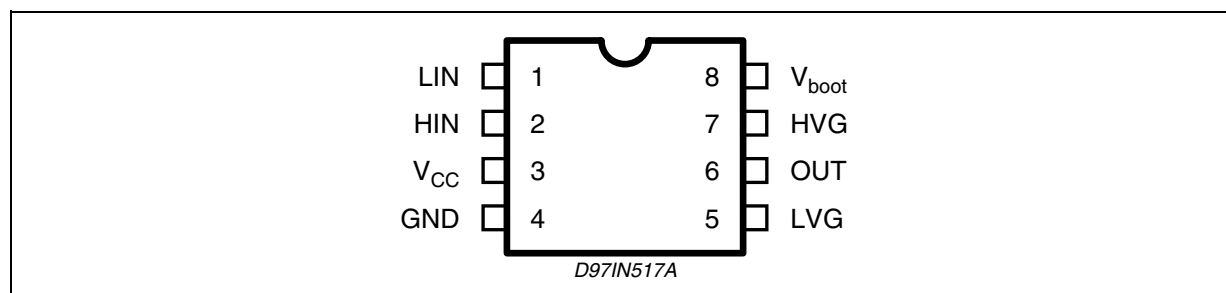
**Figure 2. Block Diagram**



**Table 2. Absolute Maximum Rating**

Symbol	Parameter	Value	Unit
$V_{out}$	Output Voltage	-3 to $V_{boot} - 18$	V
$V_{cc}$	Supply Voltage	- 0.3 to +18	V
$V_{boot}$	Floating Supply Voltage	- 1 to 618	V
$V_{hvg}$	High Side Gate Output Voltage	- 1 to $V_{boot}$	V
$V_{lvg}$	Low Side Gate Output Voltage	-0.3 to $V_{cc} + 0.3$	V
$V_i$	Logic Input Voltage	-0.3 to $V_{cc} + 0.3$	V
$dV_{out}/dt$	Allowed Output Slew Rate	50	V/ns
$P_{tot}$	Total Power Dissipation ( $T_j = 85^\circ\text{C}$ )	750	mW
$T_j$	Junction Temperature	150	$^\circ\text{C}$
$T_{stg}$	Storage Temperature	-50 to 150	$^\circ\text{C}$

Note: ESD immunity for pins 6, 7 and 8 is guaranteed up to 900V (Human Body Model)

**Figure 3. Pin Connection (Top view)****Table 3. Pin Description**

N.	Name	Type	Function
1	LIN	I	Low Side Driver Logic Input
2	HIN	I	High Side Driver Logic Input
3	Vcc	I	Low Voltage Power Supply
4	GND		Ground
5	LVG (*)	O	Low Side Driver Output
6	OUT	O	High Side Driver Floating Reference
7	HVG (*)	O	High Side Driver Output
8	Vboot		Bootstrap Supply Voltage

(\*) The circuit guarantees 0.3V maximum on the pin (@  $I_{sink} = 10\text{mA}$ ). This allows to omit the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

**Table 4. Thermal Data**

Symbol	Parameter	SO8	Minidip	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction to Ambient	150	100	$^\circ\text{C/W}$

**Table 5. Recommended Operating Conditions**

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V <sub>out</sub>	6	Output Voltage		Note 1		580	V
V <sub>BS</sub> (*)	8	Floating Supply Voltage		Note 1		17	V
f <sub>sw</sub>		Switching Frequency	HVG, LVG load CL = 1nF			400	kHz
V <sub>cc</sub>	3	Supply Voltage				17	V
T <sub>j</sub>		Junction Temperature		-45		125	°C

**Note 1:** If the condition V<sub>boot</sub> - V<sub>out</sub> < 18V is guaranteed, V<sub>out</sub> can range from -3 to 580V

(\*): V<sub>BS</sub> = V<sub>boot</sub> - V<sub>out</sub>

**Table 6. Electrical Characteristics**

(V<sub>cc</sub> = 15V; T<sub>j</sub> = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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**AC OPERATION**

t <sub>on</sub>	1 vs 5 2 vs 7	High/Low Side Driver Turn-On Propagation Delay	V <sub>out</sub> = 0V		225	300	ns
t <sub>off</sub>		High/Low Side Driver Turn-Off Propagation Delay	V <sub>out</sub> = 0V		160	220	ns
t <sub>r</sub>	7,5	Rise Time	C <sub>L</sub> = 1000pF		70	100	ns
t <sub>f</sub>	7,5	Fall Time	C <sub>L</sub> = 1000pF		40	80	ns
DT	7,5	Dead Time		220	320	420	ns

**DC OPERATION****Low Supply Voltage Section**

V <sub>ccth1</sub>	3	V <sub>cc</sub> UV Turn On Threshold		9.1	9.6	10.1	V
V <sub>ccth2</sub>		V <sub>cc</sub> UV Turn Off Threshold		7.9	8.3	8.8	V
V <sub>cchys</sub>		V <sub>cc</sub> UV Hysteresis		0.9			V
I <sub>qccu</sub>		Undervoltage Quiescent Supply Current	V <sub>cc</sub> ≤ 9V		250	330	μA
I <sub>qcc</sub>		Quiescent Current	V <sub>cc</sub> = 15V		350	450	μA
R <sub>dson</sub>		Bootstrap Driver on Resistance (**)	V <sub>cc</sub>		125		Ω

**Bootstrapped Supply Voltage Section**

V <sub>BStH1</sub>	8	V <sub>BS</sub> UV Turn On Threshold		8.5	9.5	10.5	V
V <sub>BStH2</sub>		V <sub>BS</sub> UV Turn Off Threshold		7.2	8.2	9.2	V
V <sub>BShys</sub>		V <sub>BS</sub> UV Hysteresis		0.9			V
I <sub>QBS</sub>		V <sub>BS</sub> Quiescent Current	HVG ON			250	μA
ILK		High Voltage Leakage Current	V <sub>hvg</sub> = V <sub>out</sub> = V <sub>boot</sub> = 600V			10	μA

**High/Low Side Driver**

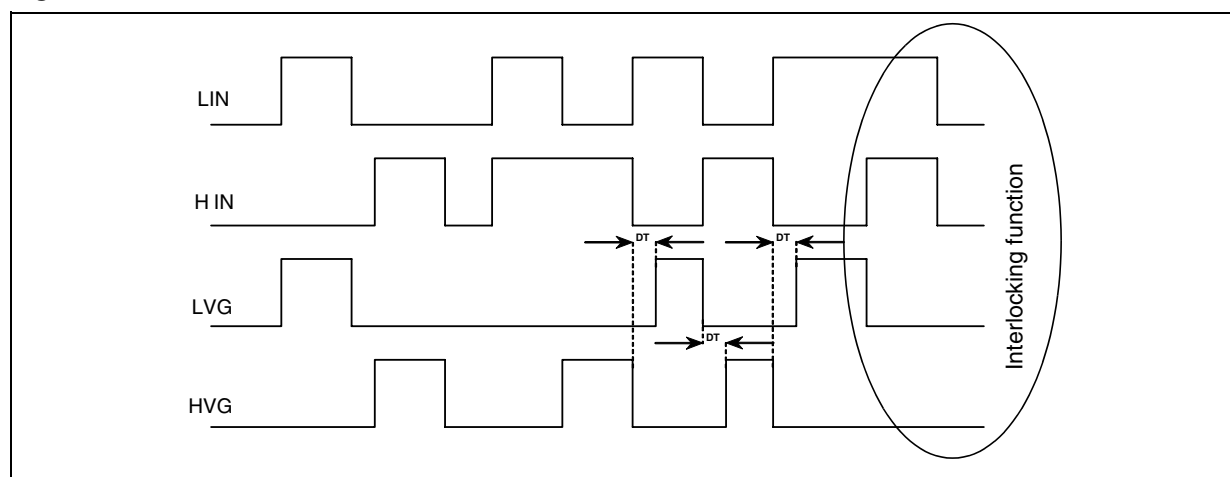
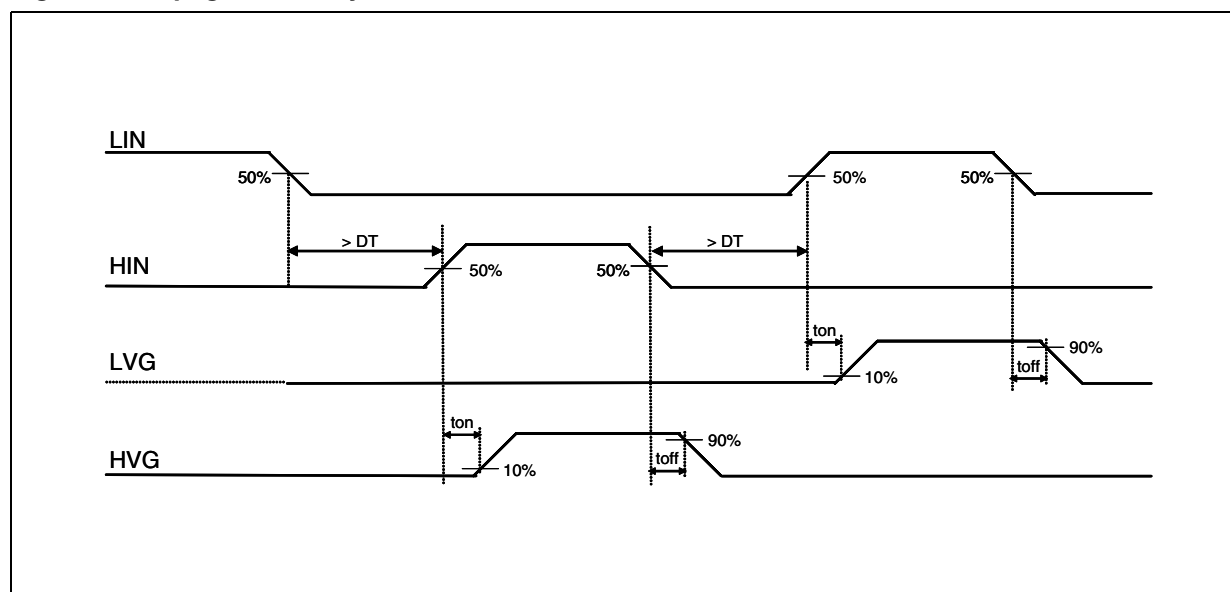
I <sub>so</sub>	5,7	Source Short Circuit Current	V <sub>IN</sub> = V <sub>ih</sub> (tp < 10μs)	300	400		mA
I <sub>si</sub>		Sink Short Circuit Current	V <sub>IN</sub> = V <sub>il</sub> (tp < 10μs)	500	650		mA

**Table 6. Electrical Characteristics** (continued)(V<sub>CC</sub> = 15V; T<sub>j</sub> = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>Logic Inputs</b>							
V <sub>il</sub>	1, 2	Low Level Logic Input Voltage				1.1	V
V <sub>ih</sub>		High Level Logic Input Voltage		1.8			V
I <sub>ih</sub>		High Level Logic Input Current	V <sub>IN</sub> = 15V		20	70	μA
I <sub>il</sub>		Low Level Logic Input Current	V <sub>IN</sub> = 0V	-1			μA

(\*\*) R<sub>DS(on)</sub> is tested in the following way:  $R_{DS(on)} = \frac{(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})}{I_1(V_{CC}, V_{CBOOT1}) - I_2(V_{CC}, V_{CBOOT2})}$

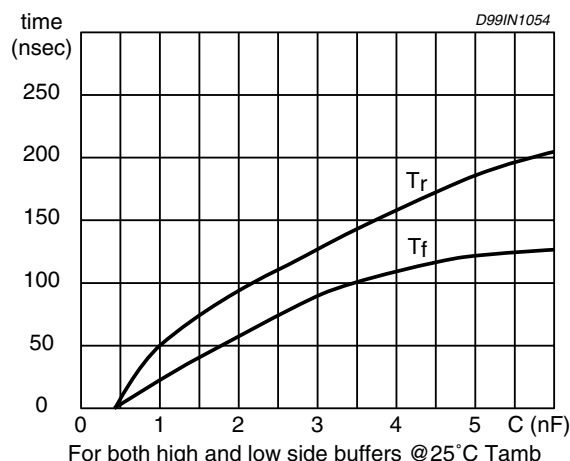
where I<sub>1</sub> is pin 8 current when V<sub>CBOOT</sub> = V<sub>CBOOT1</sub>, I<sub>2</sub> when V<sub>CBOOT</sub> = V<sub>CBOOT2</sub>.

**Figure 4. Dead Time Waveforms Definitions****Figure 5. Propagation Delay Waveform Definitions**

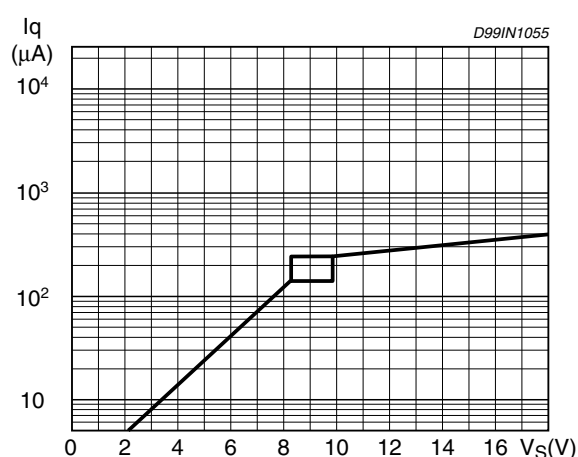
### 3 INPUT LOGIC

Input logic is provided with an interlocking circuitry which avoids the two outputs (LVG, HVG) to be active at the same time when both the logic input pins (LIN, HIN) are at a high logic level. In addition, to prevent cross conduction of the external MOSFETs, after each output is turned-off the other output cannot be turned-on before a certain amount of time (DT) (see Figure 4).

**Figure 6. Typical Rise and Fall Times vs. Load Capacitance**



**Figure 7. Quiescent Current vs. Supply Voltage**



#### 3.1 BOOTSTRAP DRIVER

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (fig. 8a). In the L6388 a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in fig. 8b

An internal charge pump (fig. 8b) provides the DMOS driving voltage .

The diode connected in series to the DMOS has been added to avoid undesirable turn on of it.

#### 3.2 CBOOT selection and charging

To choose the proper CBOOT value the external MOS can be seen as an equivalent capacitor. This capacitor CEXT is related to the MOS total gate charge :

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors CEXT and CBOOT is proportional to the cyclical voltage loss .

It has to be:

$$C_{BOOT} \gg C_{EXT}$$

e.g.: if  $Q_{gate}$  is 30nC and  $V_{gate}$  is 10V,  $C_{EXT}$  is 3nF. With  $C_{BOOT} = 100nF$  the drop would be 300mV.

If HVG has to be supplied for a long time, the CBOOT selection has to take into account also the leakage losses.

e.g.: HVG steady state consumption is lower than 200μA, so if HVG  $T_{ON}$  is 5ms, CBOOT has to supply 1μC to CEXT. This charge on a 1μF capacitor means a voltage drop of 1V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has great leakage current). This structure can work only if  $V_{OUT}$  is close to GND (or lower) and in the meanwhile the LVG is on. The charging time ( $T_{charge}$ ) of the CBOOT is the time in which both conditions are fulfilled and it

has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS RDSON (typical value: 125 Ohm). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

$$V_{\text{drop}} = I_{\text{charge}} R_{\text{dson}} \rightarrow V_{\text{drop}} = \frac{Q_{\text{gate}}}{T_{\text{charge}}} R_{\text{dson}}$$

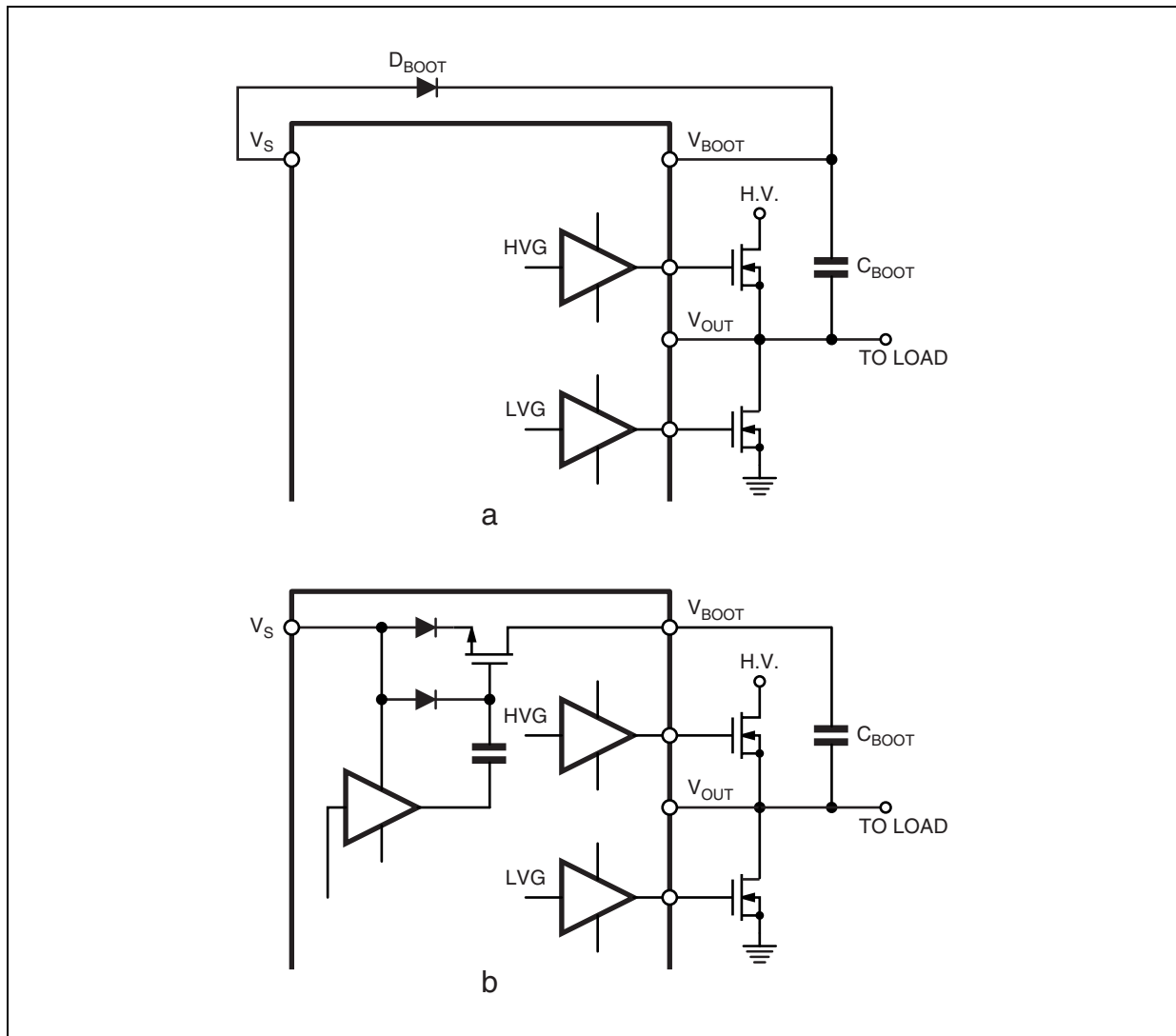
where  $Q_{\text{gate}}$  is the gate charge of the external power MOS,  $R_{\text{dson}}$  is the on resistance of the bootstrap DMOS, and  $T_{\text{charge}}$  is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30nC the drop on the bootstrap DMOS is about 1V, if the  $T_{\text{charge}}$  is 5μs. In fact:

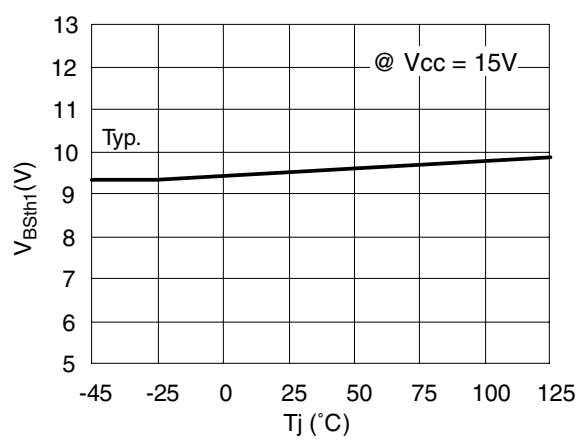
$$V_{\text{drop}} = \frac{30\text{nC}}{5\mu\text{s}} \cdot 125\Omega \sim 0.8\text{V}$$

$V_{\text{drop}}$  has to be taken into account when the voltage drop on  $C_{\text{BOOT}}$  is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

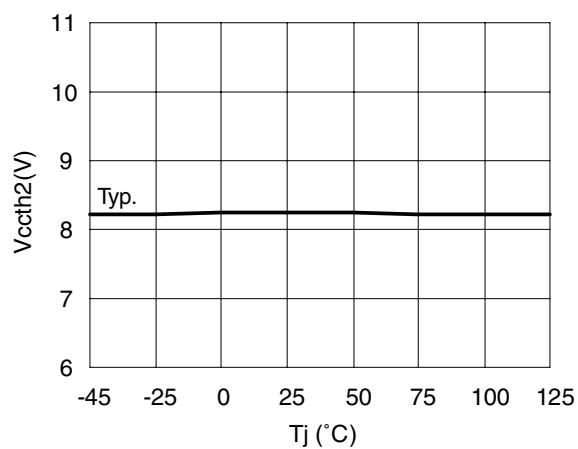
**Figure 8. Bootstrap Driver.**



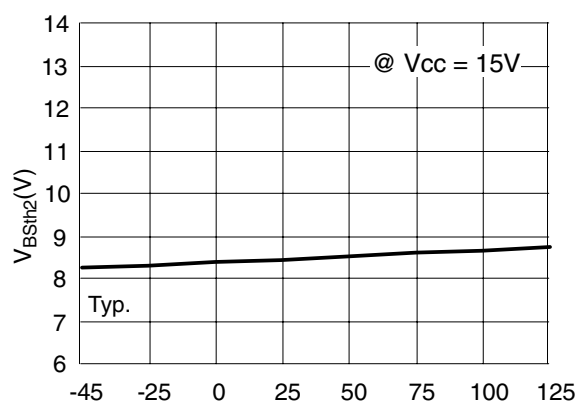
**Figure 9.  $V_{BOOT}$  UV Turn On Threshold vs. Temperature**



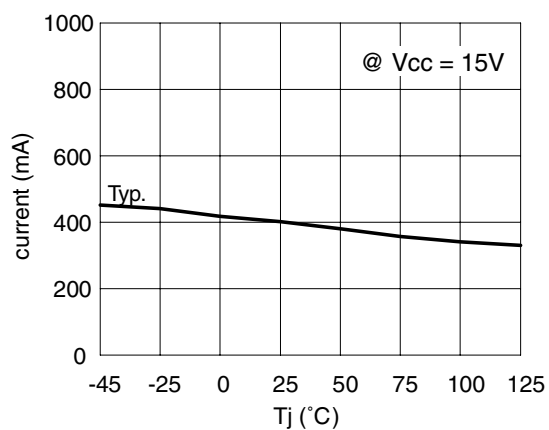
**Figure 12.  $V_{CC}$  UV Turn Off Threshold vs. Temperature**



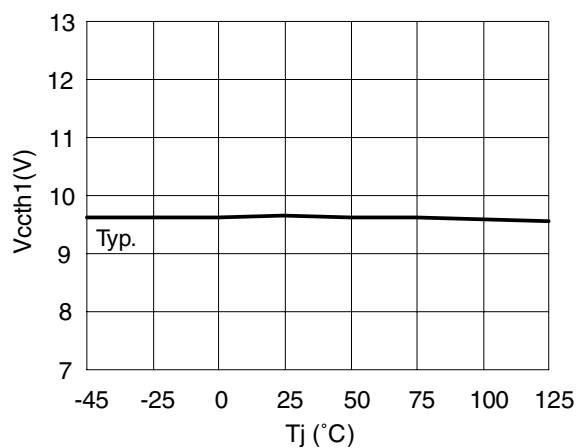
**Figure 10.  $V_{BOOT}$  UV Turn Off Threshold vs. Temperature**



**Figure 13. Output Source Current vs. Temperature**



**Figure 11.  $V_{CC}$  UV Turn On Threshold vs. Temperature**



**Figure 14. Output Sink Current vs. Temperature**

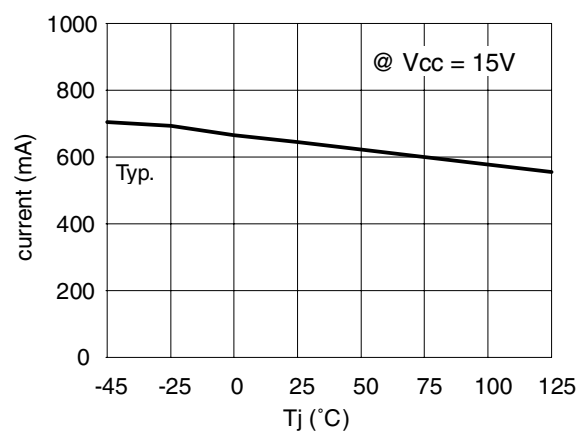


Figure 15. DIP8 Mechanical Data & Package Dimensions

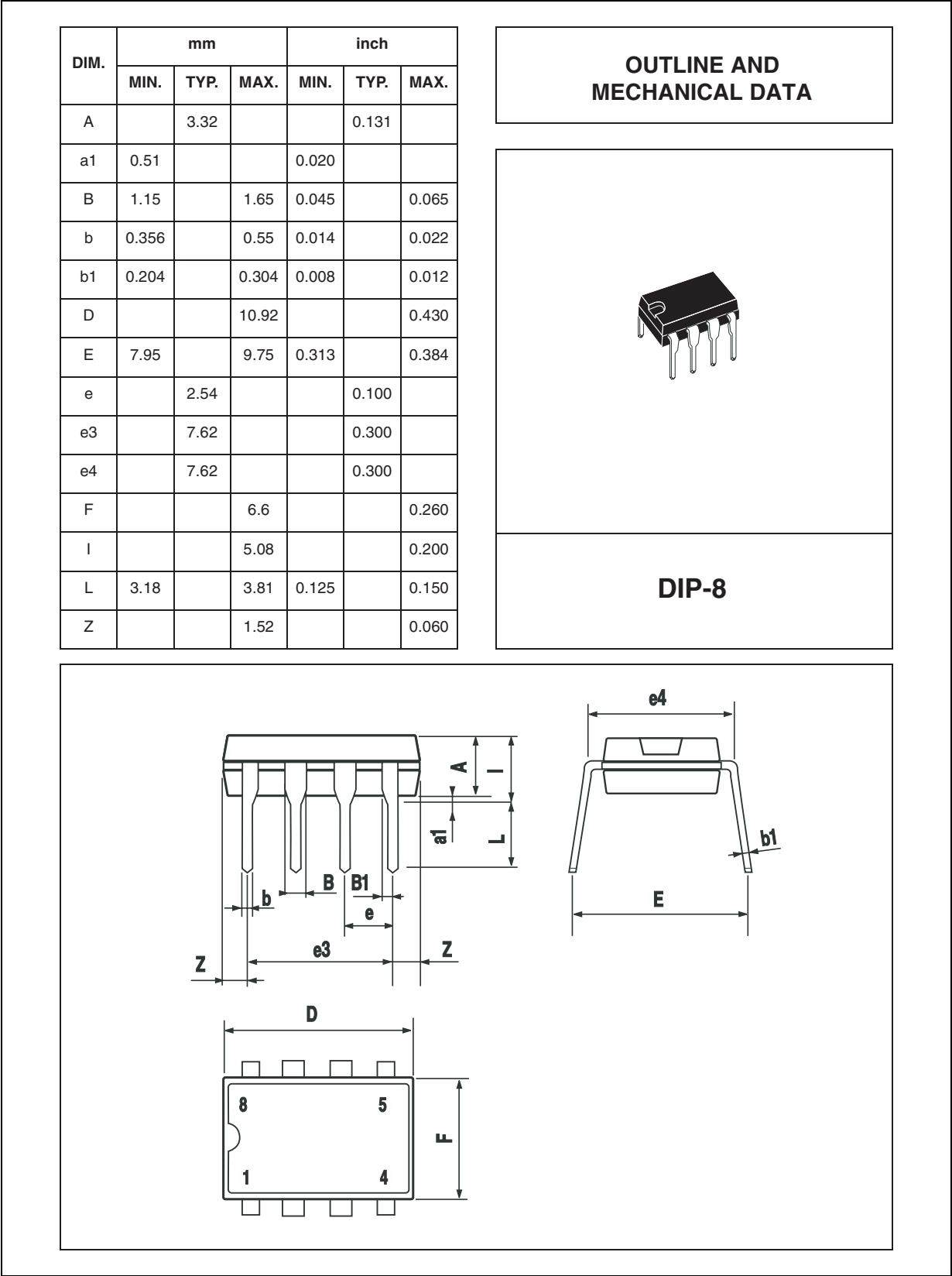


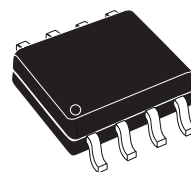


Figure 16. SO8 Mechanical Data &amp; Package Dimensions

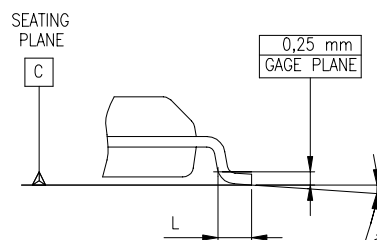
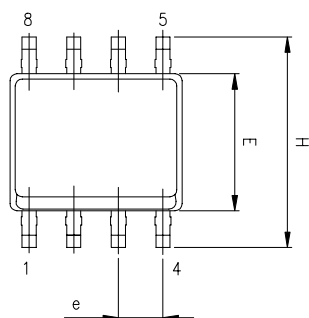
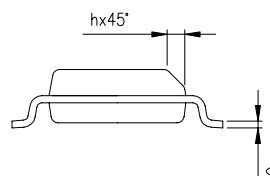
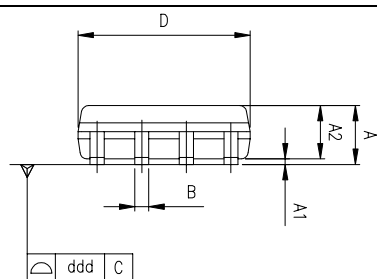
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

Note: (1) Dimensions D does not include mold flash, protrusions or gate burrs.  
Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

### OUTLINE AND MECHANICAL DATA



**SO-8**



0016023 C

**Table 7. Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
January 2005	1	First Issue
May 2005	2	Changed from Preliminary Data to Final

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