



L6327
L6332

6 / 4 CHANNEL VOLTAGE SENSE GMR PREAMPLIFIER

PRODUCT PREVIEW

- Power Supplies +5Vdc, -5Vdc
- Current bias or voltage bias (selectable) / Differential Voltage Sense architecture
- 6 or 4 channel versions
- 38-pin TSSOP package (for either 6 or 4 channels)
- Internal reference Resistor for read and write currents
- Read channel -3dB bandwidth > 400MHz (Rmr=50 ohm no interconnect)
- Input equivalent preamplifier voltage noise 0.5nV/rHz nominal
- Input equivalent MR bias current noise 10 pA/rHz nominal
- MR bias current programmable (5 bit DAC) 1.5-7.0mA nominal MR bias voltage programmable (5 bit DAC) 65-335mV nominal
- Programmable gain (100V/V, 150, 200 and 250V/V) and read bandwidth
- Write frequency up to 300 MHz (Lh=70nH, Rh=20 ohms, Ch=2pF, VEE=-5V)
- Rise/Fall time 0.6ns (Iw =40mA 0-pk, Lh=70nH, Rh=20 ohms, Ch=2pF, VEE=-5V)
- Write current programmable (5 bit DAC) 15-60mA
- PECL write data input
- Bi-directional 16-bit TTL Serial interface for head selection, read/write currents selection, chip parameters modification, chip enable, vendor code and fault status read back registers
- 2-pin mode selection (R/W, MRR)
- Bank write feature for servo write
- Digital buffered head voltage DBHV / Analog buffered head voltage ABHV pin (gain 5)
- Thermal asperity detection & correction with adjustable sensitivity level (6 bit DAC)
- Automatic successive approximation digital measurement of temperature and Rmr (7 bits)
- Read and write head open/short detection, low low supply detect and temperature monitoring (high temperature warning and Analog Temperature Diode Voltage measurement)
- Low write frequency detection.
- WRITE to READ fast recovery 150ns (same



head, including 100ns blanking period)

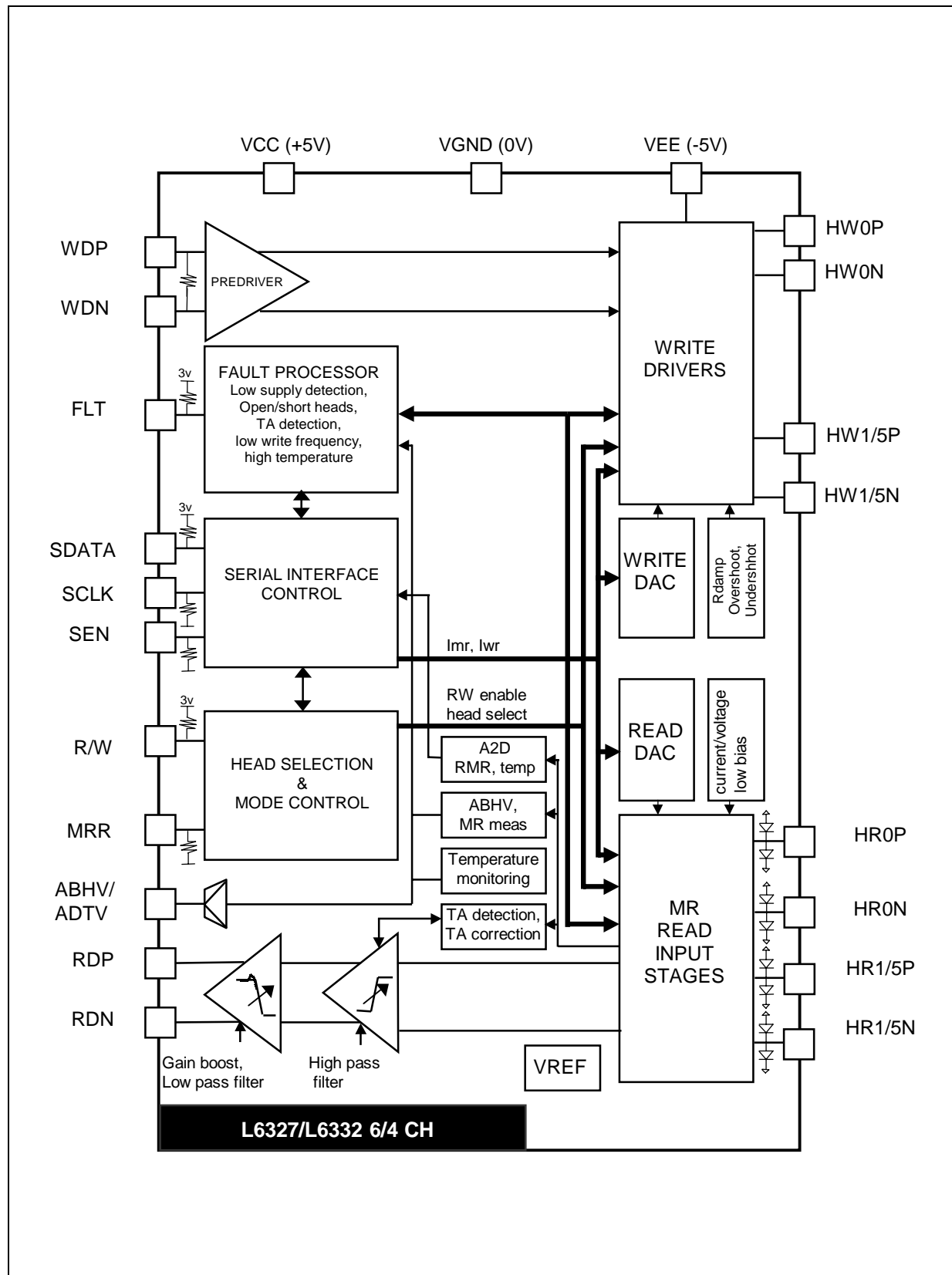
- Head-to-head switch in READ mode - 10μs (nom)
- Head and MR bias current switching transient current head protection
- READ-to-WRITE switching 50ns (same head)
- Programmable read bias during write and bank write operation
- ESD diode for GMR head protection

DESCRIPTION

L6327/L6332 is a BICMOS monolithic integrated circuit GMR differential preamplifier designed for use with four-terminal magneto-resistive GMR read/inductive write heads. It is available as either a six (L6327) or four (L6332) channel device. The devices consist of a voltage-sense, current-bias or voltage-bias (selectable), differential input and differential output, low-noise, high bandwidth read amplifier and include fast current switching write drivers which support data rates in excess of 550 Mb/s with 70nH write heads.

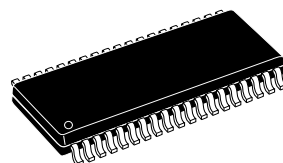
The GMR preamplifier provides programmable read current / voltage bias and write current (5 bit DAC for the read bias, 5 bit DAC for the write current), fault detection circuitry and servo writing features. Read amplifier gain, write current wave shape (overshoot, undershoot and damping) can be adjusted and a thermal asperity detection and correction circuit can be enabled and programmed with different thresholds (6 bit DAC) through a 16-bit bi-directional serial interface (SDEN, SDATA, SCLK). The device operates from a +5V supply and a -5V supply (nominal). No external components are required as a trimmed or untrimmed resistor for reference current setting is employed.

BLOCK DIAGRAM

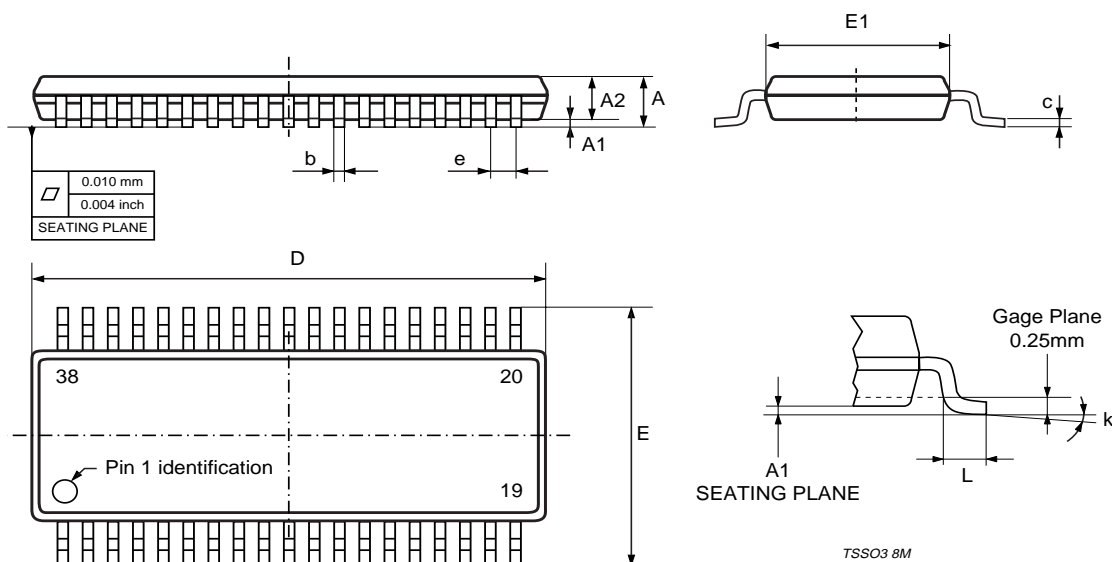


| DIM. | mm | | | inch | | |
|------|---------------------|------|------|--------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.10 | | | 0.043 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 0.85 | 0.90 | 0.95 | 0.033 | 0.035 | 0.037 |
| b | 0.17 | | 0.27 | 0.007 | | 0.011 |
| c | 0.09 | | 0.20 | 0.0035 | | 0.008 |
| D | 9.60 | 9.70 | 9.80 | 0.378 | 0.382 | 0.386 |
| E | | 6.40 | | | 0.252 | |
| e | | 0.50 | | | 0.020 | |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 |
| L | 0.50 | 0.60 | 0.70 | 0.020 | 0.024 | 0.028 |
| k | 0° (min.) 8° (max.) | | | | | |

OUTLINE AND MECHANICAL DATA



TSSOP38 Thin Shrink Small Outline Package



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