L5300RPT

5 V low dropout voltage regulator

Datasheet – production data

Features

Max DC supply voltage	V_S	40V
Max output voltage tolerance	ΔV_0	+/-2%
Max dropout voltage	V_{dp}	500mV
Output current	I_o	300mA
Quiescent current	I_{qn}	55 µA(1)

1. Typical value

- Operating DC supply voltage range 5.6 V to 40 V
- Low dropout voltage
- 300 mA current capability
- Low quiescent current
- Very low consumption mode
- Precision output voltage 5 V +/- 2 %
- Reset circuit sensing the output voltage
- Programmable reset pulse delay with external capacitor
- Thermal shutdown and short-circuit protection
- Wide temperature range (T_j = -40 °C to 150 °C)

PPAK

Description

L5300RPT is a low dropout linear regulator with low voltage reset. Only a low-value ceramic capacitor is required for stability (above or equal 220 nF).

Typical quiescent current is 55 µA in light load condition.

On chip trimming results in high output voltage accuracy (2 %). Accuracy is kept over a wide temperature range, line and load variation.

The maximum input voltage is 40 V. The max output current is internally limited. An internal temperature protection disables the voltage regulator output.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PPAK	L5300RPT	L5300RPTTR

Contents

1 Block diagram and pins description 5

2 Electrical specifications 7

2.1 Absolute maximum ratings 7

2.2 Thermal data 7

2.3 Electrical characteristics 8

2.4 Electrical characteristics curves 10

3 Application information 13

3.1 Voltage regulator 13

3.2 Reset 15

4 Package and PCB thermal data 16

5 Package and packing information 19

5.1 ECOPACK® 19

5.2 PPAK mechanical data 20

5.3 PPAK packing information 22

6 Revision history 23

List of tables

Table 1. Device summary . . . 1
Table 2. Pins description . . . 6
Table 3. Absolute maximum ratings . . . 7
Table 4. Thermal data . . . 7
Table 5. General . . . 8
Table 6. Reset . . . 9
Table 7. PPAK thermal parameter . . . 18
Table 8. PPAK mechanical data . . . 21
Table 9. Document revision history . . . 23

List of figures

Figure 1. Block diagram . . . 5
Figure 2. Configuration diagram (top view) . . . 6
Figure 3. Output voltage vs T_j . . . 10
Figure 4. Output voltage vs V_S . . . 10
Figure 5. Drop voltage vs output current . . . 10
Figure 6. Current consumption vs output current . . . 10
Figure 7. Current consumption vs output current (at light load condition) . . . 10
Figure 8. Current consumption vs input voltage (I_o = 0.1 mA) . . . 10
Figure 9. Current consumption vs input voltage (I_o = 100 mA) . . . 11
Figure 10. Current limitation vs T_j . . . 11
Figure 11. Current limitation vs input voltage . . . 11
Figure 12. Short-circuit current vs T_j . . . 11
Figure 13. Short-circuit current vs input voltage . . . 11
Figure 14. V_{Rhth} vs T_j . . . 11
Figure 15. V_{Rlth} vs T_j . . . 12
Figure 16. I_{cr} vs T_j . . . 12
Figure 17. I_{dr} vs T_j . . . 12
Figure 18. Application schematic . . . 13
Figure 19. Stability region . . . 14
Figure 20. Maximum load variation response . . . 14
Figure 21. Reset time diagram . . . 15
Figure 22. PPAK PC board . . . 16
Figure 23. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition . . . 16
Figure 24. PPAK thermal impedance junction ambient single pulse . . . 17
Figure 25. Thermal fitting model of a Vreg in PPAK . . . 17
Figure 26. PPAK dimension . . . 20
Figure 27. PPAK suggested pad layout and tube shipment (no suffix) . . . 22
Figure 28. PPAK tape and reel shipment (suffix “TR”) . . . 22

1 Block diagram and pins description

Figure 1. Block diagram

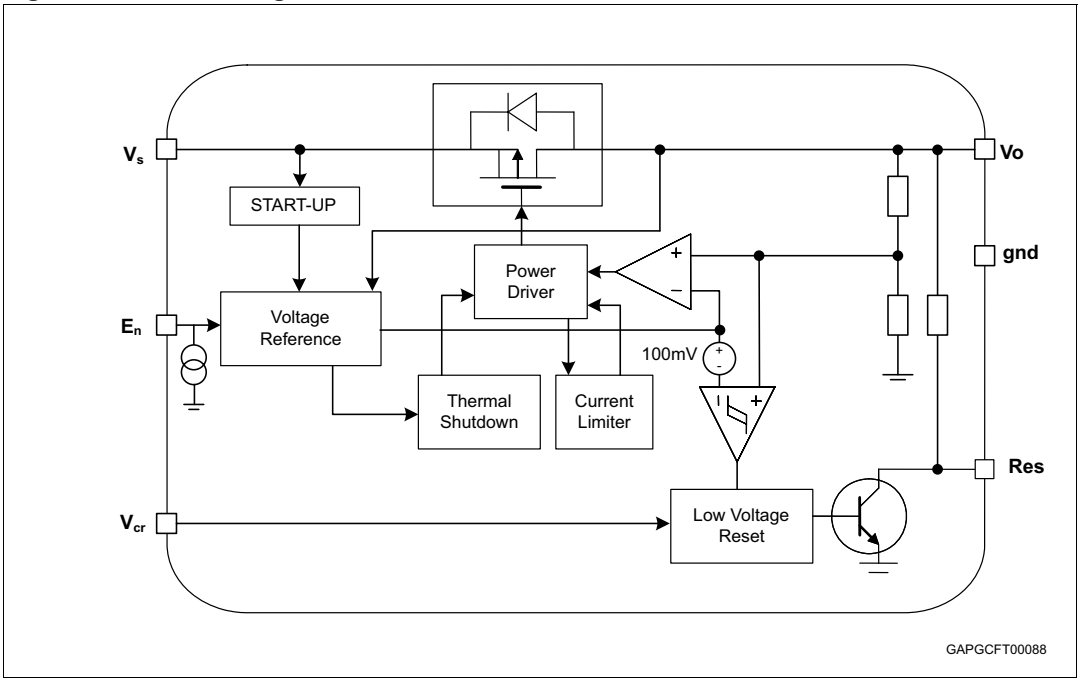


Figure 2. Configuration diagram (top view)

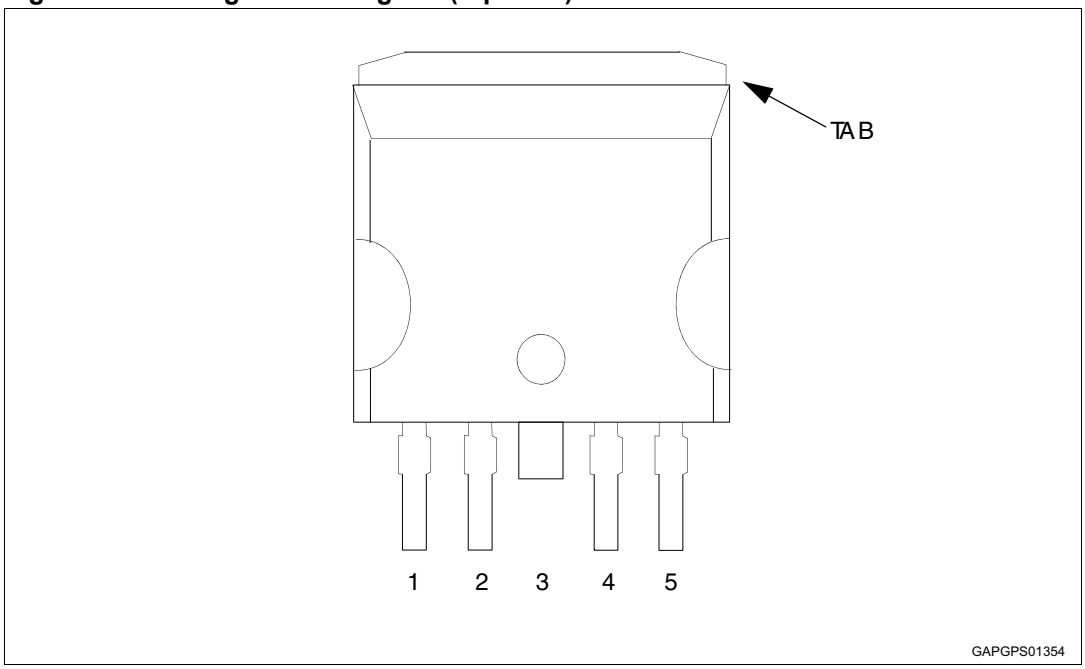


Table 2. Pins description

N°	Name	Function
1	V_S	Supply voltage, block directly to GND on the IC with a capacitor.
2	R_{es}	Reset output. Internally connected to V_o through a 20 KΩ pull up resistor. This pin is pulled low when $V_o < V_{o\_th}$. Keep open if not needed.
3	GND	Ground is internally electrically connected to TAB.
4	V_{cr}	Reset delay. Connect an external capacitor between V_{cr} pin and ground to adjust the reset delay time. Keep open if not needed.
5	V_o	5 V regulated output. Block to GND with a ceramic capacitor (≥ 220 nF for regulator stability).

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the *Table 3: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{sdc}	DC supply voltage	-0.3 to 40	V
I_{sdc}	Input current	Internally limited	
V_{odc}	DC output voltage	-0.3 to 6	V
I_{odc}	DC output current	Internally limited	
$V_{od\ Res}$	Open drain output voltage R_{es}	-0.3 to V_{Vodc} + 0.3	V
$I_{od\ Res}$	Open drain output current R_{es}	Internally limited	
V_{cr}	V_{cr} voltage	-0.3 to V_{Vo} + 0.3	V
T_j	Junction temperature	-40 to 150	°C
$V_{ESD\ HBM}$	ESD HBM voltage level (HBM-MIL STD 883C)	+/- 2	kV
$V_{ESD\ CDM}$	ESD CDM voltage level (CDM- AEC-Q100-011)	+/- 750	V

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction to case	5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction to ambient	45.5	°C/W

2.3 Electrical characteristics

Values specified in this section are for V_S = 5.6 V to 31 V, T_j = -40 °C to +150 °C unless otherwise stated.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_o	V_{o_ref}	Output voltage	V_S = 8 V to 18 V I_o = 8 mA to 300 mA	4.9	5.0	5.1	V
V_o	V_{o_ref}	Output voltage	V_S = 5.6 V to 31 V I_o = 8 mA to 300 mA	4.85	5.0	5.15	V
V_o	V_{o_ref}	Output voltage	V_S = 5.6 V to 31 V I_o = 0.1 mA to 8 mA	4.75	5.0	5.25	V
V_o	I_{short}	Short-circuit current	V_S = 13.5 V	0.8	1.8	2.6	A
V_o	I_{lim}	Output current capability(1)	V_S = 13.5 V	0.6	1.6	2.5	A
V_S, V_o	V_{line}	Line regulation voltage	V_S = 6 V to 28 V I_o = 50 mA			40	mV
V_o	V_{load}	Load regulation voltage	V_S = 13.5 V I_o = 8 mA to 300 mA T_j = 25 °C			40	mV
			V_S = 8 V to 18 V I_o = 8 mA to 300 mA			55	
V_S, V_o	V_{dp}	Drop voltage(2)	I_o = 300 mA			500	mV
V_S, V_o	SVR	Ripple rejection	f_r = 100 Hz (3)		60		dB
V_o	I_{oth_H}	Normal consumption mode output current	V_S = 8 V to 18 V	8			mA
V_o	I_{oth_L}	Very low consumption mode output current	V_S = 8 V to 18 V			1.1	mA
V_o	I_{oth_Hyst}	Output current switching threshold hysteresis	V_S = 13.5 V T_j = 25 °C		0.8		mA
V_S, V_o	I_{qn_1}	Current consumption with regulator enabled $Iqn\_1 = I_{Vs} - I_o$	V_S = 13.5 V, I_o = 0.1 mA to 1 mA,		55	80	µA
V_S, V_o	I_{qn_300}	Current consumption with regulator enabled $Iqn\_300 = I_{Vs} - I_o$	V_S = 13.5 V, I_o = 300 mA,		3	4.2	mA
	T_w	Thermal protection temperature		150		190	°C
	T_{w_hy}	Thermal protection temperature hysteresis			10		°C

1. Measured output current when the output voltage has dropped 100 mV from its nominal value obtained at 13.5 V and I_o = 75 mA.
2. V_S - V_o measured dropout when the output voltage has dropped 100 mV from its nominal value obtained at 13.5V and I_o = 75 mA.
3. Guaranteed by design.

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
R_{es}	V_{Res_l}	Reset output low voltage	R_{ext} = 5 kΩ V_o > 1 V			0.4	V
R_{es}	I_{Res_lkg}	Reset output high leakage current	$V_{Res} = V_o$			1	µA
R_{es}	R_{Res}	Pull up internal resistance	Versus V_o	10	20	40	kΩ
R_{es}	V_{o_th}	V_o out of regulation threshold	V_o decreasing	6	8	10	% below V_{o_ref}
V_{cr}	V_{RIth}	Reset timing low threshold	V_S = 13.5 V	16	19	22	% V_{o_ref}
V_{cr}	V_{Rhth}	Reset timing high threshold	V_S =13.5 V	47	50	53	% V_{o_ref}
V_{cr}	I_{cr}	Charge current	V_S = 13.5 V	10	20	30	µA
V_{cr}	I_{dr}	Discharge current	V_S = 13.5 V	10	20	30	µA
R_{es}	t_{rr}	Reset reaction time	$V_o = V_{o\_th}$ - 100 mV			2	µs
R_{es}	t_{rd}	Reset delay time	V_S = 13.5 V, C_{tr} = 1 nF	2	4	6	ms

2.4 Electrical characteristics curves

Figure 3. Output voltage vs T_j

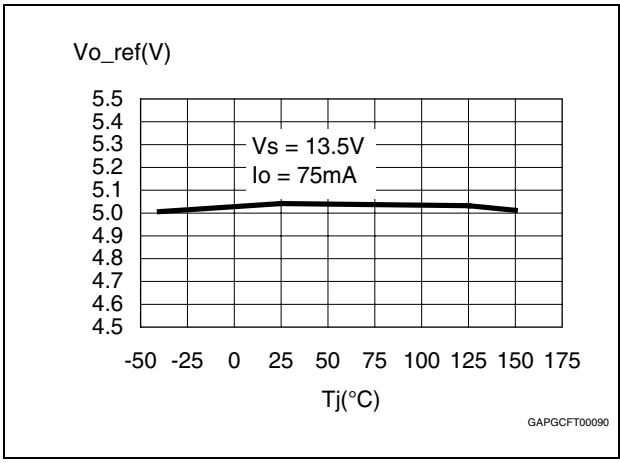


Figure 4. Output voltage vs V_S

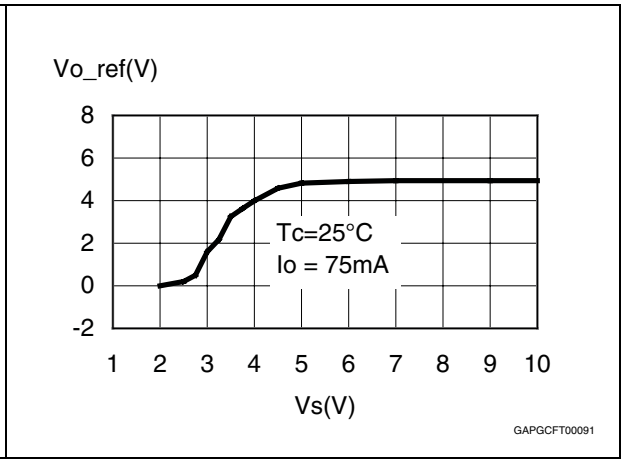


Figure 5. Drop voltage vs output current

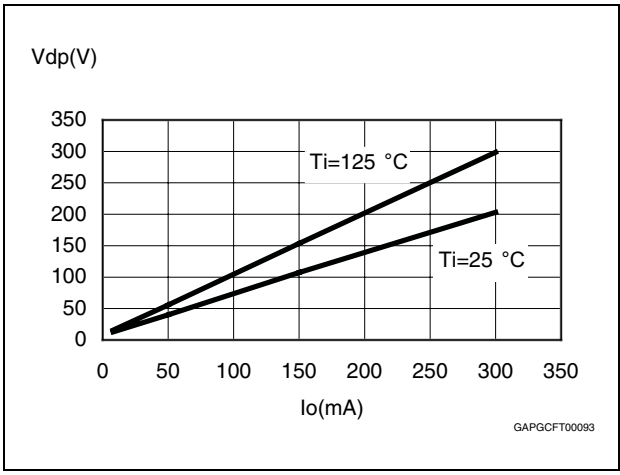


Figure 6. Current consumption vs output current

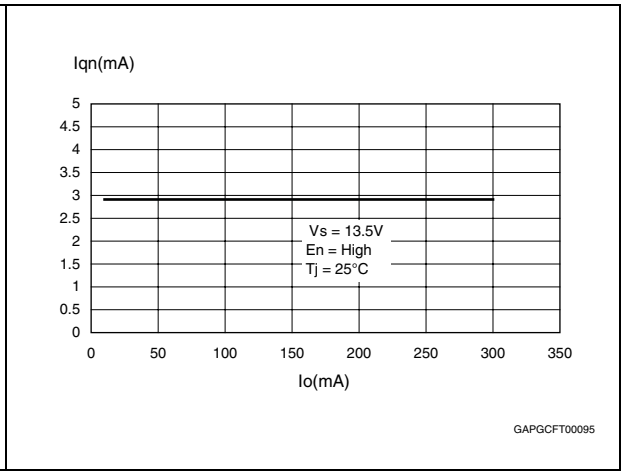


Figure 7. Current consumption vs output current (at light load condition)

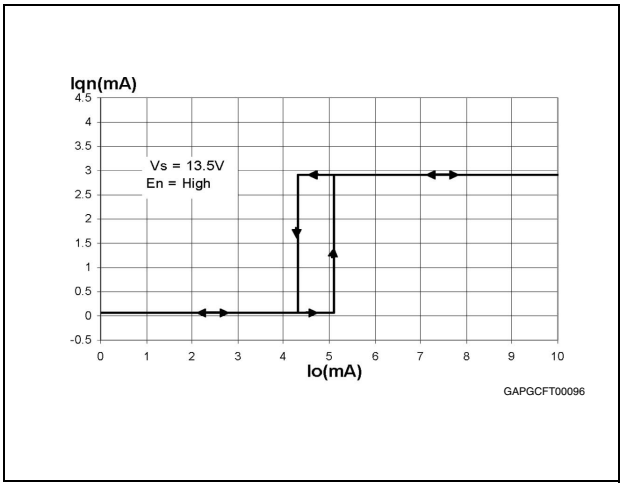


Figure 8. Current consumption vs input voltage (I_o = 0.1 mA)

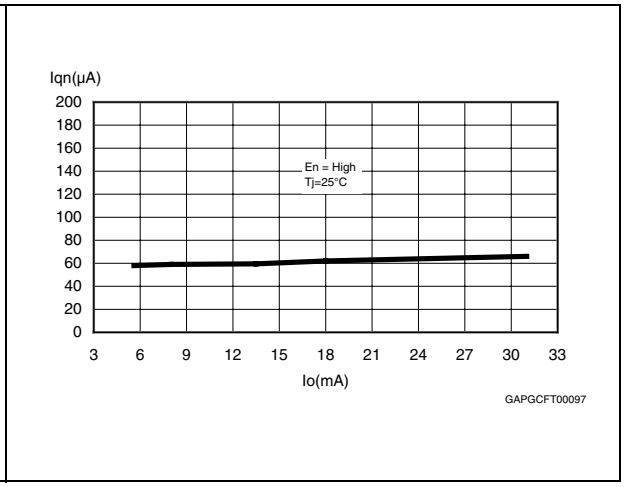


Figure 9. Current consumption vs input voltage (I_o = 100 mA)

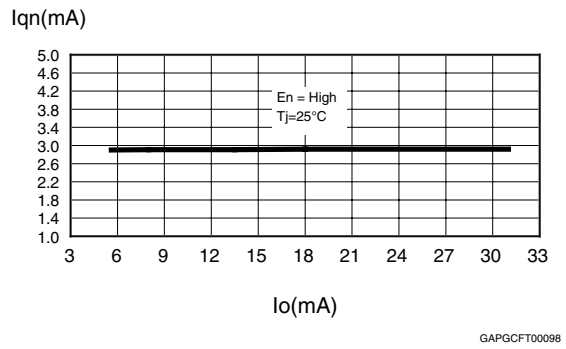


Figure 10. Current limitation vs T_j

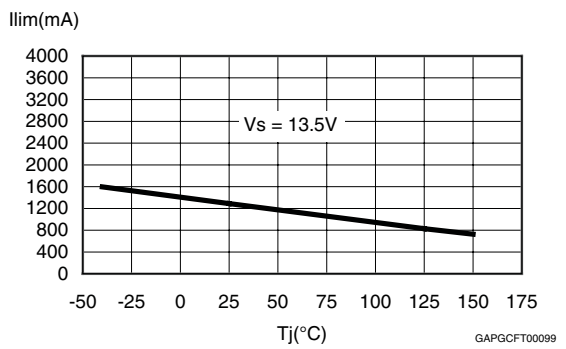


Figure 11. Current limitation vs input voltage

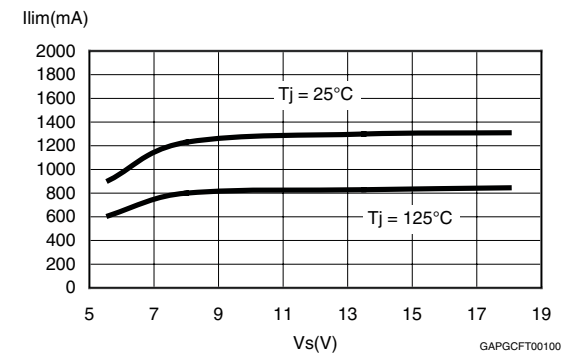


Figure 12. Short-circuit current vs T_j

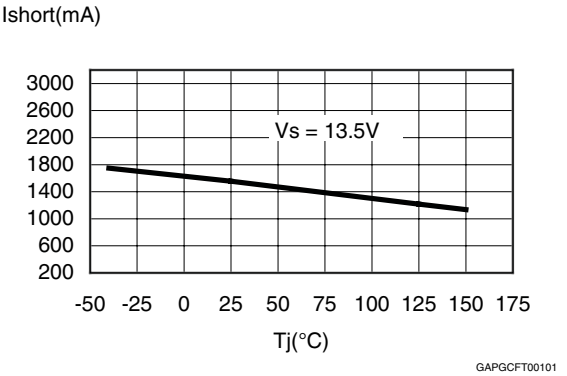


Figure 13. Short-circuit current vs input voltage

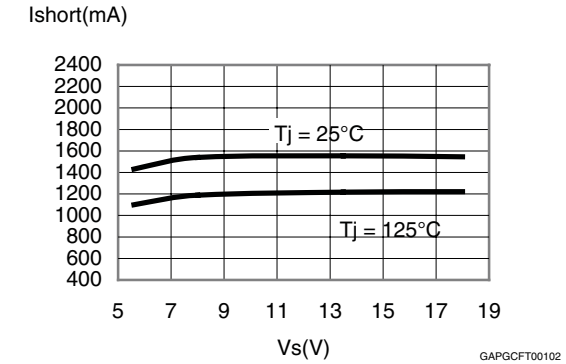


Figure 14. V_{Rhth} vs T_j

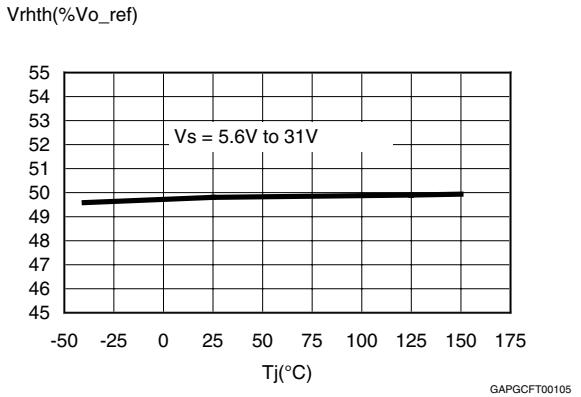


Figure 15. V_{Rlth} vs T_j

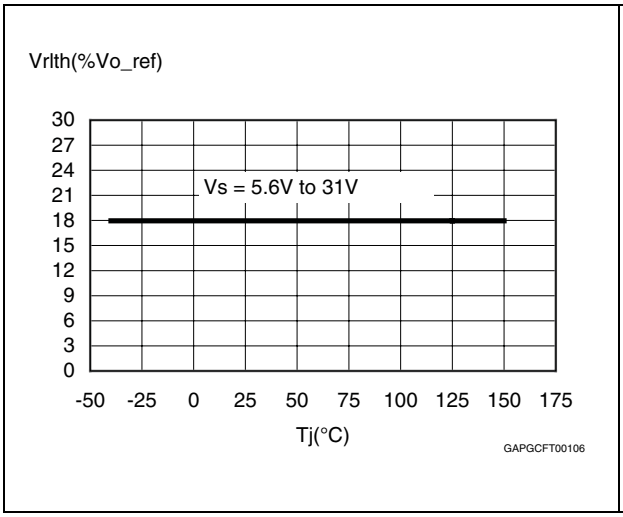


Figure 16. I_{cr} vs T_j

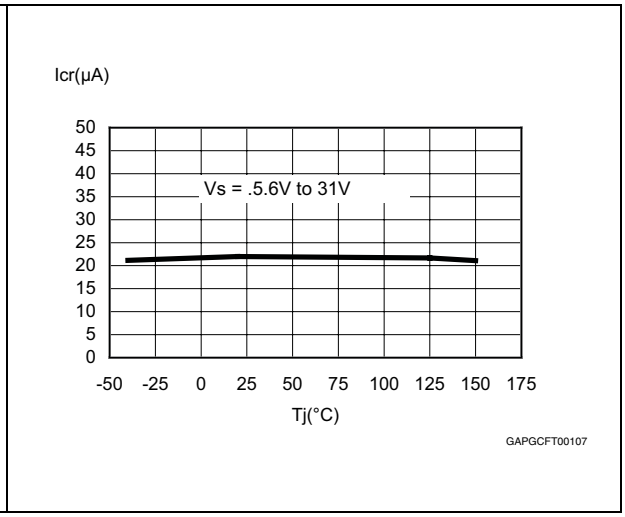
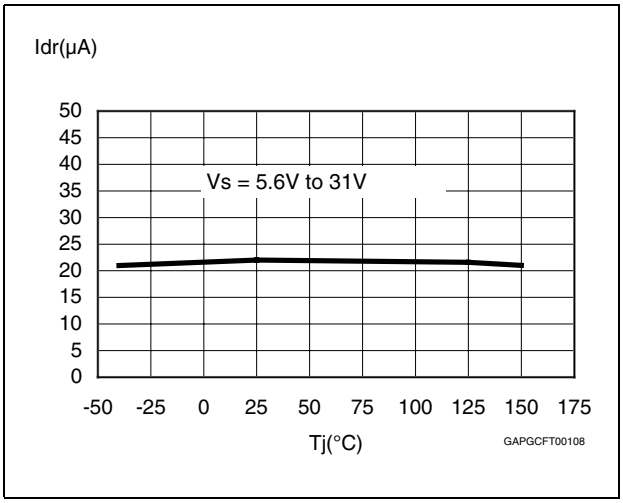


Figure 17. I_{dr} vs T_j

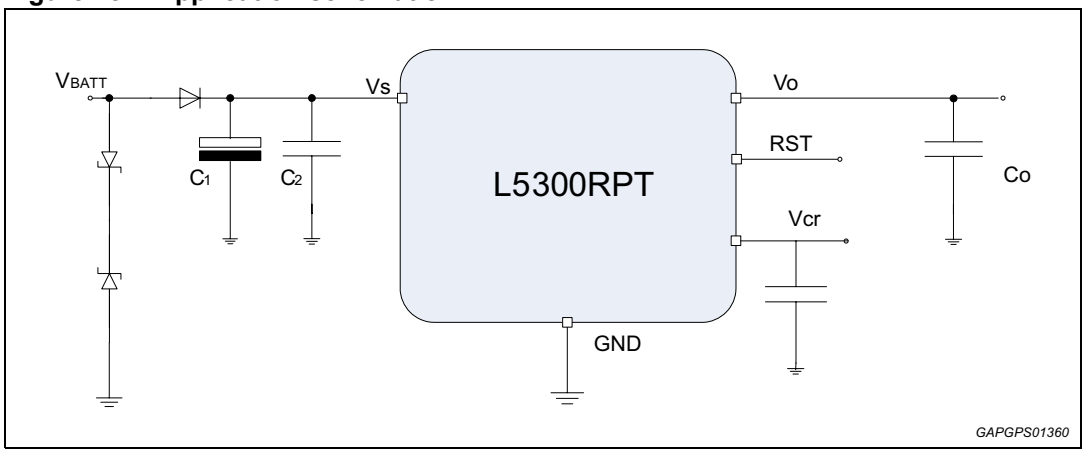


3 Application information

3.1 Voltage regulator

The voltage regulator uses a p-channel mos transistor as a regulating element. With this structure a very low dropout voltage at current up to 300 mA is obtained. The output voltage is regulated up to input supply voltage of 40 V. The high-precision of the output voltage (2%) is obtained with a pre-trimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions the quiescent current goes down to 55 µA only (low consumption mode). This procedure features a certain hysteresis on the output current (see *Figure 7*). Short-circuit protection to GND and a thermal shutdown are provided.

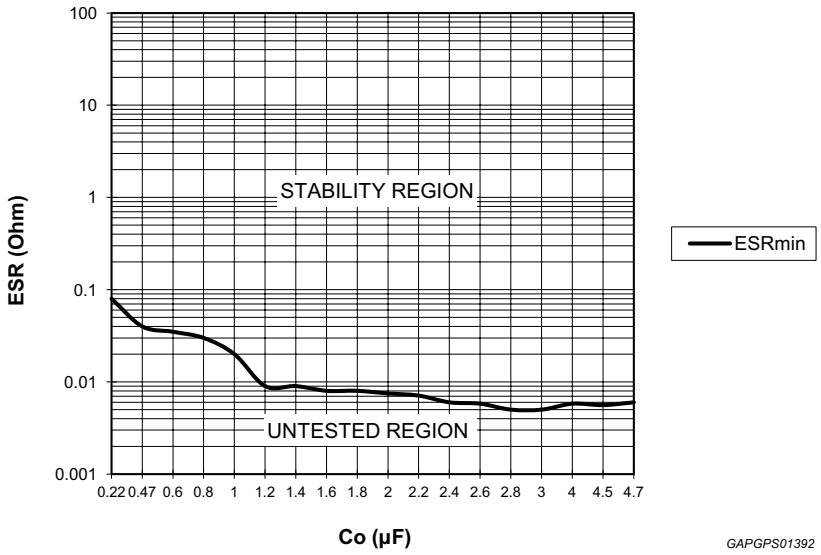
Figure 18. Application schematic



The input capacitor $C_1 \geq 100$ µF is necessary as backup supply for negative pulses which may occur on the line. The second input capacitor $C_2 \geq 220$ nF is needed when the C_1 is too distant from the V_S pin and it compensates smooth line disturbances. The C_0 ceramic capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations. Suggested value is $C_0 = 220$ nF with $ESR \geq 100$ mΩ.

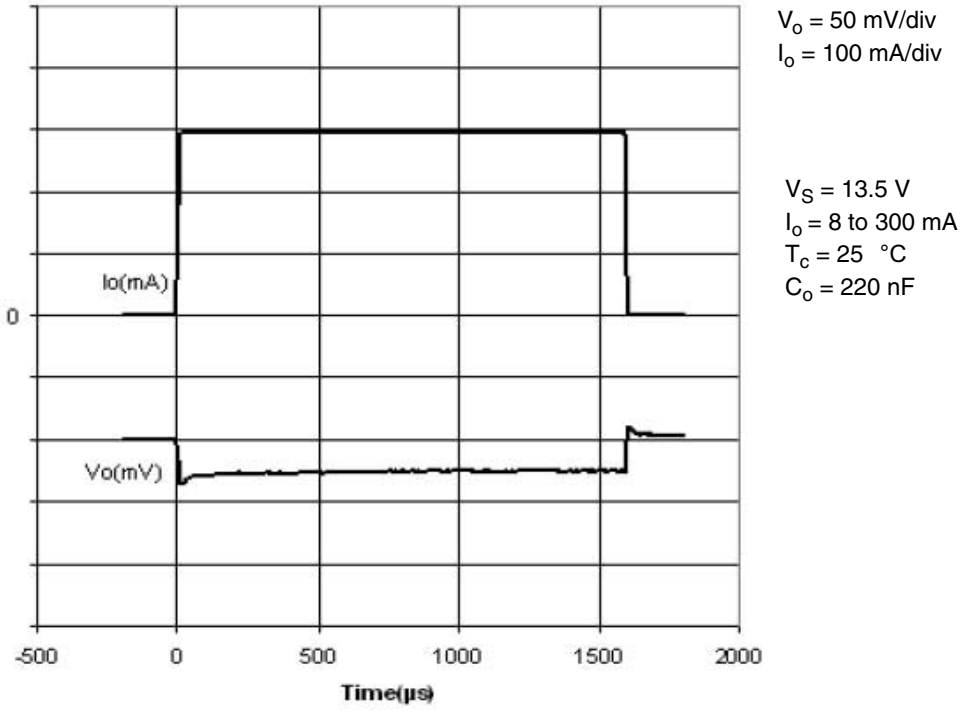
Stability region is reported in *Figure 19*.

Figure 19. Stability region



Note:
The curve which describes the minimum ESR is derived from characterization data on the regulator with connected ceramic capacitors which feature low ESR values (at 100 kHz). Any capacitor with further lower ESR than the given plot value must be evaluated in each and every case.

Figure 20. Maximum load variation response



3.2 Reset

The reset circuit monitors the output voltage V_o. If the output voltage becomes lower than V_{o_th} then R_{es} goes low with a delay time (t_{rr}). When the output voltage becomes higher than V_{o_th} then R_{es} goes high with a delay time t_{rd}. This delay is obtained by 32 periods of oscillator. The oscillator period is given by:

Equation 1

$$T_{osc} = [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{cr} + [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{dr}$$

and reset pulse delay t_{rd} is given by:

Equation 2

$$t_{rd} = 32 \times T_{osc}$$

Where:

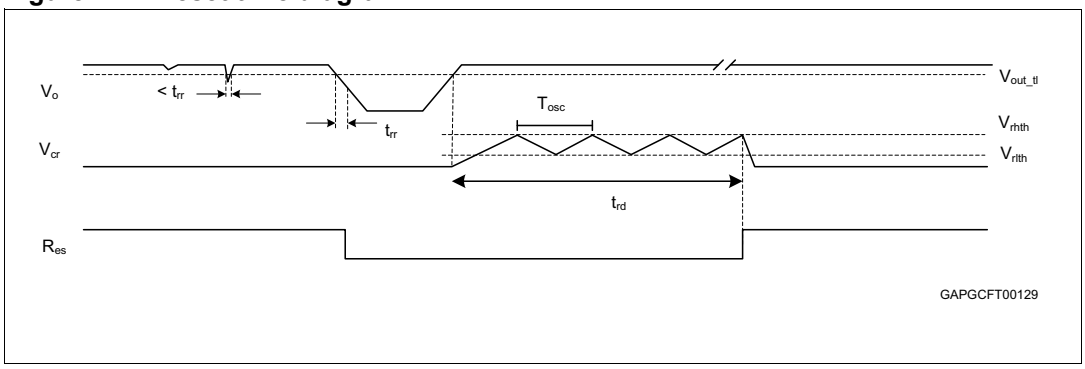
I_{cr} = 20 µA is an internally generated charge current,

I_{dr} = 20 µA is an internally generated discharge current,

V_{Rhth} = 2.5 V (typ) and V_{Rlth} = 0.95V (typ) are two voltage thresholds,

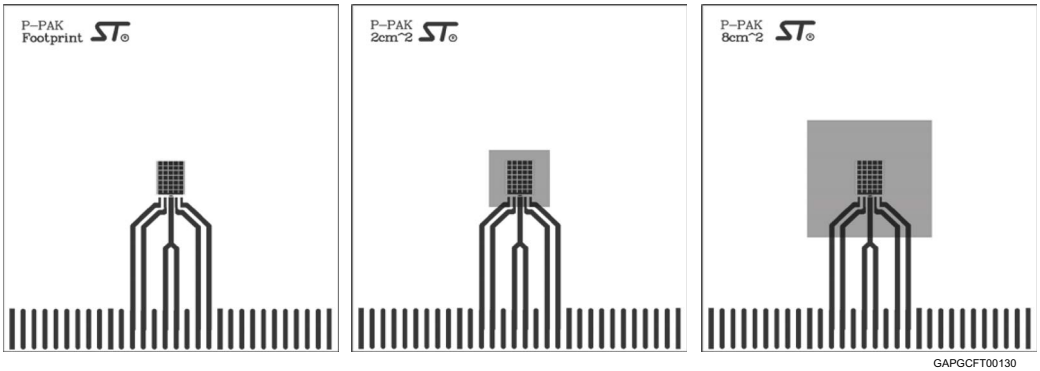
C_{tr} is an external capacitor put between V_{cr} pin and GND.

Figure 21. Reset time diagram



4 Package and PCB thermal data

Figure 22. PPAK PC board



Note:
Layout condition of R_{th} and Z_{th} measurements (Board finish thickness 1.6 mm +/- 10%; Board double layer; Board dimension 78 x 86; Board Material FR4; Cu thickness 0.070 mm (front and back side); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm

Figure 23. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

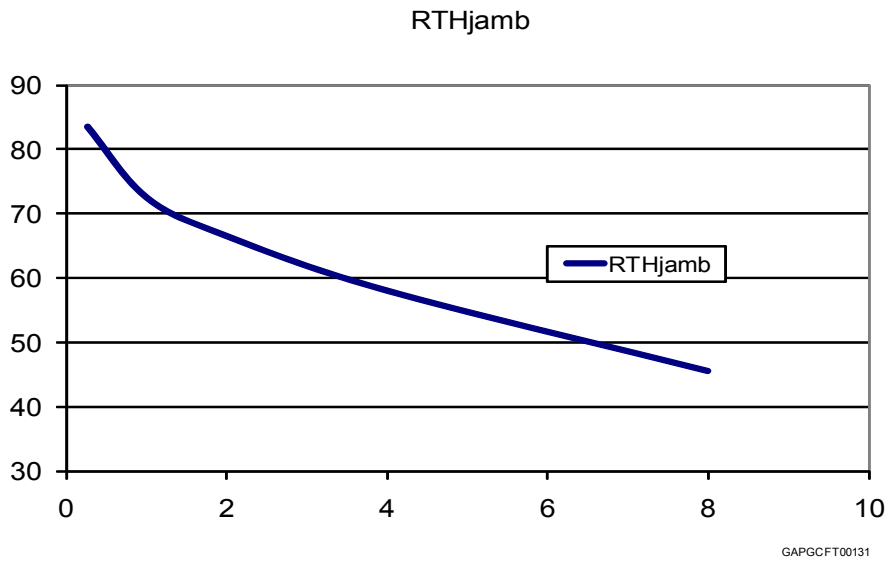
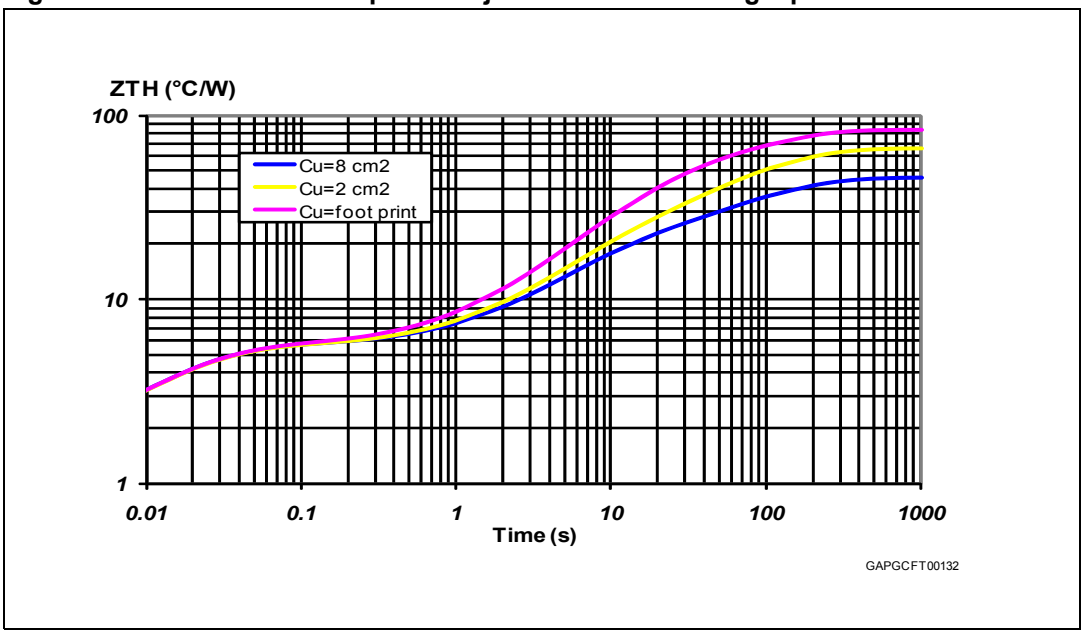


Figure 24. PPAK thermal impedance junction ambient single pulse



Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 25. Thermal fitting model of a Vreg in PPAK

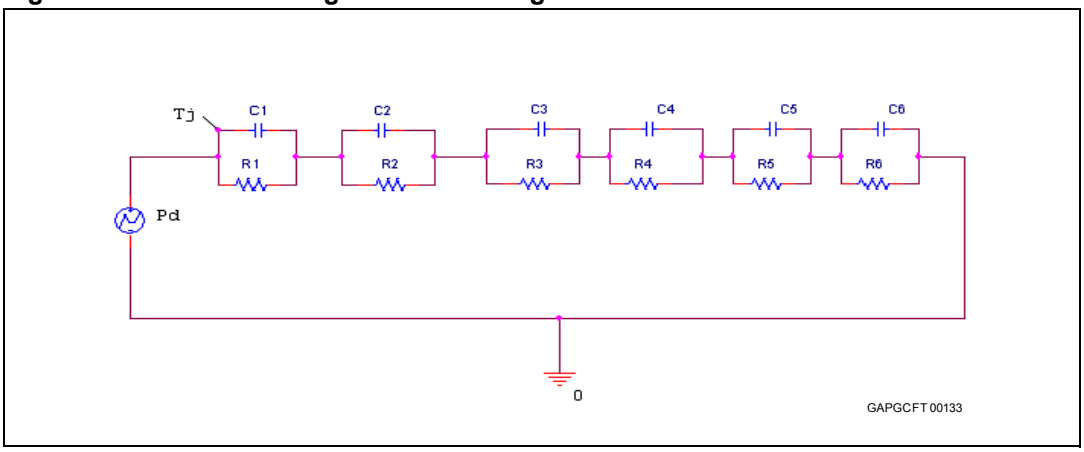


Table 7. PPAK thermal parameter

Area (cm^2)	Footprint	4	8
R1 (°C/W)	1.2		
R2 (°C/W)	1.8		
R3 (°C/W)	2.5		
R4 (°C/W)	14	12	12
R5 (°C/W)	28	22	12
R6 (°C/W)	36	27	16
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.005		
C3 (W.s/°C)	0.01		
C4 (W.s/°C)	0.6	0.6	0.6
C5 (W.s/°C)	0.8	2	4
C6 (W.s/°C)	3	5	9

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.2 PPAK mechanical data

Figure 26. PPAK dimension

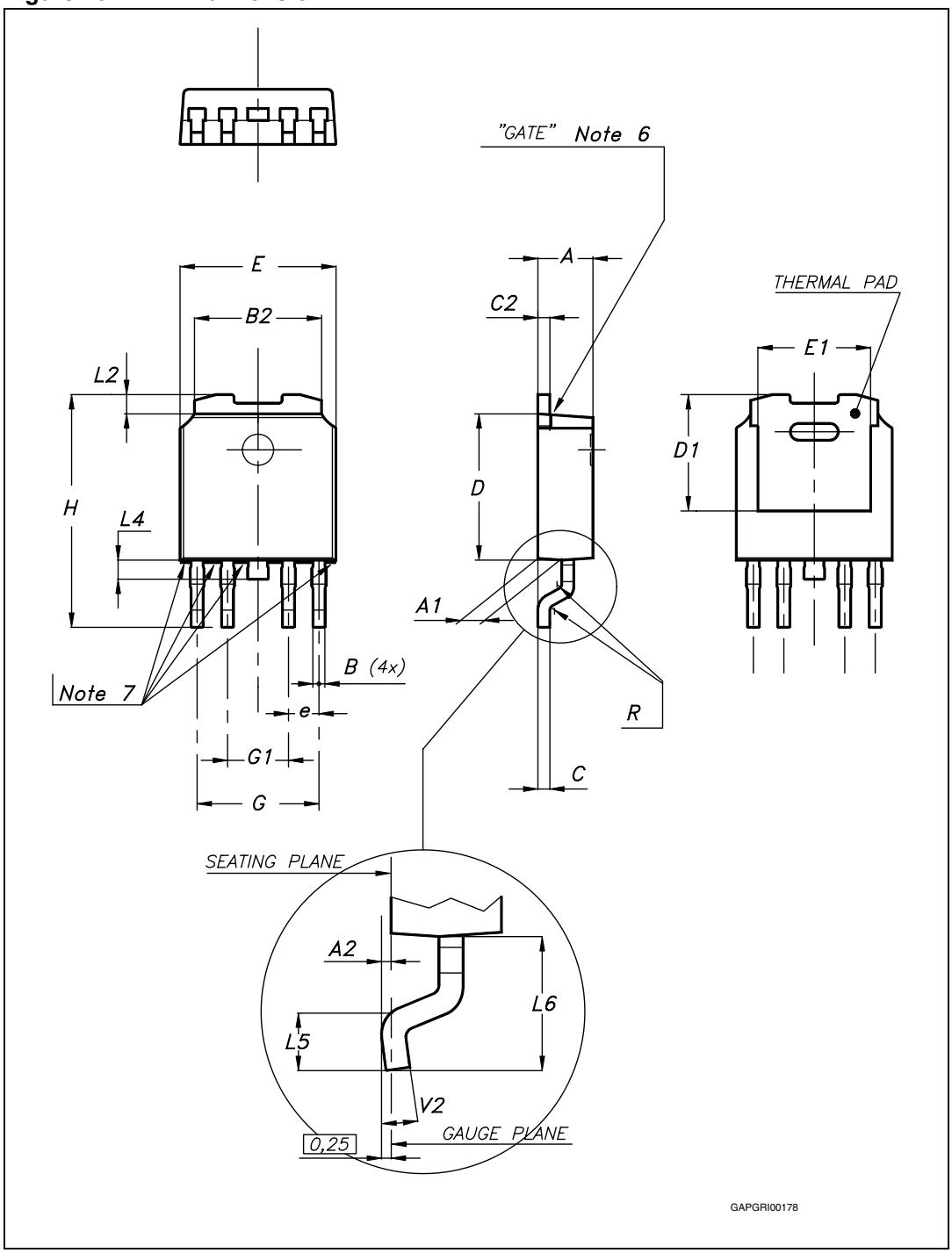
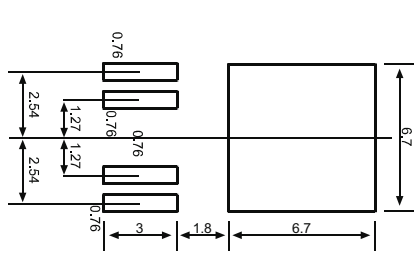


Table 8. PPAK mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D1		5.1	
D	6.00		6.20
E	6.40		6.60
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
L5	1.00		
L6		2.80	
R		0.2	
V2	0º		8º
Package weight	Gr. 0.3		

5.3 PPAK packing information

Figure 27. PPAK suggested pad layout and tube shipment (no suffix)



Base q.ty	75
Bulk q.ty	3000
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

All dimensions are in mm.

GAPGPS01358

Figure 28. PPAK tape and reel shipment (suffix "TR")

Reel dimensions

Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

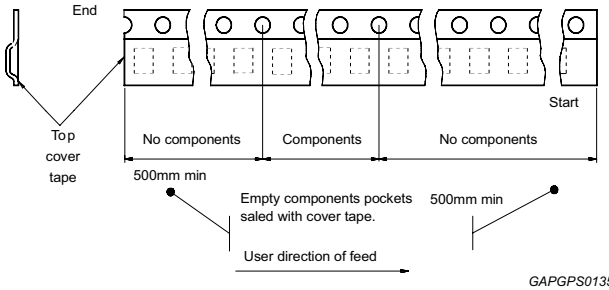
All dimensions are in mm.

Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	16
Tape hole spacing	**P0 (± 0.1)**	4
Component spacing	**P**	8
Hole diameter	**D (± 0.1/-0)**	1.5
Hole diameter	**D1 (min)**	1.5
Hole position	**F (± 0.05)**	7.5
Compartment depth	**K (max)**	2.75
Hole spacing	**P1 (± 0.1)**	2

All dimensions are in mm.



GAPGPS01359

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Jul-2007	1	Initial release.
09-Aug-2007	2	*Table 6: Reset* - reset reaction time note deleted. *Section 3.2* updated
16-Mar-2009	3	Changed features table on the cover page *Table 5: General* – V_{o_ref}: deleted row and added 3 new rows *Table 6: Reset* – I_{Res_lkg}: deleted Test condition – V_{o_th}: deleted I_o = 1 to 300 mA and V_S = 5.6 to 31V, added "V_o decreasing" for Test condition – V_{RIth}: changed min/typ/max values – T_{rd}: changed min/typ/max values *Section 3.2: Reset* – t_{rd}: changed coefficient – V_{RIth}: changed coefficient

Table 9. Document revision history (continued)

Date	Revision	Changes
20-Sep-2010	4	Changed the title of the document *Features* in cover page – Changed typical quiescent current value in table from 60 µA to 55 µA *Description* in cover page – Changed typical quiescent current value from 60 µA to 55 µA – Changed dropped current value from 10 µA to 5 µA *Table 2: Pins description* – Updated pins sequence *Table 3: Absolute maximum ratings* – I_{SDC}: changed symbol from I_{VSDC} – I_{ODC}: changed symbol from I_{VODC} – $V_{ESD\ CDM}$: added standard for parameter Updated *Table 4: Thermal data* *Table 5: General* – I_{short}: changed min/typ/max value – I_{lim}: changed min/typ/max value, changed parameter – V_{line}: changed test condition – V_{load}: changed test condition, added new spec. – SVR: deleted min value, added typ value – I_{qn_300}: changed typ/max value – I_{oth_H}, I_{oth_L}, I_{oth_Hyst}: added new rows – Updated all tablefootnote *Table 6: Reset* – V_{Res_I}: changed test condition – V_{Res_lkg}: added test condition *Section 3.2: Reset* – Changed text Deleted Figure 3: Behavior of output current versus regulated voltage V_o Added *Section 2.4: Electrical characteristics curves* Added *Chapter 4: Package and PCB thermal data*
12-Oct-2010	5	Updated *Section 3.1: Voltage regulator*
27-Jan-2012	6	Updated *Figure 19: Stability region on page 14*.
07-Feb-2012	7	Modified *Figure 19: Stability region on page 14*.
04-May-2012	8	Updated *Figure 26: PPAK dimension on page 20* and *Table 8: PPAK mechanical data*.

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