L3GD20H

MEMS motion sensor: three-axis digital output gyroscope

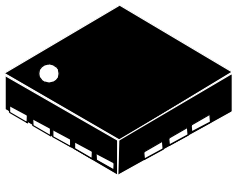
Datasheet — preliminary data

Features

- Wide supply voltage, 2.2 V to 3.6 V
- Wide extended operating temperature range (from -40 °C to 85 °C)
- Low voltage compatible IOs, 1.8 V
- Low power consumption
- Embedded power-down
- Sleep mode
- Fast turn-on and wake-up
- Three selectable full scales up to 2000 dps
- 16 bit rate value data output
- 8 bit temperature data output
- I²C/SPI digital output interface
- 2 dedicated lines (1 interrupt, 1 data ready)
- User enable integrated high-pass filters
- Embedded temperature sensor
- Embedded 32 levels of 16 bit data output FIFO
- High shock survivability
- ECOPACK® RoHS and “Green” compliant

Applications

- Gaming and virtual reality input devices
- Motion control with MMI (man-machine interface)
- GPS navigation systems
- Appliances and robotics



LGA-16 (3x3x1 mm)

Description

The L3GD20H is a low-power three-axis angular rate sensor.

It includes a sensing element and an IC interface able to provide the measured angular rate to the external world through digital interface (I²C/SPI).

The sensing element is manufactured using a dedicated micromachining process developed by ST to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The L3GD20H has a full scale of ±245/±500/±2000 dps and is capable of measuring rates with a user selectable bandwidth.

The L3GD20H is available in a plastic land grid array (LGA) package and can operate within a temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order code	Temperature range (°C)	Package	Packing
L3GD20H	-40 to +85	LGA-16 (3x3x1)	Tray
L3GD20HTR	-40 to +85	LGA-16 (3x3x1)	Tape and reel

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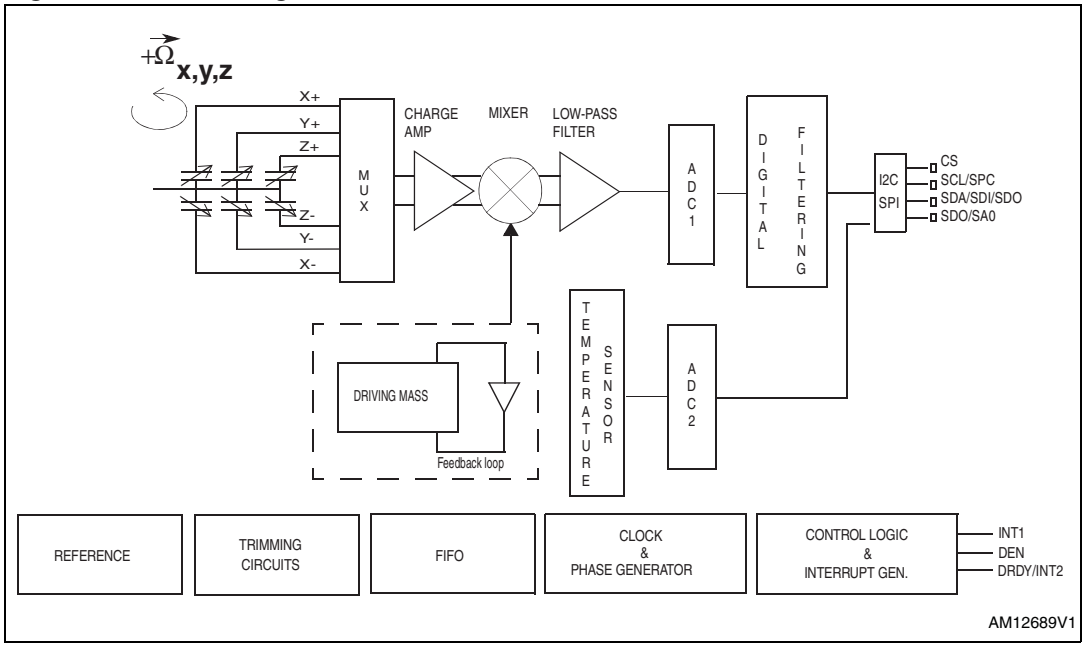
1 Block diagram and pin description

Figure 1. Block diagram



The vibration of the structure is maintained by a drive circuitry in a feedback loop. The sensing signal is filtered and appears as digital signal at the output.

1.1 Pin description

Figure 2. Pin connection

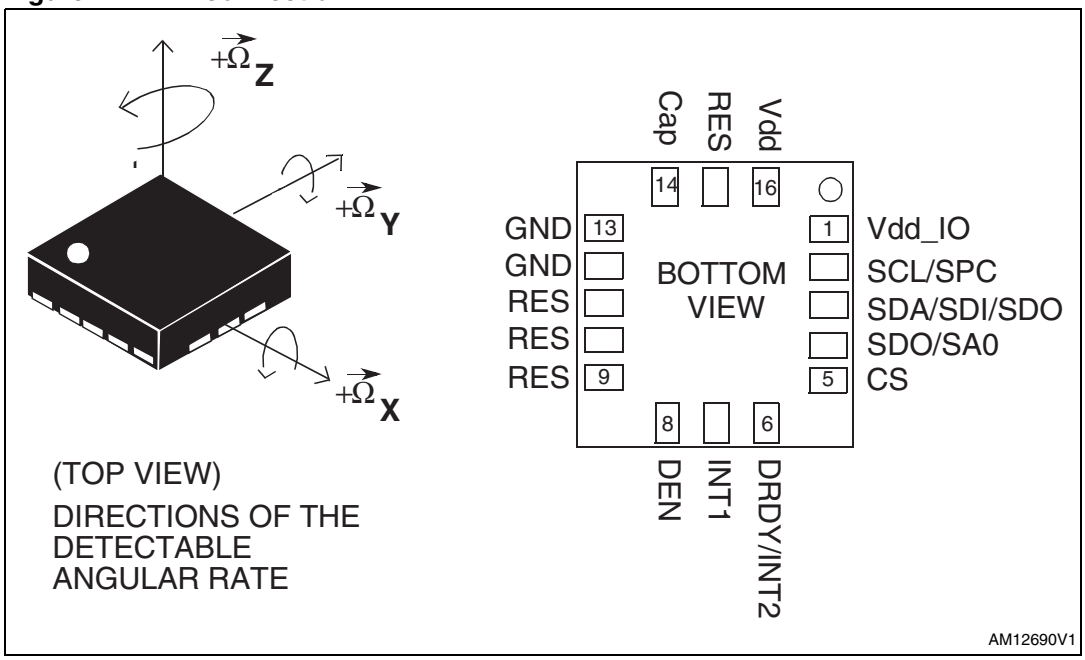


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO(1)	Power supply for I/O pins
2	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
3	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
5	CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
6	DRDY/INT2	Data ready/fifo interrupt (FIFO Threshold/overrun/empty)
7	INT1	Programmable Interrupt
8	DEN	Gyroscope data enable
9	Reserved	Connect to GND
10	Reserved	Connect to GND
11	Reserved	Connect to GND
12	GND	0 V supply
13	GND	0 V supply
14	Cap	Connect to GND with ceramic capacitor(2)
15	Reserved	Connect to Vdd
16	Vdd(3)	Power supply

1. Recommended 100 nF filter capacitor.
2. 10 nF (+/-10%), 25 V. 1 nF minimum value has to be guaranteed under 12 V bias condition.
3. Recommended 100 nF plus 10 µF capacitors.

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted[a]

Table 3. Mechanical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
FS	Measurement range	User selectable		±245 ±500 ±2000		dps
So	Sensitivity			8.75 17.50 70.00		mdps/digit
SoDr	Sensitivity change vs. temperature[2]	From -40 °C to +85 °C Delta from T = 25 °C		±2		%
DVoff	Digital Zero-rate level	FS = 2000 dps		±25		dps
OffDr	Zero-rate level change vs temperature[3]	FS = 2000 dps		±0.04		dps/°C
NL	Non linearity[3]	Best fit straight line		0.2		% FS
Rn	Rate noise density[3]	BW = 50 Hz		0.011		dps/($\sqrt{Hz}$)
ODR	Digital output data rate[3]			11.9/23.7/ 47.3/94.7/ 189.4/ 378.8/ 757.6		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Guaranteed by design.
3. The period (1/ODR), length of time between two consecutive sampling, must be derived by the reciprocal of the maximum. and minimum ODR limits: for example for ODR = 189.4 Hz, sampling period range will be within [4591 µs, 6211 µs] (where ODR minimum and maximum have been approximated at 162 Hz, 219 Hz respectively).

a. The product is factory calibrated at 3.0 V. The operational power supply range is specified in *Table 4*.

2.2 Electrical characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted[b]

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
Vdd	Supply voltage		2.2	3.0	3.6	V
Vdd_IO	I/O pins supply voltage[2]		1.71		Vdd+0.1	V
Idd	Supply current			5.0		mA
IddSL	Supply current in sleep mode[3]	Selectable by digital interface		2.5		mA
IddPdn	Supply current in power-down mode	Selectable by digital interface		1		µA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
Ton	Turn-on time[4]	LPF2 disabled ODR = 190 Hz		50		ms
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.
3. Sleep mode introduces a faster turn-on time related to power down mode.
4. Time to obtain stable Sensitivity (within ±5% of final value) after exiting power-down mode. It is guaranteed by design.

b. The product is factory calibrated at 3.0 V.

2.3 Temperature sensor characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted[c]

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
TSDr	Temperature sensor output change vs temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

c. The product is factory calibrated at 3.0 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

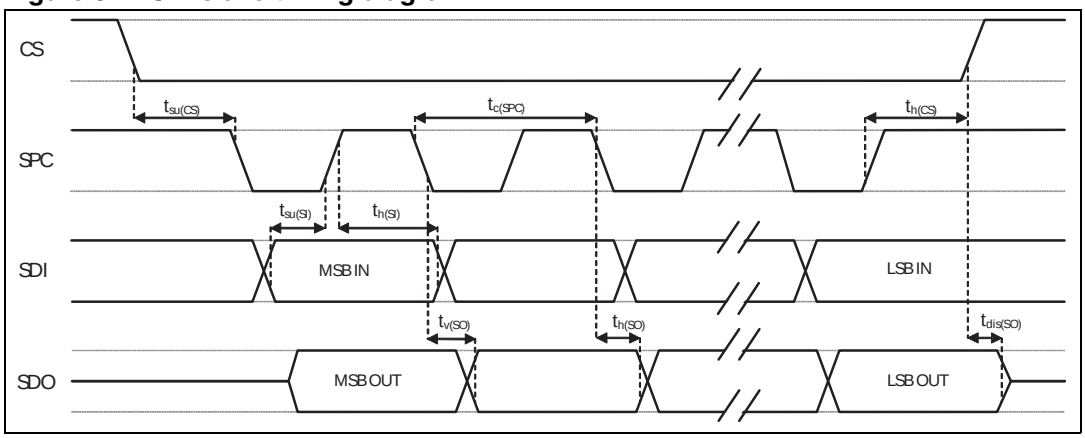
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	20		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	5		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 3. SPI slave timing diagram(d)



d. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both Input and Output port.

2.4.2 I²C - Inter IC control interface

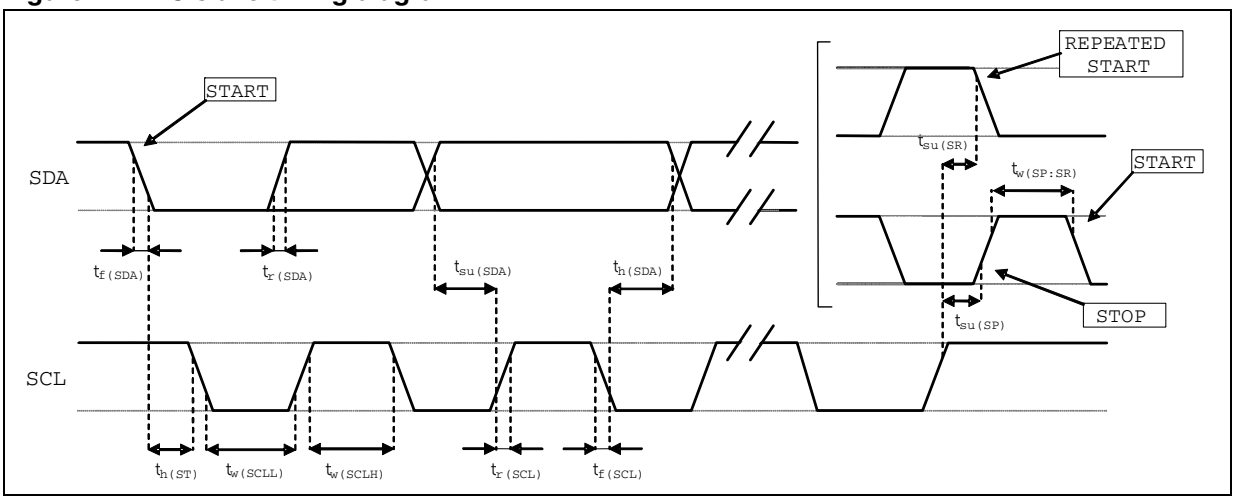
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C Standard mode(1)		I²C Fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.
2. Cb = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram(e)



e. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration g for 0.1 ms	10,000	*g*
ESD	Electrostatic discharge protection	2 (HBM)	kV
Vin	Input Voltage on any control pin (including CS,SCL/SPC,SDA/SDI/SDO,SDO/SA0,DEN)	0,3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part

This is an ESD sensitive device, improper handling can cause permanent damage to the part

2.6 Terminology

2.6.1 Sensitivity

An angular rate gyroscope is device that produces a positive-going digital output for counterclockwise rotation around the sensible axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

2.6.2 Zero-rate level

Zero-rate level describes the actual output signal if there is no angular rate present. Zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

2.7 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

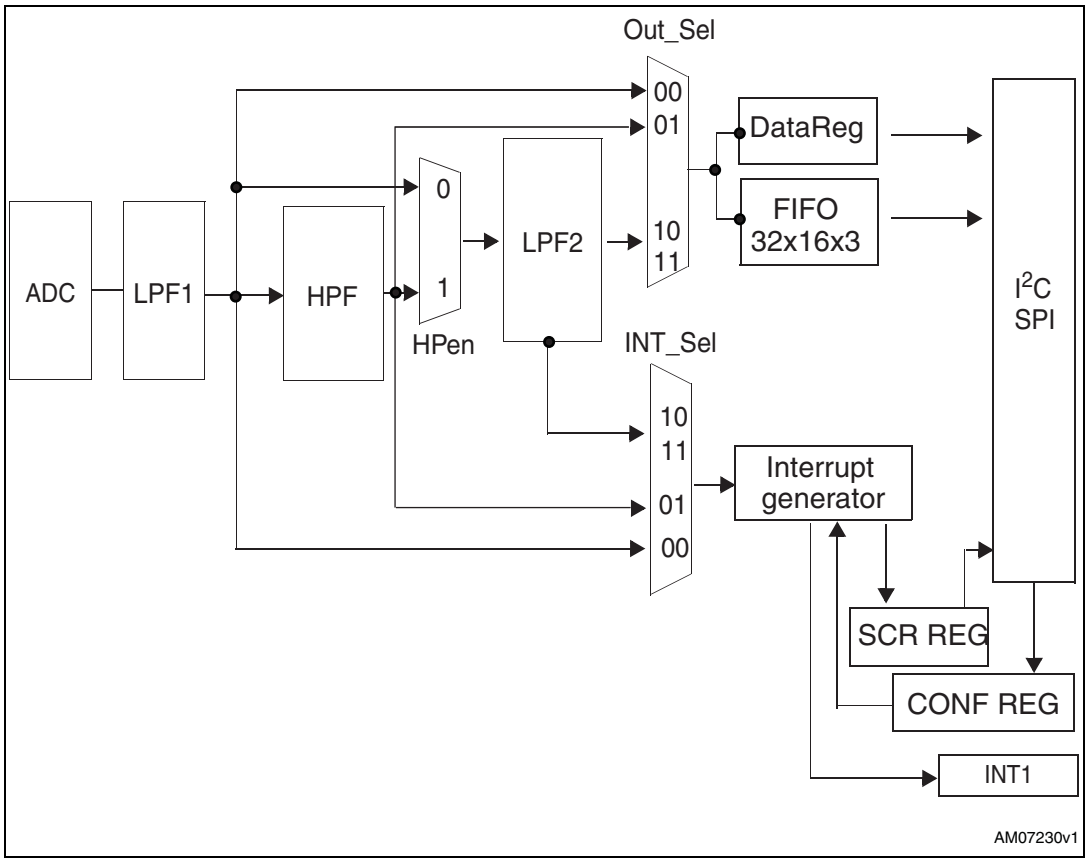
Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

3 Digital main blocks

3.1 Block diagram

Figure 5. Block diagram



3.2 FIFO

The L3GD20H embeds a 32-slot, 16 bit data FIFO for each of the three output channels, yaw, pitch and roll. This allows a consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to six different modes: Bypass mode, FIFO-mode, Stream mode, Stream-to-FIFO mode, Bypass-to-Stream, Bypass-to-FIFO.

4 Digital interfaces

The registers embedded inside the L3GD20H may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I^2C interface, CS line must be tied high (i.e connected to Vdd_IO).

Table 9. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL/SPC	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)
SDA/SDI/SDO	I^2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO/SA0	SPI Serial Data Output (SDO) I^2C less significant bit of the device address

4.1 I^2C serial interface

The L3GD20H I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 10. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through external pull-up resistor. When the bus is free both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with the normal mode.

4.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave ADdress (SAD) associated to the L3GD20H is 110101xb. SDO/SA0 pin can be used to modify less significant bit of the device address. If SDO/SA0 pin is connected to voltage supply LSb is ‘1’ (address 1101011b) else if SDO/SA0 pin is connected to ground LSb value is ‘0’ (address 1101010b). This solution permits to connect and address two different gyroscopes to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the L3GD20H behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address will be transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is 1, the SUB (register address) will be automatically incremented to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was ‘1’ (Read), a repeated START (SR) condition will have to be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the Master will transmit to the slave with direction unchanged. *Table 11* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 11. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SDO	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 12. Transfer when Master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 13. Transfer when Master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 14. Transfer when Master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 15. Transfer when Master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to be read.

In the presented communication format MAK is Master Acknowledge and NMAK is No Master Acknowledge.

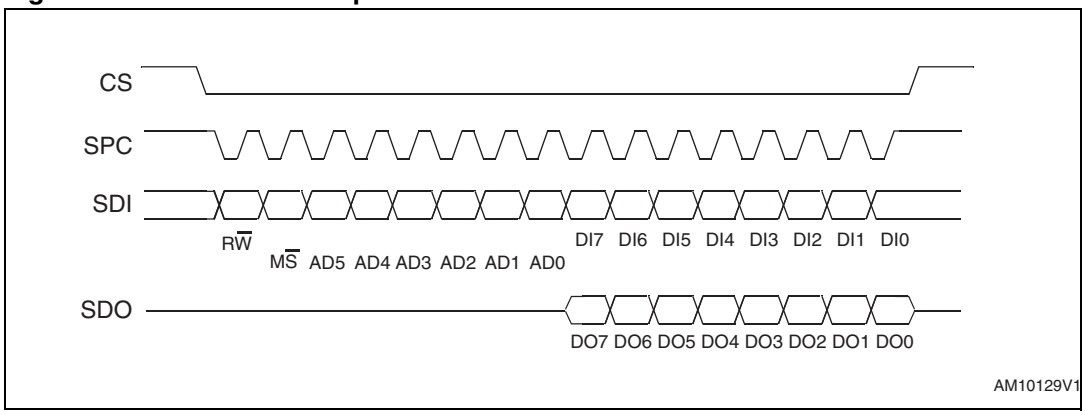
In order to disable the I2C block it is needed to write '1' in bit 3 of register located in address 39h.

4.2 SPI bus interface

The SPI is a bus slave. The SPI allows to write and read the registers of the device.

The Serial Interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 6. Read and write protocol



CS is the Serial Port Enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written into the device (MSb first).

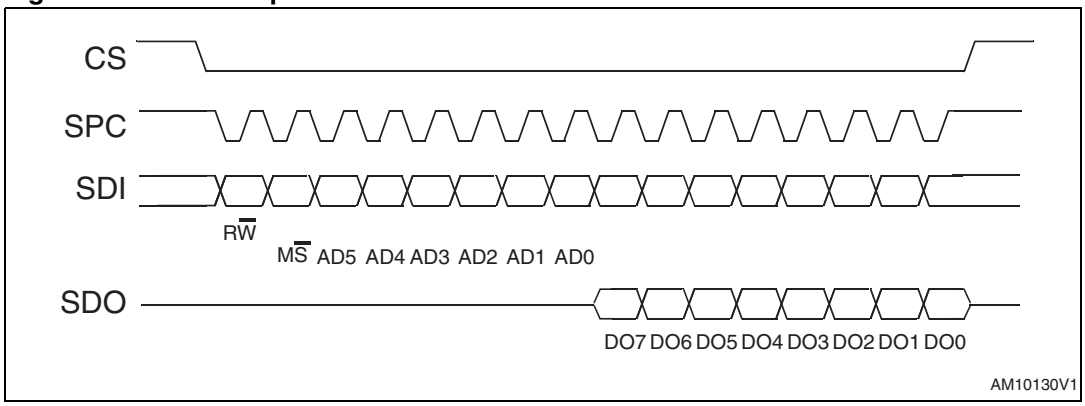
bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When M$\overline{S}$ bit is 0 the address used to read/write data remains the same for every block. When M$\overline{S}$ bit is 1 the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

4.2.1 SPI read

Figure 7. SPI read protocol



The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

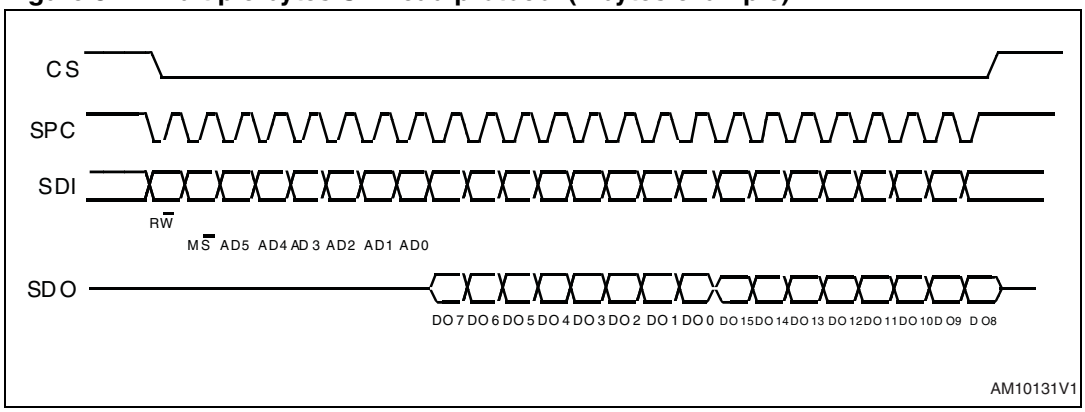
bit 1: MS bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

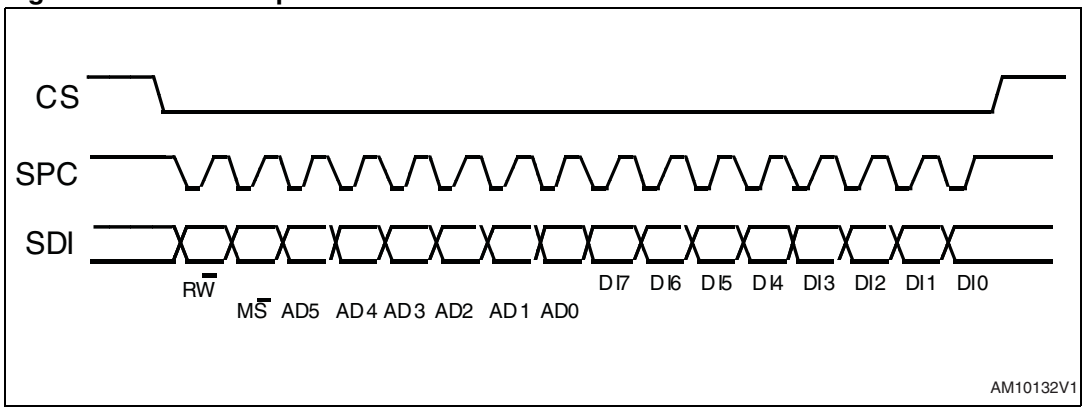
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 8. Multiple bytes SPI read protocol (2 bytes example)



4.2.2 SPI write

Figure 9. SPI write protocol



The SPI Write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

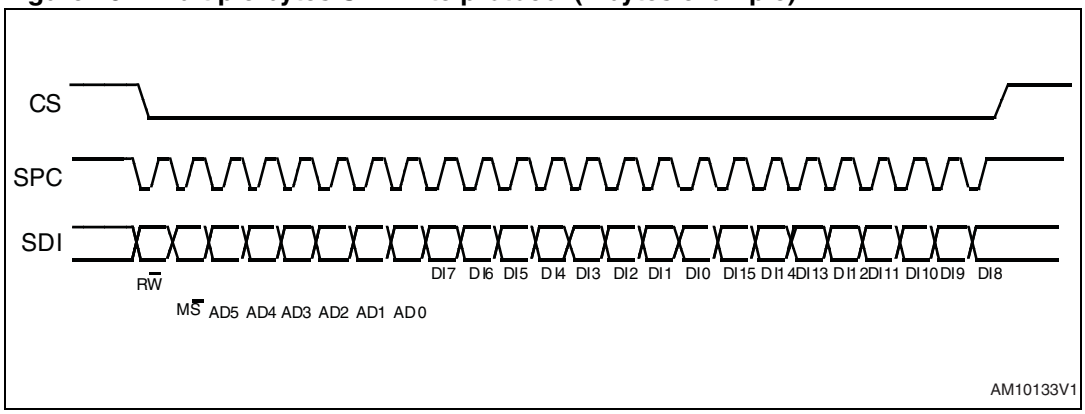
bit 1: MS bit. When 0 do not increment address, when 1 increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

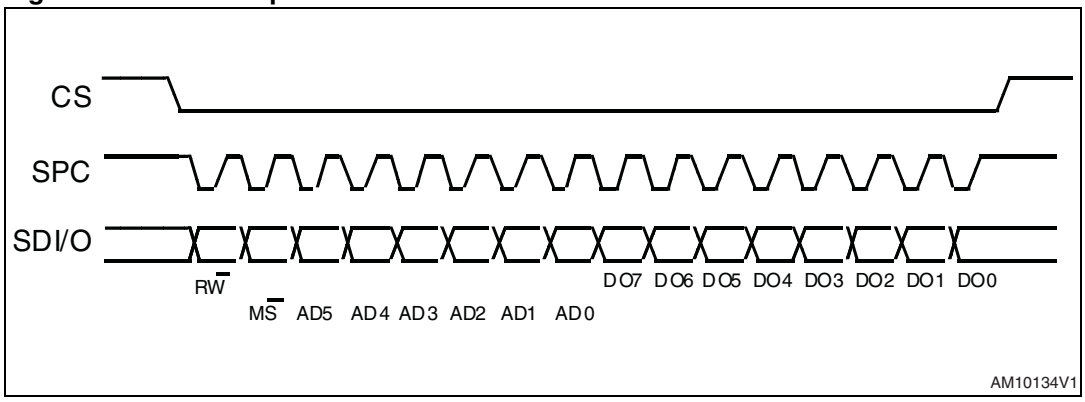
bit 16-... : data DI(...-8). Further data in multiple byte writing.

Figure 10. Multiple bytes SPI write protocol (2 bytes example)



4.2.3 SPI read in 3-wires mode

Figure 11. SPI read protocol in 3-wires mode



The SPI Read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: M$\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

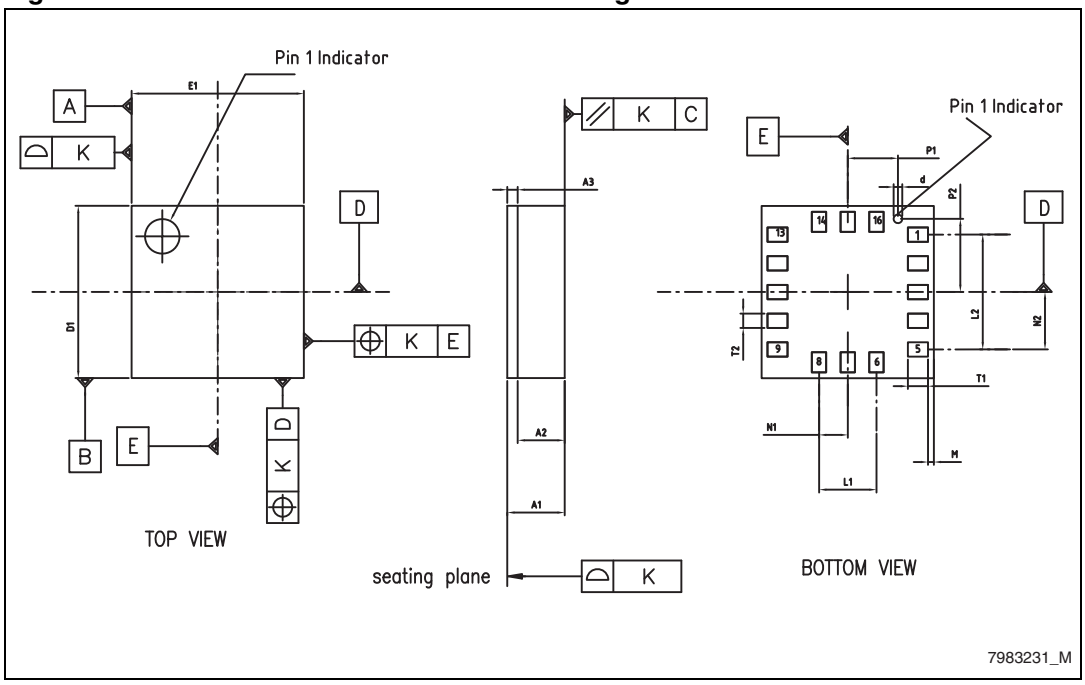
5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 16. LGA 3x3x1.0 16L mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1			1
A2		0.785	
A3		0.200	
D1	2.850	3.000	3.150
E1	2.850	3.000	3.150
L1		1.000	1.060
L2		2.000	2.060
N1		0.500	
N2		1.000	
M	0.040	0.100	
P1		0.875	
P2		1.275	
T1	0.290	0.350	0.410
T2	0.190	0.250	0.310
d		0.150	
k		0.050	

Figure 12. LGA 3x3x1.0 16L mechanical drawing



6 Revision history

Table 17. Document revision history

Date	Revision	Changes
20-Jul-2012	1	Initial release.

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