

EMIF02-SPK01C2

2 line EMI filter and ESD protection

Main product characteristics

Where EMI filtering in ESD sensitive equipment is required:

- Mobile phones and communication systems
- Computers and printers and MCU Boards

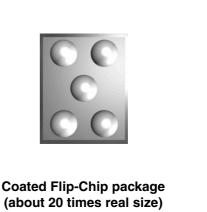
Description

The EMIF02-SPK01C2 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference. The Flip-Chip packaging means the package size is equal to the die size.

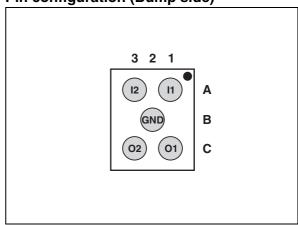
This filter includes ESD protection circuitry, which prevents damage to the application when it is subjected to ESD surges up to 15 kV.

Benefits

- EMI symmetrical (I/O) low-pass filter
- High efficiency EMI filter (-33 dB @ 900 MHz)
- Very low PCB space consumption: 1.07 mm x 1.47 mm
- Very thin package: 0.695 mm
- Coating resin on back side and lead free package
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging.



Pin configuration (Bump side)



Complies with following standards:

IEC 61000-4-2

level 4 input pins 15 kV (air discharge)

8 kV (contact discharge

level 1 output pins 2 kV (air discharge)

2 kV (contact discharge

MIL STD 883G - Method 3015-7 Class 3

Characteristics EMIF02-SPK01C2

1 Characteristics

Figure 1. Basic cell configuration

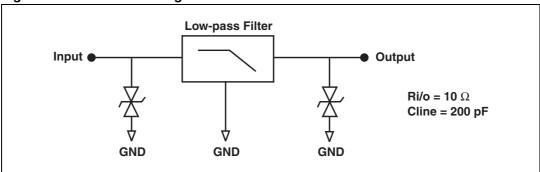


Table 1. Absolute ratings (limiting values)

| Symbol | Parameter | Value | Unit |
|------------------|------------------------------|-------------|------|
| T _j | Maximum junction temperature | 125 | °C |
| T _{op} | Operating temperature range | -40 to +85 | °C |
| T _{stg} | Storage temperature range | -55 to +150 | °C |

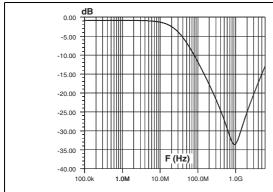
Table 2. Electrical characteristics ($T_{amb} = 25^{\circ} C$)

| Symbol | Parameters | |
|-------------------|--|---------------------------------|
| V _{BR} | Breakdown voltage | I _{PP} |
| I _{RM} | Leakage current @ V _{RM} | |
| V _{RM} | Stand-off voltage | IB . |
| V _{CL} | Clamping voltage | VCL VBR VRM IRM IRM VRM VBR VCL |
| R _d | Dynamic impedance | lR |
| I _{PP} | Peak pulse current | |
| R _{I/O} | Series resistance between input and output | IPP |
| C _{line} | Input capacitance per line | ' |

| Symbol | Test conditions | Min | Тур | Max | Unit |
|-------------------|--------------------------------|-----|-----|-----|------|
| V _{BR} | I _R = 1 mA | 6 | 8 | | V |
| I _{RM} | V _{RM} = 3 V per line | | | 500 | nA |
| R _{I/O} | Tolerance ±20% | | 10 | | Ω |
| C _{line} | V _R = 0 V | | 200 | | pF |

EMIF02-SPK01C2 Characteristics

Figure 2. S21 (dB) attenuation measurement Figure 3. Analog crosstalk measurement



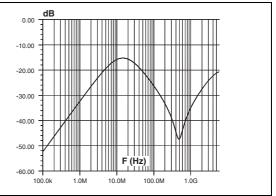
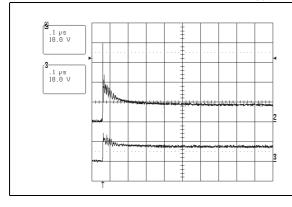


Figure 4. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input V_{in} and one output V_{out}

Figure 5. ESD response to IEC 61000-4-2 (- 15 kV air discharge) on one input V_{in} and one output V_{out}



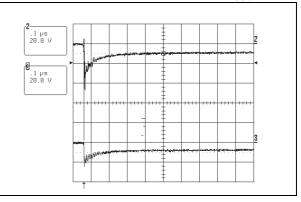
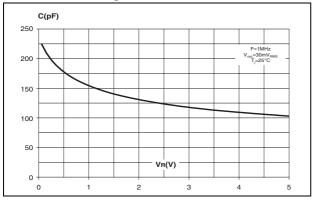


Figure 6. Line capacitance versus applied voltage



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Figure 7. Aplac model

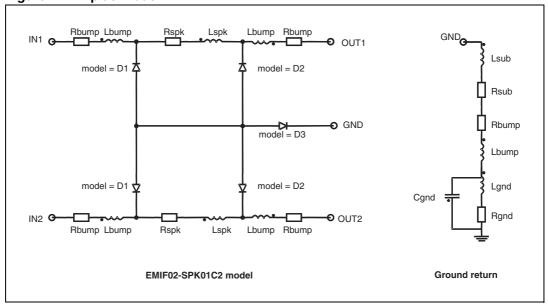
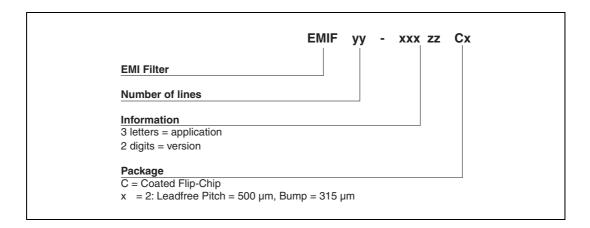


Figure 8. Aplac parameters

| Model D1 Model D3 CJO=Cdiode1 CJO=Cdio BV=7 BV=7 IBV=1u IBV=1u IKF=1000 IKF=1000 IS=10f IS=10f | BV=7 IBV=1u | aplacvar Ls 1nH e2 aplacvar Rs 150m aplacvar Rspk 10 aplacvar Lspk 10p aplacvar Cdiode1 234pF |
|--|----------------------------|---|
| CJO=Cdiode1 | BV=7 IBV=1u IKF=1000 | aplacvar Rspk 10 aplacvar Lspk 10p |
| IBV=1u IBV=1u IKF=1000 IKF=1000 IS=10f IS=10f | IBV=1u IKF=1000 | aplacvar Lspk 10p |
| IKF=1000 IKF=1000 IS=10f IS=10f | IKF=1000 | |
| IS=10f IS=10f | | aplacvar Cdiode1 234pF |
| | IS=10f | |
| | 10-101 | aplacvar Cdiode2 3.5ppF |
| ISR=100p ISR=100p | ISR=100p | aplacvar Cdiode3 1nF |
| N=1 N=1 | N=1 | aplacvar Lbump 50pH |
| M=0.3333 M=0.3333 | M=0.3333 | aplacvar Rbump 10m |
| RS=0.7 RS=0.12 | RS=0.3 | aplacvar Rsub 0.5m |
| VJ=0.6 VJ=0.6 | VJ=0.6 | aplacvar Lsub 10pH |
| TT=50n TT=50n | TT=50n | aplacvar Rgnd 1m |
| | | aplacvar Lgnd 50pH |
| | | aplacvar Cgnd 0.15pF |

2 Ordering information scheme



3 Package information

Figure 9. Flip-Chip Dimensions

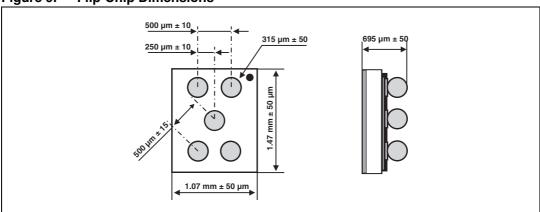
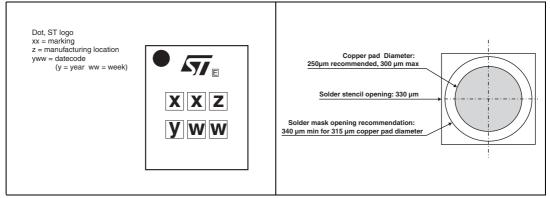


Figure 10. Marking

Figure 11. Footprint recommendation



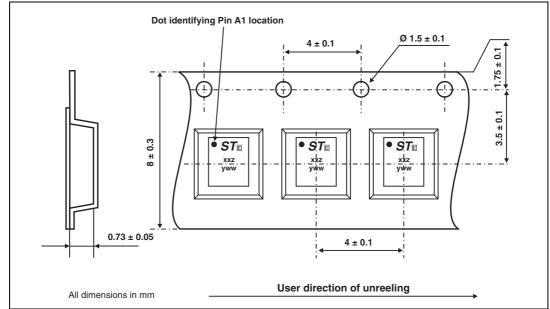


Figure 12. Flip-Chip tape and reel specification

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

| Ordering code | Marking | Package | Weight | Base qty | Delivery mode |
|----------------|---------|-----------|--------|----------|------------------|
| EMIF02-SPK01C2 | FX | Flip-Chip | 2.3 mg | 5000 | 7" Tape and reel |

5 Revision history

| Date | Revision | Changes |
|-------------|----------|------------------|
| 26-Jan-2006 | 1 | Initial release. |

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