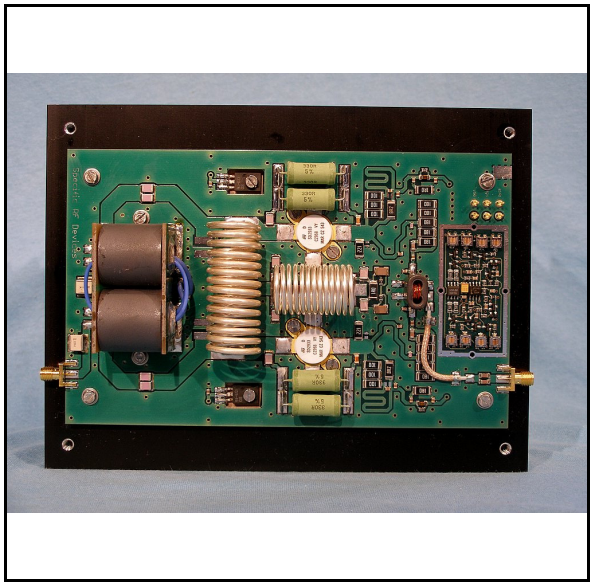
DB-2933-54

RF POWER amplifier using 2 x SD2933 N-Channel enhancement-mode lateral MOSFETs



General feature

- Excellent thermal stability
- Frequency: 1.6 - 54MHz
- Supply voltage: 48V
- Output power: 400W typ.
- Input power 10W max.
- Efficiency: 57% - 76%
- IMD at 300WPEP < -26dBc
- Load mismatch: 3:1all phases

Description

The DB-2933-54 is a RF broadband power amplifier intended for linear or nonlinear operation over the band 1.6 to 54 MHz using 2x SD2933 gold metallized N-channel MOS field-effect transistors. The temperature compensating biasing circuit supports class B and class AB operation.

DB-2933-54 is designed in cooperation with Specific RF Devices.

(e-mail : specific.rf.devices@t-online.de)

Order Code

- DB-2933-54

Contents

1 Electrical data

1.1 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
P_{IN}	Input power	16	W
P_{OUT}	Output power	500	W
V_{DD}(1)	Drain supply voltage	50	V
V_{GG}	Gate biasing voltage	15	V
I_{DD}	Drain current	20	A
P_{DISS}	Power dissipation	400	W

1. V_{GG} from 9 to 15V and P_{IN} < 16W

2 Electrical characteristics

T_A = +25 °C, V_{DD} = 48V, I_{DQ} = 2 x 900mA

Table 2. Electrical Specification

Symbol	Test Conditions	Min	Typ	Max	Unit
Freq	Frequency range	1.6		54	MHz
P_{OUT}	P_{IN} = 10W	300	400		W
Gain	P_{IN} = 10W		16.2 ±0.6dB		dB
ND	P_{IN} = 10W		57 - 76		%
H2	2^{ND} Harmonic @ P_{OUT} = 300W		-26 / -49		dBc
H3	3^{RD} Harmonic @ P_{OUT} = 300W		-13 / -58		dBc
VSWR	Load mismatch all phases @ P_{OUT} = 300W			3:1	

3 Typical performance

Figure 1. Output power & efficiency vs frequency

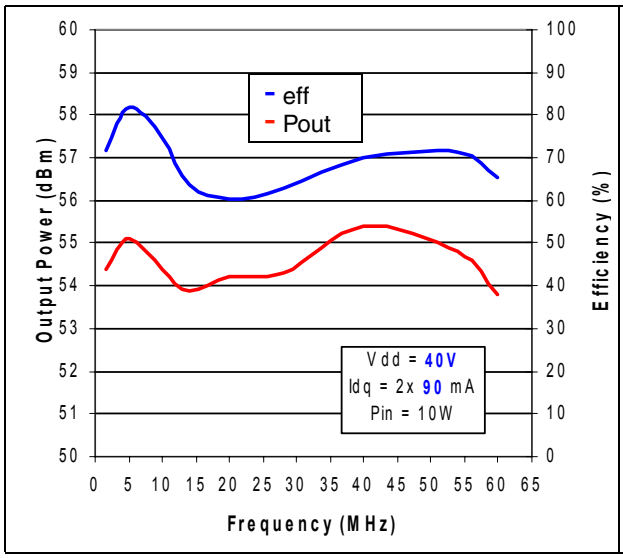


Figure 2. Output power & efficiency vs frequency

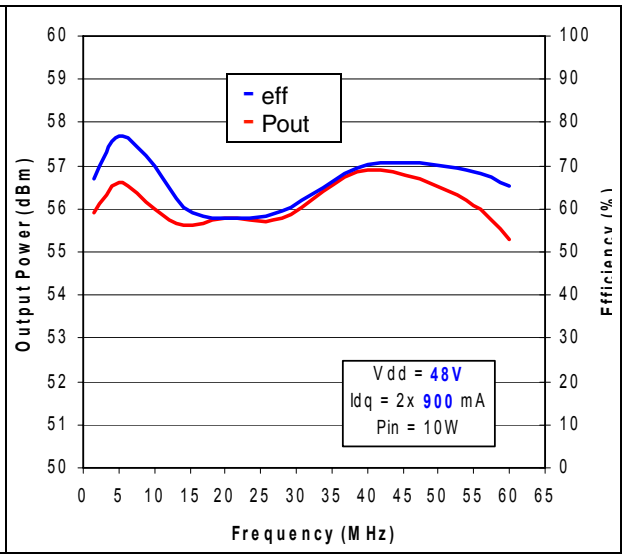


Figure 3. IMD vs frequency

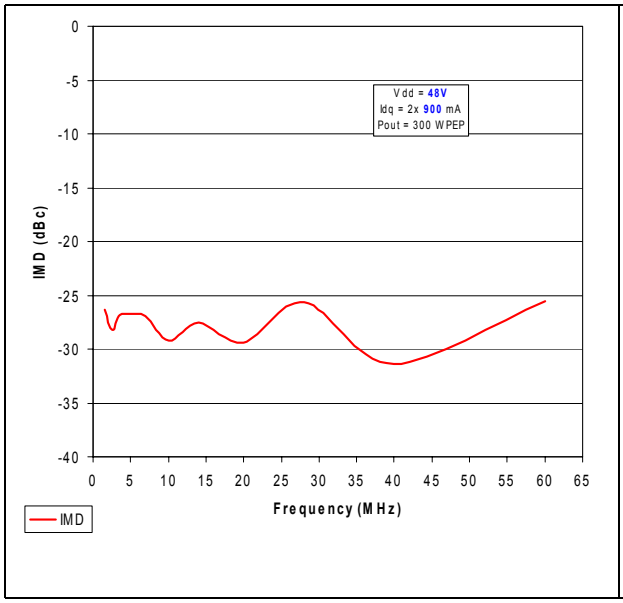


Figure 4. Output power vs drain voltage

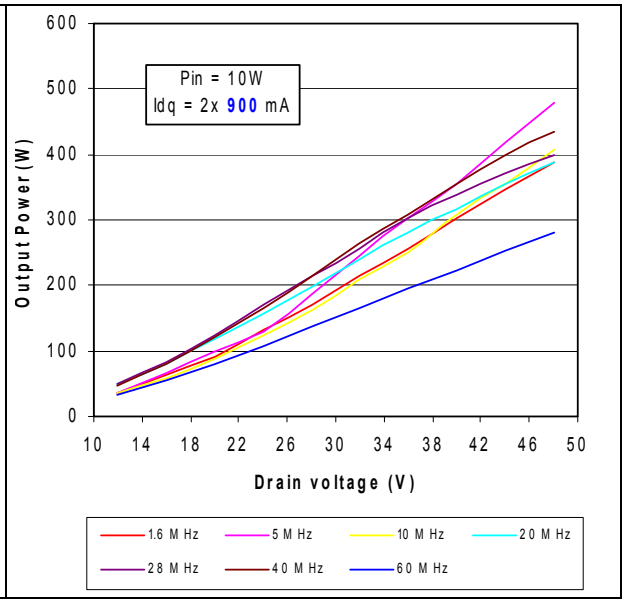
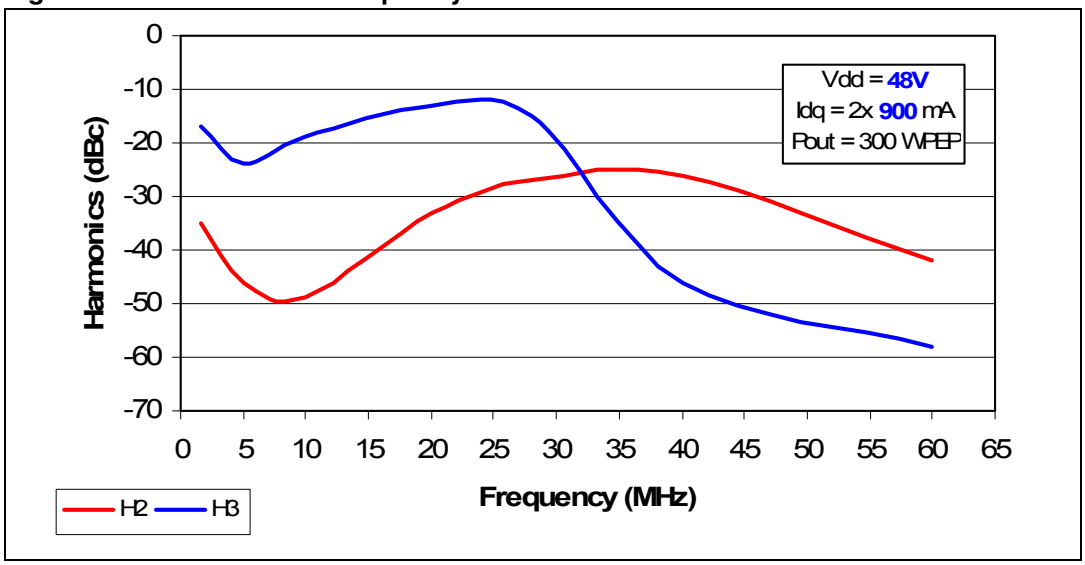


Figure 5. Harmonics vs frequency



4 Photos of DB-2933-54 amplifier

Figure 6. Top view

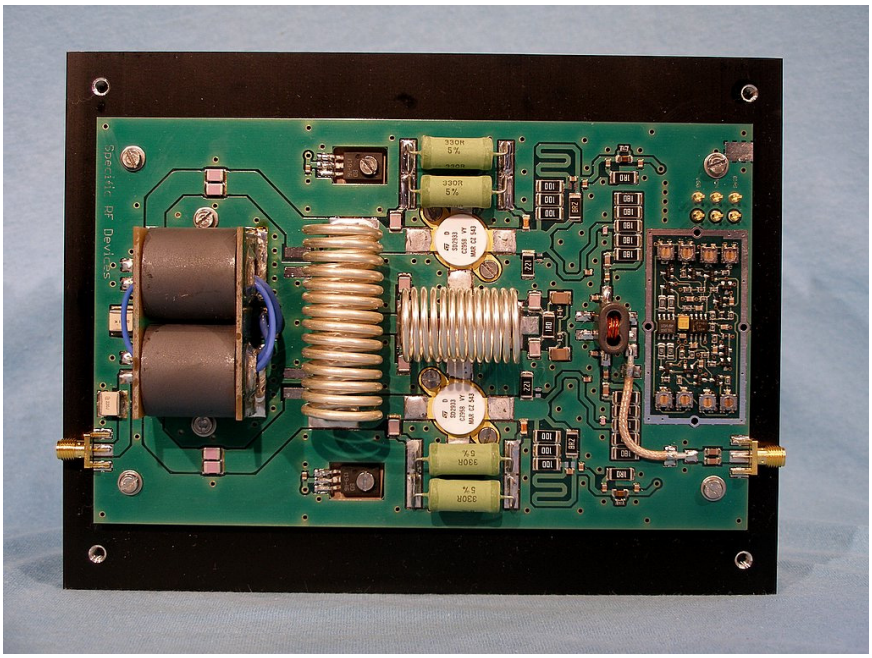
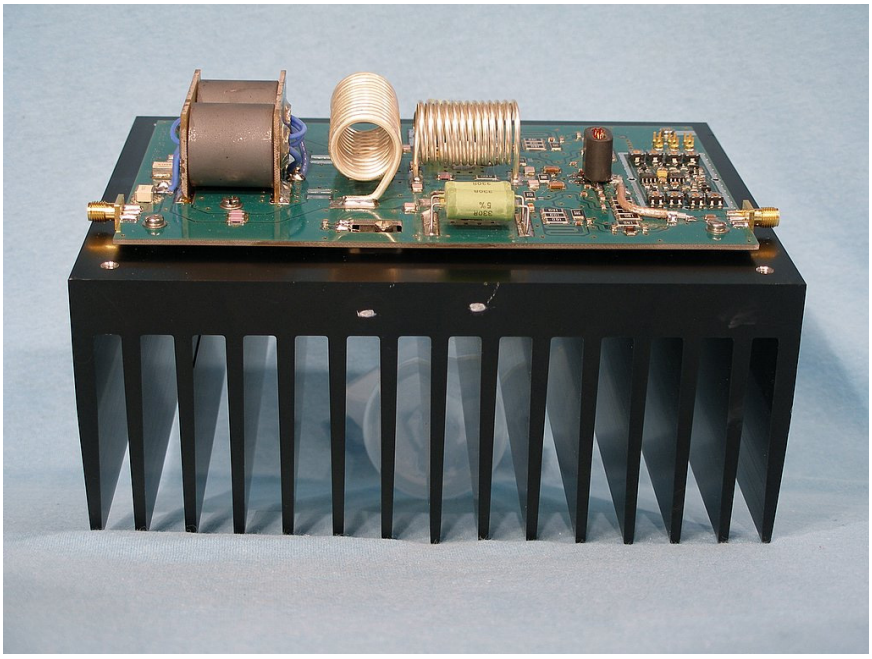


Figure 7. Side view



5 DB-2933-54 class of operation

- class B : a low bias point with ~100mA per transistor
- class AB : a higher bias point with ~ 900mA per transistor

To select a bias point, DB-2933-54 has a control port “BIAS”.

- The bias point is 2x 100 mA if “BIAS” is left open and in this case a DC voltage of ~5V is present
- The bias point is 2 x 900 mA if “BIAS” is connected to ground.

"PA_ON" control port / ON-OFF bias current

- To switch-on biasing circuit, connect “PA_ON” to ground.
- To switch-off biasing circuit, left open “PA_ON”

6 SD2933 mounting recommendations

6.1 Mounting recommendations

- Ensure holes in heatsinks are free from burrs;
- Minimum depth of tapped holes in heatsinks is 6 mm;
- Use 4-40 UNC-2A cheese-head screws with a flat washer to spread the joint pressure;
- The minimum flatness of the mounting area is 0.02 mm;
- Mounting area roughness should be less than 0.5 µm (micro);
- Avoid, as much as possible, use of flux or flux solutions because flux can penetrate even when hermetically sealed ceramic-capped transistors. Tin and wash the printed-circuit board BEFORE mounting the power transistors, then solder the transistor leads without using flux;
- Transistor leads may be tinned by dipping them full-length into a solder bath at a temperature of about 230°C. No flux should be used during tinning;
- Recommended heatsink compounds : WPSII (silicon free) from Austerlitz Electronics, 340 from Dow Corning etc.

6.2 Mounting sequence

- Apply a thin layer of evenly distributed heatsink compound to the flange;
- Position the device with flat washers in place;
- Tighten the screws until finger tight (0.05 Nm);
- Further tighten the screws until the specified torque is reached;
- For M174, M177 & M244 type of packages, torque should be minimum 0.6 Nm and 0.75 Nm max.

Table 3. DMOS Packages - List of materials

Package Type	Description	Flange	Leadframe	Ceramic insulator	Plating		Torque (Nm)	
					Leads	Flange	Min	Max
M174	0.500 DIA 4L NON HERM W/FLANGE	Cu	ALLOY 42 (Fe58 / Ni42)	BeO (99.5% min)	Au (100µ min) over Ni (100µ min / 350µ max)	Ni(100µ min) + Pd (10µ min)	0.6	0.75
M174 (Moly disk)	0.500 DIA 4L NON HERM W/FLANGE (MOLY DISK)	Cu-Mo-Cu	ALLOY 42 (Fe58 / Ni42)	BeO (99.5% min)	Au (100µ min) over Ni (100µ min / 350µ max)	Ni(100µ min) + Pd (10µ min)	0.6	0.75
M177	0.550 DIA 4L NON HERM W/FLANGE	Cu-Mo-Cu	ALLOY 42 (Fe58 / Ni42)	BeO (99.5% min)	Au (60µ min) over Ni (100µ min / 350µ max)	Au (100µ min) over Ni (100µ min / 350µ max)	0.6	0.75
M244	2x 0.400x0.425 WIDE 2L LAP N/H FLANGE	W (85%) - Cu (15%)	ALLOY 42 (Fe58 / Ni42)	BeO(99.5 % min)	Au (60µ min) over Ni (100µ min / 350µ max)	Au (60µ min) over Ni (100µ min / 350µ max)	0.6	0.75

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

8 Revision history

Table 4. Revision history

Date	Revision	Changes
19-Oct-2006	1	Initial release

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