AN420
Application note

Expanding A/D resolution of the ST6 A/D converter

1 Introduction

Occasionally the analog signal provided by external sensors require an Analog to Digital conversion with a resolution of greater than 8 bits. In order to extract the full information for subsequent data processing within the microcontroller a higher resolution Analog to Digital is thus required.

The solution described in this note enables this higher resolution with the on-chip 8-bit A/D converter of the ST62, using only an additional Operational Amplifier (OpAmp) and a few resistors

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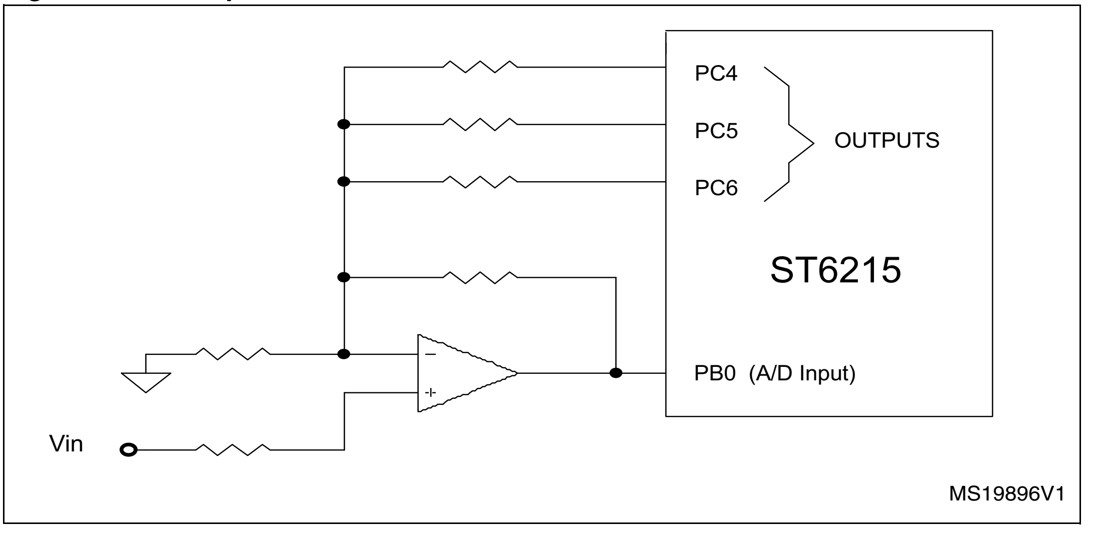
2 Overview

The technique implemented is that of the Algebraic Adder, a full discussion of the principle of operation is included in this note.

A practical example of the external components used is shown in the following figure:

Figure 1. Example circuit



The resistances are selected by the ST62 I/O pins depending on the analog input voltage.

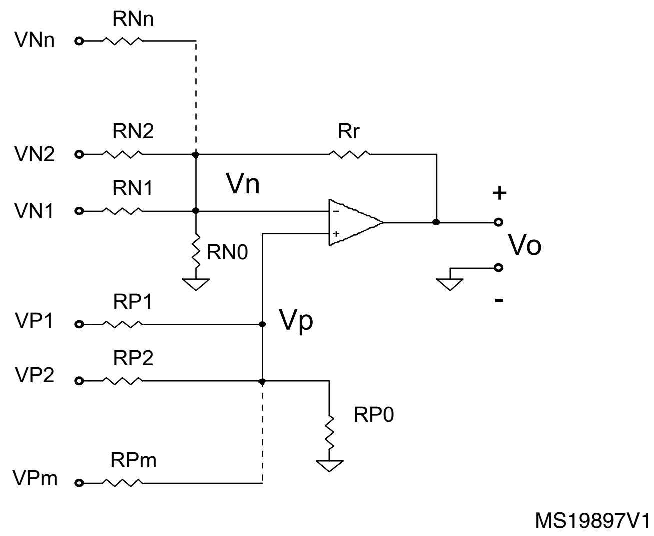
The selection programmed modifies the output voltage of the OpAmp in such a way that the following A/D conversion is always made with the maximum input range of the converter.

This selection is made by software, therefore the total conversion time is increased versus a normal 8-Bit conversion, however the precision is increased and the input voltage range can be enlarged.

3 Principle of operation of an algebraic adder

Figure 2 represents the generic algebraic adder.

Figure 2. Generic algebraic adder



The circuit generates an output voltage equal to: *i*

(1)

$$V_0 = \sum_{i=1}^{m} K_i \times V_{P_i} - \sum_{i=1}^{n} K_i \times V_{N_j}$$

To minimize the effects of the input polarizing currents, the total resistances seen from the two inputs of the OpAmp should be the same. Therefore:

(2)

$$\frac{1}{R_r} + \frac{1}{R_{N_0}} + \sum_{j=1}^{n} \frac{1}{R_{N_j}} = \frac{1}{R_{P_0}} + \sum_{i=1}^{m} \frac{1}{R_{P_i}} = \frac{1}{R_T}$$

The two resistances RP0 and RN0 are needed to satisfy the above relation. In general, only one of them will be needed.

To analyze the circuit, let us calculate the input voltages:

$$V_P = \frac{\sum_{i=1}^{m} G_{P_i} \times V_{P_i}}{G_{P_0} + \sum_{i=1}^{m} G_{P_i}} \qquad \text{where} \qquad G_x = \frac{1}{R_x} \tag{3}$$

$$V_n = \frac{V_0 \times G_R + \sum_{j=1}^{n} G_{N_j}}{G_{N_0}} \tag{4}$$

Relation (2) becomes:

$$G_{N_0} + G_R + \sum_{j=1}^{n} G_{N_j} = G_{P_0} + \sum_{j=1}^{m} G_{P_j} = G_T \tag{5}$$

From 3, 4 and 5 we get:

$$V_0 = -\sum_{j=1}^{n} V_{N_j} \times \frac{R_r}{R_{N_j}} + \sum_{i=1}^{m} V_{P_i} \times \frac{R_r}{R_{P_i}} \tag{6}$$

Relation (6) is the relevant formula to be used. It also explains the name given to this circuit, since the output voltage is the 'algebraic sum' of the input voltages. To design the actual circuit, you chose one value of Rr (arbitrarily). The other resistances are then determined by the desired coefficients:

$$K_i = \frac{R_r}{R_{P_i}} \qquad K_j = \frac{R_r}{R_{N_j}} \tag{7}$$

Finally, the values for R_{N0} and R_{P0} are chosen, based on (2).

4 Example

Let us assume we have a voltage swing of 10 volts (0 to 10) that we want to convert with a 10-bit resolution. And let us assume we have a set of voltage sources VNj that we can switch between 0 to 5 volts under software control, and each one independently from the other.

Let us also assume we can 'cut' the 10 volt swing in 4 'pieces' of 2.5 volts each, and that every 'piece' can be converted with 8-bit resolution. The overall resolution will therefore be:

2^8 (ST6 A/D resolution) * 2^2 (# of 'pieces') = 2^{10}

Let us call V_{in} the actual value of the source to be converted. For instance, if V_{in} ε [10, 7,5] volts, we could supply the ST6 A/D with the voltage:

$(V_{in}\text{-}7.5\text{volt})x2 => \varepsilon[0,5]\text{volt}$

or, for (10,7.5) volts:

$(V_{in}\text{-}1.5xV_{N1})x2 = 2xV_{in}\text{-}3xV_{N1}$

where V_{N1} is one of the V_{Nj} sources, either 0 or 5 volts. In similar fashion, for the other intervals, we could obtain:

(7.5, 5) volts

$(V_{in}\text{-}V_{N2})x2 = 2xV_{in}\text{-}2xV_{N2}$

(5, 2.5) volts

$(V_{in}\text{-}0.5xV_{N3})x2 = 2xV_{in}\text{-}V_{N3}$

(2.5, 0) volts

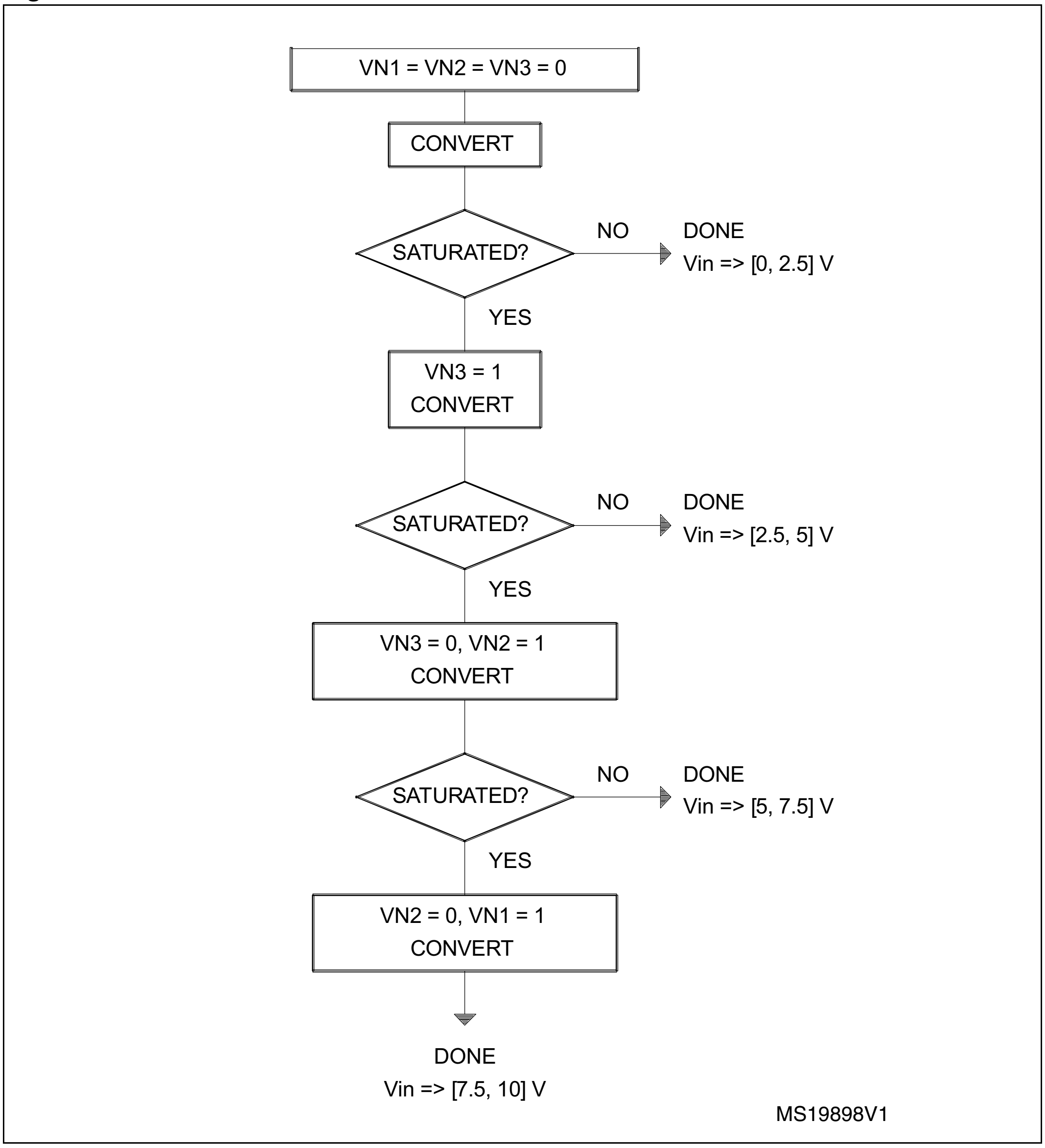
$(V_{in}\text{-}0xV_{N4})x2 = 2xV_{in}$

So, relation (6) becomes:

$V_0 = 2xV_{in}\text{-}3xV_{N1}\text{-}2xV_{N2}\text{-}V_{N3}$ where $V_{in} = V_{P1}$

The software driving the conversion will therefore verify if, given a certain status of the V_{Nj} voltages, the conversion is far from being saturated. If so, another try will be performed with a different status of the V_{Nj} voltages. Figure 3 gives the flow chart of such software.

Figure 3. Conversion routine



The actual circuit values are calculated as follows. With arbitrarily chosen Rr equal to 10 KΩ, the other resistor values are given by:

$$\frac{R_r}{R_{P1}} = 2 \Rightarrow R_{P1} = 5000\Omega$$

$$\frac{R_r}{R_{N1}} = 3 \Rightarrow R_{N1} = 3333\Omega$$

$$\frac{R_r}{R_{N2}} = 2 \Rightarrow R_{N2} = 5000\Omega$$

$$\frac{R_r}{R_{N3}} = 1 \Rightarrow R_{N3} = 10\Omega$$

To satisfy relation (2), we obtain the following values, as indicated in *Figure 4*.

$$\frac{1}{R_r} + \frac{1}{R_{N0}} + \frac{1}{R_{N1}} + \frac{1}{R_{N2}} + \frac{1}{R_{N3}} + \frac{1}{R_{N0}} + 0.0007$$

$$\frac{1}{R_{P0}} + \frac{1}{R_{P1}} = \frac{1}{R_{P0}} + 0.0002$$

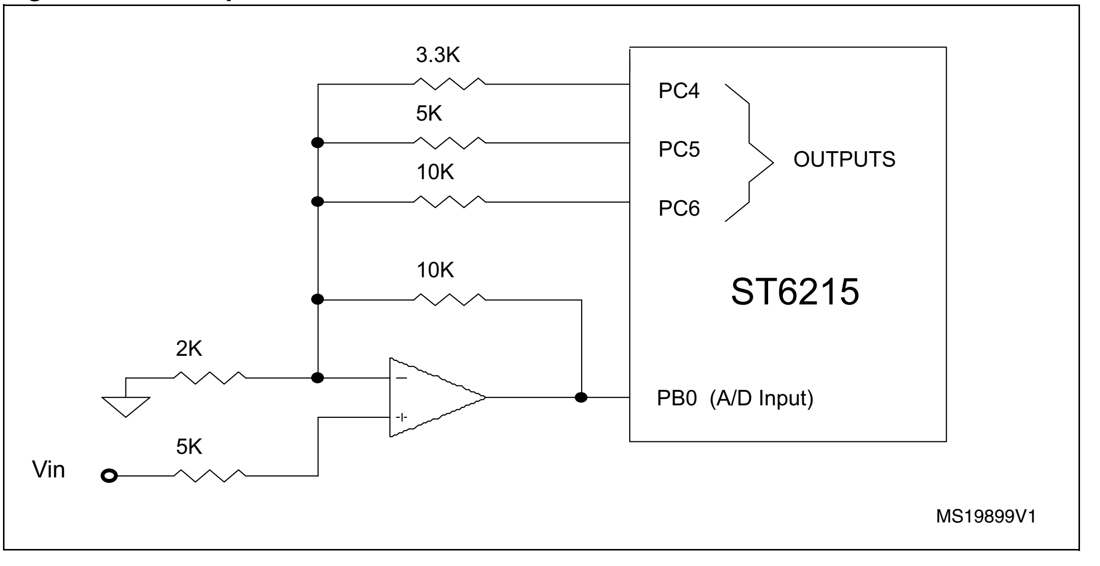
$$\frac{1}{R_{N0}} + 0.0007 = \frac{1}{R_{P0}} + 0.0002$$

$$\text{Assuming } \frac{R}{P0} = \infty \Rightarrow R_{N0} = 2K\Omega$$

5 Application example

An example ST62 software program follows on the next pages. It executes the program flow of *Figure 3* in the application circuit of *Figure 4*.

Figure 4. Example circuit



The ST6215 pin allocation is arbitrary. The three outputs can drive other identical circuits, when more the one 10-bit A/D channel is needed. Also, a different number of 'pieces' can be used to achieve a different resolution.

```
;*********************************************************************************
;* File name: HIRES_AD.ASM
;*
;* ALGEBRAIC ADDER AND ST6 A/D CONVERTERS - Application note software
;* This software is an example on how to increase the ST6 converter
;* resolution. Please refer to the application note for further
;* explanations.
;*
;* Allocation of pins: PC4, PC5 and PC6 are, respectively, voltage sources
;* VN1, VN2 and VN3. PB0 is an A/D input
;*
;*********************************************************************************
          .input "6215_reg.asm" ;ST6215 standard definitions file
VN1  .equ 4                    ;PC4 bit select
VN2  .equ 5                    ;PC5 bit select
VN3  .equ 6                    ;PC6 bit select
drcs  .def 0bfh,0ffh,0ffh      ;shadow register for Data Register C
```

```
Hres .def 0bdh,0ffh,0ffh    ;MS 2 bits of conversion result, and
                            ;conversion flag

conv_f .equ 7;the MSB of Hres is the high resolution

                            ;end of conversion flag

c1 .equ 6                    ;conversion step flags

c2 .equ 5

c3 .equ 4

c4 .equ 3                   ;using Hres

Lres .def 0beh,0ffh,0ffh    ;LSB of conversion result

;************************** N O T E ***********************************************

;register W is used to save the accumulator contents

;in standard interrupt routines

;*********************************************************************************

          .org 880h         ;one module only. Do not use this

                            ;assembly directive if you organize

                            ;your software in linkable modules

init ldi drb,1

          ldi orb,1 ;PB0 is analog input

          ldi ddrc,070h ;PC4..6 are open drain outputs

          ldi orc,070h ;PC4..6 are push-pull outputs now

          ldi drcs,0 ;assume PC7 is input with pull-up,

                            ;no interrupt

          ldi ior,10h ;enable interrupts

          ldi Hres,0

          reti ;initialize interrupt machine

conv                         ;this is an endless loop converting

                            ;PB0 input with 10-bit resolution

                            ;the first time here after reset,

                            ;VN1=VN2=VN3=0

          set conv_f,Hres

          set c1,Hres

          set 5,adcr ;start high resolution conversion

          jrs conv_f,Hres,$

          nop ;here the high resolution result is

                            ;available in Hres-Lres

          jp conv

adcint

          ld w,a ;save accumulator

          ld a,adr ;in accumulator conversion result

          jrs c1,Hres,c1conv
```

```
            jrs c2,Hres,c2conv
            jrs c3,Hres,c3conv
c4conv      ldi Hres,3
            ld Lres,a
            ld a,drcs
            res VN1,a
            ld drcs,a
            ld drc,a          ;VN1=VN2=VN3=0
            jp convout
c1conv      pi a,0ffh
                              jrnz c1c1
lr Hres
            ld Lres,a
convout     d a,w
            reti
c1c1        ld a,drcs
            set VN3,a
            ld drcs,a
            ld drc,a          ;VN1=VN2=0, VN3=1
            set 5,adcr         ;start conversion
            res c1,Hres
            set c2,Hres
            jp convout        ;exit interrupt
c2conv      cpi a,0ffh
            jrnz c2c1
            ldi Hres,1
            ld Lres,a
            jp convout
c2c1        ld a,drcs
            res VN3,a
            set VN2,a
            ld drcs,a
            ld drc,a           ;VN1=VN3=0, VN2=1
            set 5,adcr         ;start conversion
            res c2,Hres
            set c3,Hres
            jp convout        ;exit interrupt
c3conv      cpi a,0ffh
            jrnz c3c1
```

```
                ldi Hres,2
                ld Lres,a
                jp convout
c3c1            ld a,drcs
                res VN2,a
                set VN1,a
                ld drcs,a
                ld drc,a           ;VN2=VN3=0, VN1=1
                set 5,adcr         ;start conversion
                res c3,Hres
                set c4,Hres
                jp convout         ;exit interrupt
                .org 0ff0h
                jp adcint         ;A/D interrupt vector
                .org 0ffeh
                jp init ;reset vector
                .end
```

6 Revision history

Table 1. Document revision history

Date	Revision	Changes
21-Dec-1992	1	Initial release.
02-Nov-2011	2	Updated format and company logo.