AN4086
Application note

Buck voltage regulator using the PM8903

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Introduction

The PM8903 is a compact, high-efficiency, monolithic step-down switching voltage regulator which can deliver up to 3 A of continuous current. The IC minimizes external components and board space by incorporating low-resistance MOSFETs into the IC. It is used in applications including CPU, DSP and FPGA power supplies, distributed power supplies, and for general DC/DC converters. The following features are incorporated:

- Input voltage range of 2.8 V to 6 V
- Adjustable output voltage to as low as 0.6 V
- PSKIP mode for optimizing efficiency at light load
- Undervoltage, overvoltage, overcurrent, and overtemperature protection
- Power Good output
- 1.1 MHz switching frequency which enables the use of a small inductor
- Low quiescent current when shut down (<15 µA)
- Interleaving synchronization (up to two ICs)
- Small VFQFPN16, 3x3 mm package

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  In *Equation 1* below, the output voltage is programmed by R_{OS} and R_{FB} using the formula:

Equation 1

$$R_{OS} = R_{FB} * V_{REF} / (V_{OUT} - V_{REF})$$

where V_{REF} is 0.6 V and R_{FB} is selected to obtain the desired regulator bandwidth (see section 6.1 of datasheet for details).

- Inductor selection

  Choosing an inductor involves a compromise between dynamic response, efficiency, cost and size. A higher inductor value will decrease the output voltage ripple, but will increase the regulator response time to load changes.

  The inductance has to be calculated to keep the ripple current (ΔI_L) between 20% and 30% of the maximum output current, using the following equation:

Equation 2

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

where F_{SW} is the switching frequency, V_{IN} is the input voltage, and V_{OUT} is the output voltage.

- Output capacitor selection

  The output capacitor bank will define the ripple voltage and affect the transient response of the regulator.

  During steady state operation, the output voltage ripple is affected by the ESR and the capacitance value according to the following equations:

Equation 3

$$\Delta V_{OUT\_ESR} = \Delta I_L \cdot ESR$$

Equation 4

$$\Delta V_{OUT\_C} = \Delta I_L \cdot \frac{1}{8 \cdot C_{OUT} \cdot F_{SW}}$$

where ΔI_L is the inductor current ripple.

During a load transient, the output capacitor bank either supplies the load current, or absorbs the energy stored in the inductor until the regulator reacts. The output voltage drop that depends on the ESR (equivalent series resistance) and on the capacitive charge/discharge is calculated according to the following:

Equation 5

$$\Delta V_{OUT\_ESR} = \Delta I_{OUT} \cdot ESR$$

$$\Delta V_{OUT\_C} = \Delta I_{OUT} \cdot \frac{L \cdot \Delta I_{OUT}}{2 \cdot C_{OUT} \cdot \Delta V_L}$$

where ΔI_L is the voltage across the inductor during the transient load [$D_{MAX} \cdot (V_{IN} - V_{OUT})$ for a load application or V_{OUT} for load release.

MLCC capacitors typically have low ESR which is good to minimize the voltage ripple, but they have low capacitance. Electrolytic capacitors have larger capacitance, which is good for minimizing voltage changes during transients, but they also have higher ESR than MLCC capacitors.

Ideally, a mix of electrolytic and MLCC capacitors can be used for minimal ripple as well as minimizing voltage changes during transient loads.

- Input capacitor selection

  The major consideration when choosing an input capacitor is the input RMS current, which depends on the output current (I_{OUT}) and the duty cycle (D) according to the following:

Equation 6

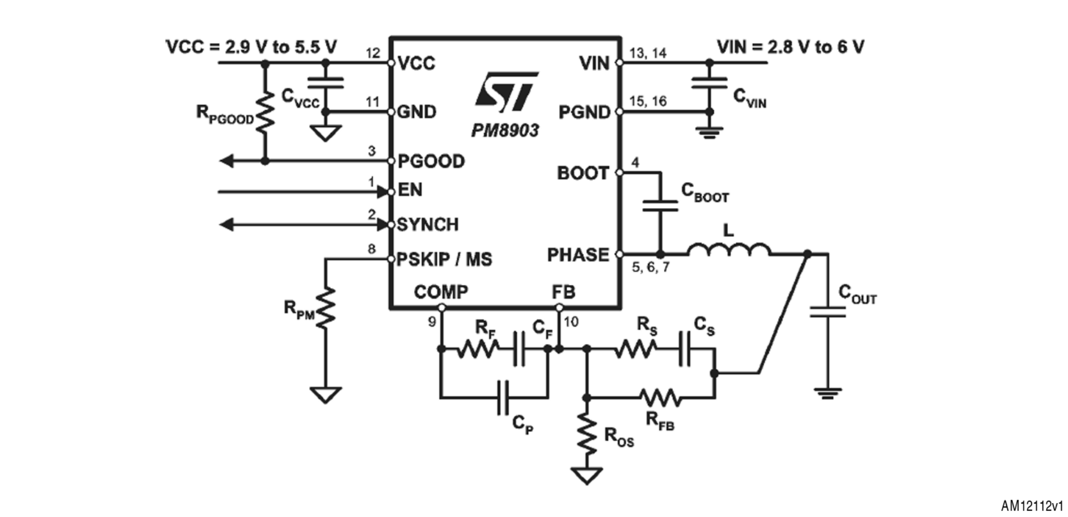
$$I_{RMS} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

Maximum I_{RMS} occurs when D = 0.5, when $I_{RMS} = \frac{I_{OUT}}{2}$.

Make sure the capacitor RMS current rating is well above the maximum operating RMS current of the regulator. For long-term reliability, a good rule of thumb is to choose a capacitor that will exhibit less than a 10 °C rise in temperature at max RMS current. Most capacitor datasheets have plots that show RMS current vs. temperature.

Another consideration is the input ripple voltage - which is caused by the ESL (equivalent series inductance) and ESR of the input capacitor and the dV/dt of the switch node. Using low ESR and ESL ceramic capacitors are effective for lowering input ripple voltage.

Figure 1. PM8903 schematic



- Design tip for input voltages of 5 V to 6 V

  For a 5 V input, the maximum rated voltage at the phase pin is 7 V. For a 6 V input, the maximum rated voltage is 7.5 V with t < 100 ns.

  If you use a 5 V to 6 V input voltage, the maximum voltage at the phase node should be measured at maximum load. This measurement should be taken on the phase node pin, using the full bandwidth setting on the oscilloscope and as short a ground as possible on the probe. If measured voltage exceeds 7 V, an R/C snubber circuit should be implemented at the phase node, as shown in *Figure 2*. Also, to be effective, the R/C should be as close as possible to the phase node pin.

Figure 2. R/C snubber circuit

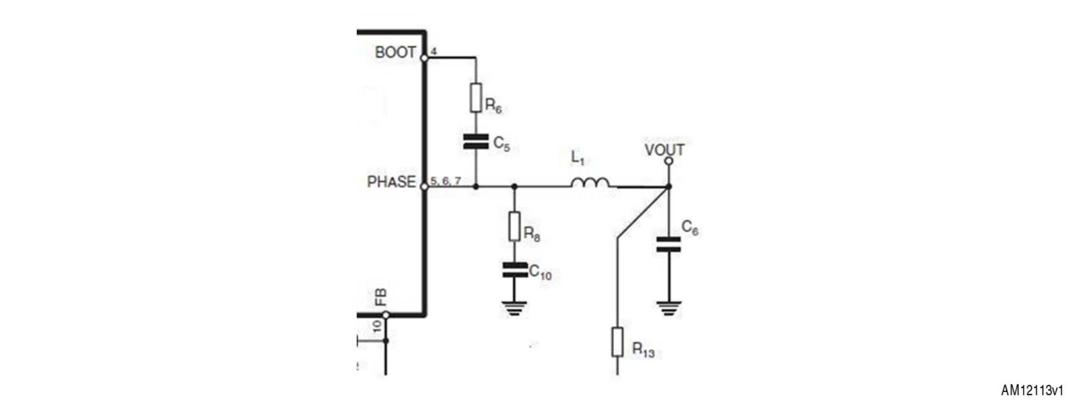


Figure 3. PM8903 demonstration board

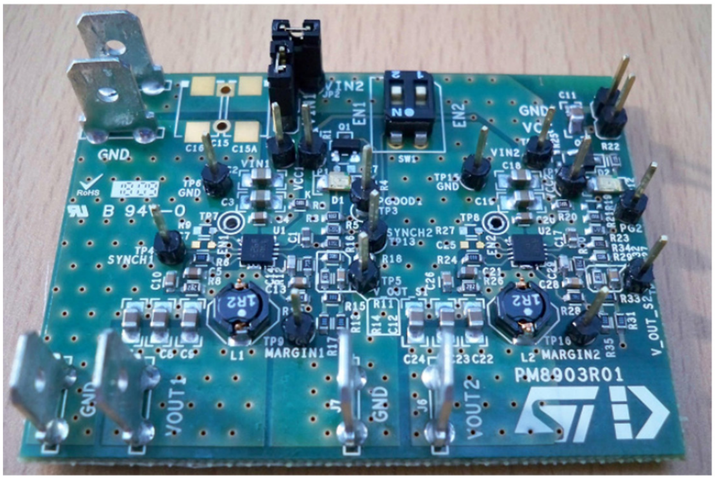


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Figure 4. PM8903 demonstration board efficiency with V_{IN} = 3.3 V, V_{OUT} = 1.5 V, and F_{SW} = 1.1 MHz

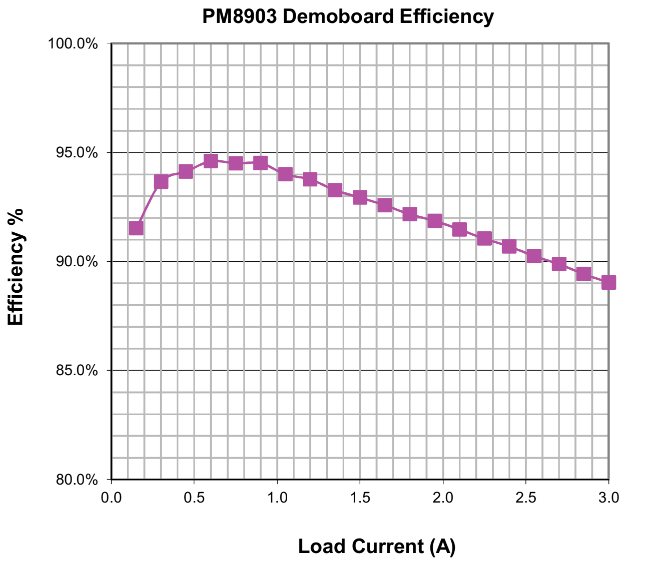

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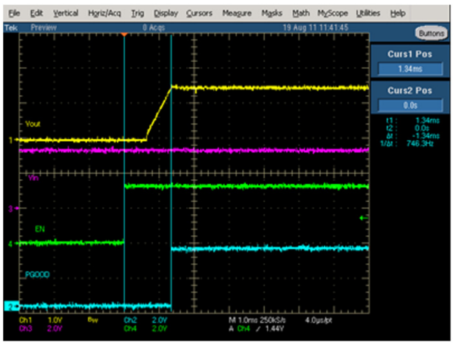
Figure 5. Startup



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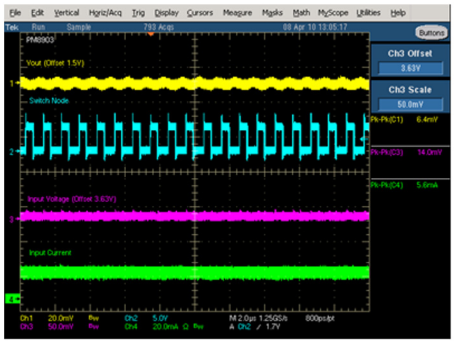
Ch 1: Output voltage
Ch 2: Power Good
Ch 3: Input voltage
Ch 4: Enable

Figure 6. V_{OUT}, V_{IN}, I_{IN} ripple



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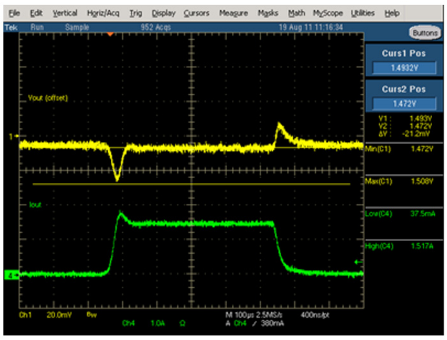
Ch 1: Output voltage ripple
Ch 2: Switch node
Ch 3: Input voltage ripple
Ch 4: Input current ripple

Figure 7. Transient load (0 A to 1.5 A)



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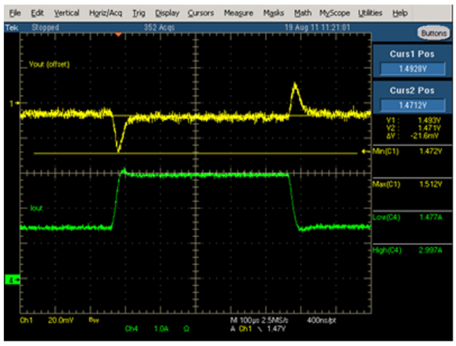
Ch 1: Output voltage (off)
Ch 4: Output current

Figure 8. Transient load (1.5 A to 3 A)



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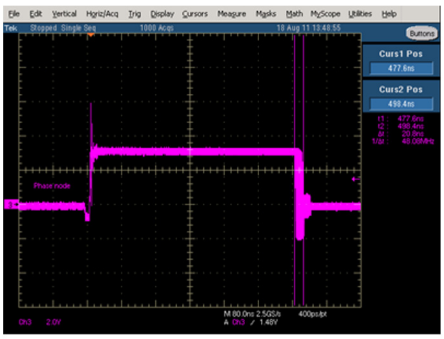
Ch 1: Output voltage (off)
Ch 4: Output current

Figure 9. Duty cycle jitter at 3 A load



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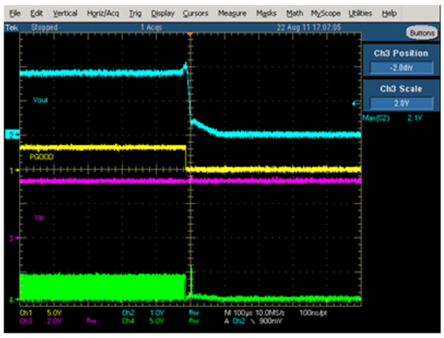
Ch 3: Switch node (persistence mode)

Figure 10. V_{OUT}, V_{IN}, I_{IN} ripple



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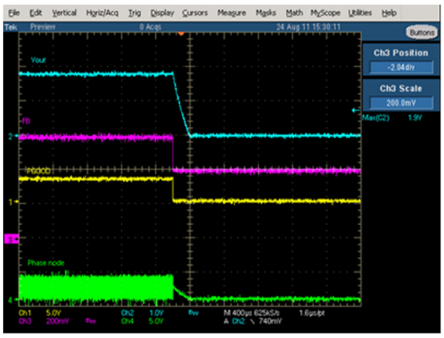
Ch 1: Power Good
Ch 2: Output voltage
Ch 3: Feedback
Ch 4: Switch node

Figure 11. Overvoltage protection



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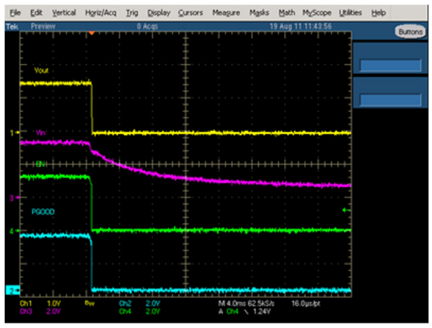
Ch 1: Power Good
Ch 2: Output voltage
Ch 3: Input voltage
Ch 4: Switch node

Figure 12. Shutdown



AM12123v1

Ch 1: Output voltage
Ch 2: Power Good
Ch 3: Input voltage
Ch 4: Enable

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
05-Jun-2012	1	Initial release.