AN3994
Application note

Managing the best in class MDmesh™ V and MDmesh™ II super junction technologies: driving and layout key notes

Introduction

One of the bigger challenges of the 21st century is to deal with the growing need for power and, at the same time, the necessity of product compactness.

The new MDmesh™ V series from STMicroelectronics, based on the super junction concept, meets these targets by offering an extremely low $R_{DS(on)}$ value in a given package, unobtainable in standard HV MOSFETs.

In addition to the dramatic reduction of $R_{DS(on)}$, super junction MOSFETs are extremely fast in transients and this may lead to some issues when a better performing technology replaces an older version on the same board with the same driving network.

The two main components in the ST super junction MOSFET family (MDmesh™ II and MDmesh™ V) are analyzed and compared in terms of energy losses, voltage, and current rates. It is shown how the external driving network impacts on their performances. Furthermore, a separate section is dedicated to the layout parasitic effects and their impact on MOSFET behavior.

It is clear in the end that layout can be crucial, especially when managing very fast transients, and it must be carefully planned in order to help the MOSFET exploit its best potential.

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1 ST multidrain technology evolution

At the beginning of 2000, STMicroelectronics introduced the super junction MOSFET technology to the market, the basic structure of which is clear from *Figure 1*:

Figure 1. Standard HV MOSFET device cross section

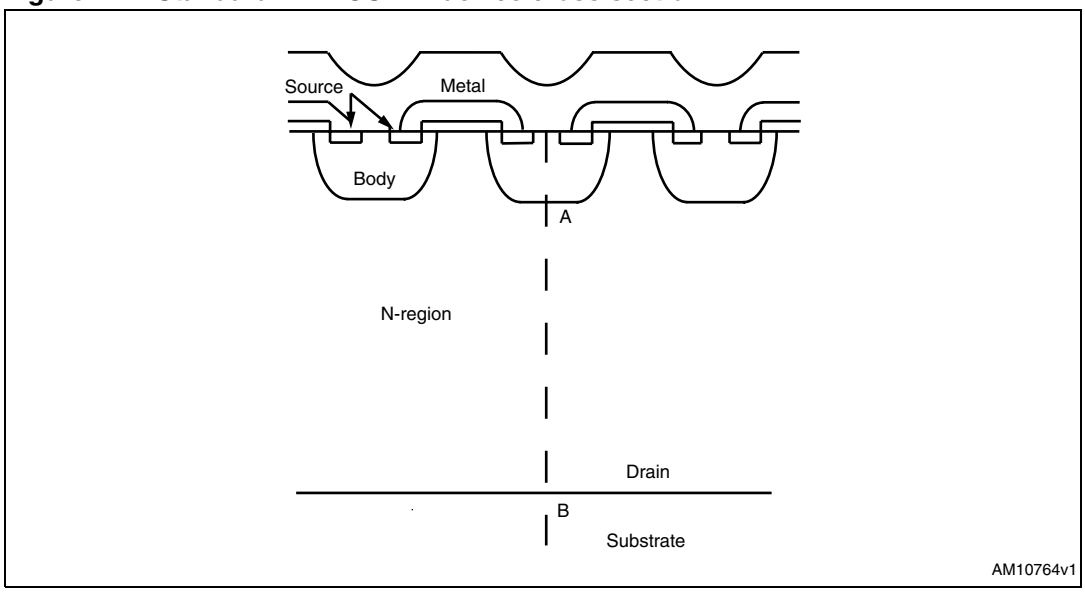
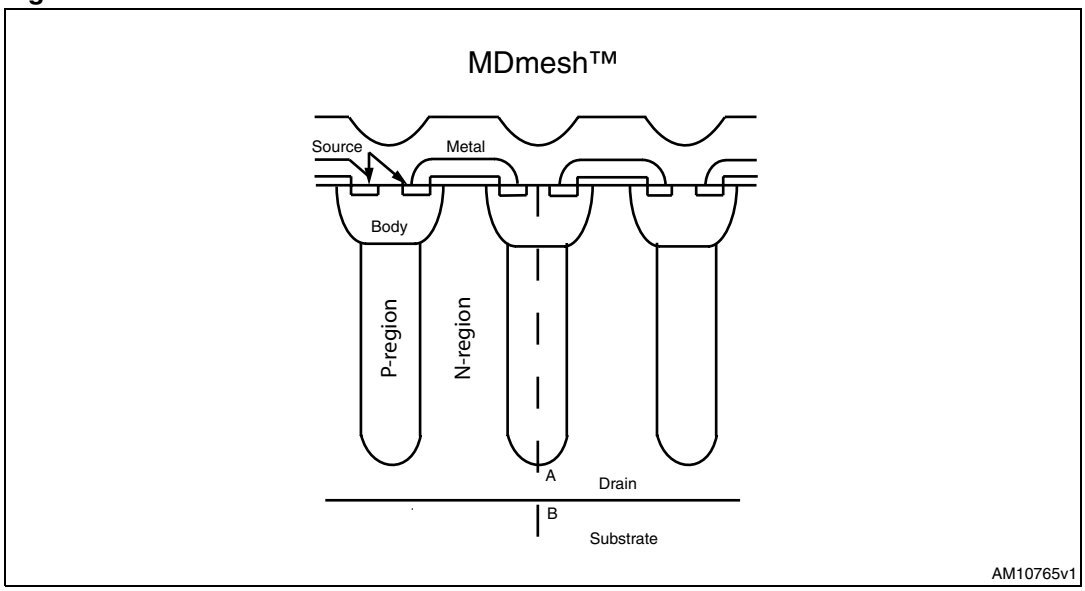
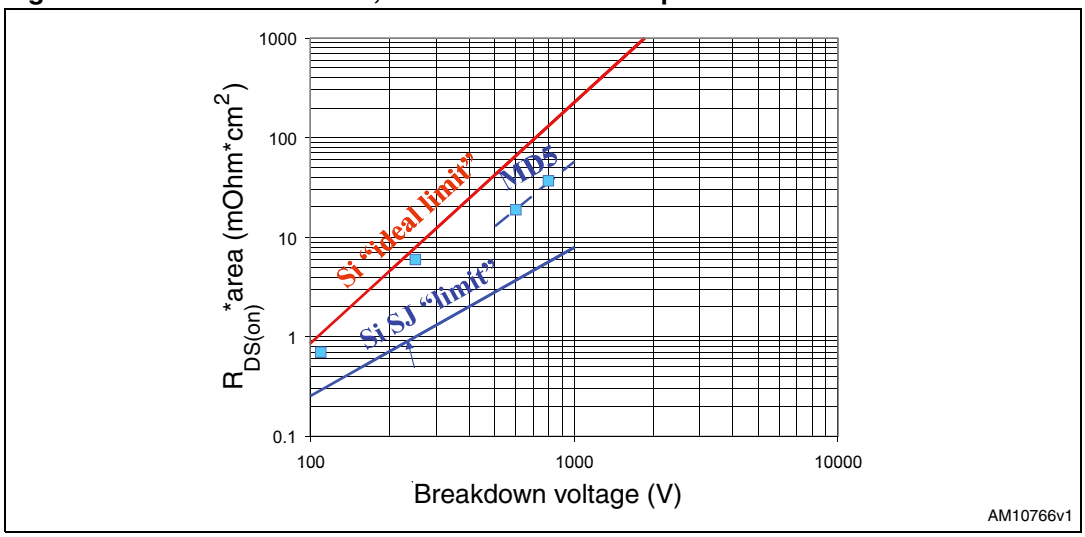


Figure 2. MD device cross section



As concerns standard MOSFET technology, designers understand that $R_{DS(on)} * area$ and breakdown voltage are associated with a theoretical limit which strictly depends on the material and can not be overcome. Development efforts of the major suppliers have mainly focused on making the $R_{DS(on)}*$ area as close as possible to this physical limit, by reducing the most important contributions of a high voltage Power MOSFET to the total $R_{DS(on)}$.

Figure 3. Silicon ideal limit, SJ limit and ST MD V position



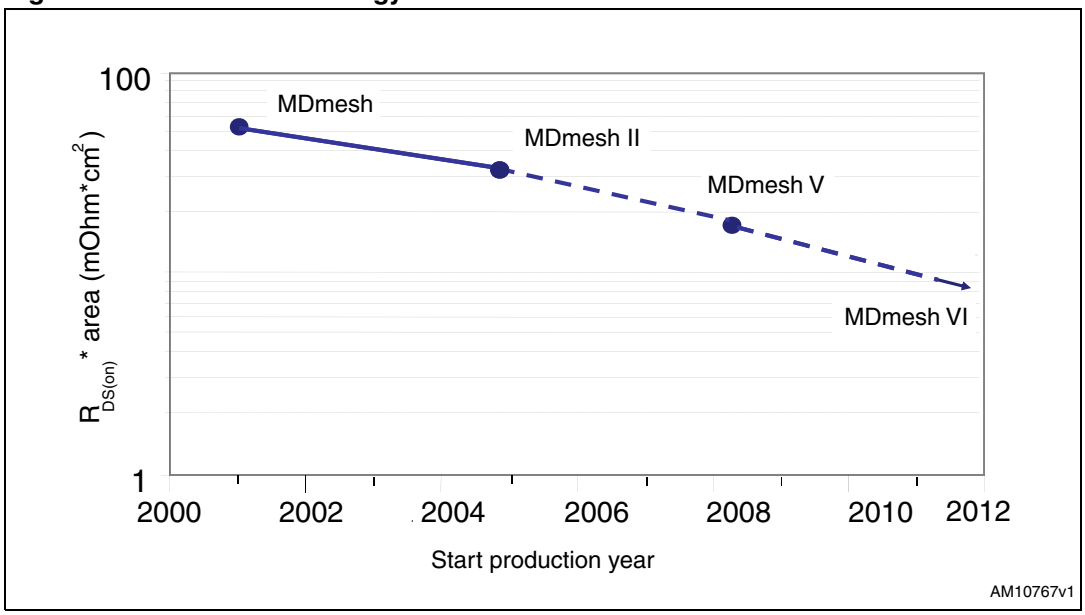
R_{JFET} and $R_{CHANNEL}$ were significantly lowered by increasing the cell density and optimizing their structure, and by also reducing, at the same time, the channel length.

Thanks to the continuos optimization of resistivity and the thickness of N-Drift, the R_{EPY} contribution has been lowered, but the need to guarantee the same breakdown voltage and avalanche capability establishes the well known “Silicon Ideal limit”, as shown in *Figure 3*.

The MD concept, based on SJ technology, has overcome this limit: through the p-doped column insertion under the device strips, it has been possible to significantly lower the resistivity of the epitaxial N region without compromising the breakdown capability and enabling a dramatic reduction in $R_{DS(on)}$: the particular p-column geometry and the alternating of p regions with n regions allows a constant electric field in the whole drain volume despite the low resistivity in the conducting region: as a direct consequence, it was possible to achieve an $R_{DS(on)} * area$ reduction, previously not possible, by keeping the same voltage capability.

From this starting point, MD technology moved towards $R_{DS(on)}$ continuous optimization, as seen in *Figure 4*.

Figure 4. ST's HV technology evolution



The MD II generation has already optimized the $R_{DS(on)}$ * area of about 40% compared to the first MD version, with an average value of about 30 mΩ*cm^2.

The excellent achievement of the MD II enabled STMicroelectronics to establish a new milestone in the power switch arena with the last MD V generation.

Thanks to a proprietary ST technology, an extremely low value of p-column distance has been reached, therefore overcoming the physical limit imposed by the diffusion process. Additionally, the geometry of the p-columns was also optimized by a more effective diffusion process which enabled up to 40% reduction of $R_{DS(on)}$ * area if compared to the previous MD II generation.

2 Parasitic capacitances overview

When dealing with high speed switching applications, the most critical MOSFET parameters limiting its dynamic response are the parasitic capacitances.

Figure 5 shows the physical origin of the parasitic component in an N-channel Power MOSFET:

Figure 5. N-channel Power MOSFET structure and intrinsic capacitances

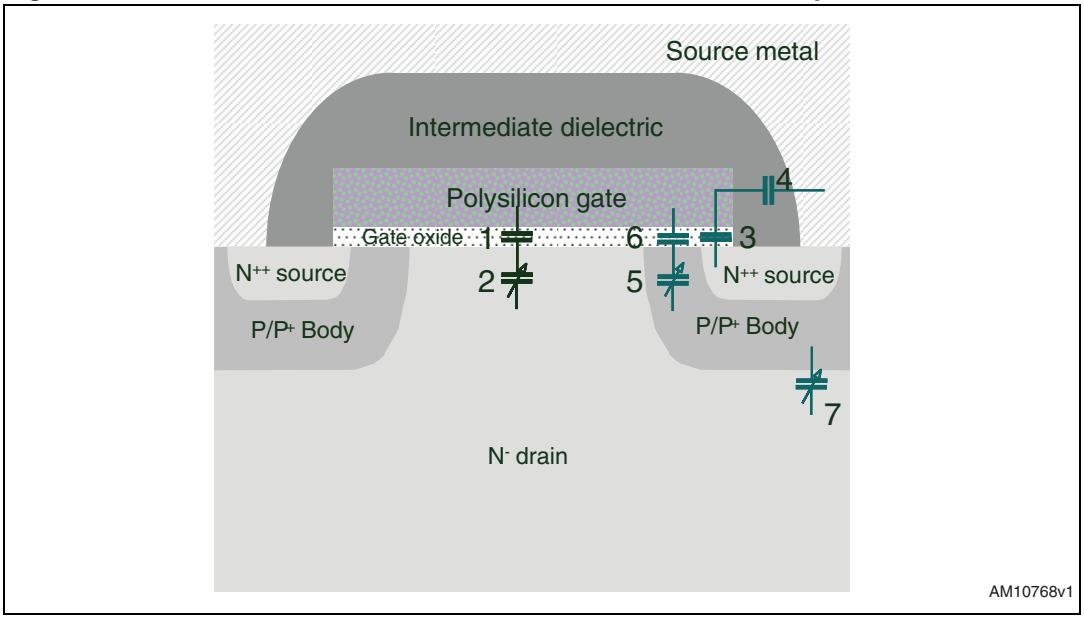
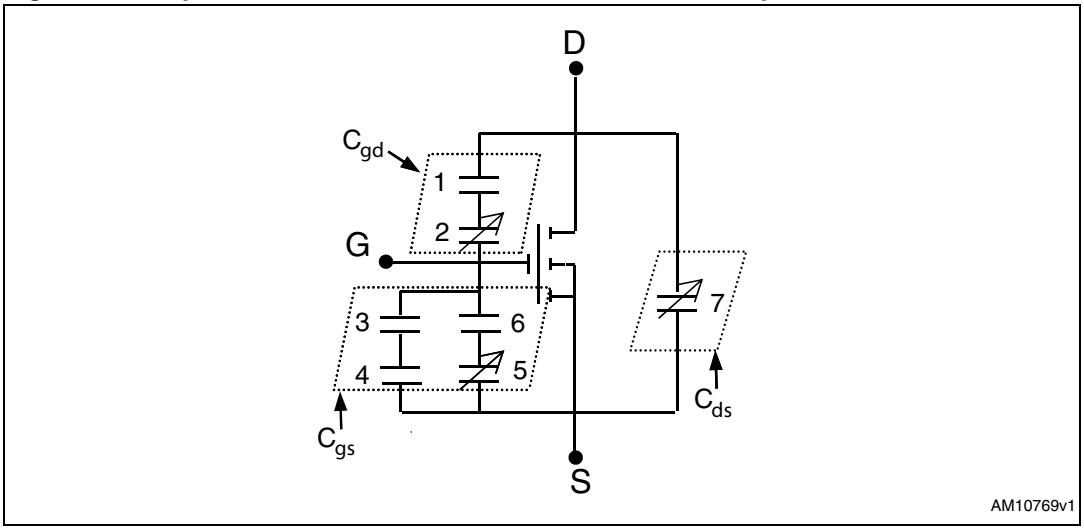


Figure 6. Equivalent model of Power MOSFET intrinsic capacitances



C_{gs} is mainly due to the overlap between the gate and the source metallization (“3” and “4” components in *Figure 5* and *6*). Capacitors “5” and “6” are MIS (metal-insulator-semiconductor) capacitors between the gate and the p-body. The C_{gs} value is linked to the geometry of the device and it's almost independent of the voltage applied.

C_{gd} is the sum of two contributions: the first one is related to the overlap of the JFET region and the gate electrode (“1” component in *Figure 5* and *6*). The second component is the capacitance of the depletion region under the gate (“2” component in *Figure 5* and *6*).

The equivalent capacitance C_{gd} decreases as the drain source voltage applied increases.

C_{ds} capacitance is the junction capacitance of the body-drain diode (“7” components in *Figure 5* and *6*). Its value varies as the p-body / n-drift junction thickness changes with the V_{DS} applied, according to the following formula:

Equation 1

$$C_{ds} \propto (\sqrt{V_{DS}})$$

The relevant datasheets report the static equivalent capacitance values in the electrical characteristics as the following:

Equation 2

$$C_{iss} = C_{gs} \oplus C_{gd} \qquad \text{measured @ } V_{GS}=0\text{ V, } V_{DS}=25\text{ V}$$

Equation 3

$$C_{rss} = C_{gd} \qquad \text{measured @ } V_{GS}=0\text{ V, } V_{DS}=25\text{ V}$$

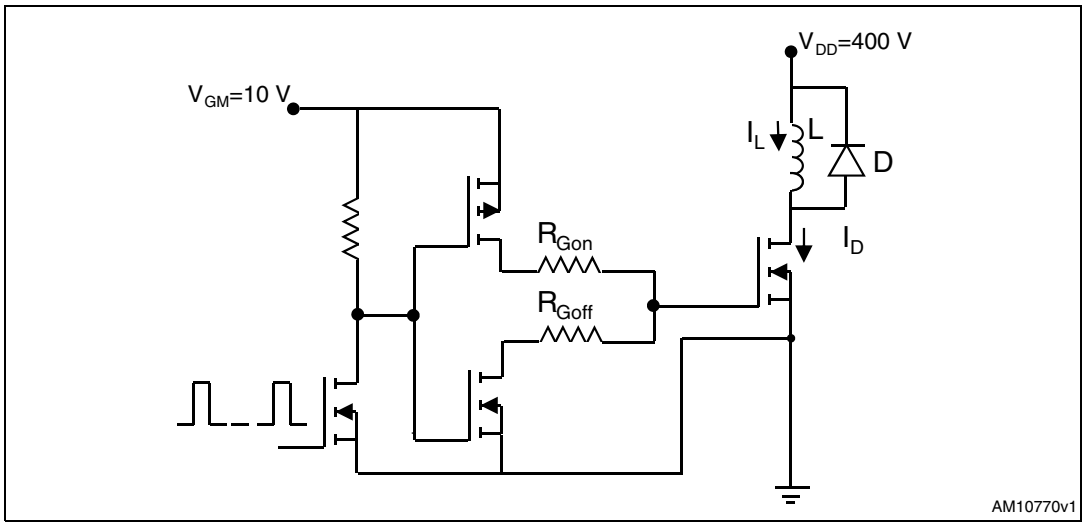
Equation 4

$$C_{oss} = C_{ds} \oplus C_{gd} \qquad \text{measured @ } V_{GS}=0\text{ V, } V_{DS}=25\text{ V}$$

C_{gd} is also called “Miller capacitance”, as it’s placed in the feedback loop between the input and the output of the device. It's value can be much larger in switching operations, contributing to the achievement of a dynamic input capacitance of the MOSFET larger than the sum of the static capacitances.

In order to simplify the switching performance comparison among MOSFETs from different manufacturers or even different MOSFET technologies of the same brand, it can be useful to consider the gate charge parameters instead of capacitances. *Figure 7* shows a clamped inductive load switching test circuit which helps to analyze the parasitic capacitance behavior during the MOSFET switching. The considerations reported in the following sections are valid if the driving source is supposed to provide any Ig current to the MOSFET input capacitances and the circuit is ideal with no stray inductances.

Figure 7. Clamped inductive load test circuit used to carry out the dynamic tests on the MOSFETs



3 MOSFET standard turn-on and turn-off analysis

The turn-on event of the MOSFET can be split into four time intervals, as *Figure 8* shows. The analysis starts from the hypothesis of a constant load current I_L flowing through the inductor L and the diode D before the commutation (turn-on) process.

After the MOSFET input has been connected to the voltage source (V_{SOURCE}=V_{GM}), the V_{GS} voltage starts to increase (PHASE “1”), but no drain current can flow till the V_{GS} reaches the V_{th} value. The MOSFET is still in OFF state, while the diode is conducting the load current. The gate current I_{Gon} is charging the C_{iss} capacitance.

The ON gate current during the t_0 to t_2 time interval follows the exponential trend of *Equation 5*:

Equation 5

$$I_{Gon(t_0,t_2)}(t) = \frac{V_{GM}}{R_{Gtot}} e^{-\frac{t}{R_{Gtot}C_{iss}}}$$

R_{Gtot} theoretically includes the R_{Gon} value (see *Figure 7*) and the other resistive components of the driving circuit.

Equation 6 assumes that the C_{iss} (V_{DS}) is constant during this time interval, which is a correct hypothesis, due to a very low dependence of the input capacitances on the V_{DS} applied.

Phase “2” is the phase of I_D rise. When V_{GS} reaches the threshold value, I_D begins to rise and at the same time, the load current begins to be shared between the diode and the MOSFET. Until the I_D is lower than the load current and the diode is in an ON state, the V_{DS} stays constant at the maximum value except for a little drop in the real voltage waveform due to the stray inductances along the switching circuit. The I_{Gon} current is still charging the C_{gs}+C_{gd} capacitances. At t_2 instant the V_{GS} reaches the plateau value.

The rate of I_D current during the t_1 to t_2 time interval satisfies *Equation 6*:

Equation 6

$$\frac{dI_D}{dt} = \frac{g_m I_{Gon(t_1,t_2)}}{C_{iss}}$$

During phase “3” and phase “4” V_{GS} is at a constant value, I_D has reached the full load condition and the diode is turned off. This enables the V_{DS} to decrease. The MOSFET is in the active region and the I_G current is now flowing only through the C_{gd} capacitance that’s discharging from a starting value of (V_{DS}-V_{PL}), while the C_{ds} capacitance is discharging from V_{DS} down to the $V_{DS(on)}$ value.

The ON gate current during the time interval (t_2 to t_4) is a fixed value and it satisfies *Equation 7*:

Equation 7

$$I_{Gon(t_2,t_4)} = \frac{V_{GM} - V_{PL}}{R_{Gtot}}$$

Figure 8. Turn-on of a MOSFET in a clamped inductive load

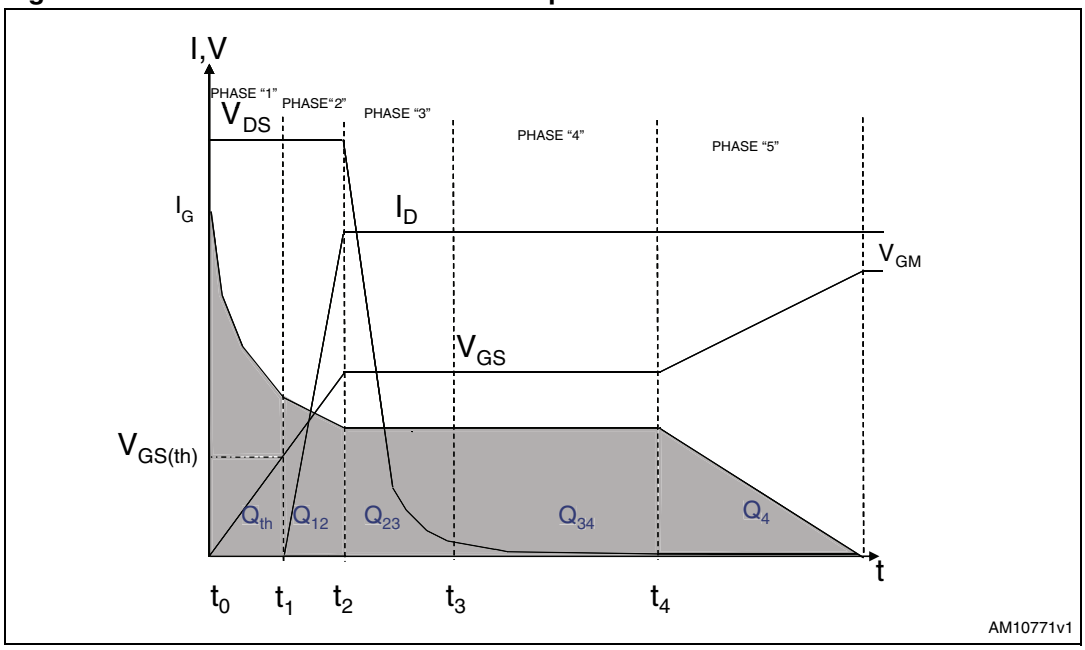
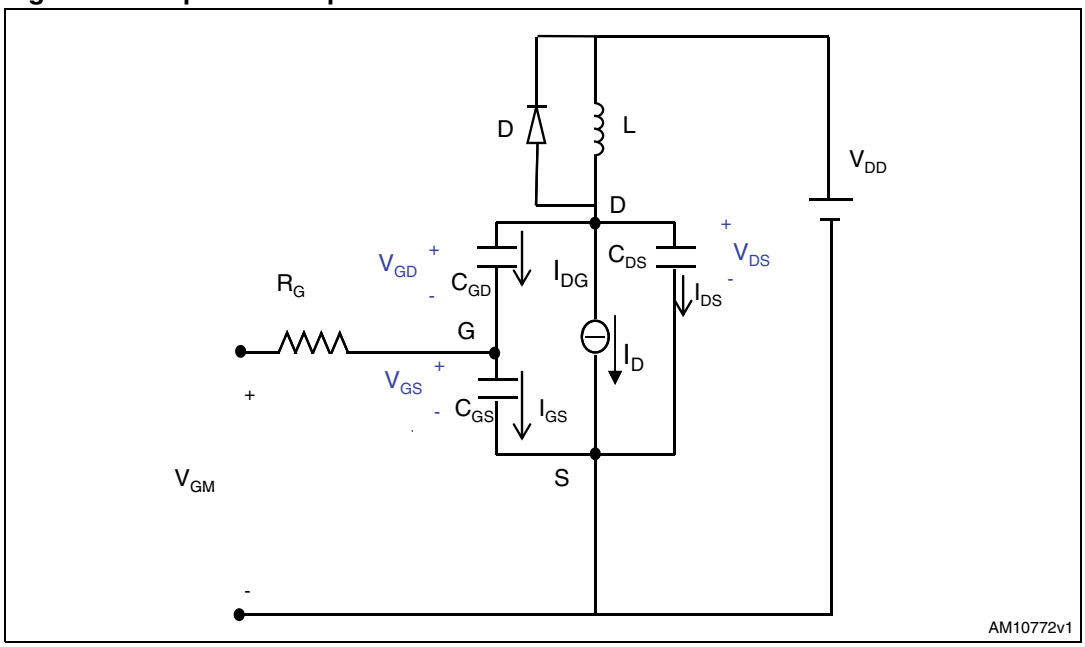


Figure 9. Equivalent capacitive model of a MOSFET



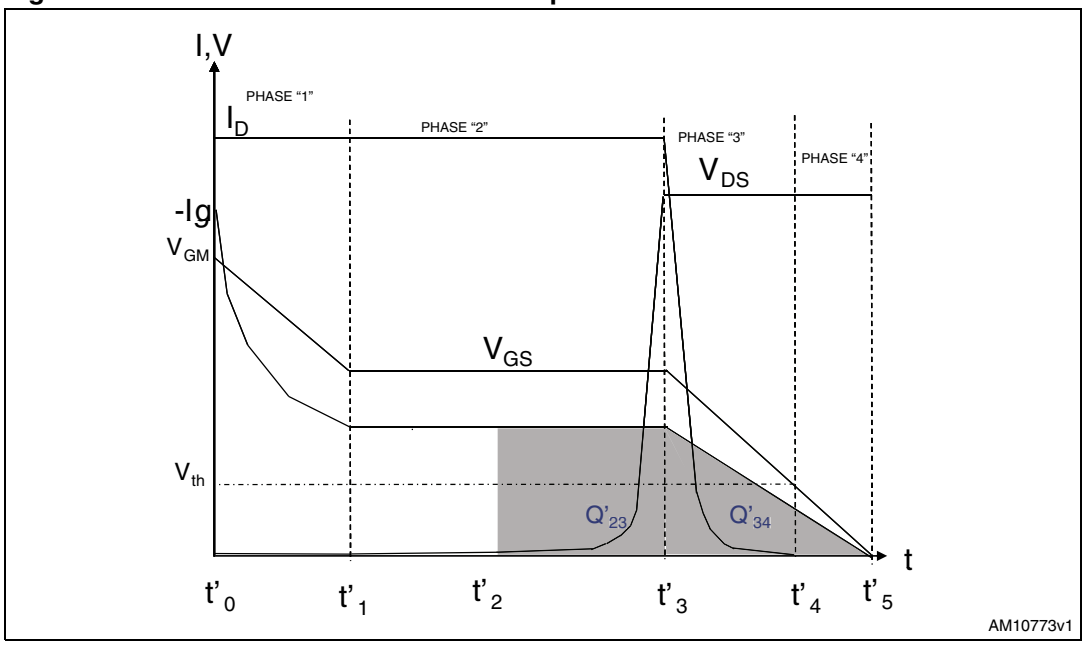
Falling rate of V_{DS} during the (t_2 to t_4) time interval is shown in *Equation 8*:

Equation 8

$$\frac{dV_{DS}}{dt} = \frac{I_{Gon(t_2,t_4)}}{C_{gd}} = \frac{V_{GM} - V_{PL}}{R_{Gtot} \otimes C_{gd}}$$

During phase “4” the voltage across the MOSFET has reached the $I_D*R_{DS(on)}=V_{DS(on)}$ value, and the device has entered the ohmic region. The V_{GS} increases up to the maximum value V_{GM}.

Figure 10. Turn-off of a MOSFET in a clamped inductive load



Similarly, the turn-off event can be split into four time intervals, as shown in *Figure 10*.

Phase “1” is the time interval needed to discharge the input capacitance C_{iss} from its initial value ($+V_{GM}$) down to the plateau level. The gate current is supplied by both C_{gs} and C_{gd} capacitors.

The I_{Goff} current during the time interval (t'_0 to t'_1) follows the same exponential trend of the turn-on during the (t_0, t_2) time interval according to *Equation 9*:

Equation 9

$$I_{Goff(t'_0,t'_1)} = -I_{Gon(t_0,t_2)}$$

During phase “2” the gate voltage has reached a fixed value (the plateau level) and the V_{DS} rises from $I_D*R_{DS(on)}=V_{DS(on)}$ up to the final value, where it is clamped by the diode. As V_{GS} is constant in this time interval, the OFF gate current flowing through the R_{Gtot} is the charging current of the C_{gd} that is charging from a negative starting voltage value (see *Figure 8* for reference) up to the V_{DS} value, while the C_{ds} capacitor is charging up to V_{DS}.

I_{Goff} current during this phase follows *Equation 10*:

Equation 10

$$I_{Goff(t'_1,t'_3)} = \frac{V_{PL}}{R_{Gtot}}$$

Phase “3” is the phase of the diode turn-on: load current begins to be shared between the MOSFET and the diode while the V_{GS} decreases from the plateau down to the V_{th} value.

This causes the lowering of the drain current down to zero. During this time interval, the gate current is mainly coming from the C_{gs} capacitor.

I_{Goff} current during this phase has the following expression:

Equation 11

$$I_{Goff(t'_3,t'_4)}(t) = \frac{V_{PL}}{R_{Gtot}} e^{-\frac{t-t'_3}{R_{Gtot}C_{iss}}} \qquad t>t'_3$$

During phase “4”, the C_{iss} fully discharges and the V_{GS} reaches the zero value.

4 Gate charge curve impact on dynamic responses

When generally dealing with MOSFET turn-on and turn-off, it implies the charging or discharging of its input capacitances. The charge transfer needed to change the voltage across these capacitors leads to unavoidable power losses which are dissipated on the gate resistors in the driving path during each switching cycle. A second but not less significant aspect is that the amount of charge directly impacts how fast the MOSFET response is during transients. For this reason, the gate charge curve analysis displayed in the datasheet is quite important in order to obtain a first outlook of the MOSFET dynamics.

As for the turn-on event, the Q_{th} charge supplied during the t_0 to t_1 (*Figure 8*) time interval is approximately:

Equation 12

$$Q_{th} = C_{iss} \otimes V_{th}$$

As V_{GS} reaches the threshold value, V_{th} and I_D start to flow. The charge to be provided during the (t_1 to t_2) time interval can be calculated by integrating the I_{Gon} (t_1 to t_2) current as follows:

Equation 13

$$Q_{12} = \int_{t_1}^{t_2} \frac{V_{gm}}{R_{Gtot}} e^{-\frac{t}{R_{GTOT} C_{iss}}} dt$$

if we assume:

Equation 14

$$t_2 = t_1 + \Delta t$$

Equation 13 can be solved and the value of ΔT can be calculated as:

Equation 15

$$\Delta t = t_2 - t_1 = -R_{Gtot} \otimes C_{iss} \otimes \ln(1 - \frac{Q_{12}}{Q_{th}})$$

The total charge supplied to the gate during the time interval (t_2 to t_3) can be easily calculated by multiplying the constant I_{Gon} value with the time interval (t_2 to t_3) as follows:

Equation 16

$$Q_{23} = I_{Gon(t_2,t_3)} \otimes (t_3 - t_2) = \frac{V_{GM} - V_{PL}}{R_{Gtot}} \otimes (t_3 - t_2)$$

Equation 17

$$t_3 - t_2 = \frac{Q_{23}}{(V_{GM} - V_{PL})} R_{Gtot}$$

Time intervals (t_2 - t_1) and (t_3 - t_2) theoretically calculated by *Equation 5* and *17* are the two ones mainly involved in the turn-on event.

As similarly done for the turn-on, once the $Q'_{23}+Q'_{34} = Q_{23}+Q_{12}$ (if referred to the turn-off, see *Figure 10*) portion of the gate charge has been read from the gate charge curve, the two time intervals (t'_3 - t'_2) and (t'_4 - t'_3) which are mainly involved in the turn-off event can be theoretically calculated as follows:

Equation 18

$$(t'_3 - t'_2) = \frac{Q'_{23} * R_{Gtot}}{V_{PL}}$$

Equation 19

$$(t'_4 - t'_3) = -R_{Gtot} * C_{iss} * \ln\left(1 - \frac{Q'_{34}}{V_{PL} * C_{iss}}\right)$$

Time intervals of *Equation 15*, *17* and *Equation 18*, *19* have been calculated by assuming that the MOSFET works at T_j=25 °C. If the MOSFET is supposed to work in a real application, the V_{th} dependence ON temperature must be considered.

Having read the total gate charge $Q_g=Q_{th}+Q_{12}+Q_{23}+Q_{34}+Q_4$ (value at the V_{GM} voltage level which is usually 10 V) (the curve V_{GS} vs. Q_g is displayed in the MOSFET datasheet), the total power loss needed to charge the gate is:

Equation 20

$$P_{GATE} = Q_g * V_{GM} * f_{sw}$$

So, by comparing the total gate charge of two MOSFETs, measured under the same test conditions of I_D, V_{DS}, I_G, it is possible to understand which of them requires the lowest driving energy if the same V_{GM} and f_{sw} is considered.

Table 1 shows the total Q_g values of four couples of MD V/MD II Power MOSFETs with similar $R_{DS(on)}$. The Q_g value of each device has been calculated from the $V_{GS}(t)$ curve of each device (see *Figure 11* and *12* for reference) and measured on bench at the same I_D and V_{DS} levels at T_c=25 °C. The newest MD V guarantees a lower Q_g value than its equivalent MD II part, this leads to less effort in terms of driving energy requirements.

Table 1. Experimentally measured Q_g of four couples of MD V/MD II

Part number	$R_{DS(on)max}$@10 V, 25°C	Q_g@400 V, I_D(A)
STP16N65M5	279 mΩ	28.4 nC@6 A
STP18NM60N	285 mΩ	31.2 nC@6 A
STP21N65M5	179 mΩ	40.4 nC@8 A
STP24NM60N	190 mΩ	42.3 nC@8 A
STP35N65M5	98 mΩ	77.4 nC@15 A
STB36NM60N	105 mΩ	80.1 nC@15 A
STB42N65M5	79 mΩ	96 nC@16 A
STW48NM60N	70 mΩ	122 nC@16 A

Figure 11. Vg(t) curve measured on STB42NM60N @16 A, 400 V, I_G=1.5 mA

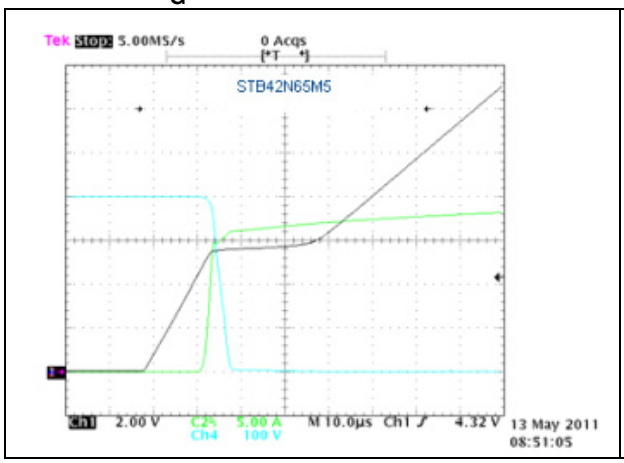
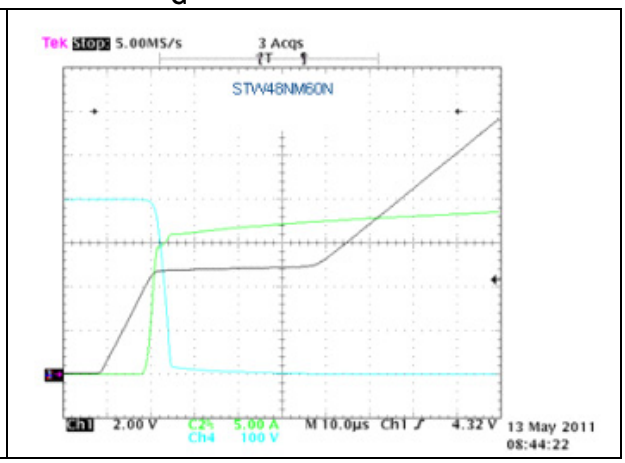


Figure 12. Vg(t) curve measured on STW48NM60N @16 A, 400 V, I_G=1.5 mA



In addition to the gate drive power losses, another contribution to the total switching loss is due to the I_D-V_{DS} cross.

If the turn-on event is considered, the main contribution over the total power dissipation is provided during phase “2” (current rise) and “3” (voltage lowering) of *Figure 8*, so the time intervals mainly involved are (t_1 to t_2), when the gate voltage is between V_{th} and V_{PL}, and the time interval (t_2 to t_3) when the gate voltage is at the Miller value. Both of them have been calculated by *Equation 15* and *17*. As for turn-off, the two time intervals mainly involved in the event are (t'_2 to t'_3) when the voltage rises up to the clamp value, and (t'_3 to t'_4) when the I_D current falls (refer to *Figure 10*). Both of them have been theoretically calculated by *Equation 18* and *19*.

The correspondence between the gate charge curve and the switching times involved in the turn-on/off event is verified until no other external phenomenon arises to change the I-V cross time duration (negligible layout parasitic inductances/capacitors, no/negligible peak recovery current of the clamp diode).

Figure 13, *15* and *Figure 14*, *16* show the turn-on and the turn-off of the fourth compared couple of *Table 1*, experimentally measured at the same current/voltage conditions of the gate charge test in *Figure 11* and *12* with an external R_{Gon}=47 Ω. The effect of these parameters is shown in *Table 2* which reports the theoretical turn-on and turn-off switching times calculated by *Equation 15*, *17* and *Equation 18*, *19* compared to the turn-on and turn-off times experimentally measured on the same devices.

Table 2. Experimentally and theoretically measured switching times and related static parameters

	V_{PL} @16 A	Q_{12} $Q_{'34}$	Q_{23} $Q_{'23}$	Experimental $t_{sw(on)}$(tot)	Theoretical $t_{sw(on)}$(tot)	Experimental $t_{sw(off)}$(tot)	Theoretical $t_{sw(off)}$(tot)
STB42N65M5	5.6V	5.2nC	5nC	≈115ns	133ns	≈80ns	89ns
STW48NM60N	4.8V	4.5nC	4.5nC	≈105ns	114ns	≈90ns	96ns

Referring to *Equation 15*, *17* and *Equation 18*, *19*, it's clear that $Q_{12}+Q_{23}$ and the V_{PL} are the two main actors impacting on the turn-on switching times. Similarly, $Q'_{23}+Q'_{34}$ and V_{PL} mainly influence the turn-off switching times. It's important to note that a device with higher V_{PL} than another, also exhibits higher V_{th} at the same I_D current.

As far as the MD V and MD II devices in *Table 2* are concerned, the STB42N65M5 shows slightly higher Q_{12} and Q_{23} charge portions than the STW48NM60N. If the other static parameters are supposed to be the same for both devices, this should be enough to have both turn-on times and turn-off times of the MD V device which are wider than MD II ones. Additionally, the MD V part exhibits a higher V_{PL} value than the MD II: this further worsens both (t_2 - t_1) and (t_3 - t_2) contributions (see *Equation 15* and *17*) on the turn-on switching times. On the other hand, a higher V_{PL} helps to reduce turn-off switching times, as can be verified by inspecting *Equation 18* and *19*. In the end, turn-on times of the MD V are wider than the MD II device due to a higher gate charge portion and V_{PL}, while the same static parameters favor the MD V at turn-off.

The different impact of the V_{PL} on turn-on and turn-off is also evident from *Equation 7*, *10*, *11*, as a higher plateau level of the MD V is directly linked to a lower I_{Gon} charging current during the entire turn-on event; the same higher V_{PL} of the MD V results in a higher I_{Goff} discharging current which helps to speed up the turn-off event.

The theoretical switching times calculated by *Equation 15*, *17* and *Equation 18*, *19* can also be used to obtain a preliminary idea of what value of R_{Gtot} in the driving stage must be adopted to guarantee a specific time interval for the turn-on or turn-off. It is anyway important to remark that the ON and OFF energy losses depend on several factors, like:

1. the circuit the MOSFET is working in (the test circuit considered in this work is a simple single ended clamped inductive load circuit);
2. the output capacitance of the MOSFET which exhibits a different voltage dependence if different SJ MOSFET families are considered (this impacts on the voltage raising/lowering of the MOSFET during the transients);
3. the parasitic capacitances and inductors of the layout which can significantly impact on the current and voltage slopes. All these effects sometimes modify the energy loss wave, and this is the reason why there is not always an exact correspondence between the switching time interval comparison and the energy value comparison in the same match.

Figure 13. Turn-on of STB42N65M5 @16 A, 400 V, 47 Ω

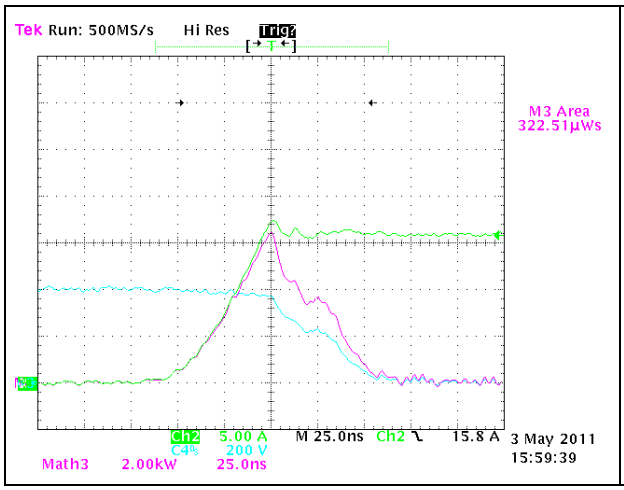


Figure 14. Turn-on of STW48NM60N @16 A, 400 V, 47 Ω

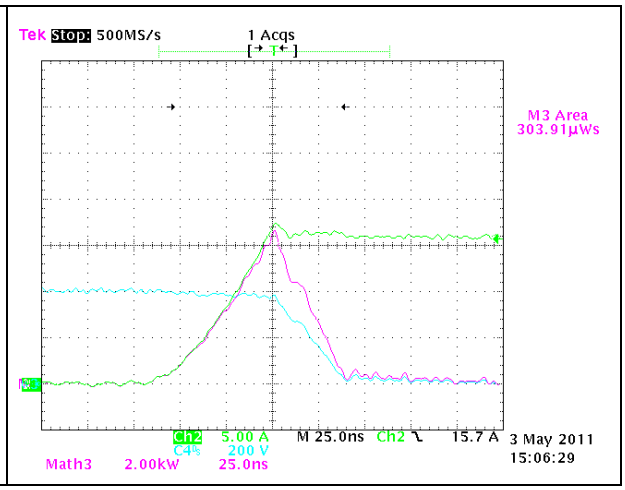


Figure 15. Turn-off of STB42N65M5 @16 A, 400 V, 47 Ω

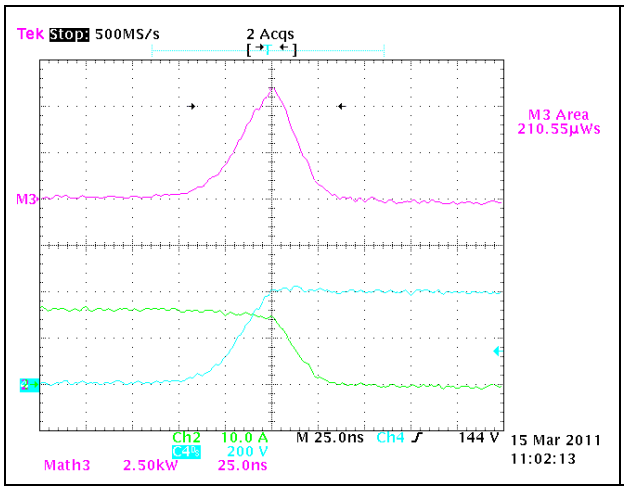
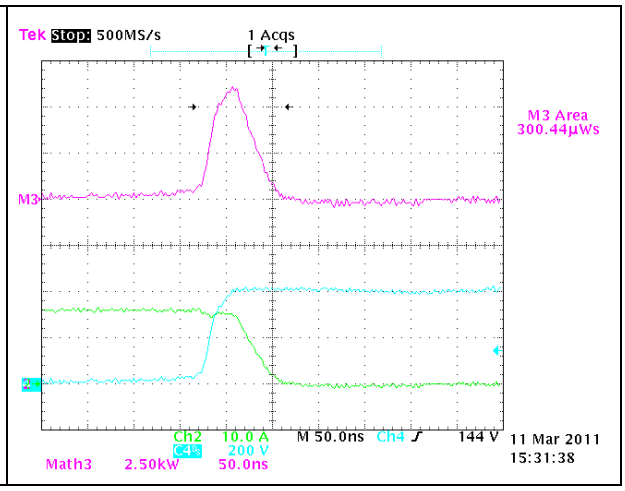


Figure 16. Turn-off of STW48NM60N @16 A, 400 V, 47 Ω

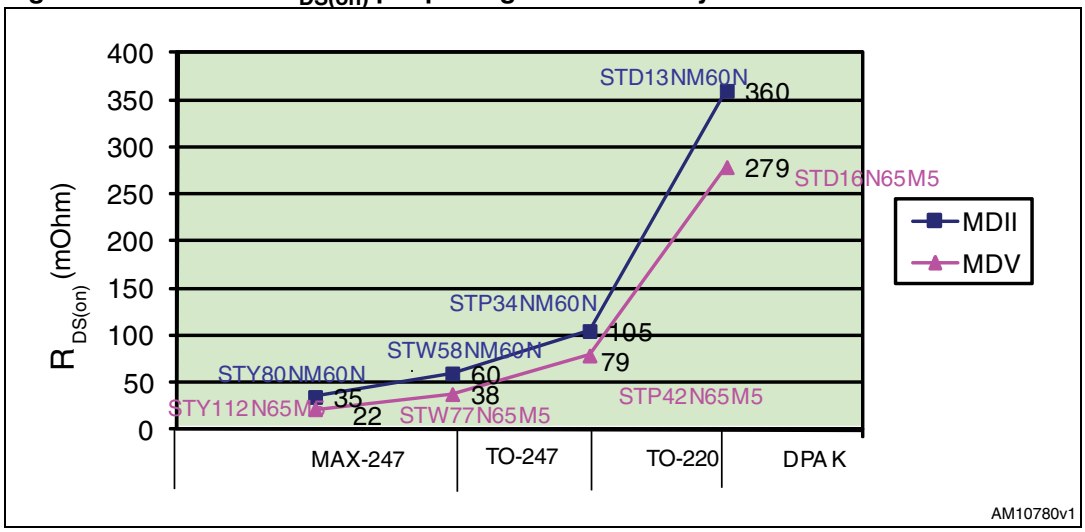


So, V_{GS} vs. Q_g curve is very important for at least two reasons: it provides information on the energy required to turn on/off the MOSFET and at the same time, it gives a rough idea of the MOSFET dynamics.

5 Latest ST MD II and MD V technology at a glance

With the MDmesh V family, STMicroelectronics reaches the lowest $R_{DS(on)}$ value per package among its HV SJ MOSFET technology product range. For example, *Figure 17* reports the lowest $R_{DS(on)max}$ achievable by the last two MD II and MD V product families.

Figure 17. Minimum $R_{DS(on)}$ per package achievable by MD II and MD V



The MD V shows lower specific $R_{DS(on)}$ if compared to its predecessor. As a consequence of this improvement, the $R_{DS(on)}$ per package is also lowered, therefore allowing the same device to be housed in a smaller package, which was not possible before. Besides the $R_{DS(on)}$, it is important to take into account the driving energy required to turn on/off the device. In order to satisfy this requirement, the MD V guarantees lower total gate charge than the MD II at the same I_D,V_{DS} and $R_{DS(on)}$ values (as shown in *Table 1*), allowing to significantly reduce the driving losses and increase the total system efficiency. The reduced $R_{DS(on)}$ values per package of MD V leads to a slight increase in thermal resistance, but this is counterbalanced by an overall static and dynamic energy loss improvement if compared to the previous MD II generation. Some exceptions on this last statement arise when small devices of the two families are compared at very low current levels, as is shown in the next section.

6 MD II and MD V: which is the lowest loss one?

A dynamic on bench comparison has been carried out on four different MD V/MD II MOSFET couples in order to provide a reliable idea of their dynamic performances. All tests have been issued by the same simple clamped inductive load test circuit (refer to *Figure 7*) where the effects of parasitic elements have been reduced in order to make the effective MOSFET behavior more understandable.

A 600 V,10 A SiC diode has been used as the clamp diode. The matches obtained under evaluation are those displayed in *Table 1*. The following graphs show the energy ON, the energy OFF, the di/dt, the dv/dt both at turn-on and turn-off of each compared match for different R_G values, and two I_D current levels.

6.1 STB42N65M5 vs. STW48NM60N

Figure 18. STB42N65M5 vs. STW48NM60N E_{on} @ 8 A/16 A, 400 V

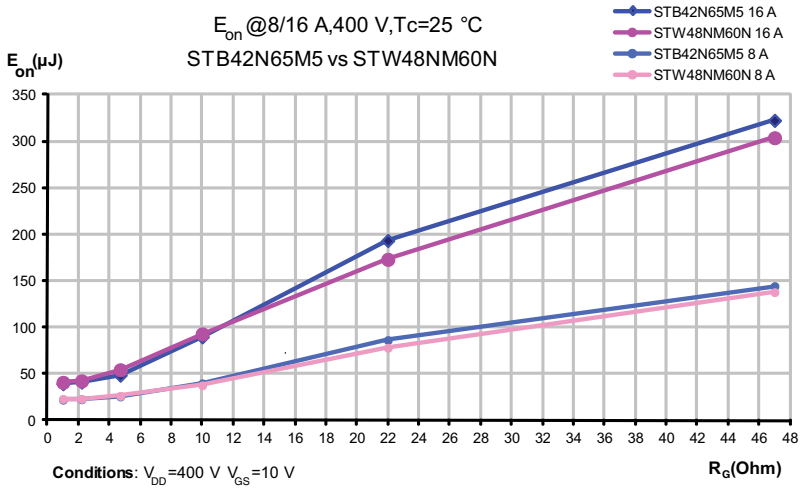


Figure 19. STB42N65M5 vs. STW48NM60N di/dt at turn-on @ 8 A/16 A, 400 V

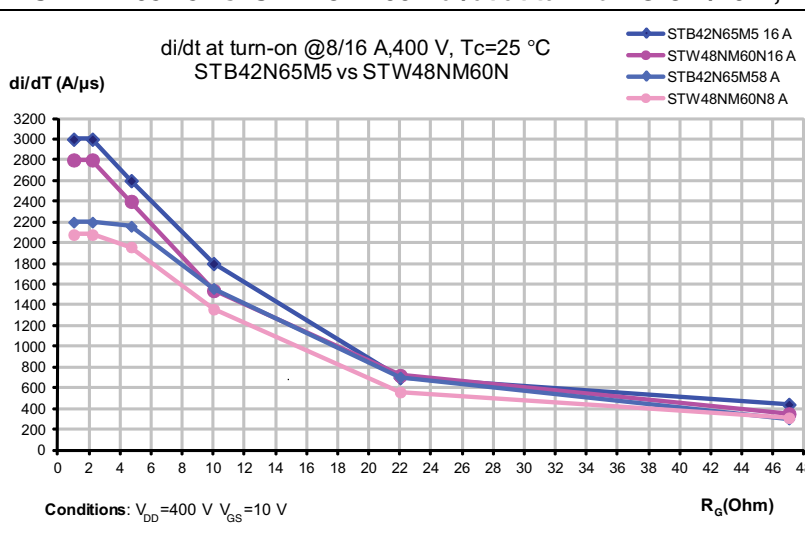


Figure 20. STB42N65M5 vs. STW48NM60N dv/dt at turn-on @ 8 A/16 A 400 V

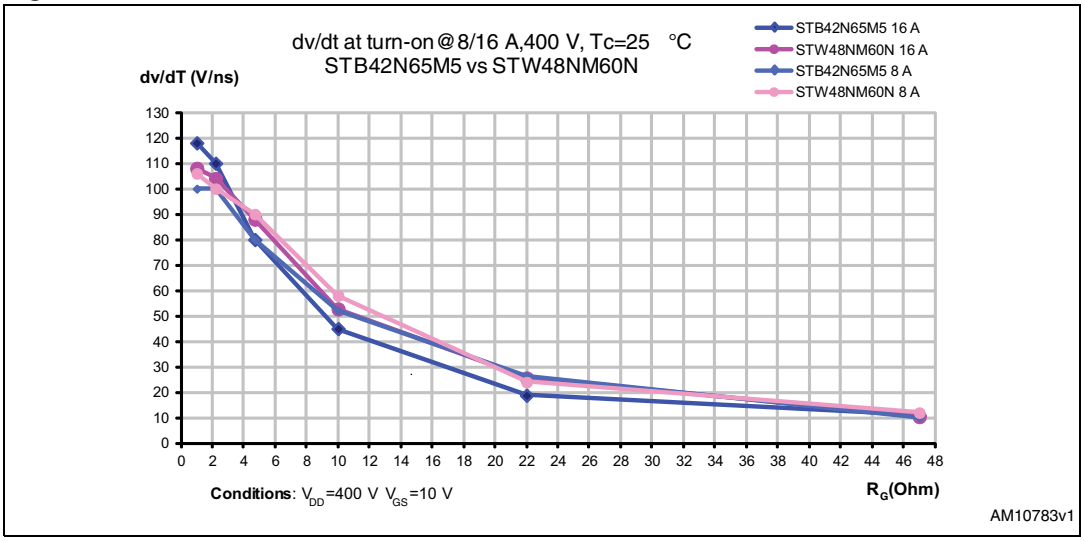


Figure 21. STB42N65M5 vs. STW48NM60N zoom of dv/dt at turn-on @ 8 A/16 A 400 V

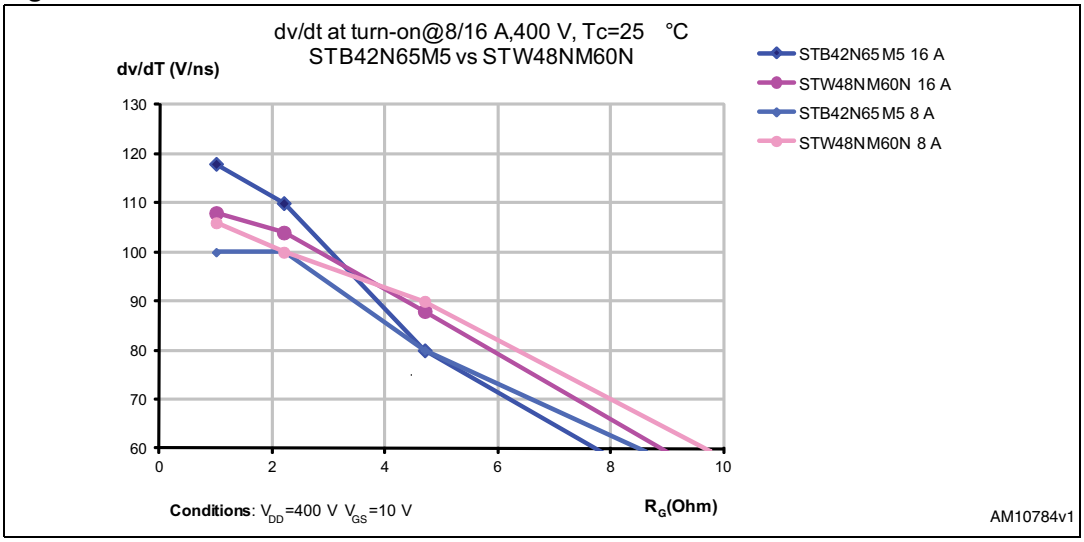


Figure 22. STB42N65M5 vs. STW48NM60N E_{off} @ 8 A/16 A, 400 V

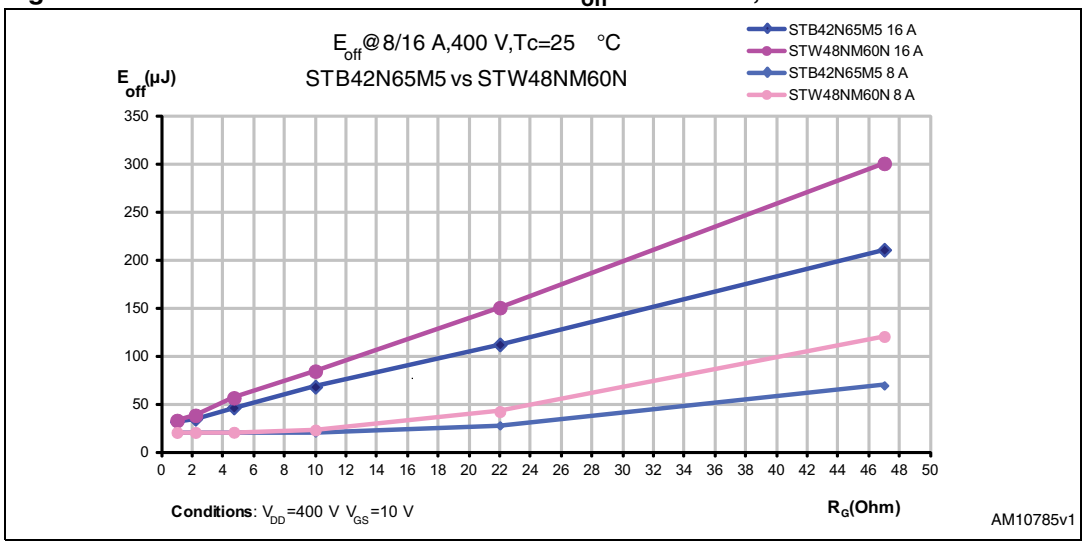


Figure 23. STB42N65M5 vs. STW48NM60N di/dt at turn-off @ 8 A/16 A, 400 V

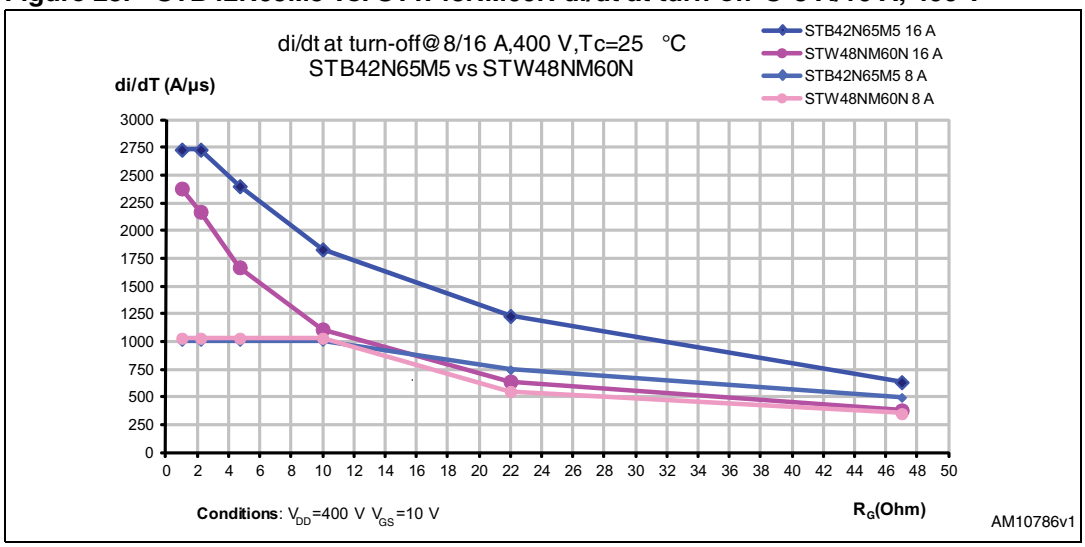
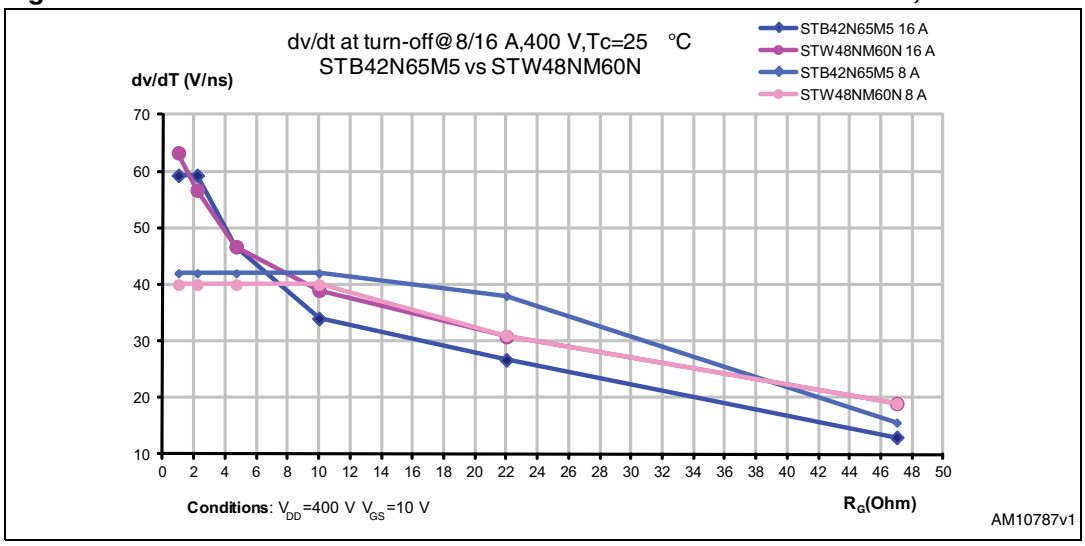


Figure 24. STB42N65M5 vs. STW48NM60N dv/dt at turn-off @ 8 A/ 16 A, 400 V



6.2 STP35N65M5 vs. STB36NM60N

Figure 25. STP35N65M5 vs. STB36NM60N E_{on} @ 7.5 A/15 A, 400 V

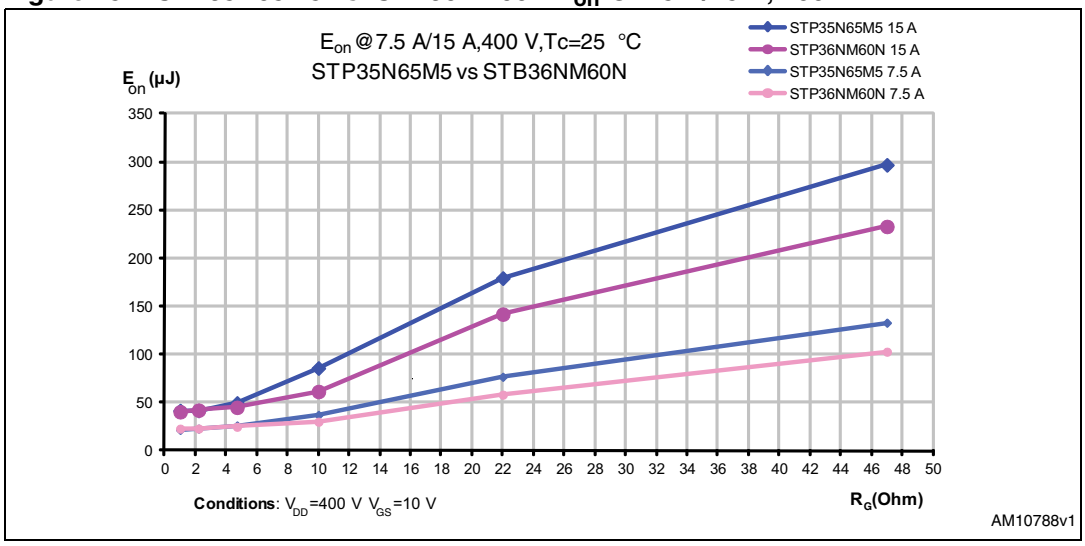


Figure 26. STP35N65M5 vs. STB36NM60N di/dt at turn-on @ 7.5 A/15 A, 400 V

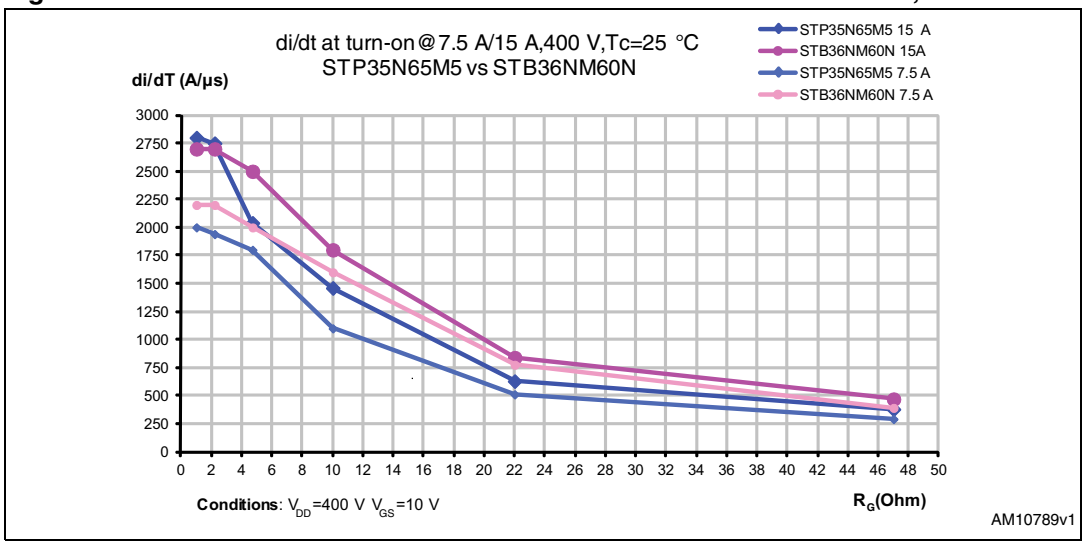


Figure 27. STP35N65M5 vs. STB36NM60N dv/dt at turn-on @ 7.5 A/15 A 400 V

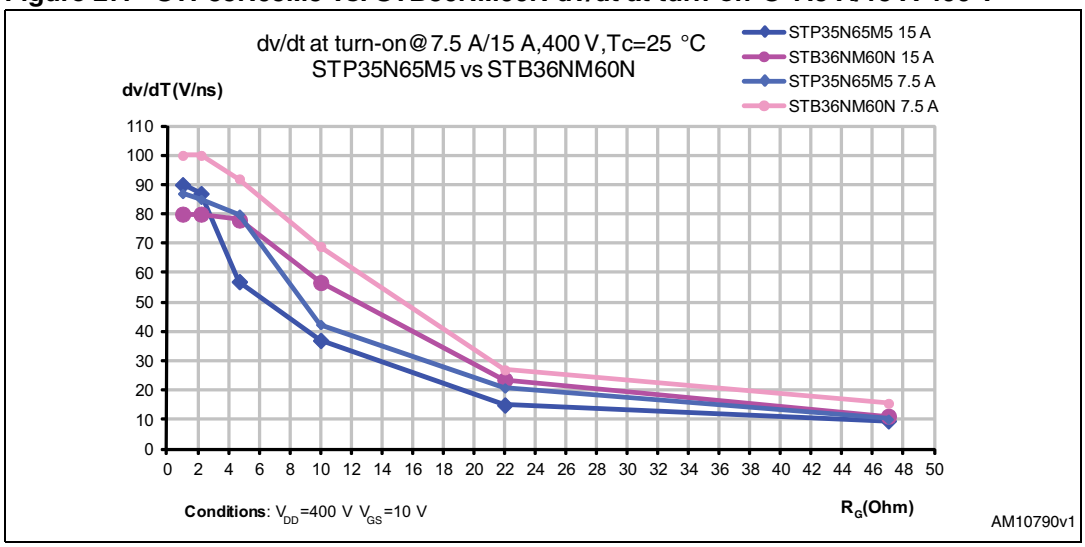


Figure 28. STP35N65M5 vs. STB36NM60N E_{off} @ 7.5 A/15 A, 400 V

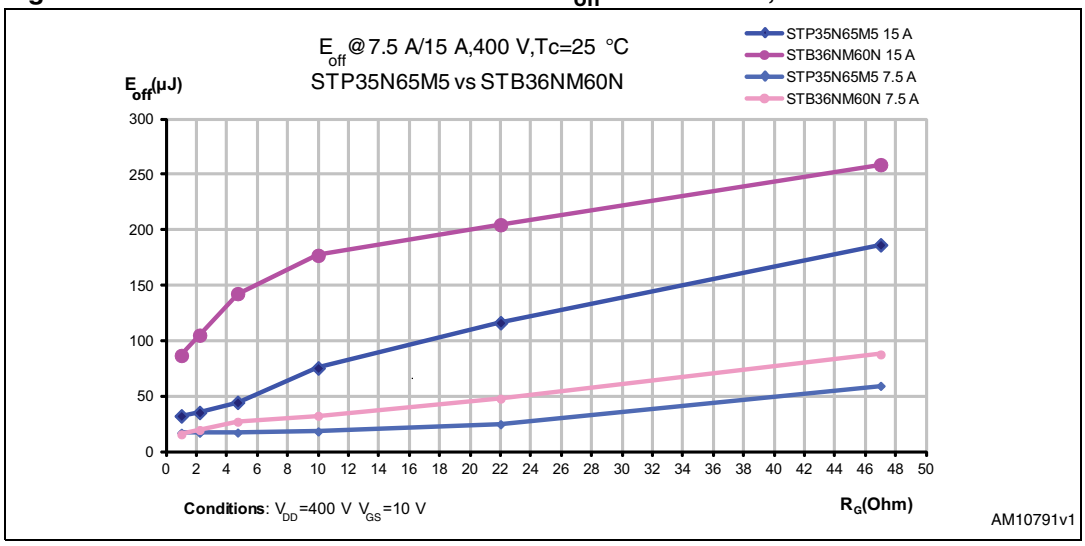


Figure 29. STP35N65M5 vs. STB36NM60N di/dt at turn-off @ 7.5 A/15 A, 400 V

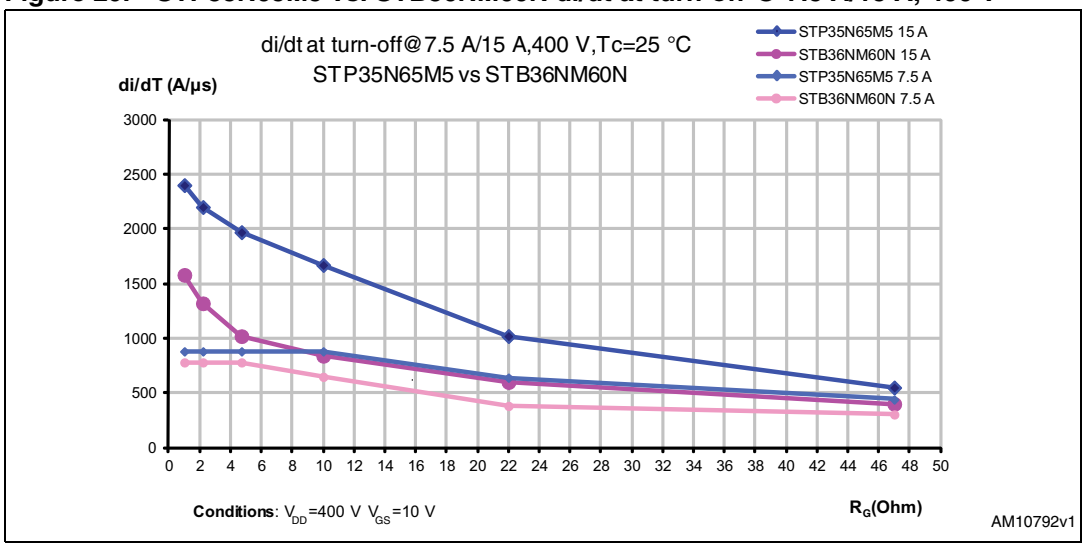
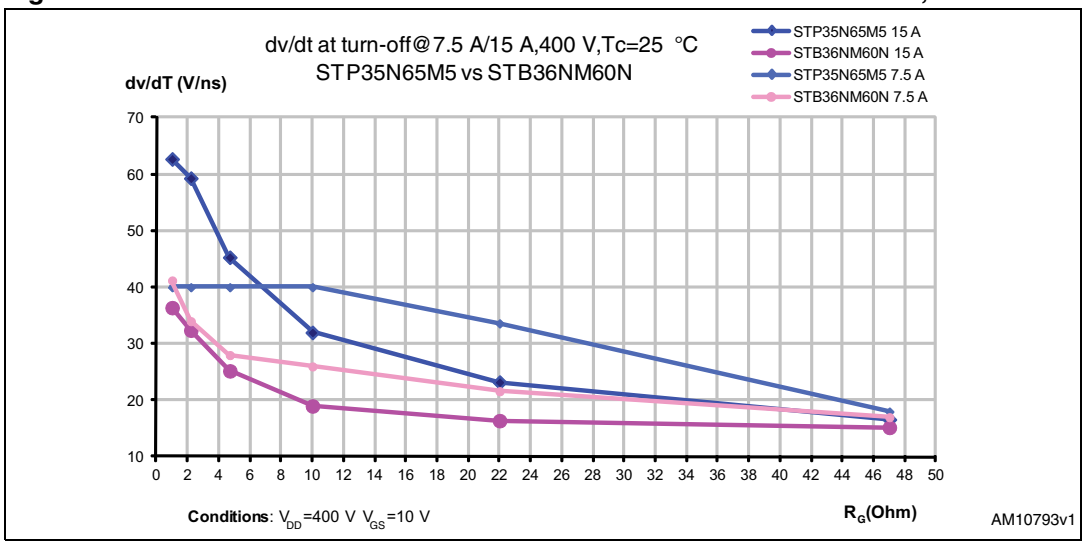


Figure 30. STP35N65M5 vs. STB36NM60N dv/dt at turn-off @ 7.5 A/15 A, 400 V



6.3 STP21N65M5 vs. STP24NM60N

Figure 31. STP21N65M5 vs. STP24NM60N E_{on} @ 4 A/ 8 A, 400 V

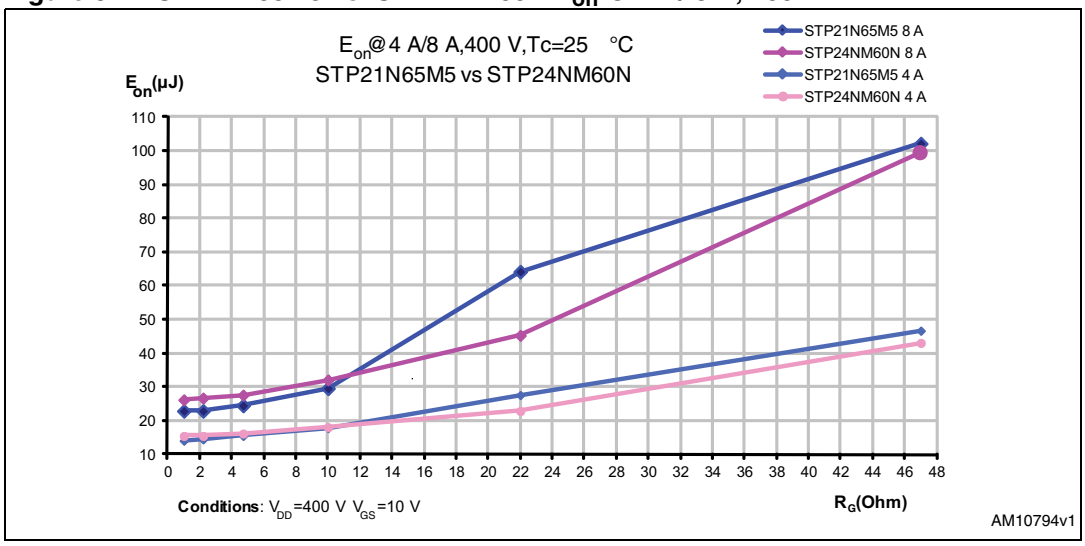


Figure 32. STP21N65M5 vs. STP24NM60N di/dt at turn-on @ 4 A/8 A, 400 V

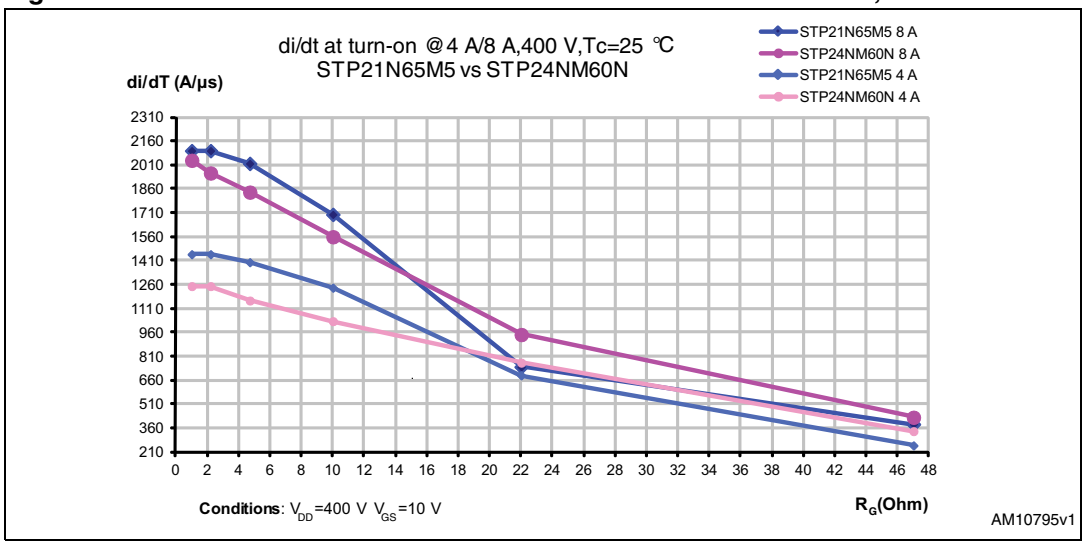


Figure 33. STP21N65M5 vs. STP24NM60N dv/dt at turn-on @ 4 A/8 A, 400 V

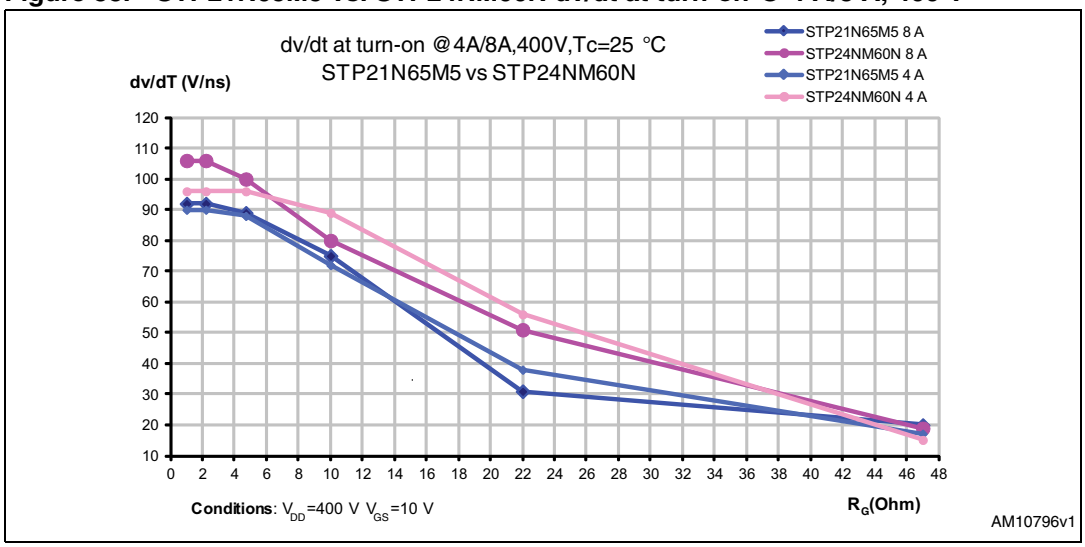


Figure 34. STP21N65M5 vs. STP24NM60N E_{off} @ 4 A/8 A, 400 V

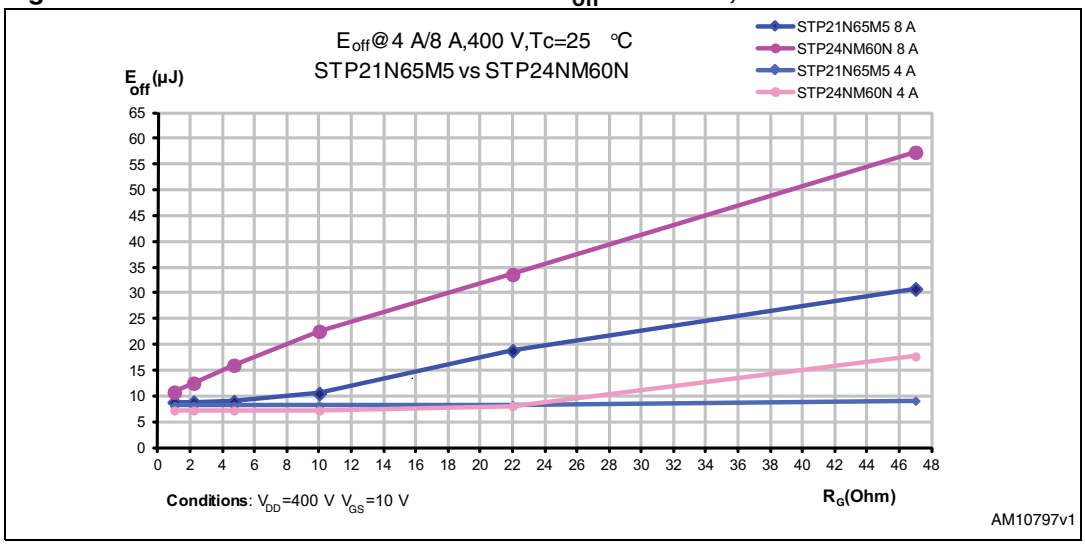


Figure 35. STP21N65M5 vs. STP24NM60N di/dt at turn-off @ 4 A/8 A, 400 V

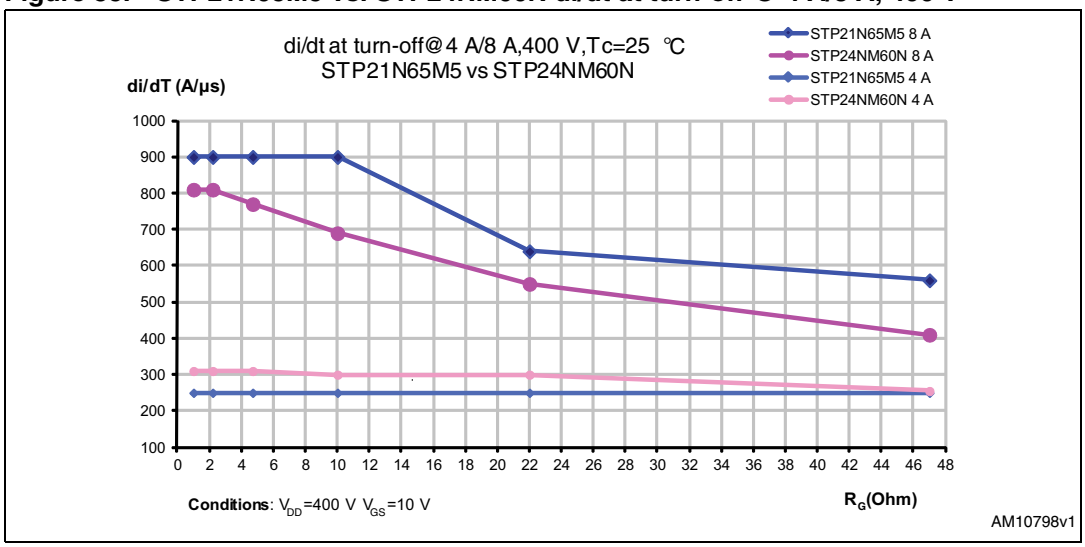
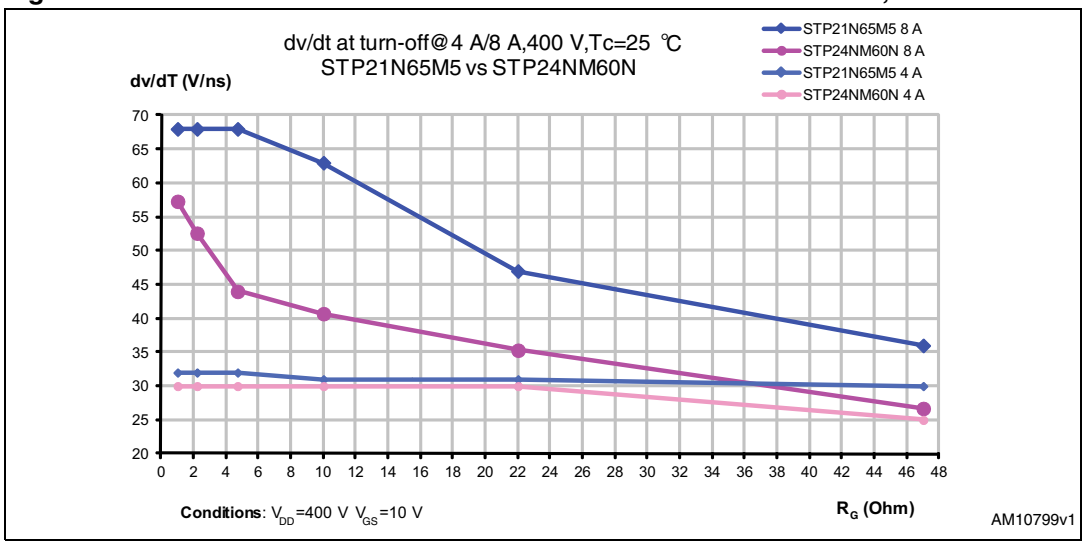


Figure 36. STP21N65M5 vs. STP24NM60N dv/dt at turn-off @ 4 A/8 A, 400 V



6.4 STP16N65M5 vs. STP18NM60N

Figure 37. STP16N65M5 vs. STP18NM60N E_{on} @ 3 A/6 A, 400 V

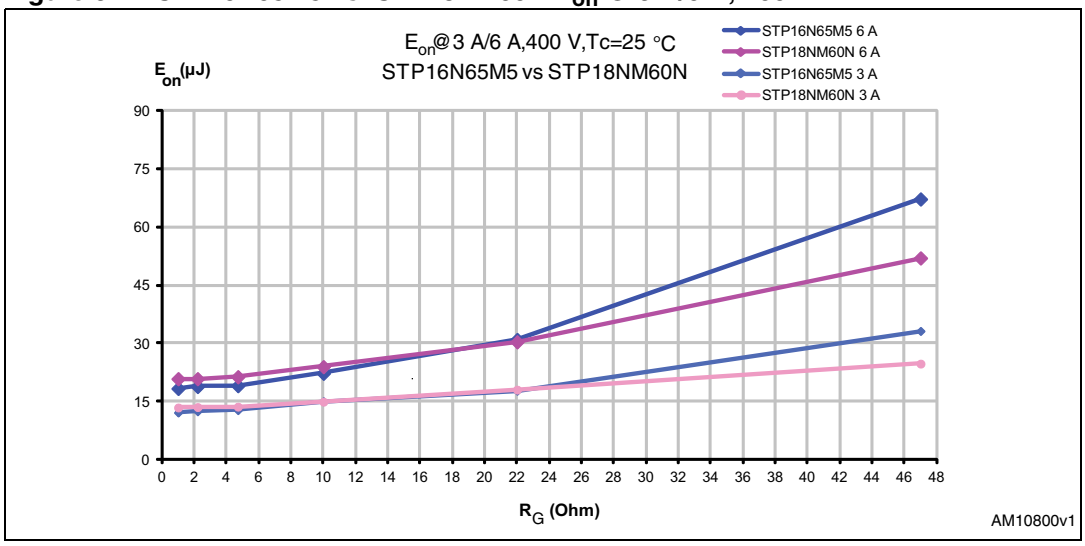


Figure 38. STP16N65M5 vs. STP18NM60N di/dt at turn-on @ 3 A/ 6 A, 400 V

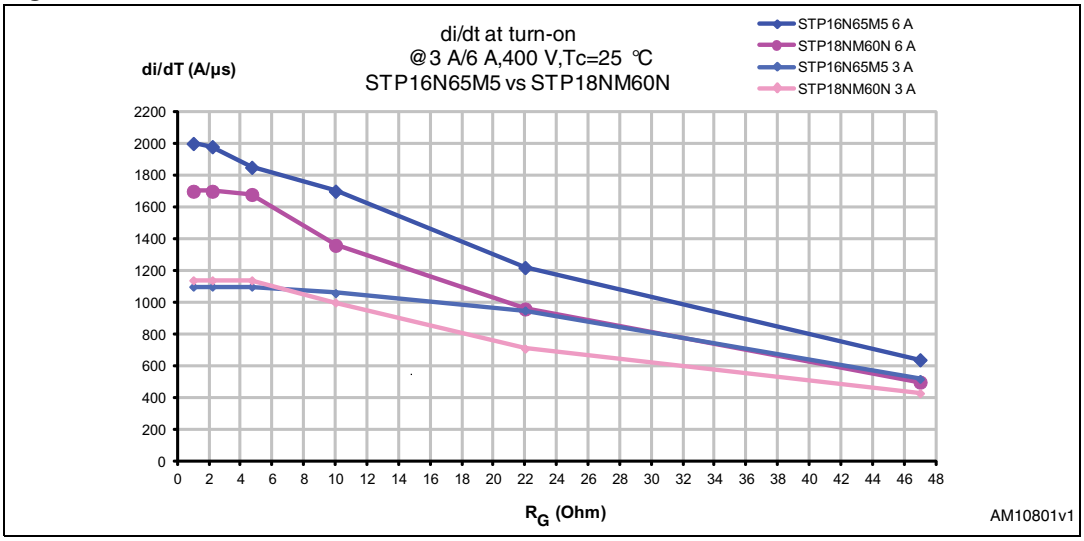


Figure 39. STP16N65M5 vs. STP18NM60N dv/dt at turn-on @ 3 A/6 A, 400 V

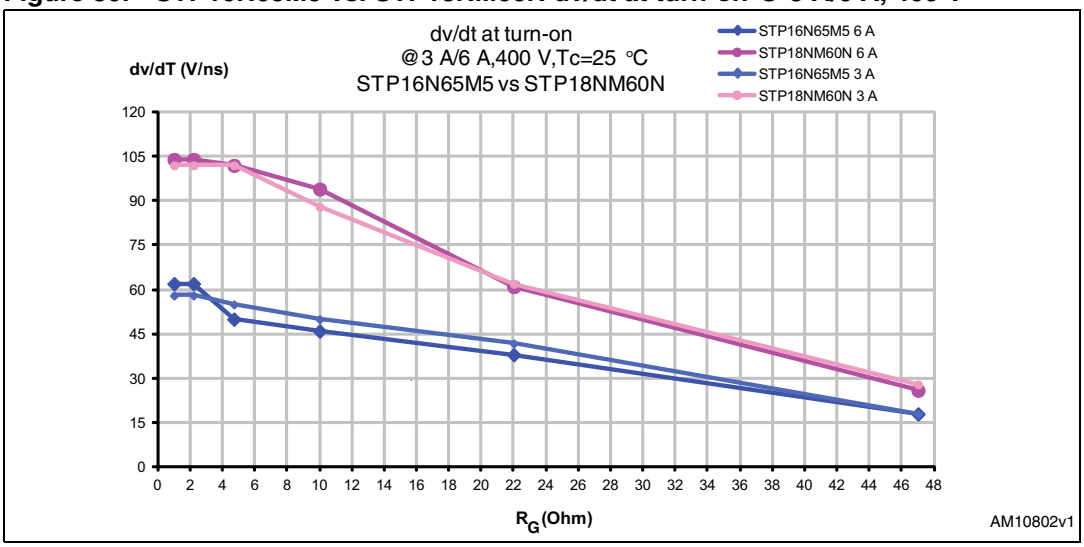


Figure 40. STP16N65M5 vs. STP18NM60N E_{off} @ 3 A/6 A, 400 V

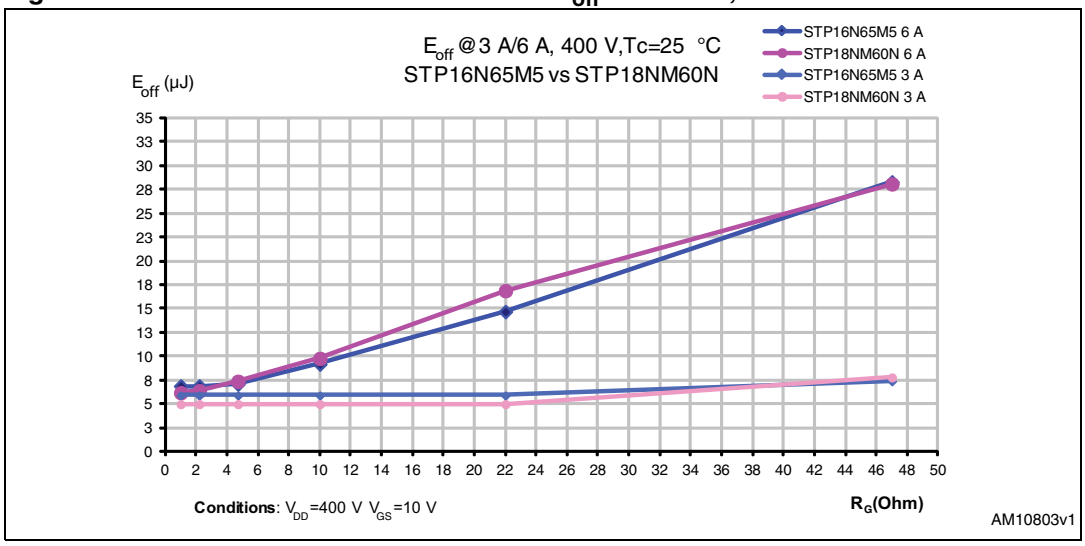


Figure 41. STP16N65M5 vs. STP18NM60N di/dt at turn-off @ 3 A/6 A, 400 V

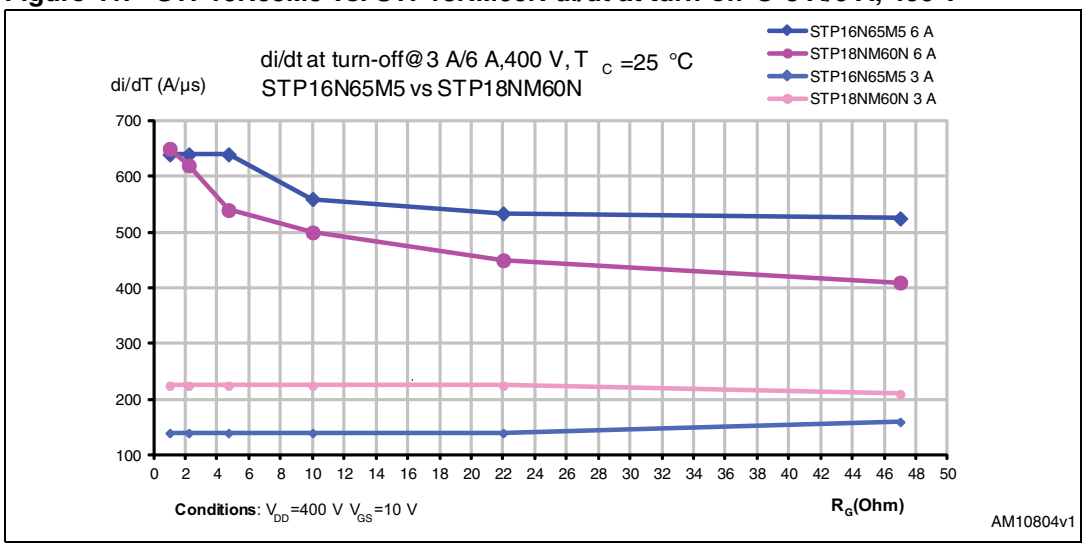
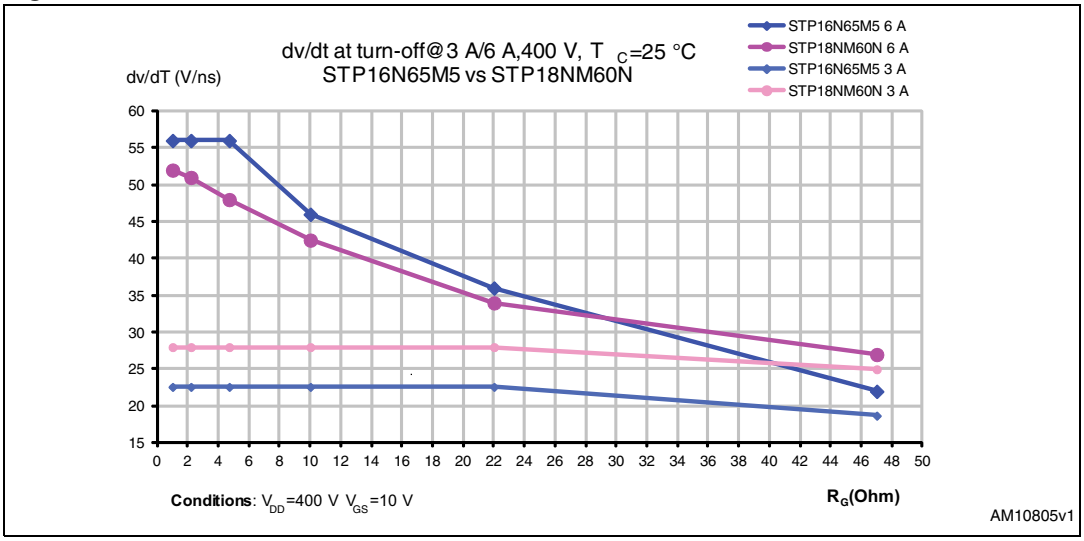


Figure 42. STP16N65M5 vs. STP18NM60N dv/dt at turn-off @ 3 A/6 A, 400 V



6.5 Comments about energy ON comparison

Considerations about energy comparison between the MD V and the MD II depend on the gate resistor selected by the user.

As for turn-on energy, the bigger sizes of the MD V list considered in this work (STP42N65M5 and STP35N65M5) perform worse than their equivalent MD II parts in the entire R_G range at the two current levels selected for the tests. This is due to the negative gate charge impact (the Q_{12}+Q_{23} portion, as explained in *Section 4*) together with the higher threshold and plateau value of these parts if compared to the MD II devices.

Smaller sizes show a slightly different dynamic behavior: MD V parts (STP21N65M5 and STP16 N65M5) perform worse than their equivalent MD II parts at relative medium/high R_G values (i.e. R_G>10 Ω for the STP21N65M5, and R_G>22 Ω for the STP16N65M5). This situation changes if low R_G values are used. Under the latter driving condition, the MD V performs better than the MD II but, it is not advised to adopt very low R_G values in most common situations due to the increased voltage/current slopes of these small devices and the consequent increased risk of spurious oscillations.

Anyway, if an MD V part (belonging to the list in *Table 1*) is used in any circuit with a specific R_{Gon} value, and it needs to be replaced with an equivalent MD II part by keeping the same E_{on} energy, this can be easily obtained by increasing its R_{Gon} value according to the charts showing the E_{on} comparison reported in this work. The same way of proceeding can be adopted if an MD V device must be used instead of an MD II equivalent part.

6.6 Comments about energy OFF comparison

As for turn-off, all MD V devices show better performances than their equivalent MD II parts. Some exceptions arise for the smaller sizes (STP21N65M5 and STP16N65M5) when current levels are significantly lower than the nominal current (see *Figure 34* and *40*).

The slightly worse MD V energy at very low current levels is linked to the behavior of the MOSFET intrinsic capacitances. Output capacitance is charged up to V_{CLAMP} during

turn-off and the energy stored during this event is added to the effective energy dissipated at turn-on in the next cycle in hard switching conditions, according to *Equation 21*:

Equation 21

$$E_{off}(diss) = E_{off}(measured) - E(C_o)$$
$$E_{on}(diss) = E_{on}(measured) + E(C_0)$$

As the current becomes lower and lower, the effective energy dissipated by the MOSFET decreases and the measured OFF energy is only the energy required by the output capacitance to enable the turn-off. This is the reason why all E_{off} curves exhibit a flat trend at low current/low R_{Goff} values. If the energy required by the MD V output capacitances is higher than that of the MD II, this leads to a higher measured E_{off} value for the MD V if compared to the MD II at the same I_D, V_{CLAMP} values.

A specific test was performed on all MD V/MD II matches analyzed in this work to confirm the different output capacitance behavior. As output capacitance of a MOSFET is voltage dependant, a constant equivalent capacitance which stores the same energy of the output switch capacitance in the entire (0 V to V_{CLAMP}=0 V to 400 V) excursion has been calculated. The MOSFET is really being turned off in an unclamped inductive load test circuit and the total energy stored in the inductor is:

Equation 22

$$E(inductive) = \frac{1}{2} \otimes L * I^2$$

This inductive energy is supposed to be applied to a constant capacitance which charges up to V_{CLAMP}:

Equation 23

$$\frac{1}{2} \otimes C_{0AV} \otimes V^2_{CLAMP} = \frac{1}{2} \otimes L \otimes I^2$$

Table 3 shows the C_{oAV} measured on all MD V/MD II devices:

Table 3. C_{oAV} experimentally measured on MD V/MD II devices

Part number	C_{0AV}@400 V
STP16N65M5	67 pF
STP18NM60N	64 pF
STP21N65M5	79 pF
STP24NM60N	75 pF
STP35N65M5	131 pF
STB36NM60N	109 pF
STB42N65M5	155 pF
STW48NM60N	162 pF

Table 3 explains why the measured E_{off} energies of MD V STP16N65M5, STP21N65M5 and STP35N65M5 are slightly worse than the MD II at very low current values and low R_{Goff} values.

Anyway, the difference in terms of E_{off} between the small sizes of MD V and MD II is so small that the two families can be considered as having the same dynamic performances under the above specified conditions of current and R_G.

7 MOSFET critical parameters in high switching environments

7.1 Parasitic inductance influence on switching losses

When considering the Power MOSFET switching characteristics, the influence of parasitic inductances must be carefully considered. Among the three main actors in a power circuit (the gate loop inductance, the common source inductance, and the main switching loop inductance) the common source inductance and the main switching loop inductance are the most critical and their respective action can not always be identified. Anyway, in most practical cases it is possible to understand what kind of parasitic inductance has the greater contribution over the other one by directly inspecting the switching waveforms.

If MOSFET transient is considered, the instantaneous drain current $I_D(t)$ and the instantaneous gate to source voltage $V_{GS}(t)$ satisfies *Equation 24*:

Equation 24

$$i_D(t) = g_{fs} \otimes (V_{GS}(t) - V_{th})$$

The drain to source voltage V_{DS} changes its value due to the voltage across the parasitic inductances according to the formula:

Equation 25

$$V_{DS} = V_{DD} - \frac{dI_D}{dt} \otimes (L_s \oplus L_D)$$

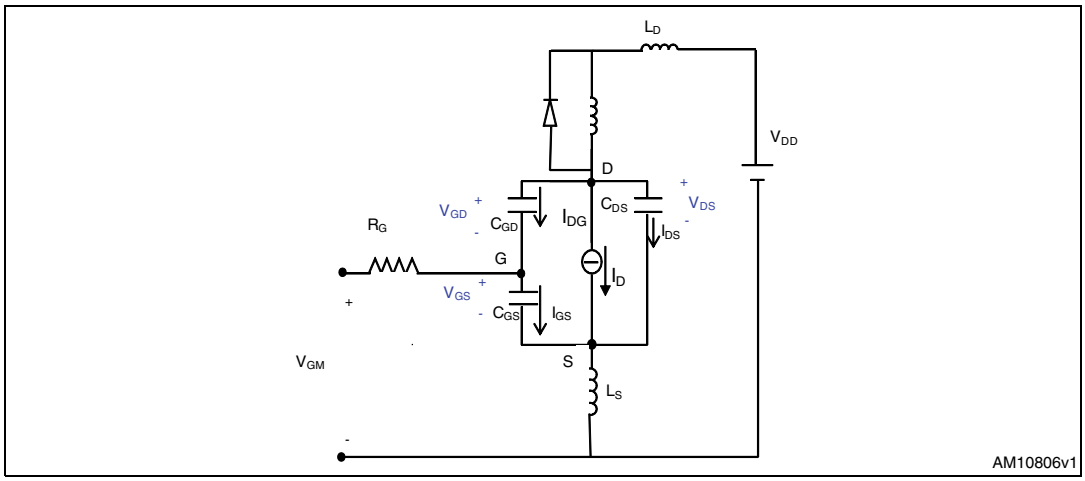
(See *Figure 43*.)

Gate to source voltage $V_{GS}(t)$ satisfies *Equation 26*:

Equation 26

$$V_{GM} = R_{Gtot}(C_{gs}\frac{dV_{GS}}{dt} - C_{gd}\frac{dV_{GD}}{dt}) + v_{GS}(t) + L_S\frac{d(I_D + I_{GS})}{dt}$$

Figure 43. Equivalent capacitive model of a MOSFET with parasitic inductances at turn-on



Both parasitic inductances (drain and common source) impact on the $V_{GS}(t)$ and $I_G(t)$ waveforms, as the voltage across the Ls is directly subtracted (or added in the case of a turn-off event) from the input V_{GM}, while the voltage induced across the L_D changes the voltage value of the C_{ds} capacitance.

The effect of both inductances on the $V_{GS}(t)$, $I_D(t)$ and V_{DS} depends on the relative values of L_D and L_s, rather than R_G and the internal MOSFET capacitances C_{gd} and C_{gs}.

Under high current levels and low L_s values, the MOSFET experiences high voltage overshoot during turn-off. Additionally, the voltage across the L_D during the positive di/dt at turn-on is subtracted from the V_{DS} voltage across the switch and this is evident as a "missing step" in the voltage waveform.

Figure 44. Turn-on of STW77N65M5@400 V, 13 A, 25 °C

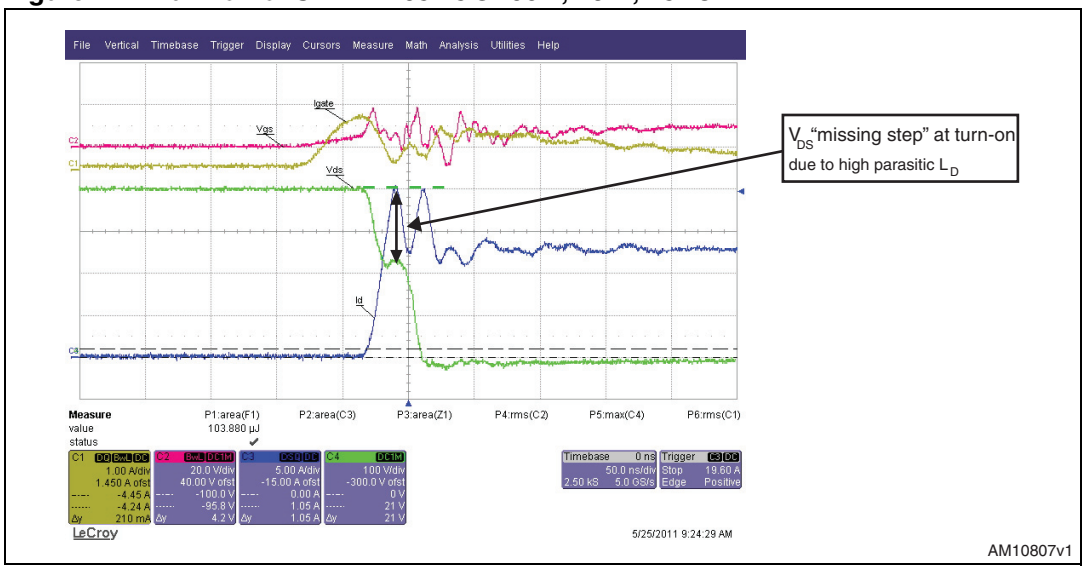


Figure 44 shows the turn-on of the STW77N65M5 working in the STEVAL-ISF001V1 3 kW PFC, where the parasitic source inductance has been dramatically cut thanks to the 4-pin solution (explained in *Section 7.2*). Nevertheless, the parasitic drain component is still present, causing the typical "missing step" in the voltage waveform.

On the contrary, as the L_s value becomes significant if compared to the L_D value, the driving loop circuit has a relevant impact on the switching behavior, slowing down the I_D current. This implies an energy loss which worsens both at turn-on and at turn-off.

In the following sections, the impact of common source inductance and the main switching loop inductance is analyzed by making the hypothesis of neglecting one of the two contributors.

7.2 Common source inductance

The source inductance plays the most important role in influencing the switching performances of a Power MOSFET, especially when high current levels need to be commutated.

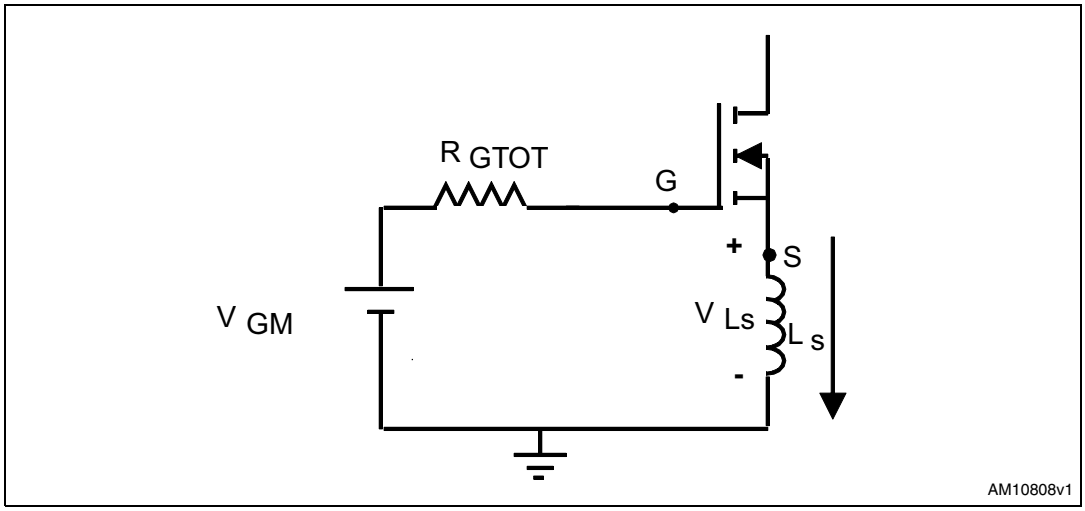
When dealing with source inductance, it is necessary to split it between an internal component (the source bond wire inside the MOSFET package) and external components including the inductance wiring between the source pin and the common ground of the PCB.

Since no optimization can be done over the internal component, particular care must be taken in controlling and reducing the external source inductance as much as possible.

The source inductance is involved in two different phenomena during the switching transient; the most visible one arises during phase “2” of turn-on and phase “3” of turn-off (see *Figure 8* and *10*).

If the turn-on event is considered, phase “2” is the phase of drain current rising. The V_{GS} voltage is between the V_{th} and the plateau level V_{PL}, as the C_{iss} capacitor is being charged by the gate current Ig. *Figure 45* shows the equivalent driving circuit referred to in this specific phase:

Figure 45. Equivalent driving circuit of a MOSFET at turn-on with parasitic source inductance



The high di/dt during turn-on (positive rate of I_D) induces a voltage V_{Ls} across the source inductor (positive value, as shown in *Figure 45*) whose value satisfies *Equation 27*:

Equation 27

$$V_{Ls} = L_s \frac{d(I_D \oplus I_{GS})}{dt} \approx L_s \frac{d(I_D)}{dt}$$

This induced V_{Ls} causes a lack of gate current due to less available voltage across the total gate resistor causing a dI/dt reduction and, as a negative consequence, a worsening I-V cross.

The source inductance, on the other hand, acts as a negative feedback in the gate driving loop, as the reduced dI/dt results in a smaller V_{Ls}, this reduced voltage across Ls leads to an increase in dI/dt. A balance is therefore established thanks to the source inductor, between the gate current and the drain current.

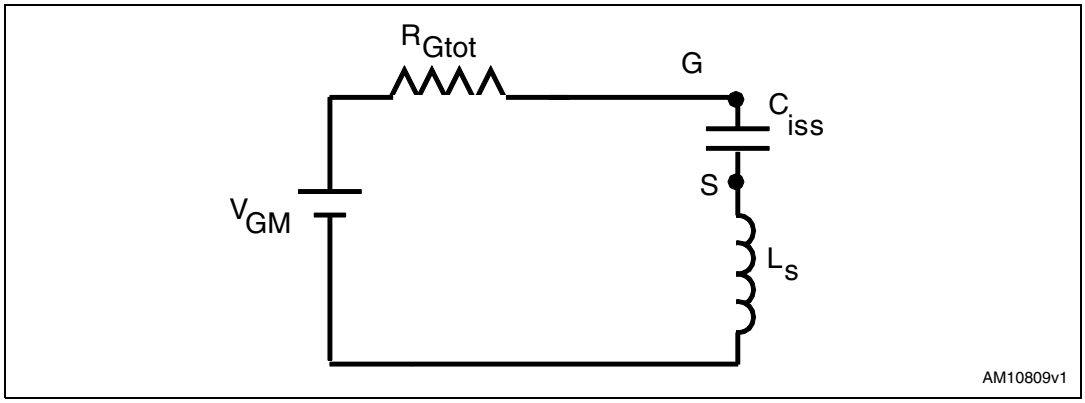
As far as the turn-off (phase “3”) is concerned, the L_s acts in a similar way by inducing a voltage V_{Ls} over the source inductor which is negative if referred to *Figure 45* as the drain current is falling down. This voltage leads to a positive Ig which has the unavoidable effect of slowing down the drain current.

As long as the V_{Ls} across the inductor is considerably less than the gate source voltage value in the commutation time interval, the effect of L_s can be neglected.

On the contrary, when high drain currents/high ΔI/dt are involved, the induced voltage V_{Ls} becomes large enough to significantly interfere with the gate bias.

A second order effect related to the source inductance is that R_{Gtot}, L_s, and C_{iss} (at turn-on) are the RLC components of a series resonant circuit, as shown in *Figure 46*.

Figure 46. Simplified equivalent series resonant model of the driving circuit of a MOSFET



As far as the resonance aspect is concerned, the phenomenon is due to the L_s inductor and the MOSFET input capacitor energy exchange (if turn-off is considered, the capacitor involved is the drain source C_{ds}). This results in the output current (gate current I_G) and voltage oscillatory spikes which can lead to unwanted turn-on if the V_{GS} voltage reaches the threshold value.

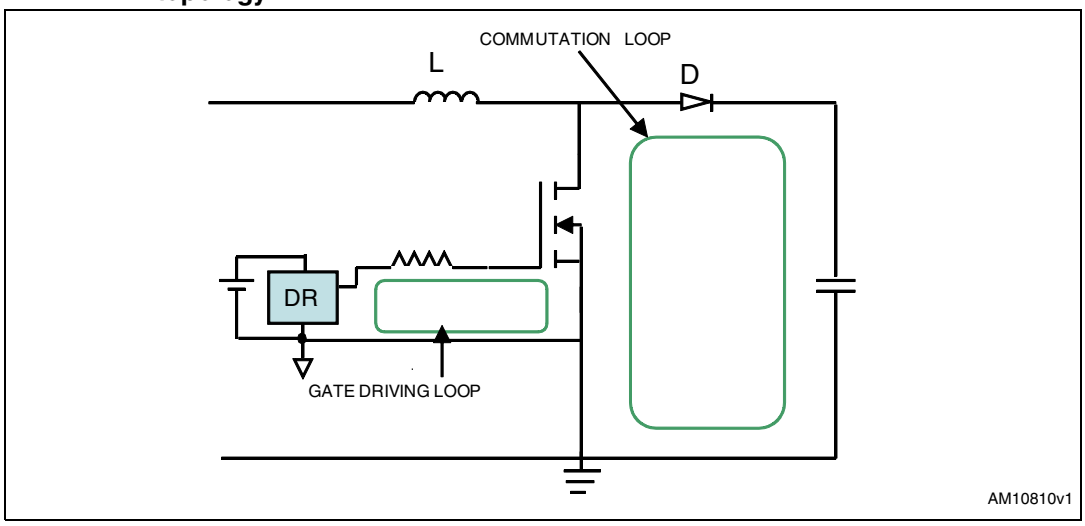
The Q factor of the resonant circuit which is also related to the L_s value and is responsible of the output signal time response, can be reduced by increasing the total gate resistor components along the driving loop (which comprises the external R_G, the MOSFET intrinsic R_G and the driver output impedance).

If especially small sizes are involved, a higher gate resistor causes under damped oscillations in the gate drive voltage waveforms but results in turn-on/turn-off time widening. On the other hand, if R_G values need to be lowered to optimize the energy losses at turn-on and turn-off, the user must accept the possibility of spurious gate driving waveforms.

7.3 Minimizing common source inductance: layout optimization and Kelvin source connection on STW77N65M5

The negative impact on turn-on and turn-off energy losses, due to the source inductance, can be minimized by taking particular care of the layout during the design phase: the gate driving loop should be as short as possible to minimize the total parasitic loop inductance and more precisely, the common source wiring between the commutation loop and the gate loop should be as short as possible (ideally zero) to minimize the slowing action of the Ls on the drain current. This could be accomplished by placing the driving stage GND directly connected to the source pin of the switch or very close to it, as shown in *Figure 47*.

Figure 47. Gate driving and main switching loops for a MOSFET in a BOOST-like topology



A simple clamped inductive load circuit test was adopted to evaluate the differences between two layout configurations and their respective effect on the switch performance. It's important to remark that all layout options described in the following sections have been implemented on the same test circuit.

All tests have been carried on the STW77N65M5, as the advantage offered by the layout optimization and the 4-pin solution (which is described shortly) is as important as high current levels are involved.

In the first layout configuration, the common source path between the main switching loop and the driving loop is a few cm long, while in the second layout configuration, the common source path has been shortened to the length of the source pin. In both cases, the drain parasitic loop inductance has been neglected thanks to a very short distance between the bus capacitors and the switch. The following curves show the E_{on} and the E_{off} energies of STW77N65M5 which were issued with the same R_G, gate driving signal (0 V to 10 V), and V_{DD}=400 V conditions.

Figure 48. STW77 energy ON difference between the standard layout and the optimized layout

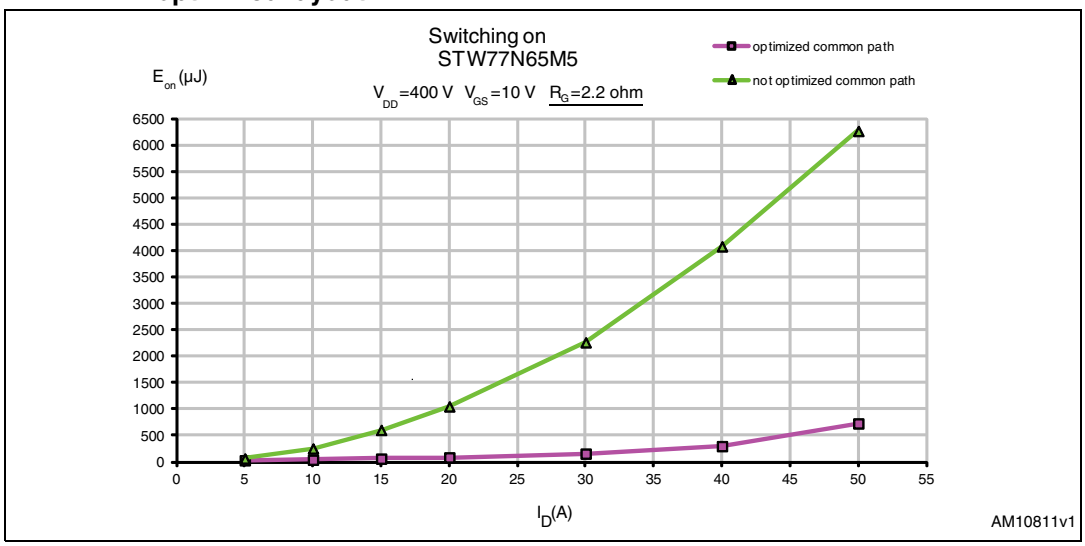


Figure 49. STW77 energy OFF difference between the standard layout and the optimized layout

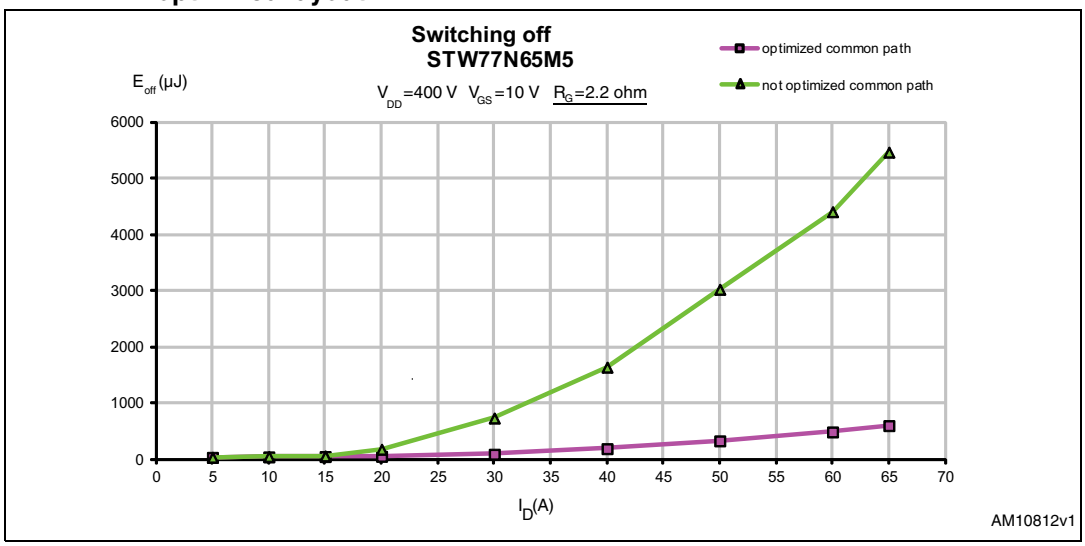


Figure 50. STW77N65M5 E_{off} @ 20 A, 2.2 Ω with non-optimized common path

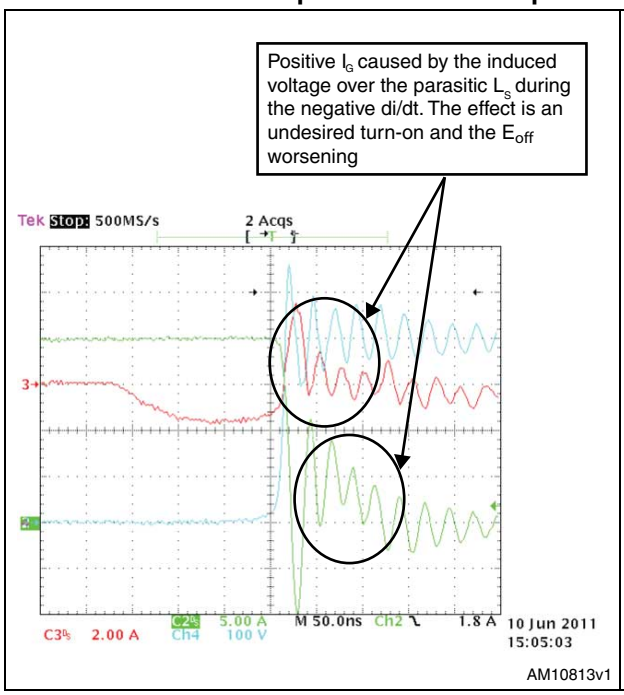


Figure 51. STW77N65M5 E_{off} @ 20 A, 2.2 Ω with non-optimized common path

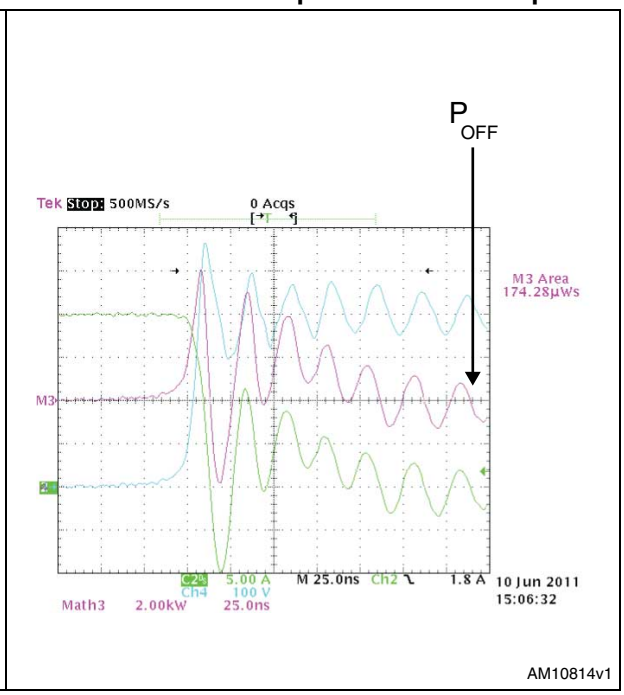


Figure 52. STW77N65M5 E_{off} @ 20 A, 2.2 Ω with optimized common path

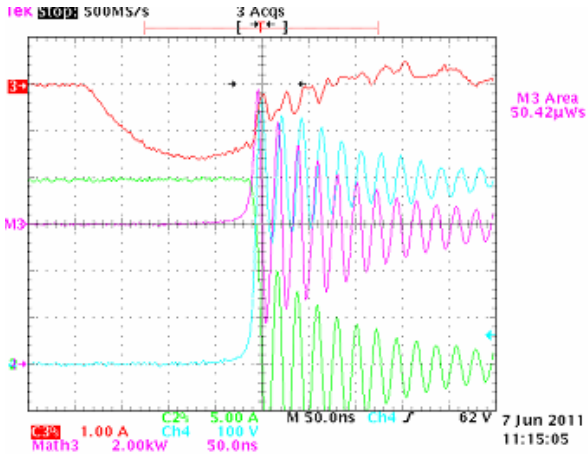


Figure 53. STW77N65M5 E_{off} @ 40 A, 2.2 Ω with non-optimized common path

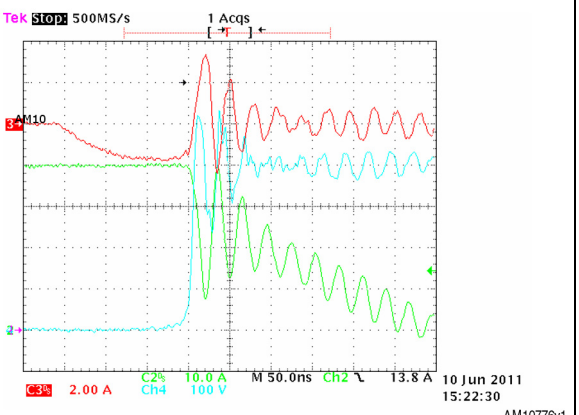


Figure 54. STW77N65M5 E_{off} @ 40 A, 2.2 Ω with non-optimized common path

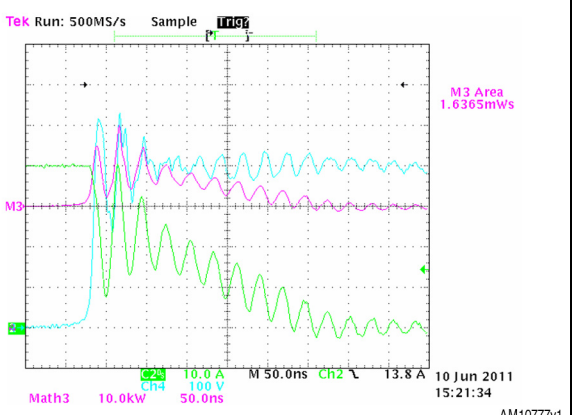


Figure 55. STW77N65M5 E_{off} @ 40 A, 2.2 Ω, 400 V with optimized common path

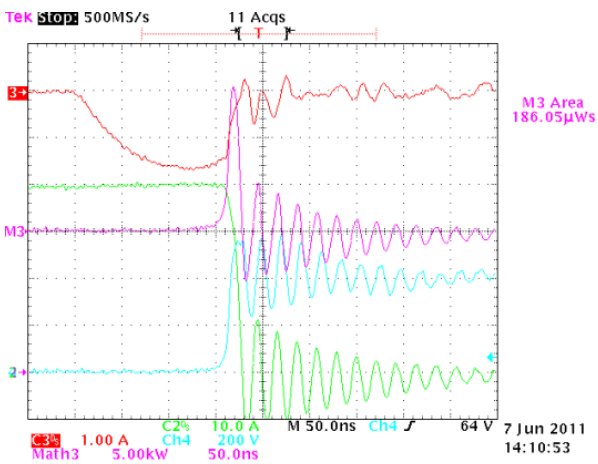


Figure 56. STW77N65M5 E_{on}@20 A, 2.2 Ω with non-optimizedcommon path

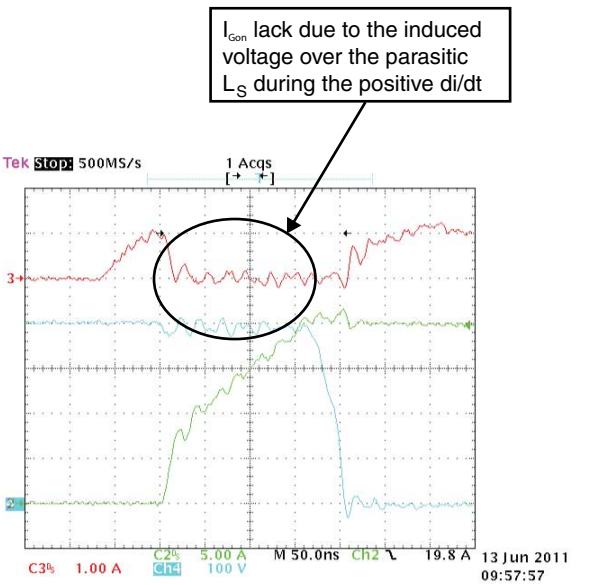


Figure 57. STW77N65M5 E_{on}@20 A, 2.2 Ω withnon-optimizedcommon path

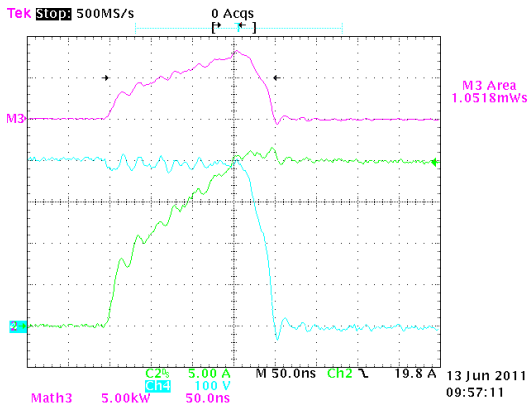


Figure 58. STW77N65M5 E_{on}@20 A, 2.2 Ω withoptimizedcommonpath

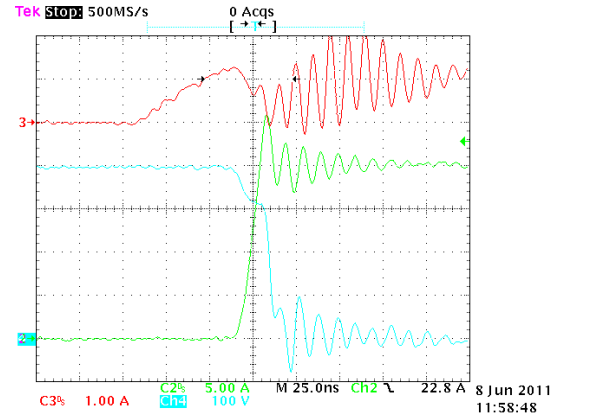


Figure 59. STW77N65M5 E_{on}@20 A, 2.2 Ω withoptimizedcommonpath

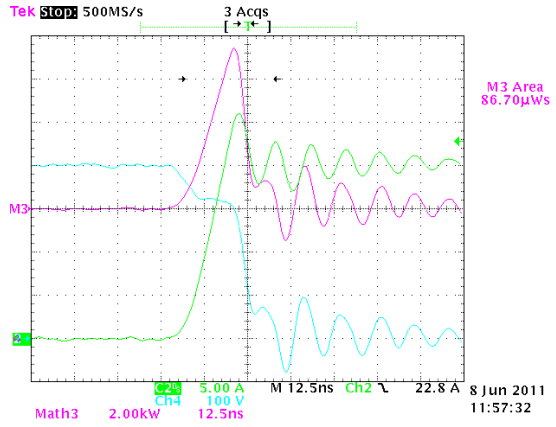


Figure 60. STW77N65M5 E_{on}@40 A, 2.2 Ω with non-optimized common path

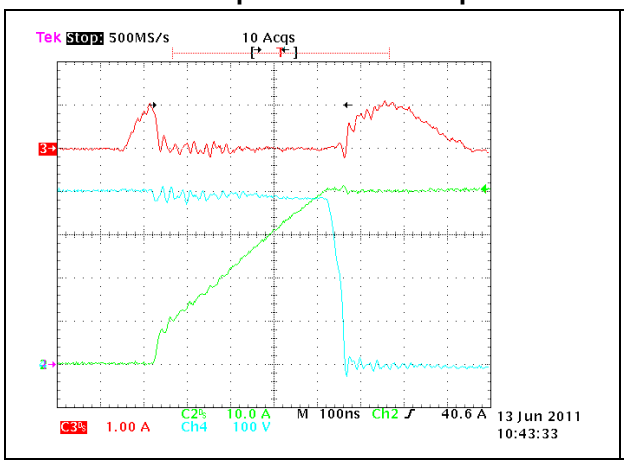


Figure 61. STW77N65M5 E_{on}@40 A, 2.2 Ω with non-optimized common path

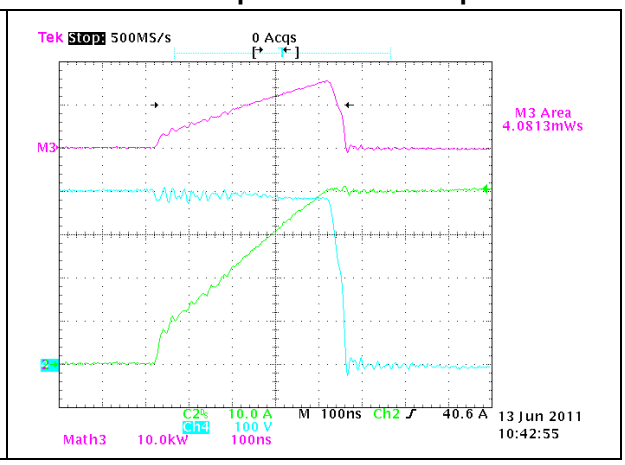


Figure 62. STW77N65M5 E_{on}@40 A, 2.2 Ω with optimized common path

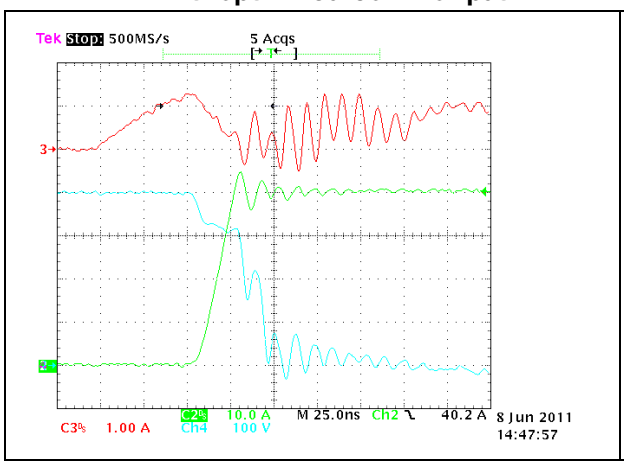
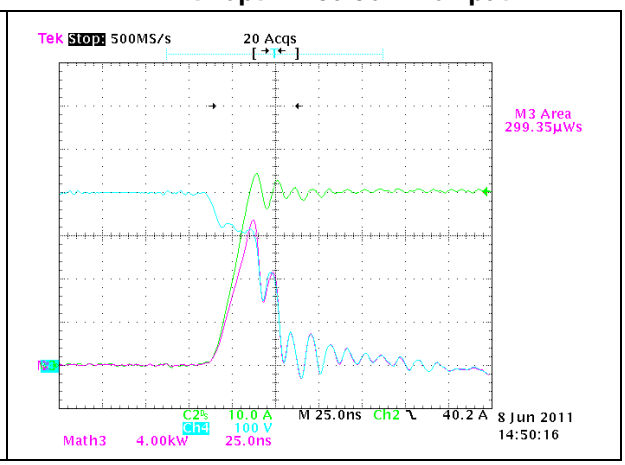


Figure 63. STW77N65M5 E_{on}@40 A, 2.2 Ω with optimized common path

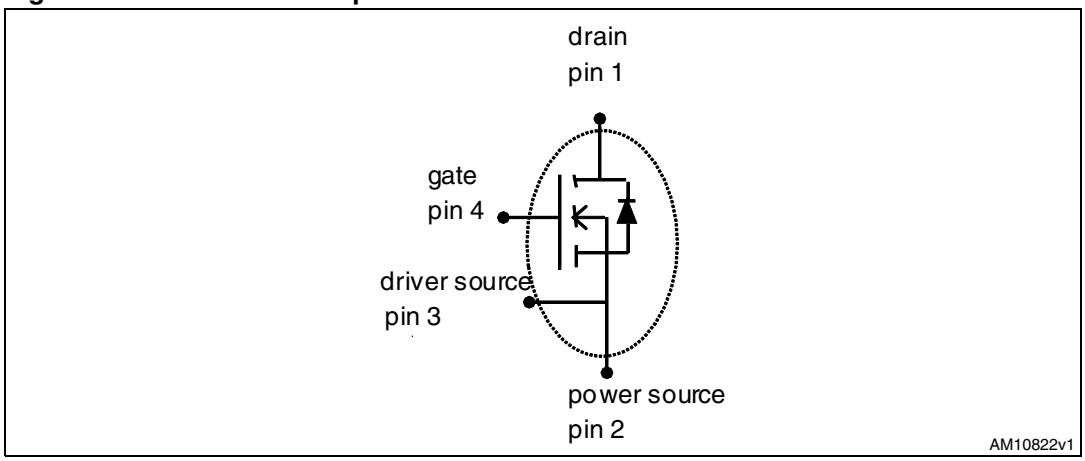


The impact of the parasitic inductance becomes heavier as the current increases, as clearly shown by the trend of E_{on} and E_{off} in *Figure 50* and *63*.

The turn-on is impacted more by the parasitic Ls rather than the E_{off}, as the di/dt starts at the very beginning of the turn-on phase, just after the V_{GS} has reached the threshold. In this situation the dI/dt and the V_{GS} are severely slowed down and the plateau region is greatly widened even if low R_G values are used. So, as evident from *Figure 60*, the main contribution over the IV cross is provided by the di/dt portion.

As for turn-off, the first part of the IV cross during the plateau region is not affected by the L_s, and can be sped up by adopting a proper R_G value. Additionally, the voltage across the switch rises in the last portion of the plateau region, due to the particular output capacitance dependence with voltage; so, this first contribution on the total energy OFF is negligible and independent of L_s. As voltage across the switch reaches the clamp value, the I_D drops down: the Ls acts during this phase, but its impact is not heavy, as clear from the waveforms in *Figure 54*.

Figure 64. Schematic of 4-pin solution



The best way to minimize the inductance influence is to adopt the Kelvin source connection (see *Figure 64*); this solution dramatically cuts the common path between the drain current and the gate current as the Kelvin pin is directly referenced to the driving stage GND. The result is that the energy losses are reduced and the rate of drain current during transients is sped up. *Figure 65* and *66*, showing the differences in terms of energy ON and energy OFF between a standard 3-pin with an optimized layout and the 4-pin, refer to the same PCB circuit of the previous sets of experimental waveforms of *Figure 48* and *49*: this leads to the obvious conclusion that the 4-pin solution allows the user to speed up the SJ MOSFET with excellent results, not reachable by the 3-pin solution even if optimized in terms of layout configuration.

Figure 65. STW77N65M5 energy ON difference between the optimized layout (3-pin) and 4-pin solution

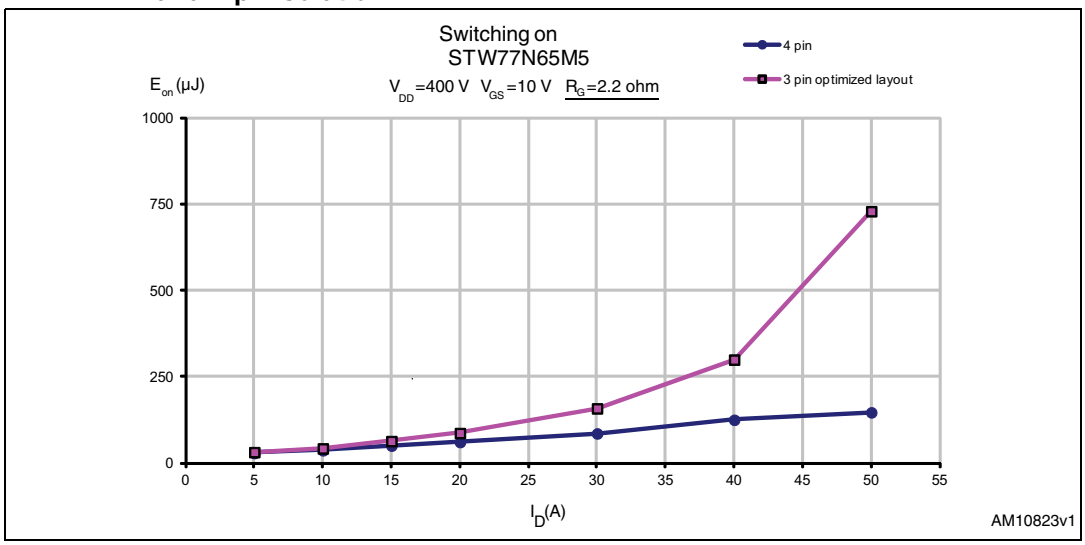


Figure 66. STW77N65M5 energy ON difference between the optimized layout (3-pin) and 4-pin solution

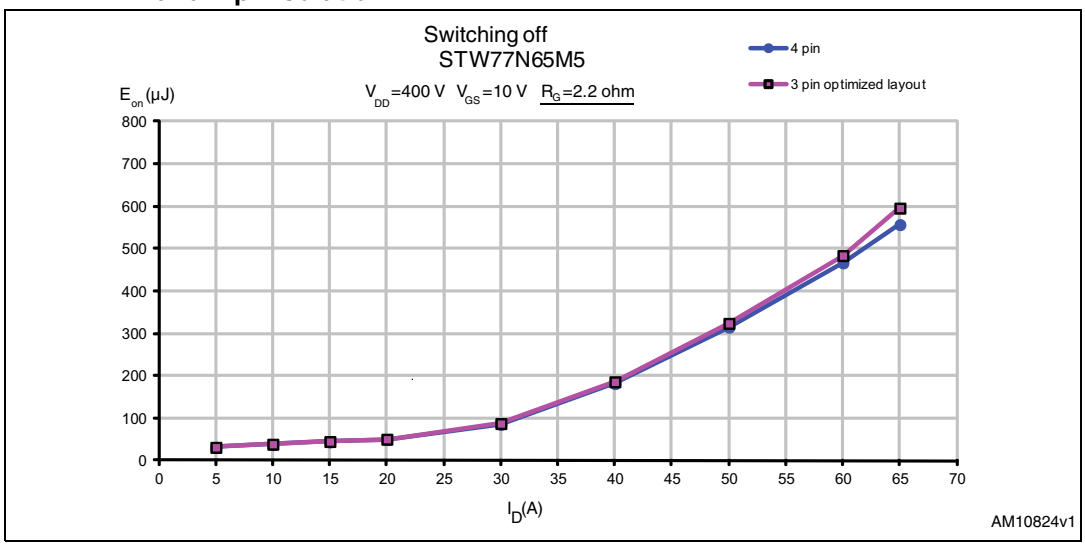


Figure 67. STW77N65M5 energy OFF difference between the optimized layout (3-pin) and 4-pin solution

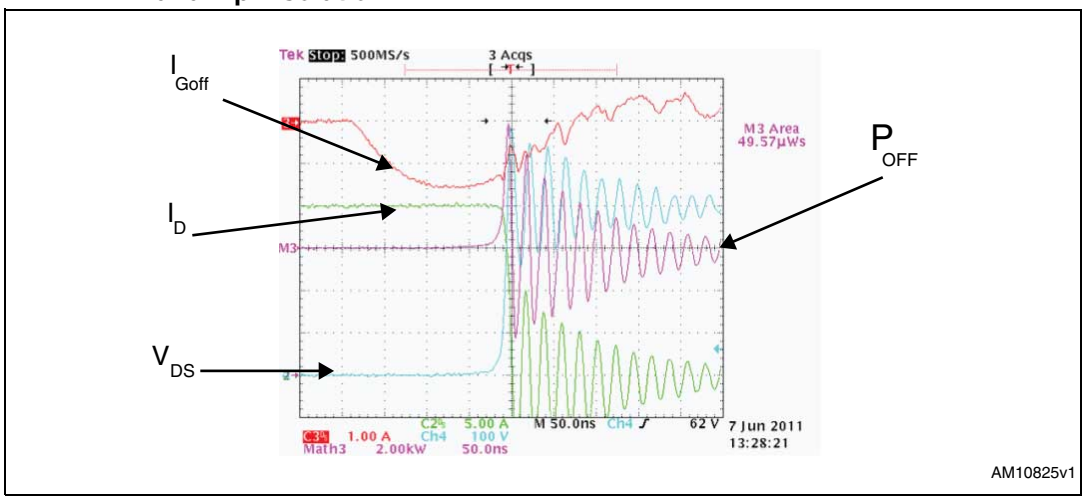


Figure 68. STW77N65M5 E_{off}@20 A, 2.2 Ω, 400 V 4-pin solution

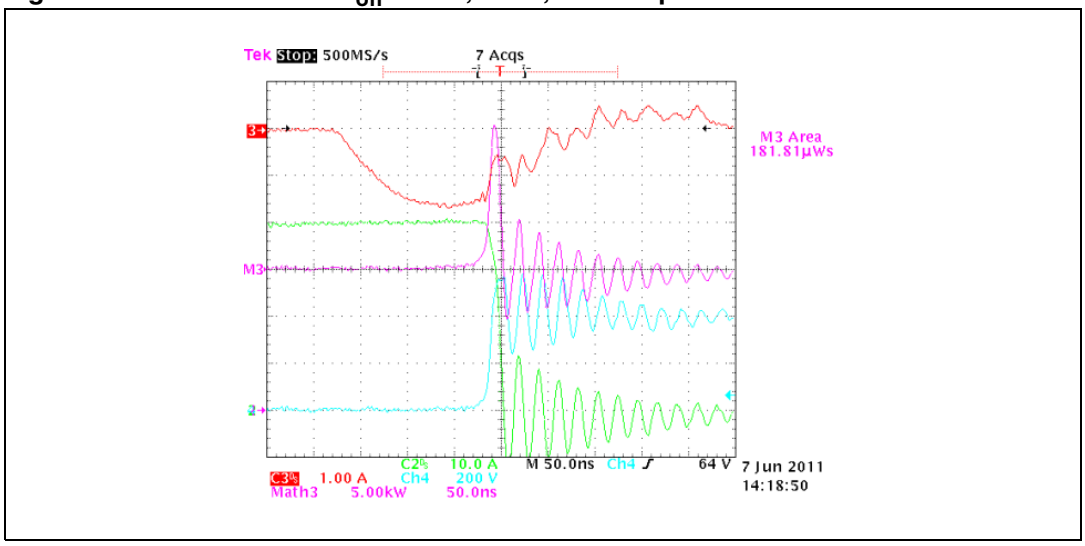


Figure 69. STW77N65M5 E_{on}@20 A, 2.2 Ω 4-pin solution

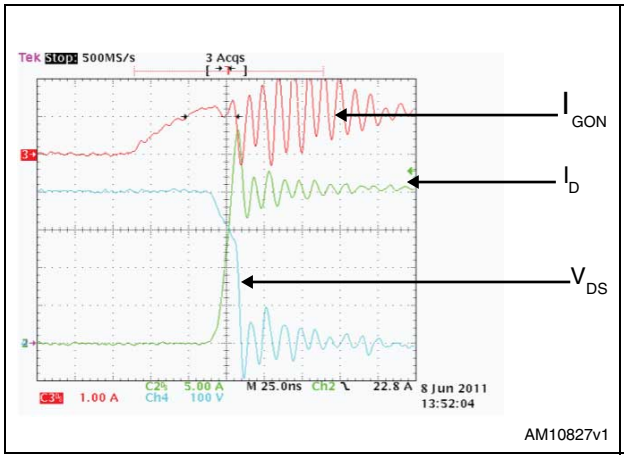


Figure 70. STW77N65M5 E_{on} @20 A, 2.2 Ω 4-pin solution

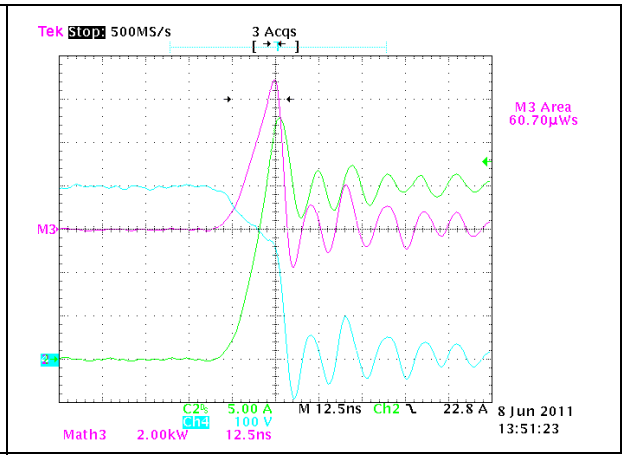


Figure 71. STW77N65M5 E_{on}@40 A, 2.2 Ω 4-pin solution

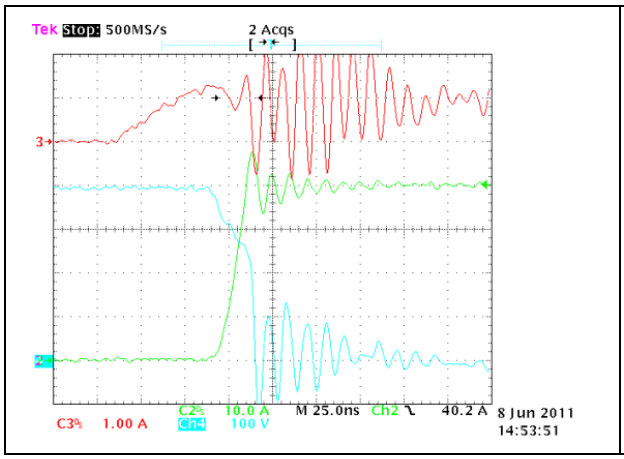
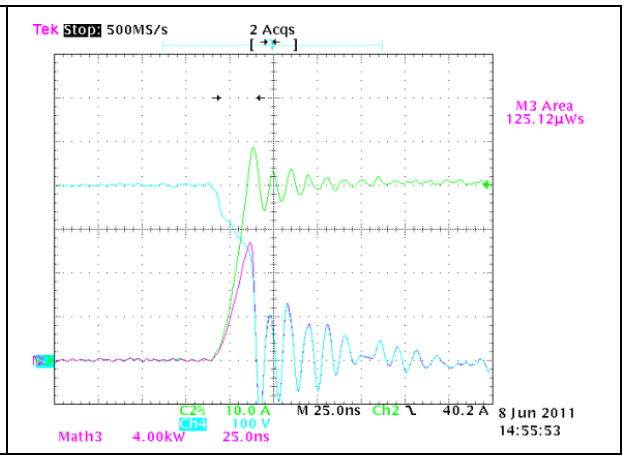


Figure 72. STW77N65M5 E_{on}@40 A, 2.2 Ω 4-pin solution



7.4 Minimizing common source inductance impact at turn-off: negative V_{GMoff}

Threshold voltage for the Power MOSFET has a negative temperature coefficient and this aspect must be carefully considered especially at turn-off, when parasitic inductances resonate with the output MOSFET capacitor and lead to oscillations in gate to source voltage waveforms. If threshold voltage is lowered because of high operation temperature, the risk of unwanted turn-on significantly increases.

In order to improve the MOSFET immunity against noise, a negative V_{GM} during turn-off is suggested.

The negative bias at turn-off also counterbalances the induced voltage VLs across the common source inductance (which is negative if referred to *Figure 73*).

If the negative V_{GMoff} is properly chosen to avoid any gate oxide damages, it contributes to the reduction of the positive gate charge amount injected during the I_D falling down and consequently to the reduction of the negative L_s impact on energy losses.

Figure 73. Basic driving stage of a Power MOSFET at turn-off with negative V_{GM}

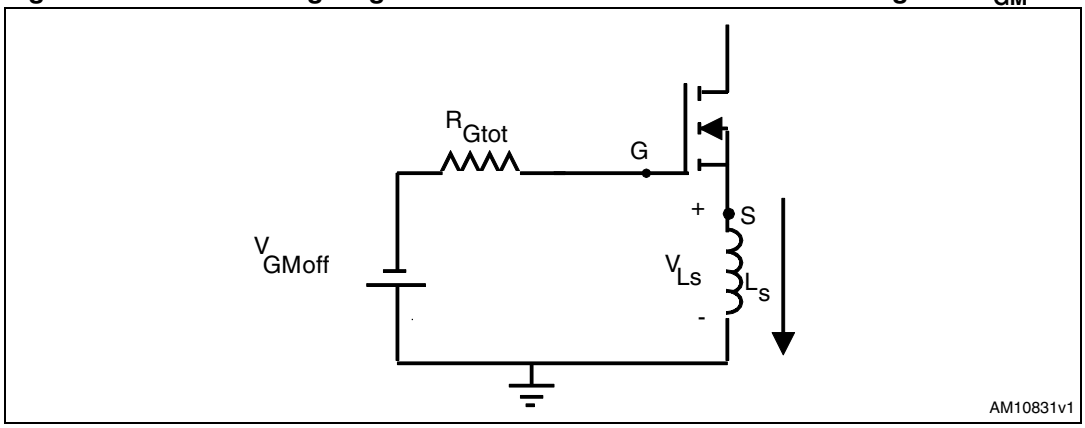


Figure 74 shows the STW77N65M5 turn-off at the test conditions below:

- V_{DS}=400 V
- I_D=52 A
- V_{GMoff}=0 V
- R_{Goff}=4.7 Ω

Figure 74. STW77N65M5 E_{off}@52 A, 4.7 Ω, 400 V, V_{GMoff}=-5 V

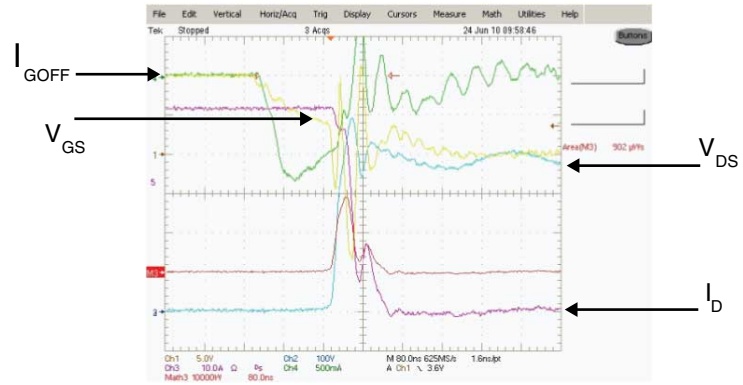
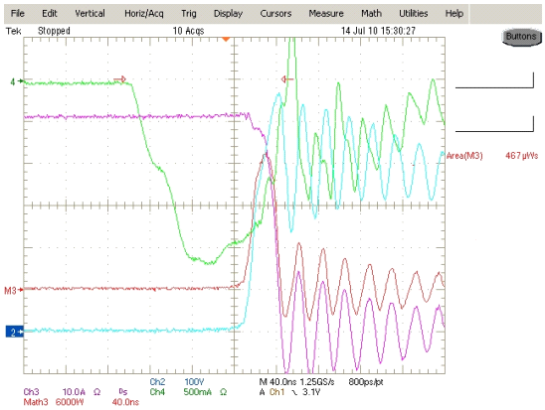


Figure 75 shows the STW77N65M5 turn-off when the negative bias voltage is adopted under the same test conditions and the same layout configuration:

- V_{DS}=400 V
- I_D=52 A
- V_{GMoff}=-5 V
- R_{Goff}=4.7 Ω

Figure 75. STW77N65M5 E_{off}@52 A, 4.7 Ω, 400 V, V_{GMoff}=-5 V



By comparing the two turn-off waveforms, it's clear that negative bias contributes to the speeding-up of the drain current falling down and to drastically reduce the energy losses at turn-off.

In this specific test, the energy OFF with negative V_{GM} is about half of the standard zero gate bias.

7.5 Switching loop inductance

The main switching loop inductance comprises several components along the power circuit, including the internal inductances of the MOSFET and the diode packages, rather than the PCB interconnections. The voltage across Ls during turn-off transient (phase of the negative di/dt) results in high voltage V_{DS} overshoot which can exceed the bus voltage and lead to MOSFET failure. Additionally, the drain inductance resonates with the MOSFET or diode capacitance, causing severe ringing over the voltage and current waveforms.

The L_D impact on the turn-on waveform has been analyzed in *Section 7.1*.

It's not easy to control the parasitic component of the switching loop as it is commonly wider than the other paths. Anyway, it is best to take care of it during the design phase in order to further improve the MOSFET dynamic performances.

8 Revision history

Table 4. Document revision history

Date	Revision	Changes
02-Dec-2011	1	Initial release.