AN3960
Application note

ESD considerations for touch sensing applications

Introduction

Electrostatic discharge (ESD) is not a new phenomenon. It is often used to describe high voltage that may produce permanent damage. ESD can be destructive and may leave a sytem in an unknown state from which recovery is impossible. Fortunately, it can be prevented by several methods. Some of these methods are cheap whilst some modify the behavior of the equipment. The ideal situation is to balance both of these factors to obtain a robust application which is not too expensive and which is unlikely to behave erratically.

This document describes ESD, its causes and risks. Several models and standards relating to ESD simulation are outlined. Typical ESD protection techniques are explained. Test results are presented for the STM8T142-EVAL evaluation board which was tested against ESD events using some of the protection methods detailed in this application note.

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1 What is ESD ?

ESD is the sudden and momentary electric current that flows between two objects at different electrical potentials.

ESD immunity is a category of electromagnetic compatibility (EMC) - the branch of electrical sciences which studies the unintentional generation, propagation and reception of electromagnetic energy with reference to its unwanted effects.

EMC describes the ability of a piece of equipment or a system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment.

1.1 Causes of ESD

One of the causes of ESD events is static electricity. Static electricity is often generated through the separation of electric charges when two materials are brought into contact and then separated, for example, rubbing a plastic comb against dry hair, removing some types of plastic packaging. In these cases, the friction between two materials creates a difference of electrical potential that can lead to an ESD stress.

Another cause of ESD damage is through electrostatic induction. This occurs when an electrically charged object is placed near a conductive object isolated from ground. The presence of the charged object creates an electrostatic field that causes electrical charges on the surface of the other object to redistribute. Even though the net electrostatic charge of the object has not changed, it now has regions of excess positive and negative charges. An ESD stress may occur when the object comes into contact with a conductive path. For example, charged regions on the surfaces of styrofoam cups or plastic bags can induce potential on nearby ESD sensitive components via electrostatic induction and an ESD stress may occur if the component is touched with a metallic tool.

2 Risks of ESD

ESD is a serious issue in solid state electronics, such as integrated circuits (ICs). ICs are made from semiconductor materials such as silicon and insulating materials like silicon dioxide. Either of these materials can suffer permanent damage when subjected to high voltages.

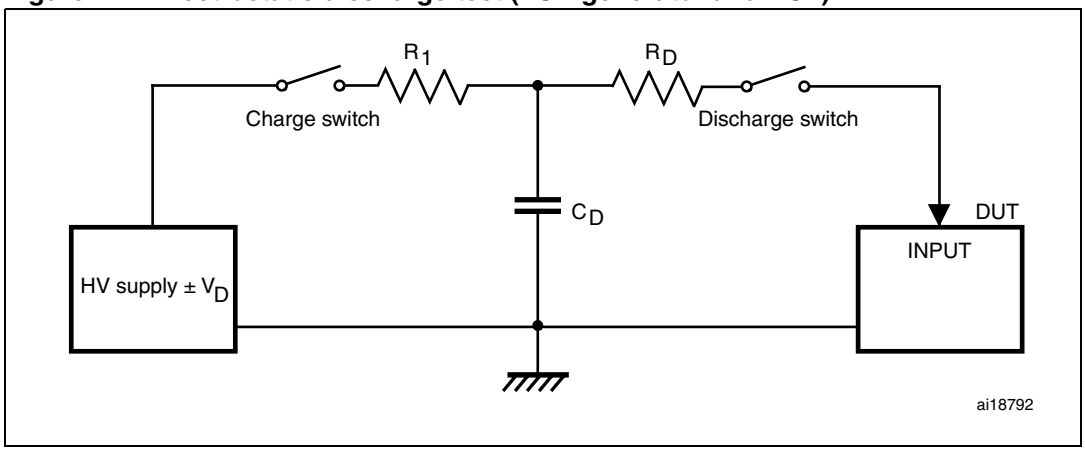
The damaging effects of ESD poses unacceptable risks in many areas of technology and it is necessary to control such interference and reduce the risks to acceptable levels through the:

- Simulation and testing of electronic devices using models
- Definition of standards

2.1 Simulation and testing of electronic devices using models

Several models describe how to simulate an ESD stress. The schematic circuit of *Figure 1*, shows how to generate an ESD event to a device under test (DUT). It is the basis of these models.

Figure 1. Electrostatic discharge test (ESD generator and DUT)



1. Legend: R_1 = resistor 1, R_D = discharge resistor, C_D = discharge capacitor, HV = high voltage, and V_D = discharge voltage. R_1, R_D, and C_D are defined according to a standard.
2. The charge and discharge switches are not closed simultaneously.

2.1.1 Human body model (HBM)

For testing the susceptibility of electronic devices to ESD stress from human contact, an ESD simulator with a special output circuit called the human body model (HBM) is often used.

This model simulates the discharge which might occur when a human touches an electronic device (either a system or a component).

The HBM consists of a capacitor in series with a resistor (see *Figure 1*). The capacitor is charged to a specified voltage from an external source, and then suddenly discharged through the resistor into an electronic terminal of the DUT.

2.1.2 Machine model (MM)

This model simulates what happens when a machine becomes electrostatically charged and subsequently discharges into an electronic device when it comes in contact with it.

The MM test circuit consists of charging up a 200 pF capacitor to a certain voltage and then discharging this capacitor directly into the DUT.

2.2 Standards overview

Standards exist for the following reasons:

- To reproduce well-defined tests in terms of their setup (bench size, type of isolating area) and conditions (such as temperature and pressure)
- To eliminate misunderstandings between manufacturers and purchasers
- To facilitate interchangeability and improvement of products
- To assist the purchaser in selecting and obtaining the appropriate product for his particular needs.

None of these reasons are paramount. Each depends on the needs of the customer who must also discuss with his purchaser.

The subsections below provide an overview of the more important ESD standards.

2.2.1 JS-001-2010 international standard

The ESD association and JEDEC solid state technology association have established a joint standard procedure for testing, evaluating, and classifying components and microcircuits according to their susceptibility to damage or degradation by exposure to a defined HBM ESD (1.5 kΩ, 100 pF and 8 kV).

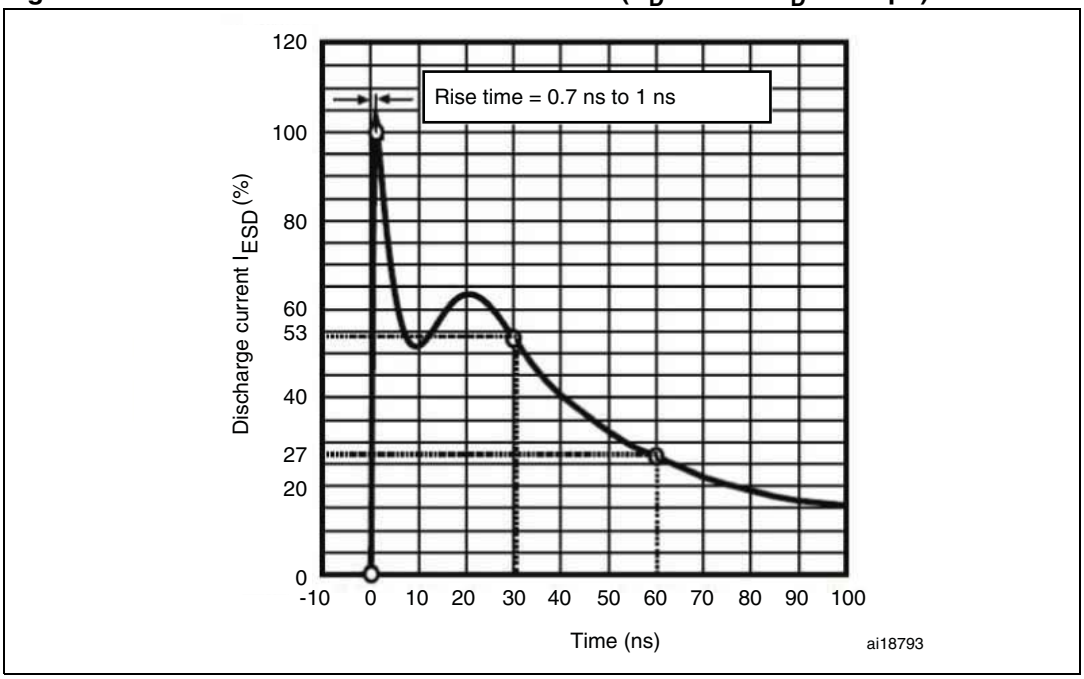
2.2.2 SP723 EIAJ IC121 standard

The SP723 EIAJ IC121 MM standard is for ensuring that the ESD capability is typically greater than 2 kV (from 200 pF) with no serial resistor. For this standard, R_D and C_D of *Figure 1* are respectively 0 Ωand 200 pF.

2.2.3 IEC61000-4-2 international standard

The IEC61000-4-2 standard for ESD protection is ±15 kV for air and ±8 kV for contact. The typical waveform of the output current of the ESD generator is described in *Figure 2*. For this standard, R_D and C_D of *Figure 1* are respectively 330 Ωand 150 pF. This standard is more accurate for performing tests at system level rather than at electronic device level.

Figure 2. IEC61000-4-2 ESD current waveform (R_D = 330 Ω/C_D = 150 pF)



2.2.4 MIL-STD-883H

This standard method classifies microcircuits according to their susceptibility to damage or degradation by exposure to ESD. For this standard R_D is 1.5 Ωand C_D is 100 pF. It is well suited for electronic device tests as ESD stress can be applied directly onto its pins.

2.2.5 ESD standard summary

An application has to align with one or more standards as agreed with the customer. *Table 1* summarizes the test conditions for the ESD standards.

Table 1. Test conditions for ESD standards

Standard	Model	R_D	C_D	±V_D
JS-001-2010	HBM	1.5 kΩ	100 pF	8 kV
SP723 EIAJ IC121	MM	0 Ω	200 pF	2 kV
IEC61000-4-2 (level 4)(1)	HBM and air discharge	330 Ω	150 pF	15 kV
	HBM, and direct discharge	330 Ω	150 pF	8 kV
MIL-STD-883H (class 3B)(2)	HBM	1.5 kΩ	100 pF	8 kV

1. Level 4 = maximum level of test voltage in the IEC61000-4-2 standard.
2. Class 3B = maximum level of test voltage in the MIL-STD-883H standard.

When an ESD event occurs, the standards outlined in *Section 2.2* describe four test results which can occur in a real application.

2.2.6 Test results of ESD standards

The test results are as follows:

- Normal performance continues within the specification limits
- Temporary degradation or loss of function or performance which is self-recoverable
- Temporary degradation or loss of function or performance which requires operator intervention or system reset (the operator can be the end user)
- Degradation or loss of function which is not recoverable due to damage of equipment (components) or software, or loss of data.

The risks of failure are the same for touch sensing application as for other applications. When a touch occurs, the system or equipment can fail if it is not sufficiently robust.

3 Protecting against ESD

An effective approach for protecting any electronic system against ESD is to mechanically minimize the pathways by which high voltages enter the system from the outside environment. This can be especially difficult if the user needs to touch the application or if there is a void or other opening in the packaging.

Mechanical switches and control potentiometers are classic system entry points for ESD stress. Changing from mechanical controls to capacitive touch controls eliminates the voids for these traditional ESD entry paths.

Some methods which protect against ESD stress include:

- Dielectric overlays (see *Section 3.1*)
- Spark gaps (see *Section 3.2*)
- Ground rings (see *Section 3.3*)
- Adding resistance (see *Section 3.4*)
- Adding diodes (see *Section 3.5*)
- ESD protection devices (see *Section 3.6*)
- Firmware (see *Section 3.7*)

3.1 Dielectric overlays

In the touch sensing application domain, a protective layer of "dielectric" material (any insulating material that can intrinsically withstand high voltages without breaking down) can be placed between the ESD source and the touch sensing application. For example, one layer of 5 mil Kapton® tape withstands 18 kV. Other dielectric overlay materials are listed in *Table 2* together with their dielectric strengths.

Table 2. Dielectric overlay materials and their dielectric strength

Material	Breakdown voltage[1] (V/mm)	Min. overlay thickness at 12 kV (mm)
Air	1200–2800	10
Dry wood	3900	3
Common glass	7900	1.5
Borosilicate glass, e.g. Pyrex®	13000	0.9
Polymethyl methacrylate (PMMA) plastic, e.g. Plexiglas®	13000	0.9
Acrylonitrile butadiene styrene (ABS) plastic	16000	0.8
Polycarbonate, e.g. Lexan®	16000	0.8
Formica plastic	18000	0.7
FR-4[2]	28000	0.4
Polyethylene terephthalate (PET) film, e.g. Mylar®	280000	0.04
Polymide film, e.g. Kapton®	280000	0.04

1. The breakdown voltage of an insulating material is the minimum voltage that causes a portion of the insulator to become electrically conductive.
2. FR-4 is a widely accepted international grade deignation for fiberglass reinforced epoxy laminates that are flame retardant.

Use of the dielectric overlay is effective and is almost mandatory for many applications however, there are some drawbacks, namely that the overlay does not surround the whole application and that an ESD event can bypass the overlay. If the user can avoid accessing the application through the front panel (example, by accessing it from the back or elsewhere) or if the ESD event can bypass the front panel, one of the other methods which protect the device against an ESD event should be considered.

3.2 Spark gaps

Physical techniques, such as the addition of spark gaps, can give supplementary protection to the input/output lines of a circuit board which are susceptible to extraneous voltage such as ESD. For example, printed circuit board (PCB) spark gaps can be used to route ESD to earth in products using capacitive sensing electrodes (see *Figure 3: PCB with spark gap*).

A spark gap consists of an arrangement of two conducting electrodes separated by a gap usually filled with a gas such as air which is designed to allow an electric spark to pass between the conductors. When the voltage difference between the conductors exceeds the gap's breakdown voltage, a spark forms, ionizing the gas and drastically reducing its electrical resistance.

The spark gap shown in *Figure 3* is an 8 mm gap which is a common PCB tolerance. The approximate breakdown of such a small spark gap is given in *Equation 1*.

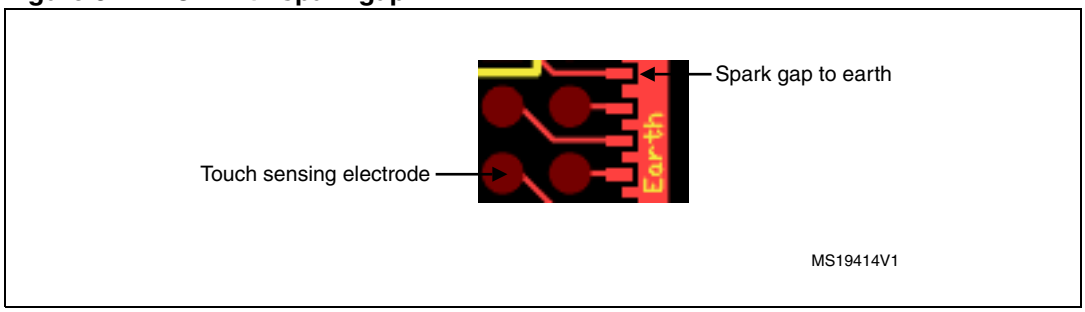
Equation 1

$$V = (3000 \times p \times d) + 1350$$

Where p is the pressure in atmospheres and d is the distance in millimetres.

This spark gap can be expected to have a peak voltage of about 2000-2500 V.

Figure 3. PCB with spark gap



1. The contact area of this spark gap needs to be free of solder resist, in order to function as a spark gap.

3.3 Ground rings

To protect against ESD stress on the touch sensing surface, a low impedance path to ground must exist through the device. The touch sensor can be protected using a ground ring (also called a guard ring) which is a ring around all the system electrodes (see *Figure 4: Ground ring*). It is placed in the border area. The ground ring can be a simple metal foil. It is necessary to ensure that there is a firm connection between the ground ring and the device system ground.

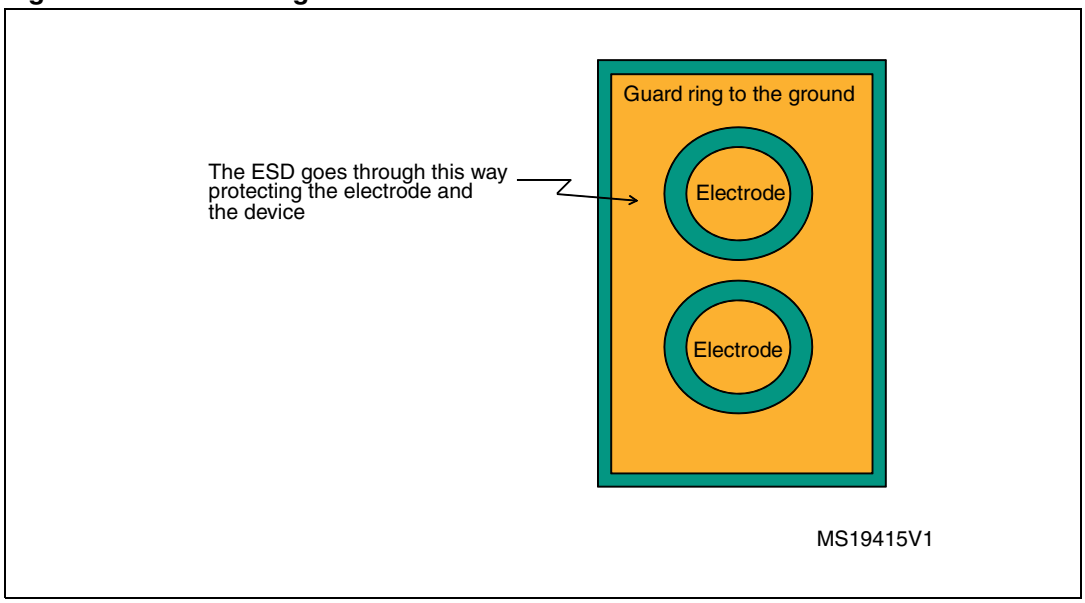
If the product is densely packed, it may not be possible to prevent an ESD stress. Consequently, the touch sensing device can be protected by controlling where the discharge occurs. This can be achieved through a combination of the:

- PCB layout
- Mechanical layout of the system
- Conductive tape or other shielding material

These three items avoid an ESD stress reaching the electrodes (and therefore the MCU) because they form a sufficient shield. For example, an ESD stress goes directly to ground if it occurs in the ground ring.

As recommended in "*PCB Layout Guidelines*", providing a hatched ground plane around the touchkey or rotary or linear sensors (other types of electrode with different shapes) can redirect the ESD stress away from the electrodes and touch sensing device.

Figure 4. Ground ring



3.4 Adding resistance

The most common method of external ESD protection is to add a small serial resistor in-line between the ESD energy source and the touch sensing device pin to be protected. A resistor as small as 50 Ω can double the ESD immunity of a CMOS device. A higher level of protection is somewhat proportional to increased serial resistance so, higher immunity is possible.

This method works for two reasons. First, the serial resistor works with the parasitic pin capacitance (typically 5 to 10 pF) of the device to create a single-pole low pass filter with a cutoff frequency below 1 GHz. This causes the serial resistor to attenuate most of an ESD event's high-frequency energy (as much as 90 % of the rising-edge power in an HBM discharge). Second, when the protection circuits of the device are operating normally, their impedance is very low (in the order of tens of ohms or less). This low impedance works with the serial resistor to create a voltage divider, so that the high voltage from an ESD stress can only bias the built-in protection circuits of the device with a portion of the total ESD voltage. This attenuation is in addition to rising-edge filtering. The sum of these effects from a simple external serial resistor dramatically improves ESD performance in a demanding application.

3.5 Adding diodes

Input/output lines that are susceptible to ESD stress are sometimes protected by adding ‘external’ diodes which shunt the high energy of the ESD stress before it can reach the device input pin. These diodes may either pass the current to the power supply rails or they may internally dissipate the unwanted power. External diodes are similar to the diodes built into a device (internal diodes) for protection but, they are designed differently. External diodes have two significant advantages:

- They can switch faster and at a lower excursion voltage than the internal diodes of the device.
- They can have much better connections to the supply rails and can carry more power.

The effects of external diodes on circuit operation are different from internal diodes, because the connections used internally cannot be achieved with external devices.

Two types of protection diode are typically used against ESD stress. Zener diodes or transient voltage suppression (TVS) avalanche diodes can be placed between an input signal and ground. In this configuration, the diode protects the CMOS input by reverse conduction whenever its voltage rises above the specified diode breakdown voltage. Negative ESD excursions are shunted to ground through normal diode action. In another configuration, diode pairs (typically Schottky diodes due to their lower forward voltage drop) are placed between the input line and the power and ground rails. These devices protect the CMOS input by normal diode conduction whenever the input line voltage moves outside the range of the power supply rails.

Diodes placed on capacitive sensed lines present the same problems to capacitive sensing circuits as they do with any analog circuit input: they can be highly capacitive (over 100 pF) and leaky. Some Schottky pairs leak over 20 µA; some avalanche diodes leak over 1 mA when operated near their reverse-standoff voltage (generating significant noise voltage as well). Although these given numbers are for the least suitable devices, the most commonly-used Schottky and TVS diodes have parasitic parameters that make them unacceptable for use in capacitive sensing applications. If the diode circuit can be designed to add only a very small amount of additional capacitance, capacitance sensing solutions can be adjusted to match. This is because compensation mechanisms are usually built into the touch sensing device for adaptation to the naturally-occurring changes in capacitance that result from environmental changes. However, leakage and bulk capacitance can create problems for any sort of capacitive sensing method, some more than others.

External diodes with high reverse leakage make the test capacitance look larger because their leakage drains test current from the circuit. This disappearing test current (which should fill the capacitance under test) has no dV/dt effect on the test load. As diode leakage currents approach the level of the test current, the apparent load capacitance approaches infinity. Also, the amount of current required to detect a 0.1 pF change in capacitance is less than 20 pA, many orders of magnitude less than the leakage current for some protection diodes. For this reason, where external diodes must be used, it is essential to specify devices with extremely low reverse leakage.

The ESDAULC6 diode from STMicroelectronics was designed to resist multiple ESD stresses. It has low capacitance (1 pF) and low leakage (less than 100 nA), both of which reduce the problems encountered when using Schottky protection diodes. The bidirectional protection ESDAXLC6 diode, with even lower capacitance (0.5 pF), can be used instead of the ESDAULC6 diode to prevent the occurrence of negative and positive pulses.

Note: Although small and inexpensive, an external diode circuit can be two to four times larger and four times more expensive than adding a serial resistor.

3.6 ESD protection devices

A very effective method to protect input/outputs lines from ESD discharges is to provide special purpose ESD protection devices on the vulnerable traces. ESD protection devices for touch sensing devices need to have a low capacitance.

Table 3 lists the ESD protection devices which are recommended for use with touch sensing microcontrollers.

Table 3. ESD protection devices

ESD protection device		Input capacitance (pF)	Leakage current	Contact discharge maximum limit (kV)	Air discharge maximum limit (kV)
Manufacturer	Part number				
Littlefuse	SP723	5	5 nA (typ)	±8 kV	±15 kV
NXP	NUP1301	0.6 (typ)	30 nA	±8 kV	±15 kV
STMicroelectronics	HSP061-8M16	0.6	100 nA	±8 kV	±15 kV
Vishay	VBUS05L1-DD1	0.3	< 0.1 µA	±15 kV	±16 kV

3.7 Firmware

When permanent damage occurs, the firmware is inefficient but, irreversible damage is not always the only consideration of an ESD stress.

The maximum risk due to an ESD stress is degradation. However, in some less negative cases (such as temporary degradation or loss of function) when a simple system reset is needed, a self-recoverable application can be implemented by using the “watchdog timer on”. The system can restart from a known state and resume normal operations. The final outcome is a robust application.

The debounce firmware method is used to filter some unwanted signals and therefore helps reduce ESD stress effects.

4 STM8T142-EVAL evaluation board: ESD tests

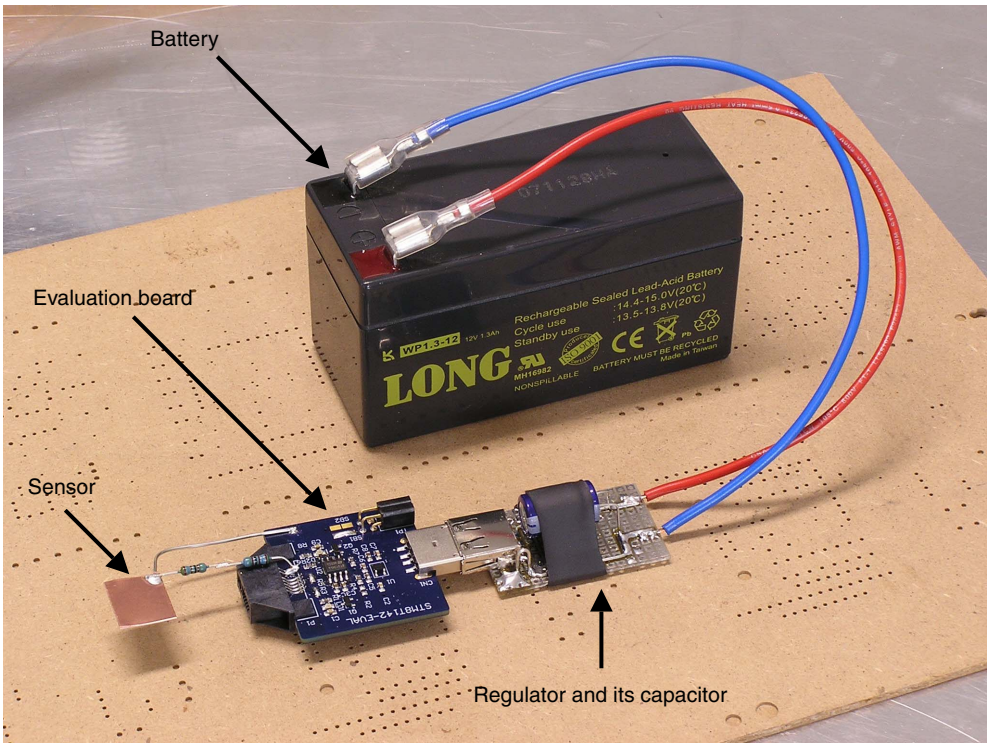
The STM8T142-EVAL evaluation board was tested against ESD stress using some of the protection methods described in *Section 3: Protecting against ESD*.

4.1 Test setup

Two ESD protection methods were tested: spark gaps and adding resistance (by testing a small serial resistor).

During the test, the STM8T142-EVAL evaluation board was supplied by a small 12 V lead-acid battery through an L7805 regulator (see *Figure 5*).

Figure 5. Test set up



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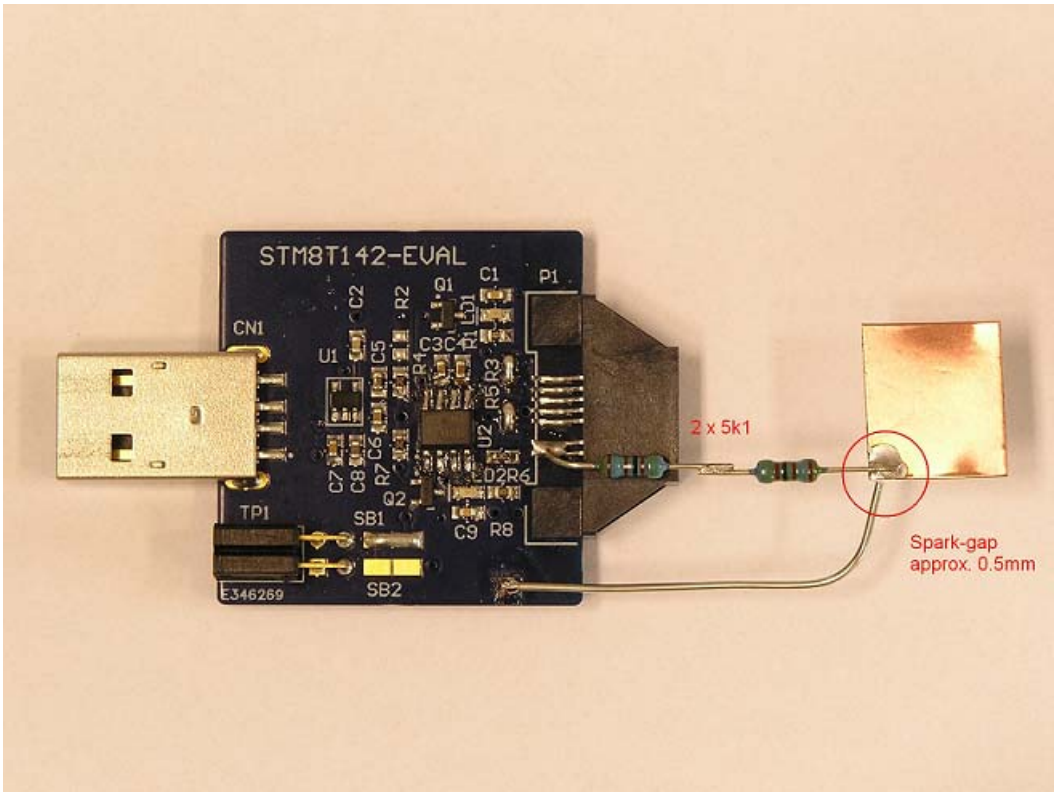
The STM8T142-EVAL evaluation board was not originally designed to take ESD stress into account:

- The onboard serial resistor (size 0603) is voltage undersized.
- The insulation distance between the electrode and the neighbouring PCB tracks is too small so that discharges can be seen directly on the device.

The following design modifications were applied (see *Figure 6*):

- A good voltage dimensioned serial resistor was used.
- Sufficient isolation distances between the electrode and neighboring PCB tracks was implemented.
- A spark gap was built to route part of the ESD energy away from the electrode to the application GND.

Figure 6. STM8T142-EVAL evaluation board modifications



4.2 Test results

Table 4. ESD discharges for tested STM8T142-EVAL evaluation board

Test condition	ESD stress through contact on the electrode(1)	ESD stress through the air
No protection	8 kV	-
With through hole resistor	12 kV	-
With through hole resistor and spark gap	> 25 kV	> 25 kV
With glass panel (0.55 mm thickness)	12 kV	-

1. The ESD stress corresponds to the limit of normal system operation (detection of touch).

5 Conclusion

Among the techniques to protect electronic systems against ESD stress, the cheapest and simplest method is to add a small serial resistor of about 50 Ω For greater robustness a diode or an ESD protection device can be added.The drawbacks of these choices are price, leakage, and input capacitance. In an environment where ESD can strike frequently, the most effective way is to use a combination of the techniques described in *Section 3: Protecting against ESD*, for example, by simultaneously using a spark gap (with a 10 kΩ serial resistor), a ground ring and robust firmware. In any touch sensing domain, most of the protection is provided by a dielectric overlay which is nearly always used. However, an ESD stress can strike from anywhere so, other methods are recommended in parrallel with a dielectric overlay.

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
03-Oct-2011	1	Initial release.