AN3400
Application note

Analysis and simulation of a BJT complementary pair in a self-oscillating CFL solution

Introduction

The steady-state oscillation of a novel zero-voltages switching (ZVS) clamped-voltage (CV) self-oscillating resonant driving system for compact fluorescent lamps (CFL), using a complementary pair of bipolar transistors on the half bridge converter section, is analyzed and simulated.

One or more auxiliary windings are added on the ballast inductor in series with the lamp in order to generate the periodic signal to supply the bases of the two complementary devices connected to each other in a common emitter half bridge topology. In fact, an LC network filters, with a resonant effect, the voltage generated by the secondary winding of the load transformer, producing a novel, periodic switching signal to accurately control the bases of the transistors. The two bipolars are supplied by a unitary control signal so it is not possible to turn on both devices at once because of their opposing base-emitter junction thresholds.

Self-oscillating operation is divided into eight stages according to the variation over a period of the driving voltage signal across the filter capacitor at the output of the transformer secondary windings. Stage-wise circuit analysis shows as the resonant filter action limits the lamp current and dominates the switching frequency of the ballast in steady-state working condition.

The half bridge of the power active devices generates a rectangular voltage waveform that drives an opportunely tuned output circuit composed of a parallel loaded RLC output circuit of which the R is the steady-state LAMP resistance. For the inverter self-oscillating condition, the switching frequency is determined by all of the circuit elements related to the oscillation frequency, such as the resonant tank, gas-discharge lamp, driving circuit, and switching devices. Depending on the circuit design, its oscillation frequency is typically around 35 to 48 kHz and can be eventually increased by shortening the storage time of the bipolars. Cost benefits are achieved by the proposed self-oscillating solution that allows to drive the CFL lamp eliminating the saturable core auxiliary transformer, placed in the more traditional standard solution, without sacrificing the performance or reducing the expected life time of the lamps.

In this paper, general structure and self-oscillating principle are discussed and verified by laboratory experiment, while analytical results are validated by mathematical simulation using the Matlab tool.

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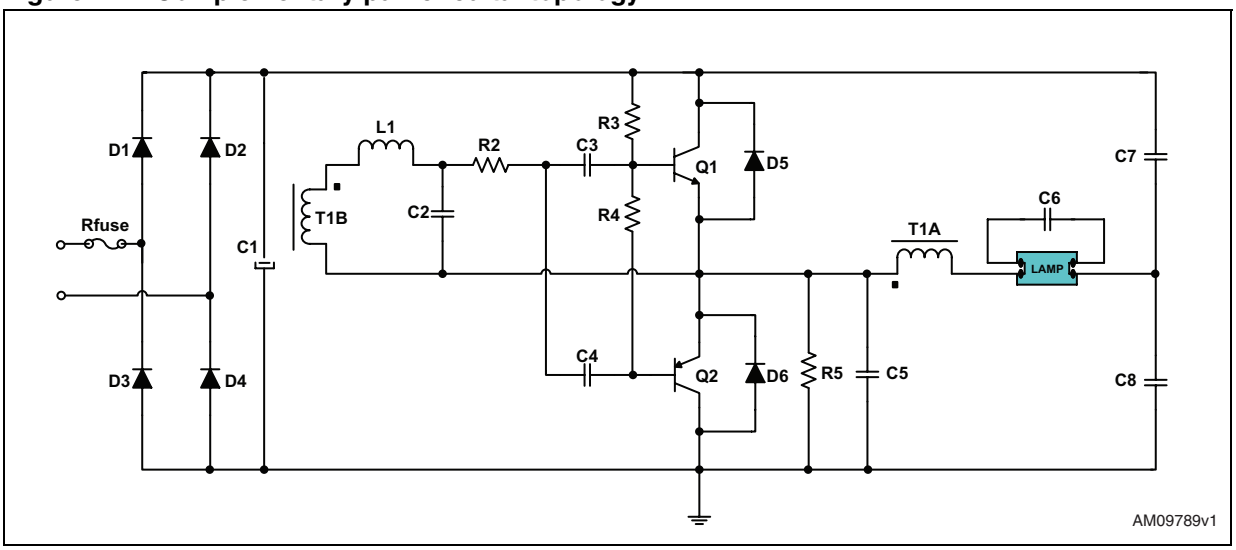
1 Circuit description

The circuit comprises a fluorescent lamp connected to a ballast inductance according to a voltage fed topology with a single voltage resonant driving system supplying the bases of two complementary bipolar transistors connected to each other in a common emitter half bridge topology.

Figure 1 depicts the complementary pair CFL board electrical schematic.

Figure 1. Complementary pair circuital topology



Based on the previous figure, the current source that flows through the load transformer T1A, is fed back through a secondary winding of the current transformer itself and, upon filtering operation of the LC network (L1-C2), is converted into a base current suitable for driving the bipolars in saturation state. Therefore, this source provides the excitation to the bases of the transistors, so that the converter oscillation is perpetuated by its own regenerative feedback means. Few additional turns (around 1-3 turns) on the ballast transformer can be added as secondary windings since the resonant effect assures that the voltage across the filter capacitor C2 results higher than that imposed by the transformer secondary (see *References 2*). Capacitors C3-C4 in series to the base, together with the magnetizing inductance of the transformer and the resonant effect of the LC filter, provide the required phase shift to maintain the oscillation condition. Soft-switching condition of the devices is achieved using the external snubber capacitor C5 inserted between the emitter and collector of the PNP bipolar Q2 to control precisely the collector-emitter voltage rise time duration and reach negligible switching losses during the turn-off switching for both bipolars. The L1-C2 network inserted at the output of the transformer secondary acts as a sinusoidal voltage generator across the C2 capacitor itself to supply the R-C network (R2-C3-C4) connected in series to the base of the transistors. All the system including the LC filter, RC driving network and RLC series load network impedance reflected from the primary side back to the secondary one of the ballast transformer, is resonant at the half bridge converter section working frequency while the single LC stage has the function of filtering the fundamental component of the voltage signal across the transformer primary opportunely lowered by the transformation ratio. In fact, the LC network should ideally be designed in order to have a cut-off frequency included between the first and the second harmonic component of the signal coming from the secondary side to filter in order to attenuate all the signal frequencies from the second one. Therefore, the half bridge section

working frequency and, consequently, the lamp power are influenced by the sizing of both L1 and C2 components. Capacitor C2 has also the function of putting the base current in phase with the collector current. Resistance R2 of the series R-C network has the function of regulating the current level to provide to the bases of both transistors acting on the power lamp. In the proposed driving solution, the two capacitors C3 and C4 are charged with opposite polarity to each other and assuming the same polarity of the base-emitter voltage of the relevant bipolar transistor. In the regular functionality, when a capacitor goes through a charging phase, before or during the conduction time of the relevant bipolar, so the opposite capacitor is discharging contemporarily with a long constant time due to the series with the breakdown resistance R4. So, this resistance R4, inserted between the bases of the two transistors, creating an alternative path for the discharge of each capacitor, also avoids that the oscillation is blocked during startup phase when one of the two capacitors is fully charged. Regulating the discharge time of each capacitor, this resistance allows to fine tune the working frequency and consequently the power supplied to the lamp. Two capacitors C3 and C4 are not totally discharged during a forcing voltage source period but maintain always a residual charge passing from the discharging to the charging transient. Therefore, current across the breakdown resistance R4 flows always in the same direction going from the PNP to the NPN base because the two capacitors maintain always the same polarity during a period of the voltage signal across the C2 filter capacitor. A breakdown resistance with a too high value can increase the working frequency but also can bring the reverse biased base-emitter junction of the inactive device in breakdown condition. And vice versa, a too low value of the breakdown resistance could cause re-conduction peaks in the PNP transistor at the high temperature when the emitter-collector voltage reaches the maximum value. In particular only the PNP device can show the phenomena above mentioned because it has a lower base-emitter breakdown voltage and it has a higher low current h_{fe} than the NPN one. Setting the resistance R4 in order to guarantee a V_{BEoff} value in the range -4 V to -7 V, it is possible to avoid breakdown phenomena for the base-emitter junctions of the bipolars and, at the same time, anomalous re-conduction effects due to unexpected disturbances.

2 Startup phase

The two bipolar transistors should have an appropriately high gain value in order to guarantee the correct ignition of the lamp during the startup phase. Compact fluorescent lamps usually require about 600 V as peak voltage to strike the arc. Once the arc is established about 100 V are enough to sustain it while, electrically, the resistance of the lamp falls from about one mega ohm down to a few hundred ohm (see *References 1*). Furthermore, the value of the load inductance L of the ballast must be chosen so that it does not saturate at the operative current of the lamp, even at high temperatures. In fact the lamp is ignited by generating an overvoltage across the capacitor C6 in parallel to the tube, through the circuit formed by the series of the ballast transformer primary inductance and C6-C7-C8 capacitors. At startup the lamp is an open circuit and the C6 capacitor imposes the resonant frequency of the circuit as C6 is much smaller than the C7-C8 ones. The imposed overvoltage is high enough to ionize almost instantaneously the gas in the lamp. Once the lamp is lighted, the capacitor C6 is short-circuited by the lamp itself and the natural frequency is determined mainly by the capacitors C7-C8 charged/discharged through the DC-AC converter. The startup network is represented by the only resistor R3, connected between the collector and the base of the high side transistor, since the capacitors in series with the bases act as a high impedance elements during the first instant of the startup.

3 Bipolar transistor operating modes

Bipolars switching in the resonant circuit have three different operating modes in normal working conditions: re-circulating, conduction and transition phases.

During the re-circulating phase, the transistor isn't yet in conduction state and passes from a first inactive state in which its B-C junction diode is activated to allow the re-circulation of load inductor demagnetization current I_{LP} shared with the external diode in anti-parallel to the device itself, to a second inactive state in which the external diode is turned off but both of the two B-E and B-C junctions are forward biased in order to complete the residual demagnetization of the Lp inductor until the forcing re-circulating current I_{LP}, that imposes the negative collector current, reaches the zero value. In conduction mode, the two B-E and B-C junctions of the transistor continue to be forward biased and the bipolar transistor conducts a positive magnetization current for the inductive load. The turn-off mechanism occurs in three stages: “storage time”, or time spent to extract the storage in excess and recombine the charge stored on the base, “current fall time”, in which the collector current passes from 90% to 10% of its maximum value, and “rise time” of the collector-emitter voltage. The transition mode occurs during the voltage rise time and represents a sort of “dead time” phase in which both bipolars are substantially inactive since only the B-C and B-E junction capacitances of both devices are interested in being charged/discharged in reverse bias. This phase anticipates the re-circulating phase preliminary to the conduction phase of the complementary device. During the turn-off process, the dynamic operation point of the transistor moves through three different operating regions on the current-voltage I_C-V_{CE} characteristic: “hard saturation region”, “quasi saturation region” and “active region”.

- Hard saturation region: at the first instance of turn-off switching time, the base-collector junction is forward biased and the base region and collector drift region are both in high-level injection condition. An excess carrier distribution fills the collector drift region and the storage time is just the time required to remove/extract this charge stored in excess. Also the contribution of charge decay due to recombination, depending on the minority-carrier lifetime, influences this phase. During the storage time process the base-emitter voltage does not change immediately from its forward bias value V_{BESAT}, due to the excess minority carriers stored in the base region, and also the collector-emitter voltage remains constant. The extent of storage time is dependent not only on the amount of excess charges remaining in the collector drift region but also on the external driving. Excess minority carriers are removed from the base region and base-collector junction at a constant rate determined by the negative base drive voltage, as well as the base drive resistance, and proportional to the reverse base current I_{Boff} slope. So the excess charge at the base-collector junction begins to reduce due to charge removal to make up for the reverse base current and the collector current continues to increase.
- Quasi saturation region: after the storage time, the forward biased base-collector junction is out of high-level injection and the remaining charges stored in the base become insufficient to support the transistor in the hard saturation region. Therefore, at this point the transistor enters quasi saturation region in which the depletion region begins to expand while a voltage appears across it and the collector-emitter voltage starts rising with a small slope. After having removed the charges in the drift region holding the bipolar in the quasi saturation region, the transistor enters the active region.
- Active region: crossing the active region, the charges stored in the base region are insufficient to support the full negative base current so the base-emitter voltage starts falling negatively and the negative base current starts reducing. Correspondingly, the stored base charges can no longer support the full load current through the collector so that also the collector current decays exponentially resulting in current fall time required

to remove remaining stored charge in base. Both of the slopes dictated by base current and collector current simultaneously decay with time due to recombination.

Collector-emitter voltage increases rapidly towards the rectified voltage upper rail V_{CC} until it is exceeded in order to turn-on the anti-parallel diode of the complementary device at the end of the rise time interval. The increasing voltage is supported across the collector drift region while the expanding depletion region at the base-collector junction sweeps out the excess charge until it totally sustains the bus voltage.

To reduce the stress on the devices, and hence the switching losses, the half bridge converter switches under zero voltage (ZVS) conditions, in which turn-on losses are absent and a favorable turn-off trajectory of power transistors can be ensured by the use of a snubber capacitor. In fact, contrary to the hard switching dynamic, in which the voltage rise was a function of the amount of charge in the drift region after the storage phase, with the soft-switching dynamic the rate of voltage rise during turn-off is controlled by the snubber capacitor connected across the device. While the voltage continues to raise, the collector current decays to zero and the load current flows into the snubber capacitor until the device voltage reaches the bus voltage. Therefore, even though turn-off does not occur at exactly zero volts, the stresses on the device are much reduced compared to hard-switching mode. When the collector current reaches the zero value, the bipolar turn-off process is completed and the load current starts to freewheel through the anti-parallel diode of the complementary device.

4 Principle of self-oscillating operation

The current through the transformer primary T1A and the resonant network at the half bridge output consists of two portions of waveforms, one when the load inductor is clamped to the upper rail at the end in common with the emitter node of the bipolars by the NPN bipolar Q1 and its anti parallel diode D5, and the other one when it is clamped by the PNP bipolar Q2 and its anti parallel diode D6 to the lower rail. The intervals, when the snubber capacitor C5 is charging/discharging while the emitter common node ramps between the rails, are generally short compared to the conduction periods. To achieve the ZVS working condition, the bipolar transistor is turned on at the end of the re-circulating phase of the residual demagnetization current from the load transformer.

Figure 2, *3*, *4*, *5* and *6*, describe the main conceptual steady-state signals related to the theoretical working principle of the proposed driving system.

These figures highlight the different operating phases of the two complementary bipolar transistors during the steady-state normal working conditions:

- Re-circulating time phases with a time length of "t_A" and "t_C" respectively for the NPN and PNP transistors
- Conduction time phases indicated with "NPN-IB_{ontime}" and "PNP-IB_{ontime}"
- Storage time phases indicated with "NPN-$IB_{storagetime}$" and "PNP-$IB_{storagetime}$"
- Dead time phases with the time length of "t_B" and "t_D" respectively for the NPN and PNP transistors.

As previously described, the "dead time phase" refers to the transient occurring during the voltage rise time and in which both of the bipolars are substantially inactive since only the B-E and B-C junction capacitances on both devices are interested in being charged/discharged in reverse bias. Moreover, from this point on and for the whole steady-state analysis subsequently explained, it is assumed to name, for the sake of simplicity, as storage time the interval including both the effective storage time and fall time of the device.

Figure 2. Steady-state waveforms: filter capacitor voltage signal (V(t)), NPN base current (I_{bnpn}) and PNP base current (I_{bpnp})

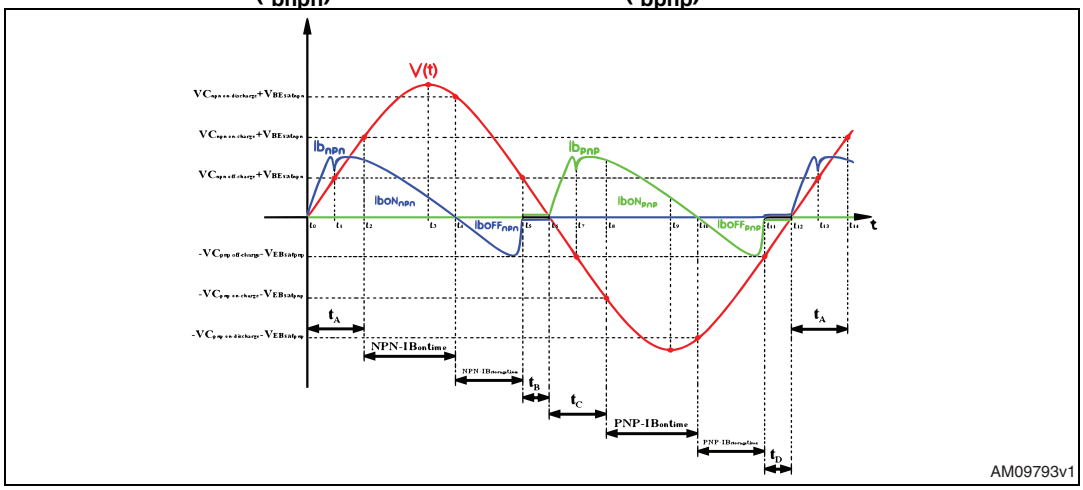


Figure 3. Steady-state waveforms: filter capacitor voltage signal (V(t)), NPN collector current (I_{Cnpn}) and PNP collector current (I_{Cpnp})

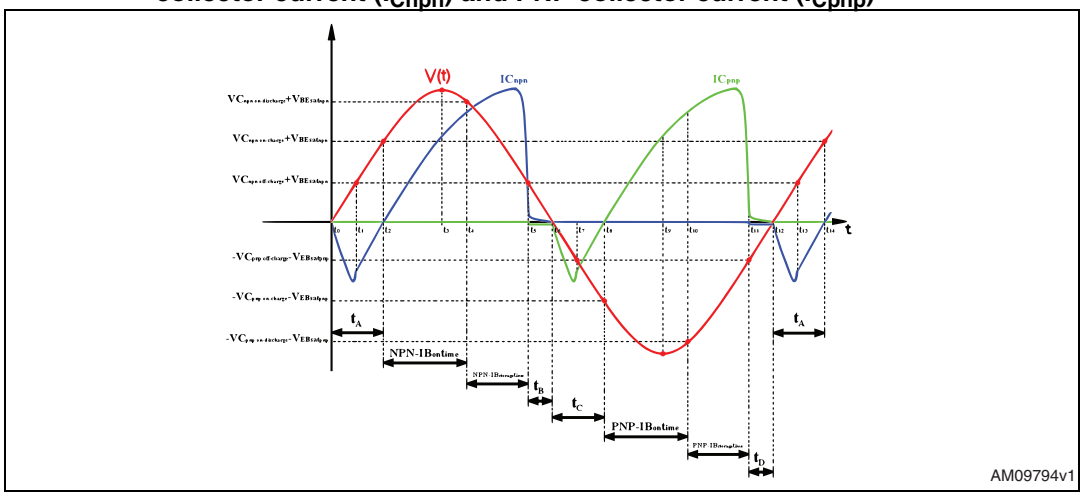


Figure 4. Steady-state waveforms: filter capacitor voltage signal (V(t)), NPN collector-emitter voltage (V_{CEnpn}) and PNP emitter-collector voltage (V_{ECpnp})

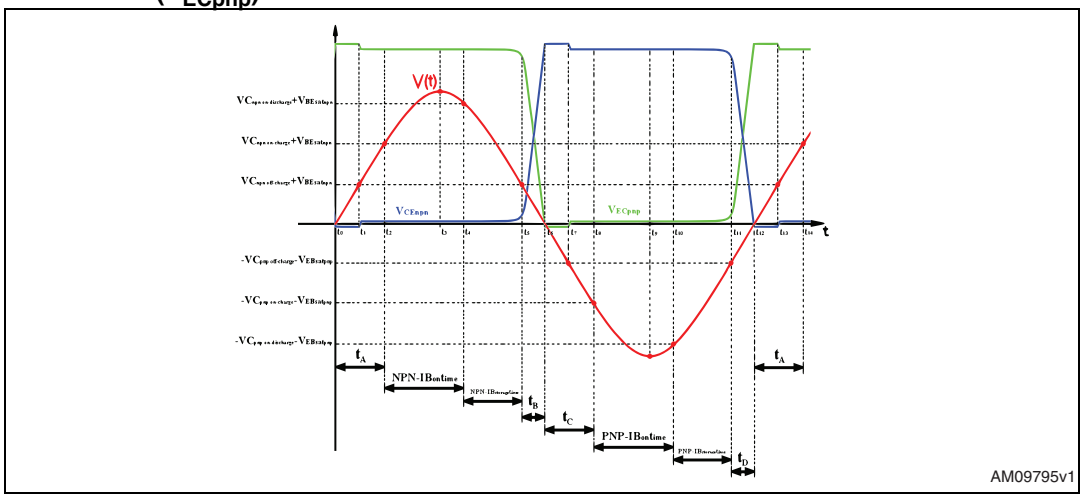


Figure 5. Steady-state waveforms: filter capacitor voltage signal (V(t)), NPN base-emitter voltage (V_{BEnpn}) and PNP emitter-base voltage(V_{EBpnp})

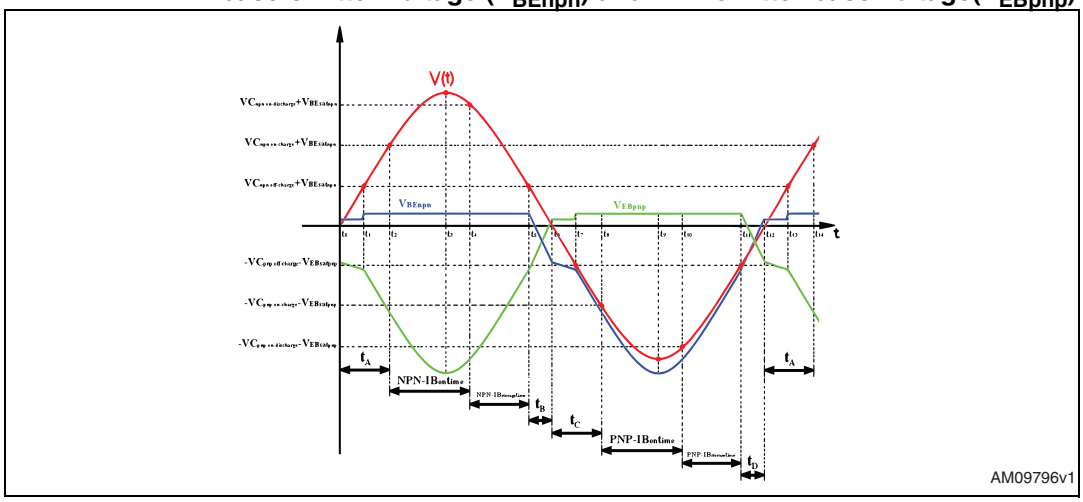
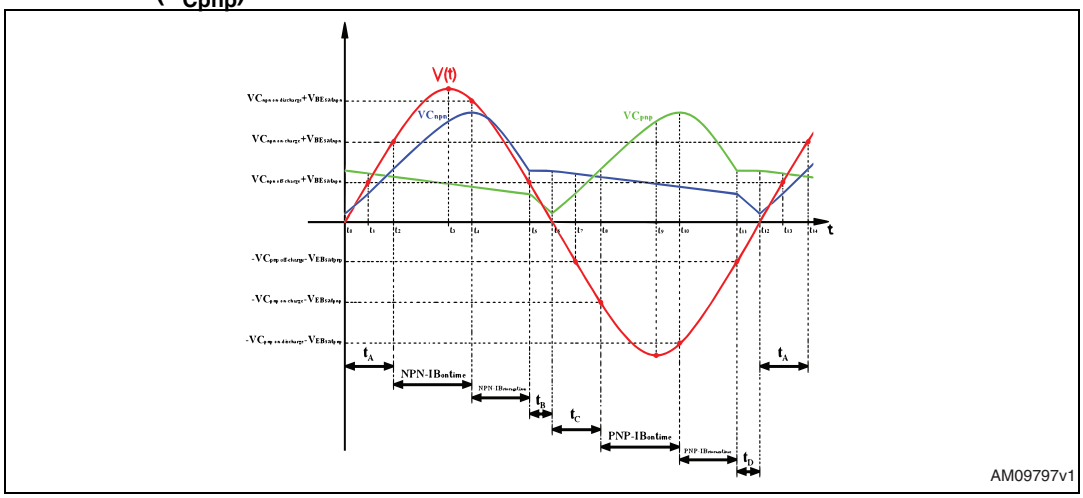


Figure 6. Steady-state waveforms: filter capacitor voltage signal (V(t)), NPN base series capacitor voltage (V_{Cnpn}) and PNP base series capacitor voltage (V_{Cpnp})



In *Figure 2* the filter capacitor voltage V(t) and the base currents I_{bnpn} and I_{bpnp} of the two bipolars during a period of the voltage signal filtered are shown. Two different signal thresholds fix respectively the turn-on and turn-off instants of the devices during their working operation period. In particular, in the previous figure it is evident that, starting from the driving source voltage, the turn-on of the NPN transistor is possible only when the V(t) is higher than the $V_{Cnpnon-char}+V_{BEsatnpn}$ value and similarly the turn-on of the PNP transistor is possible only when the V(t) is lower than the $-V_{Cpnpon-char}-V_{EBsatpnp}$ value. On the contrary, the turn-off of the NPN transistor is possible only when the V(t) is lower than the $V_{Cnpnon-dischar}+V_{BEsatnpn}$ value and, similarly, the turn-off of the PNP transistor is possible only when the V(t) is higher than the $-V_{Cpnpon-dischar}-V_{EBsatpnp}$ value.

Figure 3 shows the filter capacitor voltage V(t) and the collector currents I_{Cnpn} and I_{Cpnp} of the two bipolars during a period of the voltage signal filtered. It can be seen as the collector currents pass through the zero value at the end of the re-circulating phases in which the whole residual external demagnetization current, imposed by the load inductor, has

elapsed. Instants of turn-on switching are at t_2 (or t_{14}) and t_8 times respectively for the NPN and PNP devices.

Figure 4 shows the filter capacitor voltage V(t) and the collector-emitter voltage V_{CEnpn} signal and emitter-collector voltage signal V_{ECpnp} respectively of the NPN and PNP bipolars during a period of the voltage signal filtered. In this image the waveforms are not reported in scale since the voltage signals V_{CEnpn} and V_{ECpnp} assume far higher levels compared to the V(t) signal ones.

Figure 5 shows the filter capacitor voltage V(t) and base-emitter voltage signal V_{BEnpn} and emitter-base voltage signal V_{EBpnp} respectively of the NPN and PNP bipolars during a period of the voltage signal filtered.

Figure 6 shows the filter capacitor voltage V(t) and the voltage signals across the capacitors V_{Cnpn} and V_{Cpnp} in series, respectively, to the bases of the NPN and PNP bipolars during a period of the voltage signal filtered. It is possible to see as the different signal thresholds impose the initial instants of the charging and discharging phases for the capacitors in series to the bases.

Observing the waveforms attached, which describe the resonant driving functionality, it is clearly possible to distinguish the different working operation phases of the two devices during a switching period. In particular, when $V(t)>V_{Cnpnon\text{-}char}+V_{BEsatnpn}$ with $\frac{d}{dt}(V(t))>0$, NPN conduction time begins and when V(t) decreasing positively reaches the $V_{Cnpnon\text{-}dischar}+V_{BEsatnpn}$ value (that is $V(t)<V_{Cnpnon\text{-}dischar}+V_{BEsatnpn}$ with $\frac{d}{dt}(V(t))<0$), the NPN storage time phase starts. After the fall time period, NPN bipolar can no longer sustain its collector current so the voltage of the midpoint in common with the PNP emitter changes. At this time, the short transition mode ('dead time' after the NPN conduction time has elapsed) begins (for $0<V(t)<V_{Cnpnoff\text{-}char}+V_{BEsatnpn}$ with $\frac{d}{dt}(V(t))<0$), where both bipolars are off and the snubber capacitance carries the load resonant inductor current while the B-C junction capacitances of the devices are respectively charged (NPN) and discharged (PNP). Similarly, when $V(t)<-V_{Cpnpon\text{-}char}-V_{EBsatpnp}$ with $\frac{d}{dt}(V(t))<0$, PNP conduction time begins and when decreasing V(t), in module, negatively reaches the $-V_{Cpnpon\text{-}dischar}-V_{EBsatpnp}$ value (that is $V(t)>-V_{Cpnpon\text{-}dischar}-V_{EBsatpnp}$ with $\frac{d}{dt}(V(t))>0$), the PNP storage time phase starts. Short transition mode after the PNP conduction time ('dead time' after the PNP conduction time has elapsed) begins when $-V_{Cpnpoff\text{-}char}-V_{EBsatpnp}<V(t)<0$ with $\frac{d}{dt}(V(t))>0$ in which the B-C junction capacitances of the PNP and NPN devices are respectively charged and discharged. Re-circulating phases elapse respectively for $0<V(t)<V_{Cnpnon\text{-}char}+V_{BEsatnpn}$ and $\frac{d}{dt}(V(t))>0$ with the NPN device turned on at t_2 (or t_{14}) instant and for $-V_{Cpnpon\text{-}char}-V_{EBsatpnp}<V(t)<0$ and $\frac{d}{dt}(V(t))<0$ with the PNP device turned on at t_8 instant.

5 Steady-state stage-wise circuit analysis

This section provides a comprehensive description of the resonant filter working operation using a stage-wise circuit analysis divided into eight phases in accordance with the variation over a period of the voltage signal across the filter capacitor V(t) at the output of the transformer secondary windings. The dynamic behavior of the resonant driving system can be easily described by applying, in the time domain, Kirchhoff's voltage law on the loops containing the filter capacitor C2 and the R-C network (R2-R4-C3-C4) connected in series to the bases of the transistors and Kirchhoff's current law on the nodes with the branches of the base series capacitors connected to it. The mathematical model developed is useful for the successive simulation in Matlab environment.

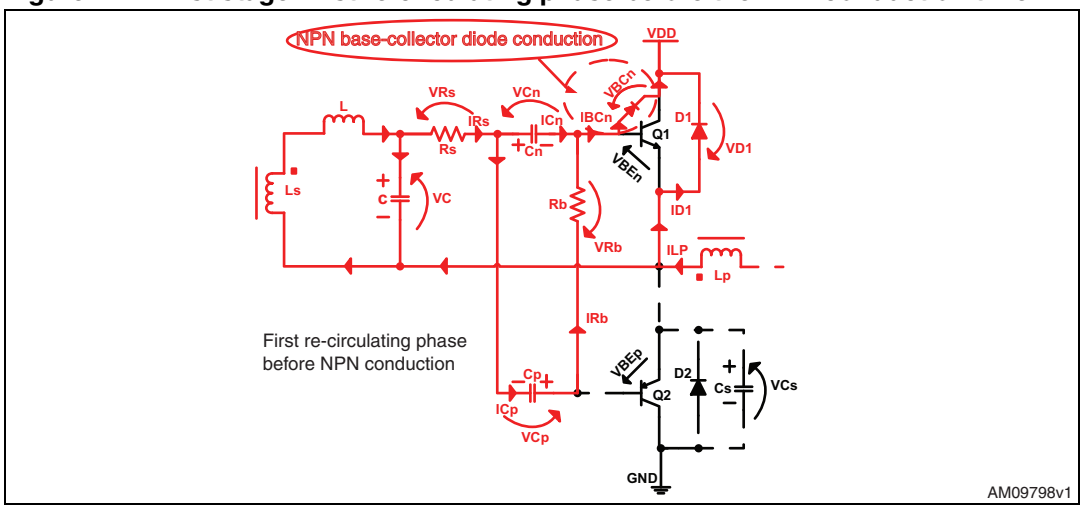
- Stage 1: $t_0<t<t_2$ and $t_{12}<t<t_{14}$: (re-circulating phase before the NPN conduction time:

$$0<V(t)< V_{Cnpnon\text{-}char}+V_{BEsatnpn} \text{ with } \frac{d}{dt}(V(t)) > 0)$$

The re-circulating phase is referred to all the demagnetization transient of the load inductor Lp elapsing until its current I_{LP} reaches the zero value at the end of this stage. This phase, in which both Q1-Q2 switches are inactive, can be subdivided into a further two sub-phases distinguished by the following:

  – First re-circulating phase before the NPN conduction time ($t_0<t<t_1$ and $t_{12}<t<t_{13}$): Both Q1-Q2 switches are turned off and the anti-parallel diode D1 of the NPN transistor conducts, sharing with the forward biased B-C NPN bipolar junction, the residual demagnetization current I_{LP} from the load inductor Lp. Voltage across the filter capacitor C increases and charges the capacitor C_n in series to the not yet forward biased NPN base-emitter junction, therefore assuming the same polarity of the relevant $V_{BEnpn\text{-}on}$, whereas the capacitor C_p begins to discharge through the breakdown resistance R_b. In this re-circulating stage, currents and voltages on the driving network are represented by the information in *Figure 7*.

Figure 7. First stage: first re-circulating phase before the NPN conduction time



According to the agreement in *Figure 7*, the following equations are valid in the driving section during the first re-circulating stage for $t_0<t<t_1$ and $t_{12}<t<t_{13}$:

System of equations 1

$$
\begin{cases}
V(t) = V_C(t) \\
V_{BEn}(t) = V_{BCn}(t) - V_{D1}(t) < V_{BEn-on} \text{ where } V_{BCn}(t) > V_{BCn-on} \text{ and } V_{D1}(t) > V_{D1-on} \\
V_{Cn}(t) = V_{Cnor1a} + \frac{1}{C_n}\int_{t0}^{t1} I_{Cn}(t)dt \quad \text{where} \quad V_{Cnor1a} = V_{Cn}(t_{0-}) \\
V_{Cp}(t) = V_{Cpor1a} - \frac{1}{C_p}\int_{t0}^{t1} I_{Cp}(t)dt \quad \text{where} \quad V_{Cpor1a} = V_{Cp}(t_{0-}) \\
I_{Cn}(t) = C_n \cdot \frac{d}{dt}(V_{Cn}(t)) \\
I_{Cp}(t) = -C_p \cdot \frac{d}{dt}(V_{Cp}(t)) \\
I_{BCn}(t) = I_{Cn}(t) + I_{Cp}(t) = I_{LP}(t) - I_{D1}(t) = I_{RS}(t) \\
V_{Cn}(t) + V_{Cp}(t) = V_{Rb}(t) = V_{BEp}(t) - V_{BEn}(t) \text{ with } V_{BEp}(t) = -V_{EBp}(t) > 0
\end{cases}
$$

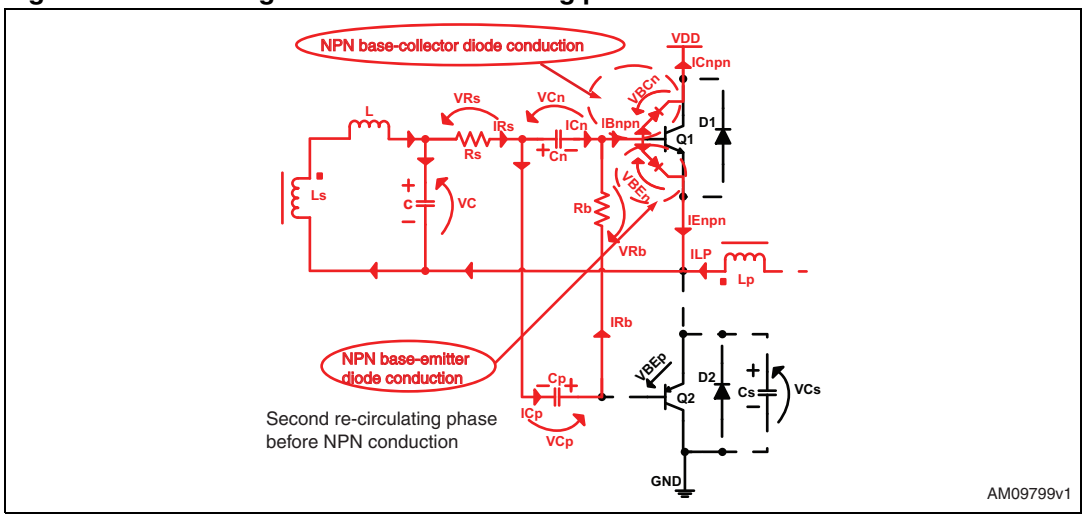
in which I_{BCn} and V_{BCn} are, respectively, the current signal and voltage signal of the NPN bipolar forward conducting B-C junction diode. During this phase, in general, $V_{BEn}(t)$ voltage is so that $0<V_{BEn}(t)<V_{BEn\text{-}on}$ for the NPN bipolar B-E junction diode, but if it were $V_{BEn}(t)<0$ the device would work in reverse active region as it is $V_{BCn}(t)>0$.

Neglecting the reverse recovery time of the anti-parallel diode D1, the subsequent phase is given by the following second re-circulating phase before the NPN conduction time.

- Second re-circulating phase before the NPN conduction time ($t_1<t<t_2$ and $t_{13}<t<t_{14}$):

  In this phase the NPN bipolar transistor acts as two uncoupled/independent diodes. In fact, the external diode D1 is turned off and the NPN device continues to be inactive but, contrary to the previous first re-circulating phase, both of its two B-E and B-C junctions are forward biased in order to complete the residual demagnetization of the Lp inductor until the forcing re-circulating current I_{LP}, that imposes the negative (extractive) collector current, reaches the zero value. Voltage across the filter capacitor C continues to increase and charge the capacitor Cn in series to the forward biased NPN base-emitter junction whereas the capacitor Cp continues to discharge through the breakdown resistance Rb. When the inductive resonant current reverses, after t_2 instant, the successive phase starts and the NPN device Q1 conducts carrying a positive (coming in) collector current I_{Cnpn}. In this second re-circulating stage, currents and voltages on the driving network are represented by the information in *Figure 8*.

Figure 8. First stage: second re-circulating phase before the NPN conduction time



According to the agreement of the previous image, the following equations are valid in the driving section during the second re-circulating stage for $t_1<t<t_2$ and $t_{13}<t<t_{14}$:

System of equations 2

$$
\begin{cases}
V(t) = V_C(t) \\
V_{BEn}(t) = V_{BEn-on} \\
V_{BCn}(t) = V_{BCn-on} \quad \text{and} \quad V_{ECn}(t) = -V_{CEn}(t) < V_{D1-on} \\
V_{Cn}(t) = V_{Cnor1b} + \frac{1}{C_n}\int_{t1}^{t2} I_{Cn}(t)dt \quad \text{where} \quad V_{Cnor1b} = V_{Cn}(t_{1-}) \\
V_{Cp}(t) = V_{Cpor1b} - \frac{1}{C_p}\int_{t1}^{t2} I_{Cp}(t)dt \quad \text{where} \quad V_{Cpor1b} = V_{Cp}(t_{1-}) \\
I_{Cn}(t) = C_n \cdot \frac{d}{dt}(V_{Cn}(t)) \\
I_{Cp}(t) = -C_p \cdot \frac{d}{dt}(V_{Cp}(t)) \\
I_{Bnpn}(t) = I_{Cn}(t) + I_{Cp}(t) = I_{Cnpn}(t) + I_{Enpn}(t) = I_{LP}(t) + I_{Enpn}(t) = I_{RS}(t) \\
V_{Cn}(t) + V_{Cp}(t) = V_{Rb}(t) = V_{BEp}(t) - V_{BEn}(t) \quad \text{with} \quad V_{BEp}(t) = -V_{EBp}(t) > 0
\end{cases}
$$

- Stage 2: $t_2<t<t_4$: (NPN conduction time: $V(t)>V_{Cnpnon-char}+V_{BEsatnpn}$ during filter capacitor C charging phase for $t_2<t<t_3$ with $\frac{d}{dt}(V(t)) > 0$ and $V(t)>V_{Cnpnon-dischar}+V_{BEsatnpn}$ during filter capacitor C discharging phase for $t_3<t<t_4$ with $\frac{d}{dt}(V(t)) < 0$).

  From the t_2 instant V(t) voltage is higher than the $V_{Cnpnon-char}+V_{BEsatnpn}$ value and increases up to reach its maximum value at t_3. NPN transistor Q1 is turned on under zero voltage switching (ZVS) and the current in the resonant load inductor increases. Capacitor C_n continues to be charged up by the source V(t), whereas capacitor C_p discharges through the breakdown resistance R_b inserted between the bases of the

two transistors. After t_3 instant voltage across the filter capacitor C decreases from its maximum value while the capacitor C_n continues to charge until it reaches its maximum value and the capacitor C_p to discharge maintaining a share of conduction current on the base I_{Bn} of the NPN bipolar Q1. During this stage, the base current I_{Bn} is the superposition of two components, one generated by the Cn charging transient and the other one generated by the C_p discharging transient through the breakdown resistance R_b. In this way, it is possible to see the voltage signal V_{Cp}, as a voltage source when the NPN device Q1 is conducting. In this stage, currents and voltages on the driving network are represented by the information in *Figure 9* and *10*.

Figure 9. Second stage: NPN conduction phase with filter capacitor charge

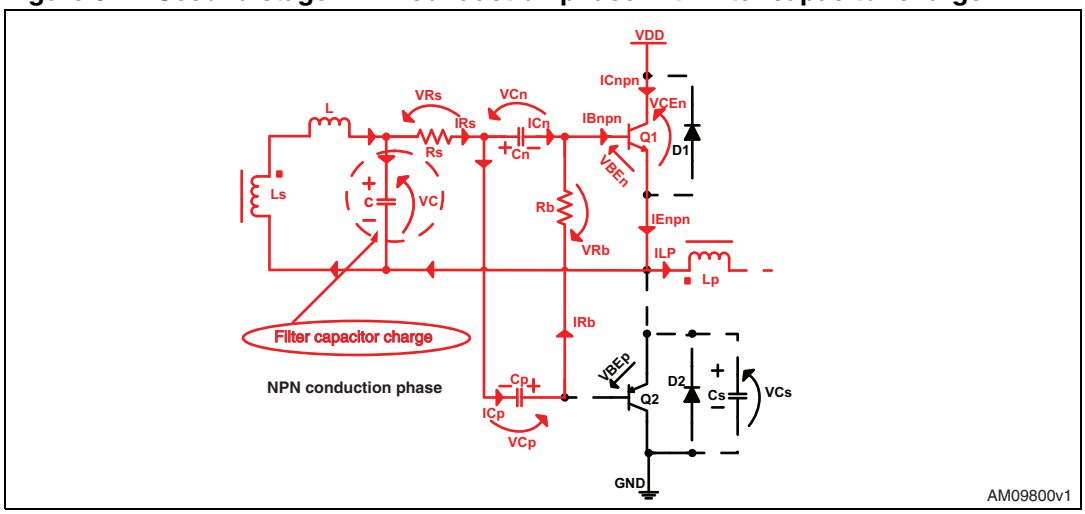
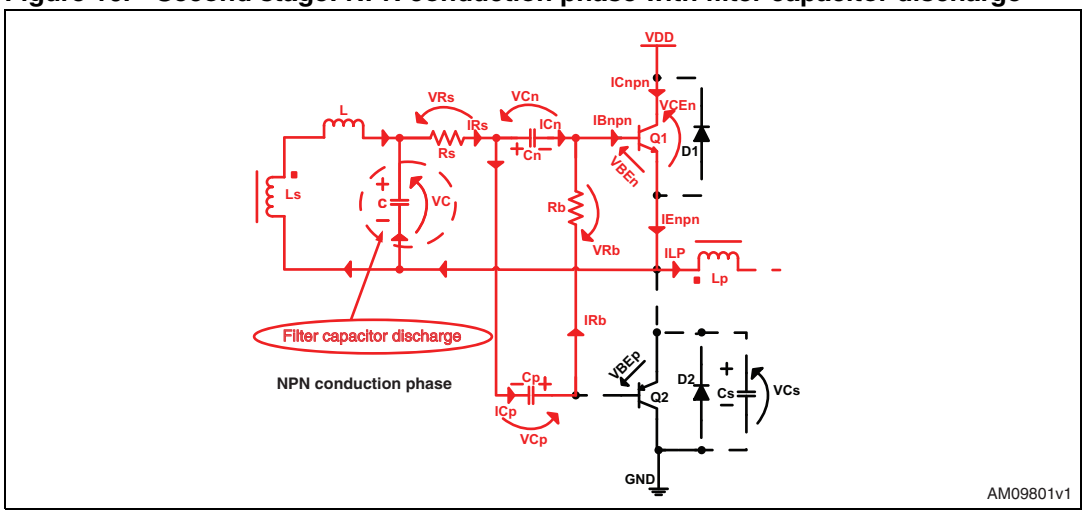


Figure 10. Second stage: NPN conduction phase with filter capacitor discharge



According to the agreement of the previous images, the following equations are valid in the driving section during the NPN conduction stage for $t_2<t<t_4$:

System of equations 3

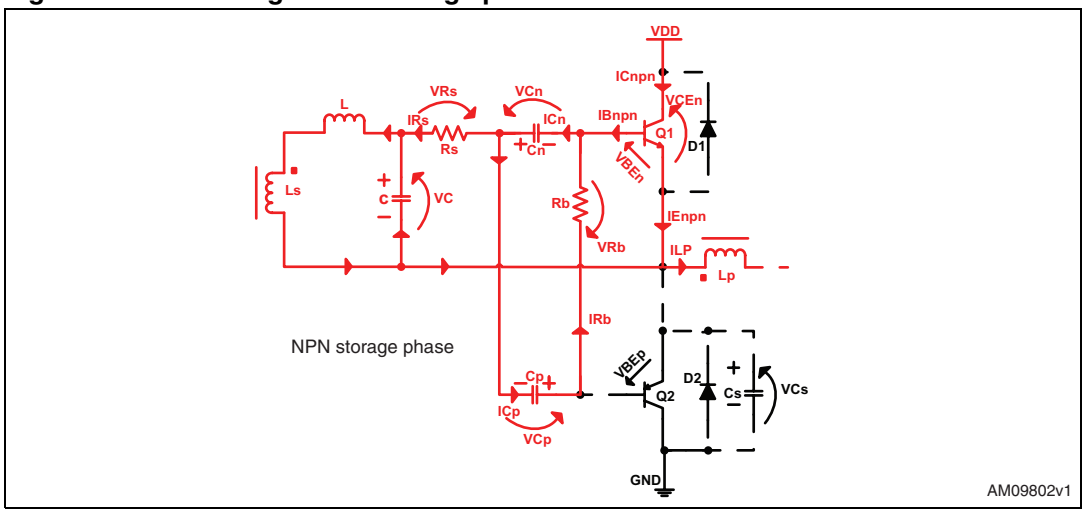
$$
\begin{cases}
V(t) = V_C(t) \\
V_{BEn}(t) = V_{BEn-sat} \\
V_{CEn}(t) = V_{CEn-sat} \\
V_{Cn}(t) = V_{Cnoc1} + \dfrac{1}{C_n}\int_{t2}^{t4} I_{Cn}(t)dt \quad \text{where} \quad V_{Cnoc1} = V_{Cnpnon-char} = V_{Cn}(t_{2-}) \\
V_{Cp}(t) = V_{Cpoc1} - \dfrac{1}{C_p}\int_{t2}^{t4} I_{Cp}(t)dt \quad \text{where} \quad V_{Cpoc1} = V_{Cp}(t_{2-}) \\
I_{Cn}(t) = C_n \cdot \dfrac{d}{dt}(V_{Cn}(t)) \\
I_{Cp}(t) = -C_p \cdot \dfrac{d}{dt}(V_{Cp}(t)) \\
I_{Bnpn-on}(t) = I_{Cn}(t) + I_{Cp}(t) = I_{Enpn}(t) - I_{LP}(t) = I_{RS}(t) \quad \text{where} \quad I_{LP}(t) = I_{Cnpn}(t) \\
V_{Cn}(t) + V_{Cp}(t) = V_{Rb}(t) = V_{BEp}(t) - V_{BEn}(t) \quad \text{with} \quad V_{BEp}(t) = -V_{EBp}(t) > 0 \\
V_C(t) = V_{RS}(t) + V_{Cn}(t) + V_{BEn}(t)
\end{cases}
$$

where $V_{BEn-sat}$ is the voltage of the forward conducting B-E junction diode of the NPN bipolar and $I_{Bnpn-on}$ is the base current for the NPN bipolar working in saturation state.

- Stage 3: $t_4<t<t_5$: (NPN storage time: $V_{Cnpnoff-char}+V_{BEsatnpn}<V(t)<V_{Cnpnon-dischar}+V_{BEsatnpn}$ with $\dfrac{d}{dt}(V(t)) < 0$)

  The decreasing voltage V(t) across the filter capacitor C equals the $V_{Cnpnon-dischar}+V_{BEsatnpn}$ value at t_4 instant. At this point the voltage on the capacitor C_n starts to decline but the stored charges of the NPN bipolar base keep the NPN conducting with a negative base current (extraction base current $I_{Bnpn-off}$) while the C_p capacitor maintains its discharging phase. After the stored excess charges have disappeared, the operating point of the NPN enters its active region and V_{CEnpn} voltage begins to increase while the collector current I_{Cnpn} drops. Therefore, the collector current I_{Cnpn} fall time phase is included in this state until the NPN bipolar Q1 is gradually soft switched on turn-off. In this stage, currents and voltages on the driving network are represented by the information in *Figure 11*.

Figure 11. Third stage: NPN storage phase



According to the agreement of the previous image, the following equations are valid in the driving section during the NPN storage time for $t_4<t<t_5$:

System of equations 4

$$
\begin{cases}
V(t) = V_C(t) \\
V_{BEn}(t) = V_{BEn-sat} \\
V_{CEn}(t) \geq V_{CEn-sat} \\
V_{Cn}(t) = V_{Cnos1} - \dfrac{1}{C_n}\int_{t4}^{t5} I_{Cn}(t)dt \quad \text{where} \quad V_{Cnos1} = V_{Cn}(t_{4-}) \\
V_{Cp}(t) = V_{Cpos1} - \dfrac{1}{C_p}\int_{t4}^{t5} I_{Cp}(t)dt \quad \text{where} \quad V_{Cpos1} = V_{Cp}(t_{4-}) \\
I_{Cn}(t) = -C_n \cdot \dfrac{d}{dt}(V_{Cn}(t)) \\
I_{Cp}(t) = -C_p \cdot \dfrac{d}{dt}(V_{Cp}(t)) \\
I_{Bnpn-off}(t) = I_{Cn}(t) - I_{Cp}(t) = I_{LP}(t) - I_{Enpn}(t) = I_{RS}(t) \text{ where } I_{LP}(t) = I_{Cnpn}(t) \\
V_{Cn}(t) + V_{Cp}(t) = V_{Rb}(t) = V_{BEp}(t) - V_{BEn}(t) \text{ with } V_{BEp}(t) = -V_{EBp}(t) > 0 \\
V_C(t) = -V_{RS}(t) + V_{Cn}(t) + V_{BEn}(t)
\end{cases}
$$

where $I_{Bnpn-off}$ is the extracting base current during the storage time of the NPN bipolar.

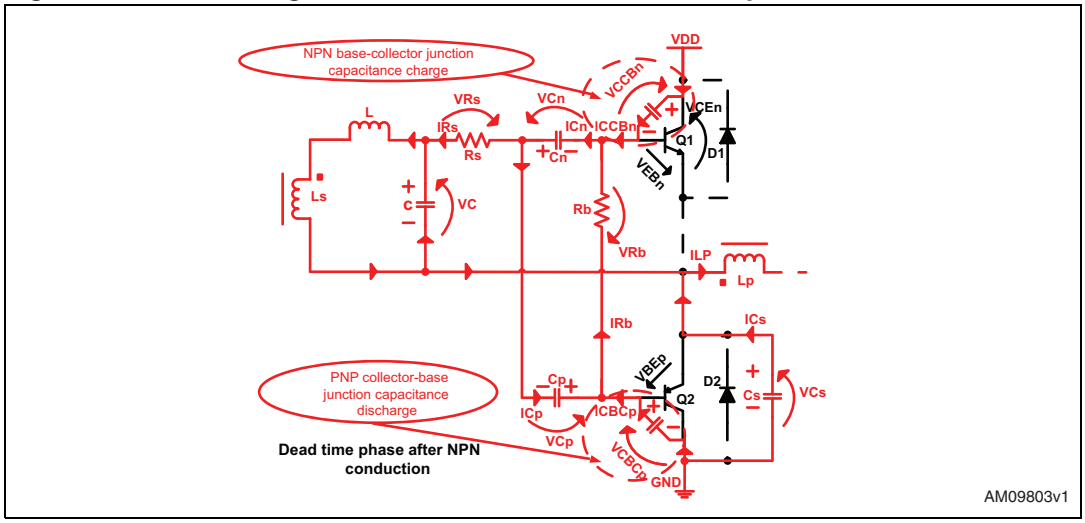
- Stage 4: $t_5<t<t_6$: (dead time after the NPN conduction phase:

  $0<V(t)<V_{Cnpnoff-char}+V_{BEsatnpn}$ with $\dfrac{d}{dt}(V(t)) < 0$)

  At t_5 instant, the load inductor current I_{LP} continues to decay and the resonant current is commutated from the NPN bipolar Q1 to the snubber capacitor C_s that discharges. As a result, the voltage on the common emitter node of the two switches decreases linearly from the upper rail to the lower rail until the emitter voltage of the PNP transistor Q2 begins to go negative with respect to the lower rail (ground reference) at t_6 and the anti-parallel diode D2 of the PNP transistor starts to conduct beginning the next fifth stage. At the end of this “dead time” stage, the voltage on the capacitor C_p is reduced

to the minimum value whereas the voltage on the capacitor C_n keeps nearly constant. The final instant t_6, from which the I_{Cp} capacitor current changes polarity, marks the change of the V(t) signal polarity and one-half of its period. In this stage, currents and voltages on the driving network are represented by the information in *Figure 12*, in which the charging/discharging effects of the reverse biased B-E junction capacitances, respectively, for the NPN and PNP devices, are neglected and so it is possible to approximate $I_{Bnpn}(t) \cong I_{CCBn}(t)$ and $I_{Bpnp}(t) \cong I_{CBCp}(t)$.

Figure 12. Fourth stage: dead time after NPN conduction phase



According to the agreement of the previous image, the following equations are valid in the driving section during the dead time after the NPN conduction phase for $t_5<t<t_6$:

System of equations 5

$$
\begin{cases}
V(t) = V_C(t) \\
V_{CEn}(t) > V_{CEn-sat} \\
-V_{BEn}(t) = V_{EBn}(t) = -(V_{DD} - V_{CCBn}(t) - V_{CS}(t)) > 0 \Rightarrow V_{BEn}(t) < 0 \\
-V_{EBp}(t) = V_{BEp}(t) = V_{CBCp}(t) - V_{CS}(t) > 0 \Rightarrow V_{EBp}(t) < 0 \\
V_{Cn}(t) = V_{Cnod1} - \dfrac{1}{C_n}\int_{t5}^{t6} I_{Cn}(t)dt \quad \text{where} \quad V_{Cnod1} = V_{Cn}(t_{5-}) \\
V_{Cp}(t) = V_{Cpod1} - \dfrac{1}{C_p}\int_{t5}^{t6} I_{Cp}(t)dt \quad \text{where} \quad V_{Cpod1} = V_{Cp}(t_{5-}) \\
I_{Cn}(t) = -C_n \cdot \dfrac{d}{dt}(V_{Cn}(t)) \\
I_{Cp}(t) = -C_p \cdot \dfrac{d}{dt}(V_{Cp}(t)) \\
I_{RS}(t) = I_{CCBn}(t) + I_{CBCp}(t) = I_{LP}(t) - I_{CS}(t) \\
I_{CS}(t) = -Cs \cdot \dfrac{d}{dt}(V_{CS}(t)) \\
V_{Cn}(t) + V_{Cp}(t) = V_{Rb}(t) = V_{BEp}(t) + V_{EBn}(t) \\
V_C(t) = -V_{RS}(t) + V_{Cn}(t) - V_{EBn}(t)
\end{cases}
$$

where I_{CCBn} is the charging current of the NPN bipolar B-C junction capacitance and I_{CBCp} is the discharging current of the PNP bipolar C-B junction capacitance.

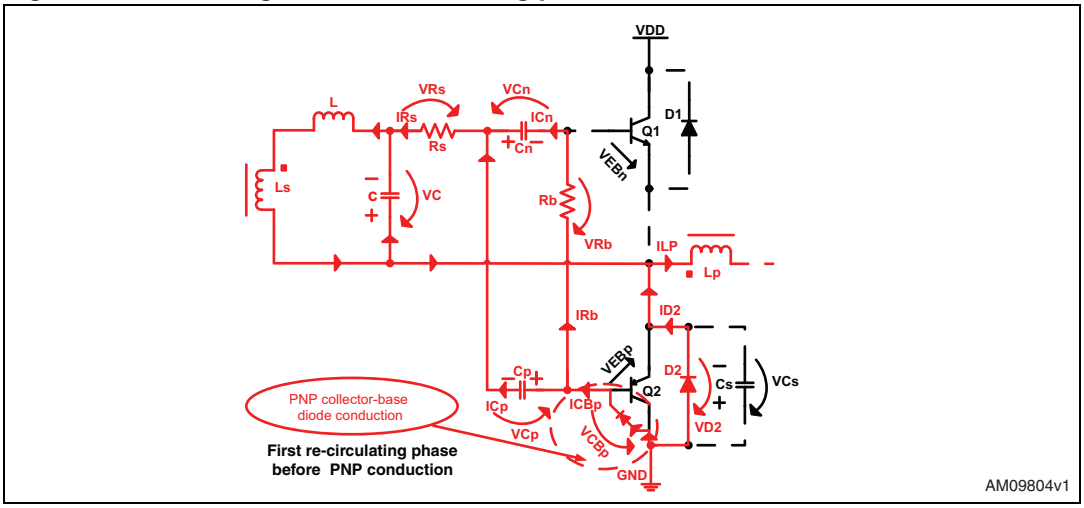
- Stage 5: $t_6<t<t_8$: (re-circulating phase before the PNP conduction time:

$$-V_{Cpnpon\text{-}char} - V_{EBsatpnp} < V(t) < 0 \text{ with } \frac{d}{dt}(V(t)) < 0$$

As done for the re-circulating phase before the NPN conduction time ($t_0<t<t_2$), this phase, in which both Q1-Q2 switches are inactive, can be subdivided into a further two sub-phases distinguished by the following:

– First re-circulating phase before the PNP conduction time ($t_6<t<t_7$): both Q1-Q2 switches are turned off and the load inductor residual magnetization current I_{LP} circulates freely through the PNP transistor anti-parallel diode D2 and the directly biased C-B junction of the PNP bipolar Q2. Voltage across the filter capacitor C increases in the opposite polarity than the NPN turn-on phase and charges the capacitor C_p in series to the not yet forward biased base of the PNP, assuming the same polarity of the relevant $V_{EBonpnp}$, while the capacitor C_n begins to decrease its charge through the breakdown resistance R_b. In this re-circulating stage, currents and voltages on the driving network are represented by the following *Figure 13*.

Figure 13. Fifth stage: first re-circulating phase before the PNP conduction time



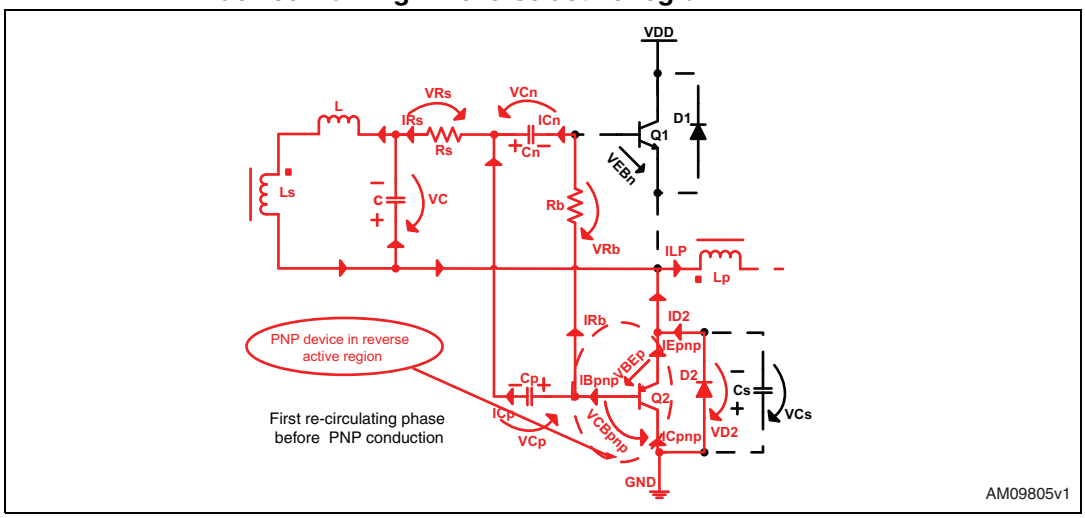
According to the agreement of the previous image, the following equations are valid in the driving section during the first re-circulating stage for $t_6<t<t_7$:

System of equations 6

$$
\begin{cases}
V(t) = -V_C(t) \\
V_{EBp}(t) = V_{CBp}(t) - V_{D2}(t) < V_{EBp-on} \text{ where } V_{CBp}(t) > V_{CBp-on} \text{ and } V_{D2}(t) > V_{D2-on} \\
V_{Cn}(t) = V_{Cnor2a} - \frac{1}{C_n}\int_{t6}^{t7} I_{Cn}(t)dt \quad \text{where } V_{Cnor2a} = V_{Cn}(t_{6-}) \\
V_{Cp}(t) = V_{Cpor2a} + \frac{1}{C_p}\int_{t6}^{t7} I_{Cp}(t)dt \quad \text{where } V_{Cpor2a} = V_{Cp}(t_{6-}) \\
I_{Cn}(t) = -C_n \cdot \frac{d}{dt}(V_{Cn}(t)) \\
I_{Cp}(t) = C_p \cdot \frac{d}{dt}(V_{Cp}(t)) \\
I_{CBp}(t) = I_{Cn}(t) + I_{Cp}(t) = I_{LP}(t) - I_{D2}(t) = I_{RS}(t) \\
V_{Cn}(t) + V_{Cp}(t) = V_{Rb}(t) = V_{EBn}(t) - V_{EBp}(t) \text{ with } V_{EBn}(t) = -V_{BEn}(t) > 0
\end{cases}
$$

where I_{CBp} and V_{CBp} are, respectively, the current and voltage signal of the forward biased C-B junction diode of the PNP bipolar. During this phase, in general, $V_{EBp}(t)$ is so that $0<V_{EBp}(t)<V_{EBp\text{-}on}$ for the PNP bipolar E-B junction diode but if it were $V_{EBp}(t)<0$ the device would work in reverse active region since it is $V_{CBp}(t)>0$. Therefore, in this last case, currents and voltages on the driving network are depicted by the information in *Figure 14*.

Figure 14. Fifth stage: first re-circulating phase before PNP conduction time with PNP device working in reverse active region



Then, the relations below between the current and voltage signals would be valid:

Equation 1

$$I_{Bpnp}(t) = I_{Cpnp}(t) - I_{Epnp}(t) = I_{Cn}(t) + I_{Cp}(t) = I_{LP}(t) - I_{D2}(t) - I_{Epnp}(t) = I_{RS}(t)$$

$$V_{Cn}(t) + V_{Cp}(t) = V_{Rb}(t) = V_{EBn}(t) + V_{BEp}(t)$$

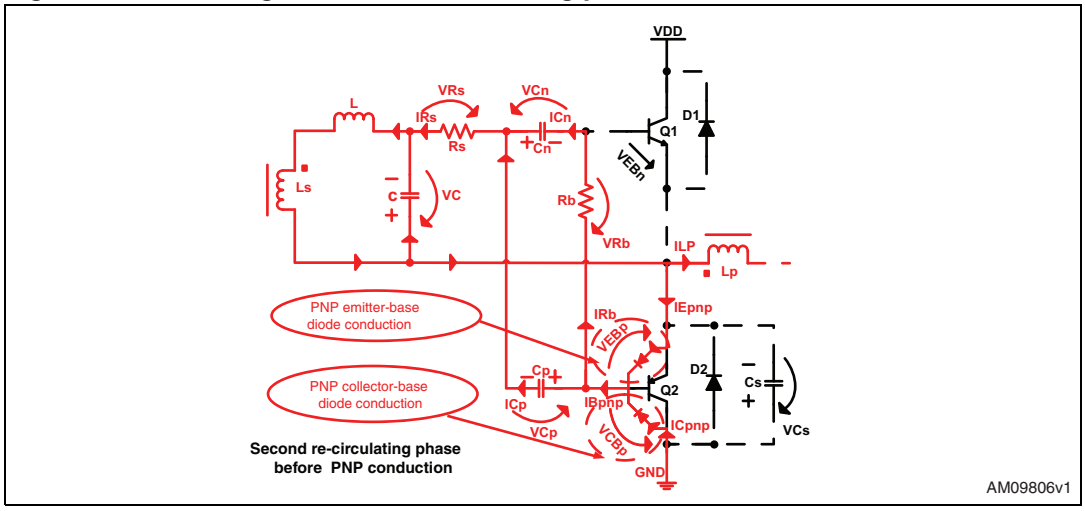
$$\text{with } V_{EBn}(t) = -V_{BEn}(t) > 0 \quad \text{and} \quad V_{BEp}(t) = -V_{EBp}(t) > 0$$

Neglecting the reverse recovery time of the anti-parallel diode D2, the subsequent phase is given by the following reported second re-circulating phase before the PNP conduction time.

– Second re-circulating phase before the PNP conduction time (t_7<t<t_8):

In this phase the PNP bipolar transistor acts as two uncoupled/independent diodes. In fact, the external diode D2 is turned off and the PNP device continues to be inactive but, contrary to the previous first re-circulating phase, both of its two E-B and C-B junctions are forward biased in order to complete the residual demagnetization of the L_p inductor until the forcing re-circulating current I_{LP}, that imposes the negative (coming in) collector current, reaches the zero value at the end of this stage. Voltage across the filter capacitor C continues to increase and charge the capacitor C_p in series to the forward biased PNP emitter-base junction whereas the capacitor C_n continues to discharge through the breakdown resistance R_b. When the inductive resonant current reverses, after t_8 instant, it is transferred naturally as a positive (extractive) collector current I_{Cpnp} to the PNP bipolar Q2 and the successive PNP conduction phase begins. In this stage, currents and voltages on the driving network are depicted by the information in *Figure 15*.

Figure 15. Fifth stage: second re-circulating phase before the PNP conduction time



According to the agreement of the previous image, the following equations are valid in the driving section during the second re-circulating stage for $t_7<t<t_8$:

System of equations 7

$$
\begin{cases}
V(t) = -V_C(t) \\
V_{EBp}(t) = V_{EBp-on} \\
V_{CBp}(t) = V_{CBp-on} \text{ and } V_{CEp}(t) = -V_{ECp}(t) < V_{D2-on} \\
V_{Cn}(t) = V_{Cnor2b} - \frac{1}{C_n}\int_{t7}^{t8} I_{Cn}(t)dt \quad \text{where} \quad V_{Cnor2b} = V_{Cn}(t_{7-}) \\
V_{Cp}(t) = V_{Cpor2b} + \frac{1}{C_p}\int_{t7}^{t8} I_{Cp}(t)dt \quad \text{where} \quad V_{Cpor2b} = V_{Cp}(t_{7-}) \\
I_{Cn}(t) = -C_n \cdot \frac{d}{dt}(V_{Cn}(t)) \\
I_{Cp}(t) = C_p \cdot \frac{d}{dt}(V_{Cp}(t)) \\
I_{Bpnp}(t) = I_{Cn}(t) + I_{Cp}(t) = I_{Cpnp}(t) + I_{Epnp}(t) = I_{LP}(t) + I_{Enpn}(t) = I_{RS}(t) \\
V_{Cn}(t) + V_{Cp}(t) = V_{Rb}(t) = V_{EBn}(t) - V_{EBp}(t) \text{ with } V_{EBn}(t) = -V_{BEn}(t) > 0
\end{cases}
$$

- Stage 6: $t_8<t<t_{10}$: (PNP conduction time: $V(t)<-V_{Cpnpon\text{-}char}-V_{EBsatpnp}$ during filter capacitor C charging phase for $t_8<t<t_9$ with $\frac{d}{dt}(V(t)) < 0$ and $V(t)<-V_{Cpnpon\text{-}dischar}-V_{EBsatpnp}$ during filter capacitor C discharging phase for $t_9<t<t_{10}$ with $\frac{d}{dt}(V(t)) > 0$).

From the t_8 instant V(t) voltage is lower than the $-V_{Cpnpon\text{-}char}-V_{EBsatpnp}$ value and decreases reaching its minimum value at t_9. PNP transistor Q2 turns on under zero voltage switching and the current in the resonant load inductor increases in module. Capacitor C_p continues to be charged up by the source V(t), whereas capacitor C_n discharges through the breakdown resistance R_b. At t_9 instant the voltage on filter capacitor C reaches its maximum inverse (negative) value. After this time V(t) decreases negatively in module whereas the capacitor C_p continues to charge until it reaches its maximum value and the capacitor C_n to discharge maintaining a share of conduction current on the base I_{Bp} of the PNP bipolar Q2. During this stage the base current I_{Bp} of the PNP bipolar transistor is the sum of the currents I_{Cn} and I_{Cp} in both capacitors. In this way, it is possible to consider the voltage signal V_{Cn}, as a voltage source when the PNP device Q2 is conducting. In this stage, currents and voltages on the driving network are represented by the information in *Figure 16* and *17*.

Figure 16. Sixth stage: PNP conduction phase with filter capacitor charge

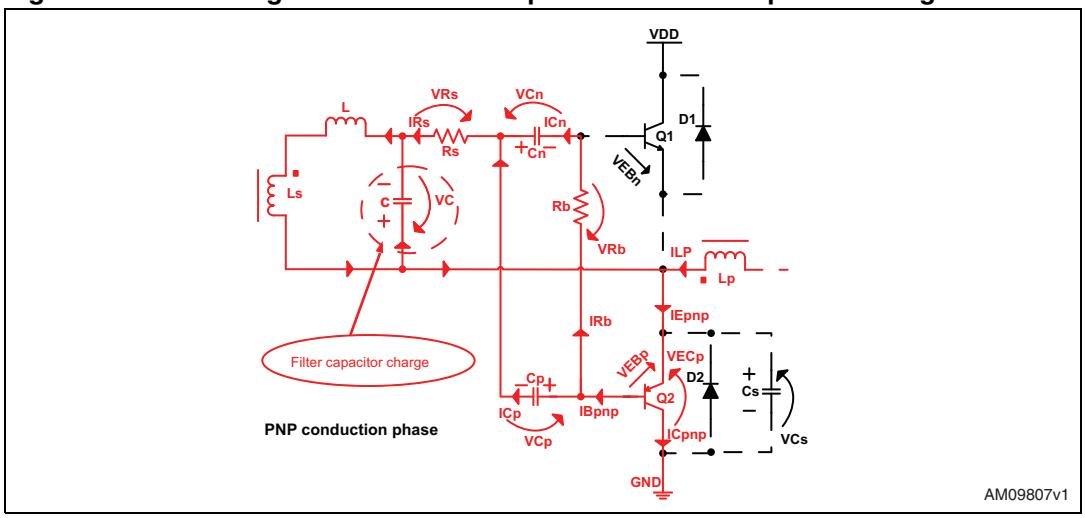
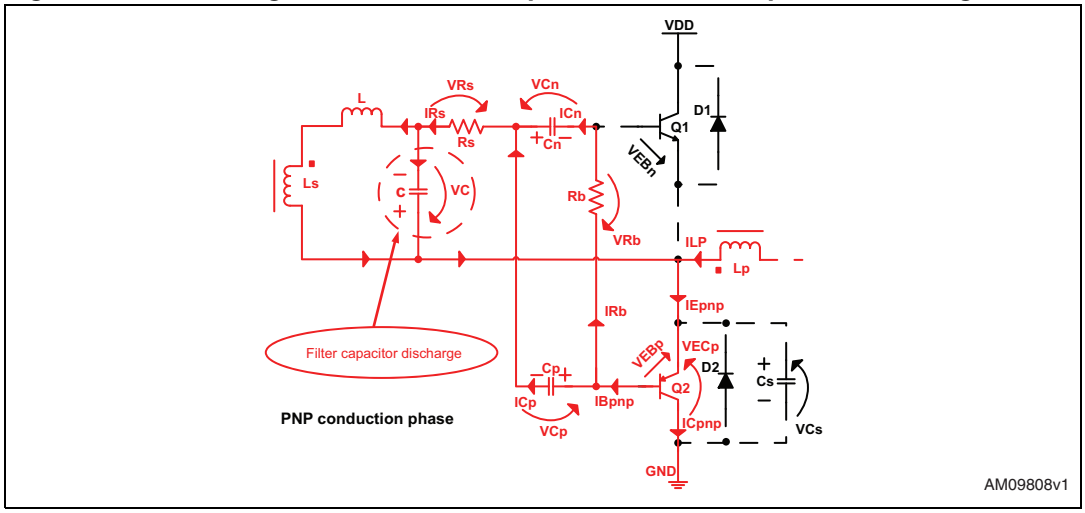


Figure 17. Sixth stage: PNP conduction phase with filter capacitor discharge



According to the agreement of the previous images, the following equations are valid in the driving section during the conduction stage of the NPN for $t_8<t<t_{10}$:

System of equations 8

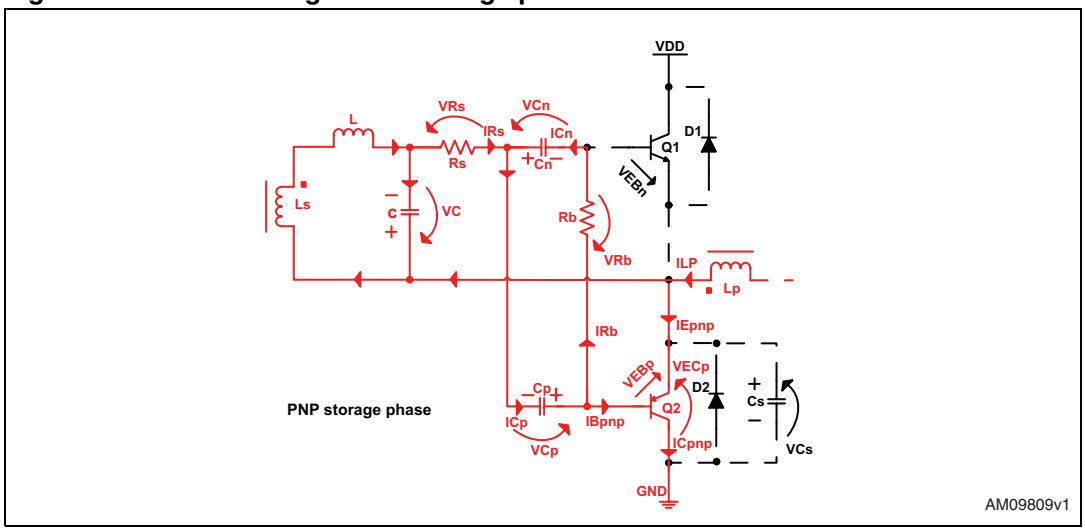
$$
\begin{cases}
V(t) = -V_C(t) \\
V_{EBp}(t) = V_{EBp-sat} \\
V_{ECp}(t) = V_{ECp-sat} \\
V_{Cn}(t) = V_{Cnoc2} - \dfrac{1}{C_n}\int_{t8}^{t10} I_{Cn}(t)dt \quad \text{where} \quad V_{Cnoc2} = V_{Cn}(t_{8-}) \\
V_{Cp}(t) = V_{Cpoc2} + \dfrac{1}{C_p}\int_{t8}^{t10} I_{Cp}(t)dt \quad \text{where} \quad V_{Cpoc2} = V_{Cpnpchar} = V_{Cp}(t_{8-}) \\
I_{Cn}(t) = -C_n \cdot \dfrac{d}{dt}(V_{Cn}(t)) \\
I_{Cp}(t) = C_p \cdot \dfrac{d}{dt}(V_{Cp}(t)) \\
I_{Bpnp-on}(t) = I_{Cn}(t) + I_{Cp}(t) = I_{Epnp}(t) - I_{LP}(t) = I_{RS}(t) \text{ where } I_{LP}(t) = I_{Cpnp}(t) \\
V_{Cn}(t) + V_{Cp}(t) = V_{Rb}(t) = V_{EBn}(t) - V_{EBp}(t) \text{ with } V_{EBn}(t) = -V_{BEn}(t) > 0 \\
V_C(t) = V_{RS}(t) + V_{Cp}(t) + V_{EBp}(t)
\end{cases}
$$

where $V_{EBp\text{-}on}$ is the voltage of the forward conducting E-B junction diode of the PNP bipolar and $I_{Bpnp\text{-}on}$ is the base current with PNP bipolar working in saturation state.

- Stage 7: $t_{10}<t<t_{11}$: (PNP storage time:
  $-V_{Cpnpon\text{-}dischar}-V_{EBsatpnp}<V(t)<-V_{Cpnpoff\text{-}char}-V_{EBsatpnp}$ with $\dfrac{d}{dt}(V(t)) > 0$)

Voltage V(t) across the filter capacitor C decreases, in module, negatively up to equal the $-V_{Cpnpon\text{-}dischar}-V_{EBsatpnp}$ value at t_{10} instant. At this point the capacitor voltage C_p starts to decline and the excess charges stored in the PNP device Q2 base keeps it conducting with a negative base current (coming-in base current $I_{Bpnp\text{-}off}$) while the C_n capacitor maintains its discharging phase. After the stored excess charges have disappeared the operating point of the PNP enters its active region and the V_{ECpnp} voltage begins to increase while the collector current I_{Cpnp} falls down. Therefore, the collector current I_{Cpnp} fall time phase is included in this state until the PNP bipolar Q2 is gradually soft-switched on turn-off. In this stage, currents and voltages on the driving network are represented by the information in *Figure 18*.

Figure 18. Seventh stage: PNP storage phase



According to the agreement of the previous image, the following equations are valid in the driving section during the PNP storage time for $t_{10}<t<t_{11}$:

System of equations 9

$$
\begin{cases}
V(t) = -V_C(t) \\
V_{EBp}(t) = V_{EBp-sat} \\
V_{ECp}(t) \geq V_{ECp-sat} \\
V_{Cn}(t) = V_{Cnos2} - \dfrac{1}{C_n}\displaystyle\int_{t10}^{t11} I_{Cn}(t)dt \quad \text{where} \quad V_{Cnos2} = V_{Cn}(t_{10-}) \\
V_{Cp}(t) = V_{Cpos2} - \dfrac{1}{C_p}\displaystyle\int_{t10}^{t11} I_{Cp}(t)dt \quad \text{where} \quad V_{Cpos2} = V_{Cp}(t_{10-}) \\
I_{Cn}(t) = -C_n \cdot \dfrac{d}{dt}(V_{Cn}(t)) \\
I_{Cp}(t) = -C_p \cdot \dfrac{d}{dt}(V_{Cp}(t)) \\
I_{Bpnp-off}(t) = I_{Cp}(t) - I_{Cn}(t) = I_{LP}(t) - I_{Epnp}(t) = I_{RS}(t) \quad \text{where} \quad I_{LP}(t) = I_{Cpnp}(t) \\
V_{Cn}(t) + V_{Cp}(t) = V_{Rb}(t) = V_{EBn}(t) - V_{EBp}(t) \quad \text{with} \quad V_{EBn}(t) = -V_{BEn}(t) > 0 \\
V_C(t) = -V_{RS}(t) + V_{Cp}(t) + V_{EBp}(t)
\end{cases}
$$

where $I_{Bpnp-off}$ is the coming-in current during the storage time of the PNP bipolar.

- Stage 8: $t_{11}<t<t_{12}$: (dead time after the PNP conduction phase:

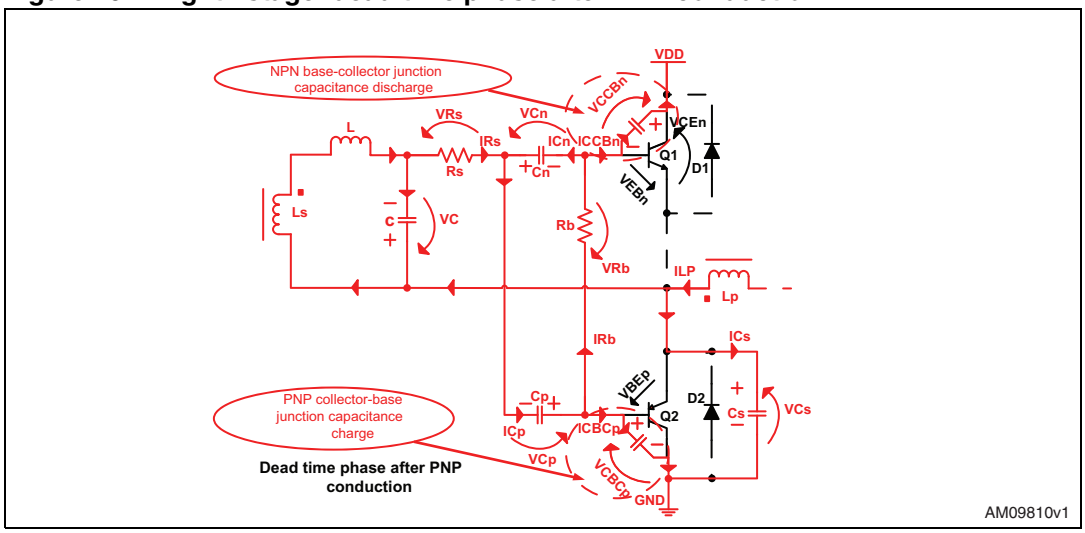
$$-V_{Cpnpoff-char}\text{-}V_{EBsatpnp} < V(t) < 0 \text{ with } \frac{d}{dt}(V(t)) > 0)$$

At t_{11} instant, the current I_{LP} in the load inductor has started to decay and the resonant current is commutated from the PNP bipolar Q2 to the snubber capacitor C_s that charges. As a result, the voltage on the common emitter node of the two switches increases linearly

from the lower rail to the upper rail until the emitter voltage of the NPN transistor Q1 begins to go positive with respect to the higher rail at t_{12} and the anti-parallel diode D1 of the NPN transistor Q1 begins to conduct, commencing again a new cycle starting from the first stage. At the end of this stage, the voltage on the capacitor Cn is reduced to the minimum value whereas the voltage on the capacitor C_p keeps nearly constant. The end of this 'dead time' (instant t_{12}), when the I_{Cn} capacitor current changes polarity, marks the change of the V(t) signal polarity and its complete evolution period. In this stage, currents and voltages on the driving network are represented by the information in *Figure 19* in which the charging/discharging effects of the reverse biased B-E junction capacitances, respectively for the PNP and NPN devices, are neglected and so is it possible to approximate

$I_{Bnpn}(t) \cong I_{CCBn}(t)$ and $I_{Bpnp}(t) \cong I_{CBCp}(t)$.

Figure 19. Eighth stage: dead time phase after PNP conduction



According to the agreement of the previous image, the following equations are valid in the driving section during the dead time after the PNP conduction phase for $t_{11}<t<t_{12}$:

System of equations 10

$$
\begin{cases}
V(t) = -V_C(t) \\
V_{ECp}(t) > V_{ECp-sat} \\
-V_{BEn}(t) = V_{EBn}(t) = -(V_{DD} - V_{CCBn}(t) - V_{CS}(t)) > 0 \Rightarrow V_{BEn}(t) < 0 \\
-V_{EBp}(t) = V_{BEp}(t) = V_{CBCp}(t) - V_{CS}(t) > 0 \Rightarrow V_{EBp}(t) < 0 \\
V_{Cn}(t) = V_{Cnod2} - \dfrac{1}{C_n}\int_{t11}^{t12} I_{Cn}(t)dt \quad \text{where} \quad V_{Cnod2} = V_{Cn}(t_{11-}) \\
V_{Cp}(t) = V_{Cpod2} - \dfrac{1}{C_p}\int_{t11}^{t12} I_{Cp}(t)dt \quad \text{where} \quad V_{Cpod2} = V_{Cp}(t_{11-}) \\
I_{Cn}(t) = -C_n \cdot \dfrac{d}{dt}(V_{Cn}(t)) \\
I_{Cp}(t) = -C_p \cdot \dfrac{d}{dt}(V_{Cp}(t)) \\
I_{RS}(t) = I_{CCBn}(t) + I_{CBCp}(t) = I_{LP}(t) - I_{CS}(t) \\
I_{CS}(t) = Cs \cdot \dfrac{d}{dt}(V_{CS}(t)) \\
V_{Cn}(t) + V_{Cp}(t) = V_{Rb}(t) = V_{BEp}(t) + V_{EBn}(t) \\
V_C(t) = -V_{RS}(t) + V_{Cp}(t) - V_{BEp}(t)
\end{cases}
$$

where I_{CCBn} is the discharging current of the NPN bipolar B-C junction capacitance and I_{CBCp} is the charging current of the PNP bipolar C-B junction capacitance.

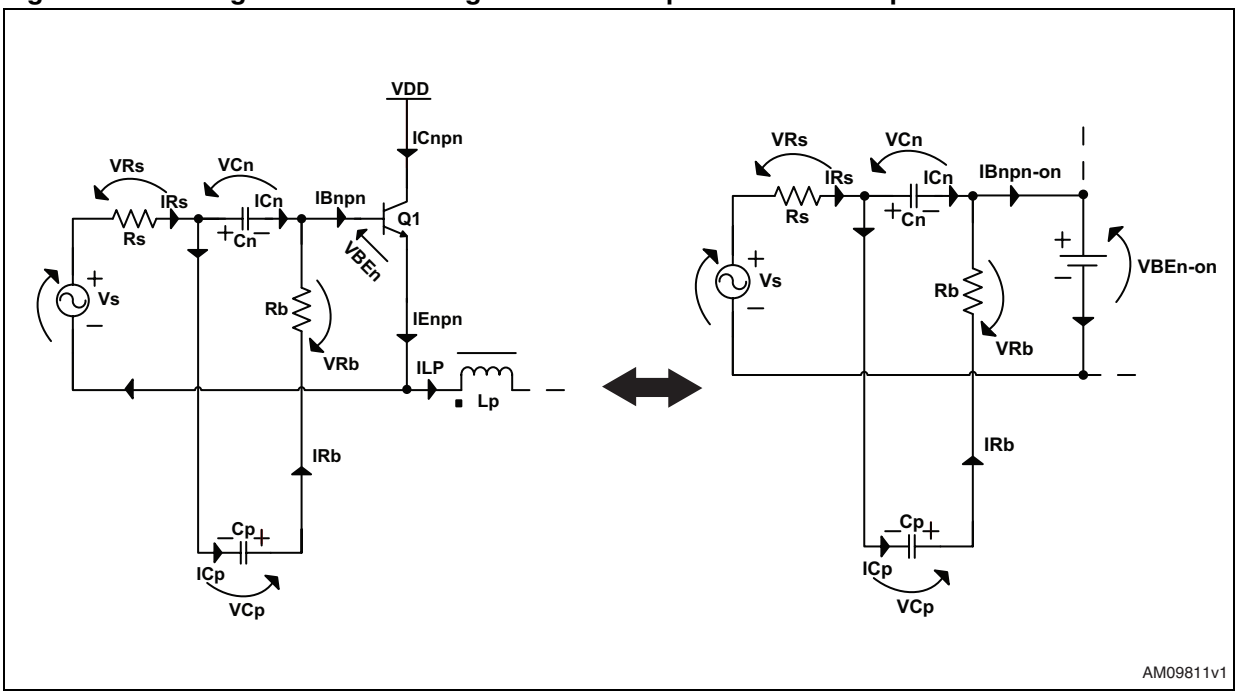
The end of this stage represents the completion of one full conversion cycle and then the process repeats returning to the original operational stage in the complementary direction using the anti-parallel diode D1 before the NPN bipolar transistor Q1 conduction phase.

After the operating modes of the bipolar transistors on the switching converter section have been identified, the corresponding Matlab models of the resonant driving network are created as explained in the following.

6 Driving network modeling

In order to simulate, in Matlab environment, the self-oscillating resonant network driving the bases of the complementary pair of bipolars in the eight different steady-state working operation phases, a possible method may be to combine, with each other, the circuital equations describing the working conditions of the devices in each stage so as to obtain only one (differential) equation in the specific state variable V_{Cn} or V_{Cp}. For example, the following circuital scheme can be taken as a reference to give a model of the NPN bipolar during the conduction time in which the filter capacitor voltage is represented by an independent voltage generator V_s.

Figure 20. Driving network modeling for the NPN bipolar conduction phase simulation



By combining, with each other, the circuital equations of the previous *System of equations 3*, which describes the working conditions of the NPN bipolar during the conduction time phase, it is possible to obtain the following second order linear differential equation with constant coefficients on the state variable V_{Cn} valid on the (t_2,t_4) time interval:

Equation 2

$$m \cdot \frac{d^2}{dt^2}(V_{Cn}(t)) + h \cdot \frac{d}{dt}(V_{Cn}(t)) + k \cdot V_{Cn}(t) = V_S - V_{BEn} + \tau_B \cdot \frac{d}{dt}(V_S(t)) - \tau_B \cdot \frac{d}{dt}(V_{BEn}(t))$$

in which:

System of equations 11

$$\begin{cases} m = R_S \cdot R_b \cdot C^2 \quad \text{with} \quad C = C_n = C_p \\ h = C \cdot (2R_S + R_b) \\ k = 1 \\ \tau_B = C \cdot R_b \\ V_{BEn} = V_{BEn-on} \\ V_S(t) = V_{C-filter}(t) \end{cases}$$

Two different conditions at the initial instant t_2, respectively, one for the V_{Cn} voltage signal and the other for its function derivative, are needed to impose in order to obtain one, and only one, solution of the *Equation 2*, therefore solving the following Cauchy problem:

System of equations 12

$$\begin{cases} m \cdot \frac{d^2}{dt^2}(V_{Cn}(t)) + h \cdot \frac{d}{dt}(V_{Cn}(t)) + k \cdot V_{Cn}(t) = V_S - V_{BEn} + \tau_B \cdot \frac{d}{dt}(V_S(t)) - \tau_B \cdot \frac{d}{dt}(V_{BEn}(t)) \\ V_{Cn}(t_2) = \gamma_1 \\ \left[\frac{d}{dt}(V_{Cn}(t))\right]_{t=t2} = \gamma_2 \end{cases}$$

As a consequence of the LC filtering action on the voltage signal at the output of the secondary windings, Vs signal can be expressed, with a good approximation, as a sinusoidal voltage generator having the below reported mathematical expression valid in the entire time interval (t_0, t_{12}):

Equation 3

$$V_S(t) = A \cdot \text{sen}(2\pi ft) \text{ with } t_0 < t < t_{12}$$

Then, imposing $V_{BEn}=V_{BEsat}$=constant for the NPN device base-emitter junction during its conduction phase (that is $\frac{d}{dt}(V_{BEn}(t)) = 0$), it is possible to change the *System of equations 12* into the form with $\omega=2\pi f$:

System of equations 13

$$\begin{cases} \frac{d^2}{dt^2}(V_{Cn}(t)) + \frac{h}{m}\cdot\frac{d}{dt}(V_{Cn}(t)) + \frac{k}{m}V_{Cn}(t) = \frac{A}{m}\cdot sen(\omega t) - \frac{V_{BEn}}{m} + \frac{\tau_B \cdot A \cdot \omega}{m}\cdot\cos(\omega t) \\ V_{Cn}(t_2) = \gamma_1 \\ \left[\frac{d}{dt}(V_{Cn}(t))\right]_{t=t2} = \gamma_2 \end{cases}$$

Therefore, the second order linear differential equation with constant coefficients on the state variable V_{Cn} takes the form of the physics law that rules the motion of a dumped harmonic oscillator driven by an externally applied forcing signal given by the superimposition of two independent sinusoidal generators $V_{S1} = \frac{A}{m}\cdot sen(\omega t)$ and $V_{S2} = \frac{\tau_B \cdot A \cdot \omega}{m}\cdot\cos(\omega t)$. After having re-written this equation in the form:

Equation 4

$$\frac{d^2}{dt^2}(V_{Cn}(t)) + 2\xi\omega_0 \cdot \frac{d}{dt}(V_{Cn}(t)) + {\omega_0}^2 \cdot V_{Cn}(t) = \frac{A}{m}\cdot sen(\omega t) - \frac{V_{BEn}}{m} + \frac{\tau_B \cdot A \cdot \omega}{m}\cos(\omega t)$$

in which it is fixed:

System of equations 14

$$\begin{cases} {\omega_0}^2 = \frac{k}{m} \\ 2\xi\omega_0 = \frac{h}{m} \Rightarrow \xi = \frac{h}{2\omega_0 m} = \frac{h}{2\sqrt{m\cdot k}} \end{cases}$$

it is possible to obtain the general solution as the sum of a transient solution (associated homogeneous equation solution or unforced equation) that depends on initial conditions, and a steady-state solution (particular solution) that is independent by the initial conditions but depends only on the amplitudes of the driving signals ($\frac{A}{m}$, and $\frac{V_{BEn}}{m}$), driving frequency (ω), undamped angular frequency (ω_0), and the damping ratio (ξ).

Steady-state solution is proportional to the driving forces with an induced phase change of ϕ as follows:

Equation 5

$$V_{Cn-steadystate}(t) = |G(j\omega)|\cdot\left(\frac{A}{m}\cdot sen(\omega t + \phi) + \frac{t_B \cdot A \cdot \omega}{m}\cdot\cos(\omega t + \phi)\right) - \frac{V_{BEn}}{{\omega_0}^2 \cdot m}$$

where $|G(j\omega)| = \frac{1}{\sqrt{(2\omega_0\omega\xi)^2 + \left({\omega_0}^2 - \omega^2\right)^2}}$ and $\phi = \angle G(j\omega) = \text{arctg}\left(\frac{2\omega\omega_0\xi}{\omega^2 - {\omega_0}^2}\right)$ are respectively module and phase of the frequency response function $G(j\omega)$.

Resolving the polynomial characteristic of *Equation 4*, the following can be obtained:

Equation 6

$$\lambda^2 + 2\xi\omega_0 \cdot \lambda + {\omega_0}^2 = 0 \Rightarrow \lambda_{1,2} = -\xi\omega_0 \pm \sqrt{(\xi\omega_0)^2 - {\omega_0}^2}$$

with $\Delta = (\xi\omega_0)^2 - {\omega_0}^2 = \frac{1}{4 \cdot m^2}(h^2 - 4mk) = \frac{4 \cdot {R_S}^2 + {R_B}^2}{4 \cdot {R_S}^2 \cdot {R_B}^2 \cdot C^2} > 0$ implying that λ_1 and λ_2 are distinct real roots and then the particular solution is on the forms:

Equation 7

$$V_{Cn-transient}(t) = c_1 \cdot e^{\lambda_1 \cdot t} + c_2 \cdot e^{\lambda_2 \cdot t}$$

The general solution V_{Cn} is the sum of steady-state solution *Equation 5* and the transient solution *Equation 7* reported as follows:

$V_{Cn}(t) = V_{Cn-steadystate}(t) + V_{Cn-transient}(t)$ valid on the (t_2,t_4) time interval in which V_{BEn}=constant for hypothesis.

In order to free the V_{Cn} signal calculation by the imposition of its derivative value at the initial instant t_2 on the Cauchy problem resolution referred to in the *System of equations 12*, the method used to simulate in Matlab environment the driving network, in each working phase for the bipolar devices, is based on resolving a system of two first order linear differential equations on the two state variables V_{Cn} and V_{Cp} combined with each other as explained in the following. By simulating with the Matlab tool, the ODE45 solver algorithm has been used for the resolution of the initial value problem concerning the system of ordinary differential equations related to each operation phase of the opportunely modeled bipolars during the steady-state working condition. The ODE45 function uses the syntax expressed by the command:

[t,Y]= ode45 (odefun, tspan, y0, options)

Input arguments to the solver are listed as:

- odefun → Function, expressed with a Matlab function-file, that evaluates the right side of the differential equations.
- tspan → Vector specifying the interval of integration (t_0,t_f). The solver imposes the initial conditions at t_0=t_{span}(1) and integrates from t_0 to t_f =t_{span}(end).
- y0 → Vector of initial conditions.
- options → Structure of optional parameters that change the default integration properties.

Output arguments for the solver are the following:

- t → Column vector of time points.
- Y → Solution array. Each row in y corresponds to the solution at a time returned in the corresponding row of t.

The solver integrates the system of differential equations y'=f(t,y) from time t_0 to t_f with initial conditions y0. Function f=odefun(t,y), for a scalar t and a column vector y, must return a column vector f corresponding to f(t,y). Each row in the solution array Y corresponds to a time returned in column vector T. The ODE45 solves with default integration parameters

replaced by property values specified in 'options', an argument created with the 'odeset' function having the following syntax:

options = odeset ('RelTol',value1,'AbsTol',value2)

in which scalar relative error tolerance RelTol is set equal to 1e-5 (1e-3 by default) and the vector of absolute error tolerance AbsTol is set equal to 1e-8 (all components are 1e-6 by default).

7 NPN conduction phase modeling

In order to adequately simulate the NPN conduction time phase through the Matlab tool, the function solution V_{Cn} of the *System of equations 12* can be equivalently obtained, together with V_{Cp} function, resolving the following system of two first order linear differential equations on the two state variables V_{Cn} and V_{Cp} valid on the $[t_2, t_4]$ time interval with the initial hypothesis of V_{BEn}=constant and $C=C_n=C_p$:

System of equations 15

$$\begin{cases} \frac{d}{dt}\left(V_{Cn-npncon}(t)\right) = -\frac{1}{C}\cdot\left(\frac{1}{R_S}+\frac{1}{R_b}\right)\cdot V_{Cn-npncon} - \frac{1}{C\cdot R_b}\cdot V_{Cp-npncon} + \frac{V_S}{C\cdot R_S} - \frac{V_{BEn}}{C\cdot R_S} \\ \frac{d}{dt}\left(V_{Cp-npncon}(t)\right) = -\frac{1}{C\cdot R_b}\cdot V_{Cn-npncon} - \frac{1}{C\cdot R_b}\cdot V_{Cp-npncon} \\ V_{Cn-npncon}(t_{2+}) = V_{Cn-npnric}(t_{2-}) \\ V_{Cp-npncon}(t_{2+}) = V_{Cp-npnric}(t_{2-}) \end{cases}$$

As seen, only two conditions, respectively, for the V_{Cn} and V_{Cp} voltages at the initial instant t_2, are needed to be imposed for the resolution of the *System of equations 15*. These two initial conditions $V_{Cn-npnric}(t_{2-}) = V_{Cn-npncon}(t_{2+})$ and $V_{Cp-npnric}(t_{2-}) = V_{Cp-npncon}(t_{2+})$, are fixed in order to guarantee the continuity for the V_{Cn} and V_{Cp} waveforms passing from the re-circulating phase to the NPN bipolar conduction time phase, being $V_{Cn-npnric}(t_{2-})$ and $V_{Cp-npnric}(t_{2-})$ the values for V_{Cn} and V_{Cp} functions obtained at the re-circulating phase final instant t_2. After that, the two V_{Cn} and V_{Cp} functions have been obtained by resolving the previous system, the NPN bipolar base current $I_{Bnpn\text{-}on}$ is directly given by the following formula:

Equation 8

$$I_{Bnpn-on}(t) = I_{Cn-npncon}(t) + I_{Cp-npncon}(t) = C\cdot\frac{d}{dt}\left(V_{Cn-npncon}(t)\right) - C\cdot\frac{d}{dt}\left(V_{Cp-npncon}(t)\right)$$

in which $V_{Cp-npncon}(t)$ is a discharging voltage on the C_p capacitor (that is $\frac{d}{dt}\left(V_{Cp-npncon}(t)\right) < 0$). After having determined, through the ODE45 simulator, in a rather large time interval (one half of the total working period), the V_{Cn} and V_{Cp} voltage functions that resolve the *System of equations 15*, then a research of the maximum value for the V_{Cn} function was imposed in order to determinate the final instant of the NPN conduction time t_4.

This NPN conduction time phase is preceded by the re-circulating phase which follows.

8 Modeling of re-circulating phase preliminary to the NPN conduction time phase

The re-circulating phase before the NPN bipolar conduction time is modeled taking into consideration the following circuital schemes in which the I_{LP} signal represents the demagnetization current of the inductor Lp and I_{BCn} is the NPN device base-collector diode junction forward biased current on the first re-circulating phase:

Figure 21. Driving network modeling for the simulation of the first re-circulating phase preliminary to the NPN bipolar conduction time phase

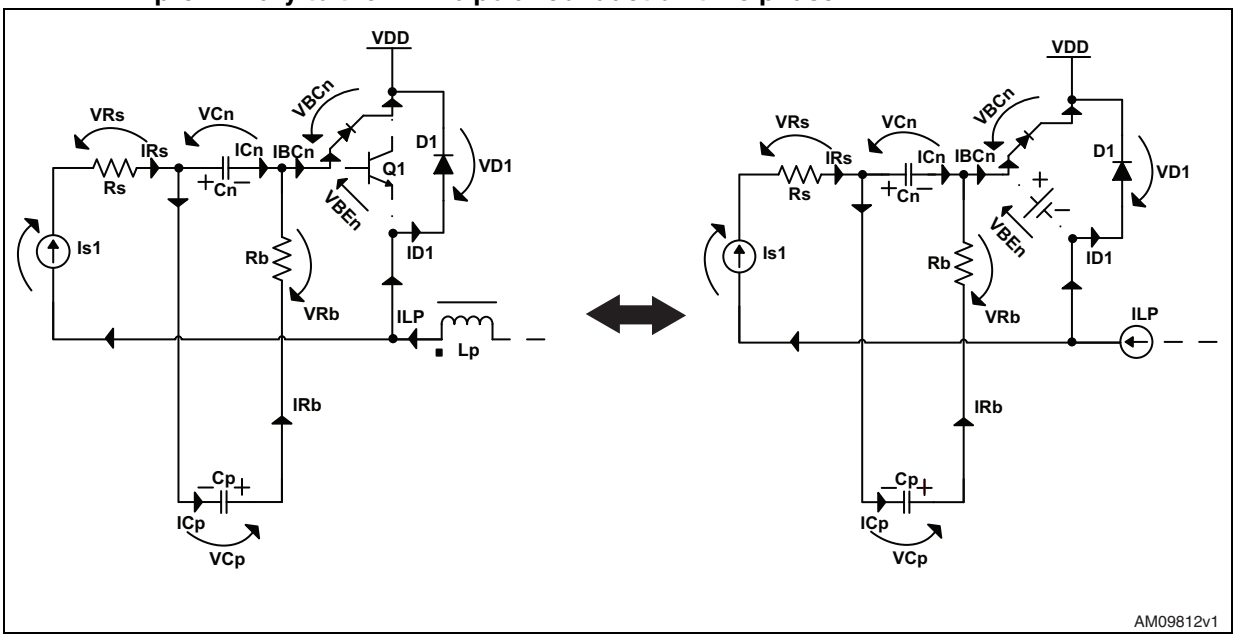
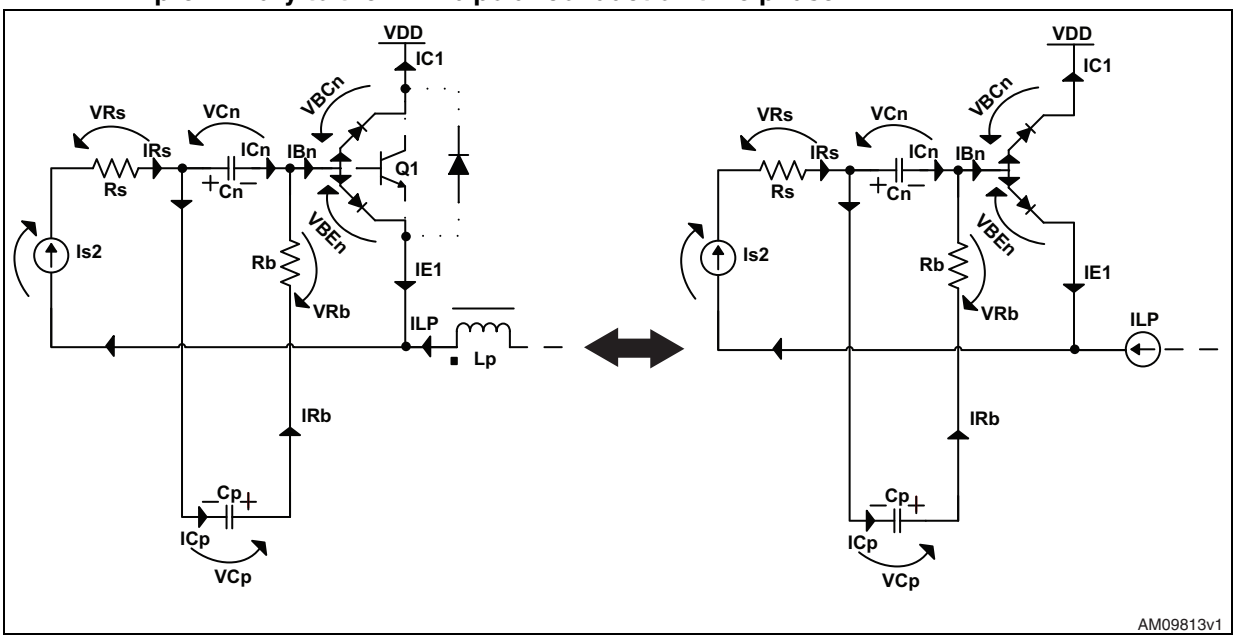


Figure 22. Driving network modeling for the simulation of the second re-circulating phase preliminary to the NPN bipolar conduction time phase



Equations of the two *System of equations 1* and *System of equations 2*, describing the working conditions of the NPN bipolar during the re-circulating phases before the NPN bipolar conduction time, can be combined with each other in order to obtain the following system of two first order linear differential equations valid on all the $[t_0,t_2]$ time interval with $C=C_n=C_p$:

System of equations 16

$$\begin{cases} \frac{d}{dt}\left(V_{Cn-npnric}(t)\right) = -\frac{1}{C\cdot R_b}\cdot V_{Cn-npnric} - \frac{1}{C\cdot R_b}\cdot V_{Cp-npnric} + \frac{I_S}{C} \\ \frac{d}{dt}\left(V_{Cp-npnric}(t)\right) = -\frac{1}{C\cdot R_b}\cdot V_{Cn-npnric} - \frac{1}{C\cdot R_b}\cdot V_{Cp-npnric} \\ V_{Cn-npnric}(t_0) = \gamma_0 \quad \text{(initial value fixed)} \\ V_{Cp-npnric}(t_0) = \vartheta_0 \quad \text{(initial value fixed)} \end{cases}$$

where:

System of equations 17

$$I_S = \begin{cases} I_{S1} = I_{RS} = I_{LP} - I_{D1} = I_{Cn} + I_{Cp} = I_{BCn} \quad \text{for} \quad t0<t<t1; \\ I_{S2} = I_{RS} = I_{LP} + I_{E1} = I_{Cn} + I_{Cp} = I_{Bn} \quad \text{for} \quad t1<t<t2; \end{cases}$$

During the simulation phase, solutions for the V_{Cn} and V_{Cp} voltage functions have been calculated with the ODE45 simulator in a time interval as large as the length of the I_s forcing

signal opportunely modeled in order to take into consideration the effect of demagnetization current for the inductor L_p.

Also in this case, for the NPN bipolar base current I_{Bnpn}, the formula below is valid during the whole re-circulating phase preliminary to the NPN conduction time phase:

Equation 9

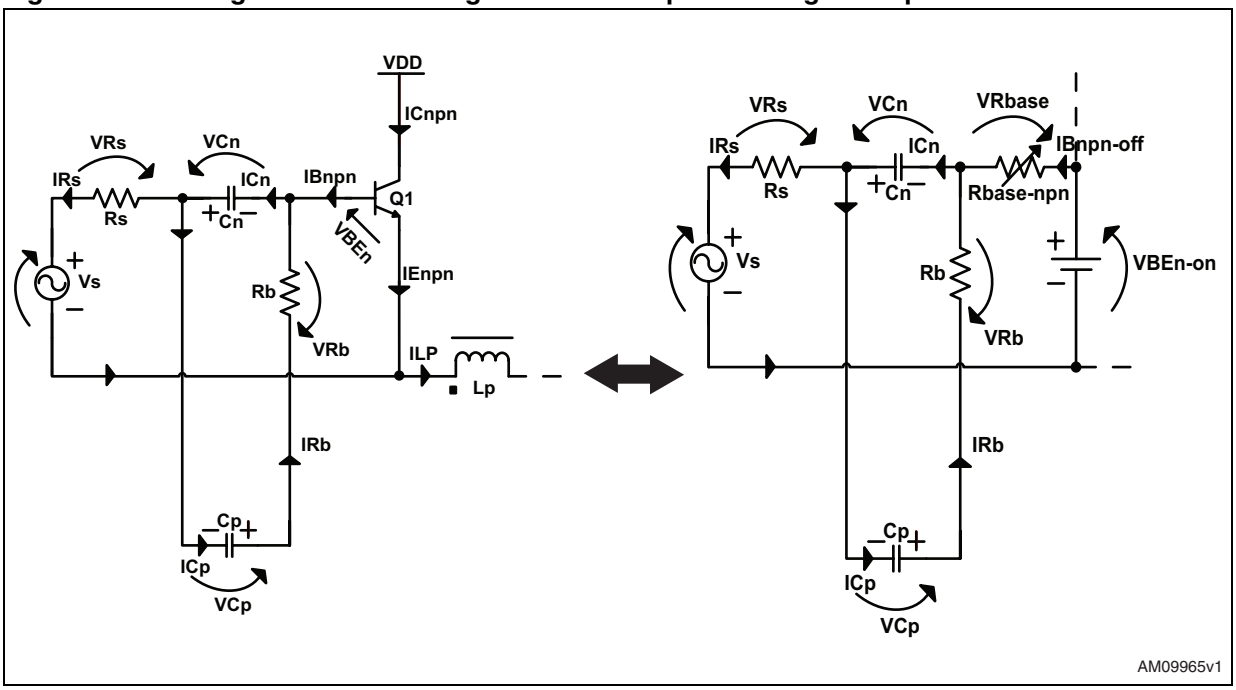
$$I_{Bnpn}(t) = I_{Cn-npnric}(t) + I_{Cp-npnric}(t) = C \cdot \frac{d}{dt}\left(V_{Cn-npnric}(t)\right) - C \cdot \frac{d}{dt}\left(V_{Cp-npnric}(t)\right)$$

in which $V_{Cp-npnric}(t)$ is a discharging voltage on the C_p capacitor (that is $\frac{d}{dt}\left(V_{Cp-npnric}(t)\right) < 0$).

9 NPN storage time phase modeling

During the NPN storage time phase the base-emitter voltage does not change from its forward bias value ($V_{BEn-on} = V_{BEn-sat}$) due to the excess minority carriers stored in the base region. A negative base current starts removing this excess carrier at a rate determined by the base driving network. NPN bipolar working condition during this phase is modeled by the following circuital scheme in which $R_{base-npn}$ is an opportunely sized variable resistor that takes into consideration the effect of the base resistance modulation (increase) due to the removal of the excess carriers:

Figure 23. Driving network modeling for the NPN bipolar storage time phase simulation



By combining, with each other, the equations of the *System of equations 4*, describing the working conditions of the NPN bipolar during the NPN bipolar storage time phase, the following system of two first order linear differential equations valid on all the $[t_4,t_5]$ time interval with $C=C_n=C_p$:

System of equations 18

$$\begin{cases} \frac{d}{dt}\left(V_{Cn-npnsto}(t)\right) = -\frac{1}{C \cdot R_b} \cdot \left(1 + \frac{R_b}{R_S + R_{Base-npn}}\right) \cdot V_{Cn-npnsto} - \frac{1}{C \cdot R_b} \cdot V_{Cp-npnsto} + \\ + \frac{V_S}{C \cdot \left(R_S + R_{Base-npn}\right)} - \frac{V_{BEn}}{C \cdot \left(R_S + R_{Base-npn}\right)} \\ \frac{d}{dt}\left(V_{Cp-npnsto}(t)\right) = -\frac{1}{C \cdot R_b} \cdot V_{Cn-npnsto} - \frac{1}{C \cdot R_b} \cdot V_{Cp-npnsto} \\ V_{Cn-npnsto}(t_{4+}) = V_{Cn-npncon}(t_{4-}) \\ V_{Cp-npnsto}(t_{4+}) = V_{Cp-npncon}(t_{4-}) \end{cases}$$

in which V_{BEn}=constant, and for $R_{Base\text{-}npn}(t)$ an increasing variability law, of the following type, is imposed:

Equation 10

$$R_{Base-npn}(t) = \alpha_1 \cdot t^n \quad \text{with} \quad 0 \le t \le \Delta_{npn}$$

where coefficients α_1 and n (this last integer number) are determined so that $R_{Base\text{-}npn}(t)$ has a fixed and constant mean value $R_{Base\text{-}npn\text{-}mean}$ during the NPN storage time period of length equal to Δ_{npn} seconds:

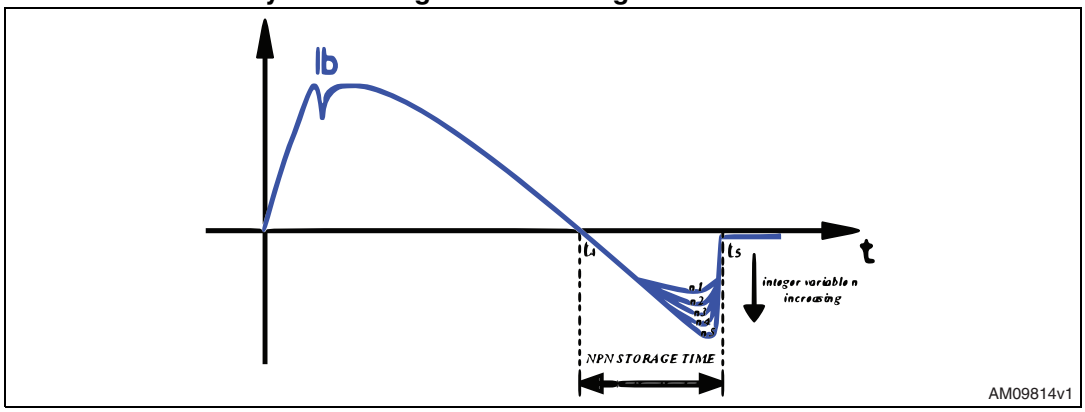
Equation 11

$$R_{Base-npn-mean} = \frac{1}{\Delta_{npn}} \cdot \int_0^{\Delta_{npn}} R_{Base-npn}(t)dt \Rightarrow \alpha_1 = \frac{R_{Base-npn-mean} \cdot \Delta_{npn} \cdot (n+1)}{\Delta_{npn}^{(n+1)}} =$$

$$(\text{by imposing} \quad \Delta_{npn} = T_{Storage-npn} = t_5 - t_4) = \frac{R_{Base-npn-mean} \cdot (n+1)}{(t_5 - t_4)^n}$$

Maintaining constant the $T_{Storage\text{-}npn}=t_5 - t_4$ time, with an increase of the function $R_{Base\text{-}npn(t)}$ order n, so also the base resistance modulation effect approximation changes with a proportional increase of the negative peak of $I_{Bnpn\text{-}off}$ current increases, as the following shows:

Figure 24. Variability of the extractive current negative peak $I_{Bnpn\text{-}off}$ versus variability of the integer n with storage time fixed



Therefore, it is important to fix correctly the two α_1 and n parameters in order to opportunely model the transistor base resistance modulation effect during the storage time phase simulation.

The following mathematical formula has been considered to make a connection among the storage time duration and the base currents developing during the conduction and storage time phases of the device (see *References 3*):

Equation 12

$$T_{storage-npn} = \sigma_{npn} \cdot \ln\left[1 + \frac{I_{Bnpn-on-average}}{\left|I_{Bnpn-off-average}\right|}\right]$$

In which:

- $I_{Bnpn-on-average} = \frac{A_{on-npn}}{T_{on-npn}}$ with A_{on-npn} area subtended to the $I_{Bnpn-on}$ current curve during the T_{on} conduction period;
- $\left|I_{Bnpn-off-average}\right| = \frac{A_{storage-npn}}{T_{storage-npn}}$ with $A_{storage-npn}$ the module of the area (positive) subtended to the $I_{Bnpn-off}$ current curve during the $T_{storage-npn}$ storage time period;
- σ_{npn} is a time constant directly connected to the lifetime of the minority carriers (electrons) in the transistor base.

Constant σ_{npn} can be experimentally calculated, with a good approximation, supposing two triangular areas subtended respectively to the $I_{Bnpn-on}$ and $I_{Bnpn-off}$ current curves and, in this case, *Equation 12* assumes the following simplified form:

Equation 13

$$T_{storage-npn} = \sigma_{npn} \cdot \ln\left[1 + \frac{I_{Bnpn-on-max}}{\left|I_{Bnpn-off-max}\right|}\right] \Rightarrow \sigma_{npn} = \frac{T_{storage-npn}}{\ln\left[1 + \frac{I_{Bnpn-on-max}}{\left|I_{Bnpn-off-max}\right|}\right]}$$

being $I_{Bnpn-on-max}$ and $\left|I_{Bnpn-off-max}\right|$ the maximum values of the conduction and extraction (in module) currents. Consequently, the σ_{npn} value can be mathematically and, in an approximate manner, determined if the values of the $T_{storage-npn}$, $I_{Bnpn-on-max}$ and $I_{Bnpn-off-max}$ assumed (measured) by the devices during the applicative steady-state working conditions are well-known.

Substituting the definitions of the $I_{Bnpn-on-average}$, $I_{Bnp-off-avarage}$ and σ_{npn} parameter to *Equation 12*, the following equation is obtained:

Equation 14

$$T_{storage-npn} = \sigma_{npn} \cdot \ln\left[1 + \frac{1}{T_{on-npn}} \cdot \frac{T_{storage-npn}}{\varepsilon_{npn}}\right]$$

in which the following is imposed:

Equation 15

$$\varepsilon_{npn} = \frac{A_{storage-npn}}{A_{on-npn}}$$

with ε_{npn} parameter depending on the recombination phenomenon of a share of the amount of charges in base. Once the two parameters σ_{npn} and $T_{on\text{-}npn}$ are fixed and well-known (the latter parameter obtained from the simulation of the previous conduction period) *Equation 14* is used to define the function of two independent variables:

Equation 16

$$f(T_{storage-npn}, \varepsilon_{npn}) = T_{storage-npn} - \sigma_{npn} \cdot \ln\left[1 + \frac{1}{T_{on-npn}} \cdot \frac{T_{storage-npn}}{\varepsilon_{npn}}\right]$$

In order to determine the length of the time interval to set for the NPN storage time simulation with the ODE45 simulator, the following procedure has been applied through the Matlab tool:

- m different $\varepsilon(i)_{npn}$ values, increasing, equally-spaced out and included between a minimum $\varepsilon_{min\text{-}npn}$ and a maximum $\varepsilon_{max\text{-}npn}$ value, are fixed in base to the recombination characteristics of the minority carriers in base of the bipolar examined, that is:

Equation 17

$$\varepsilon(i)_{npn} \quad \text{for } i = 1 \div m \quad \text{with } \varepsilon_{min-npn} \le \varepsilon(i)_{npn} \le \varepsilon_{max-npn}$$

and also with:

Equation 18

$$\varepsilon(j)_{npn} \ne \varepsilon(j+1)_{npn} \text{ for } j = 1 \div (m-1)$$

Equation 19

$$\varepsilon(k)_{npn} - \varepsilon(k-1)_{npn} = \varepsilon(k+1)_{npn} - \varepsilon(k)_{npn} \quad \text{for } k = 2 \div (m-1)$$

- m zeros of the defined function $f(T_{storage\text{-}npn}, \varepsilon_{npn})$ are evaluated with the Matlab tool for each $\varepsilon(i)_{npn}$ fixed:

Equation 20

$$f(T(i)_{storage-npn}, \varepsilon(i)_{npn}) = 0 \qquad \text{for } i = 1 \div m$$

- $T_{storage\text{-}npn}$ final value is obtained performing an arithmetical average operation among all the $T(i)_{storage\text{-}npn}$ so calculated:

Equation 21

$$T_{storage-npn} = \text{mean}\left(T(1)_{storage-npn}, \ldots\ldots, T(m)_{storage-npn}\right) = \frac{1}{m} \cdot \sum_{i=1}^{m} T(i)_{storage-npn}$$

Setting the values $\varepsilon_{min\text{-}npn}$, $\varepsilon_{max\text{-}npn}$ with the two parameters σ_{npn} and $T_{on\text{-}npn}$ well-known, a realistic evaluation of the effective NPN device storage time can be obtained applying the procedure of calculation previously explained.

After having found, with the ODE45 simulator, in the calculated time interval $T_{storage\text{-}npn}$, the solutions of the *System of equations 18* for the V_{Cn} and V_{Cp} voltage functions, then the NPN bipolar base current $I_{Bnpn\text{-}off}$ is given by the following formula:

Equation 22

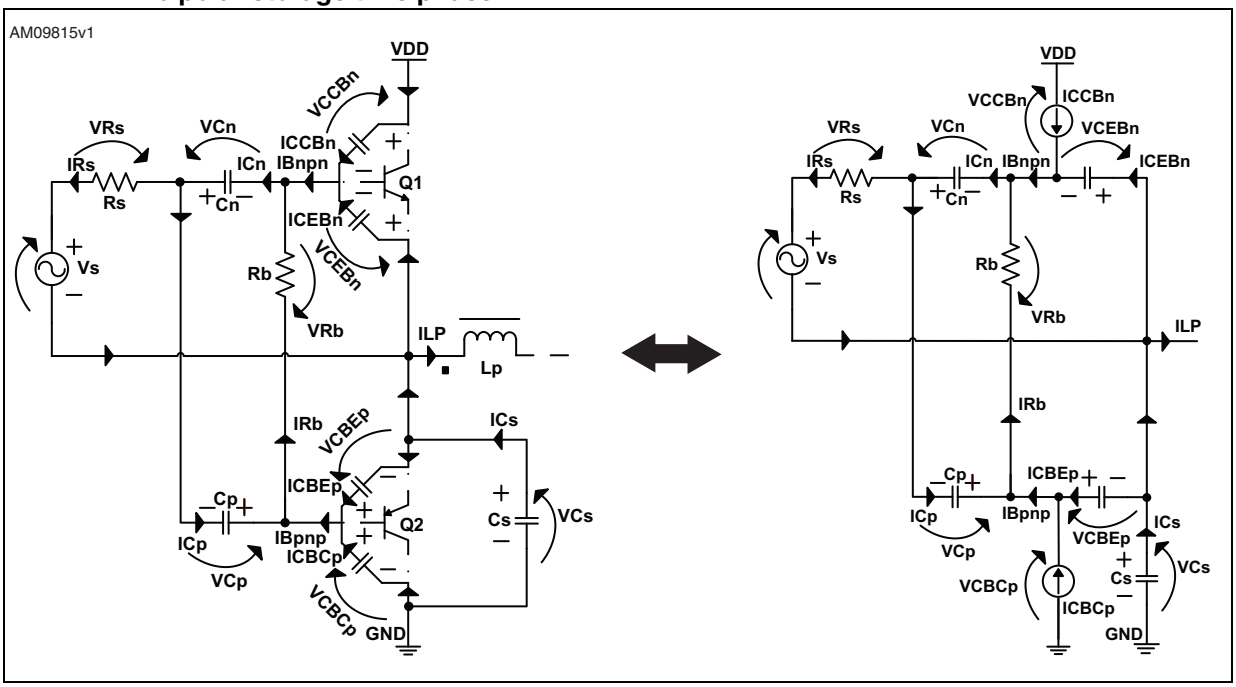
$$I_{Bnpn-off}(t) = I_{Cn-npnsto}(t) - I_{Cp-npnsto}(t) = -C \cdot \frac{d}{dt}\left(V_{Cn-npnsto}(t)\right) + C \cdot \frac{d}{dt}\left(V_{Cp-npnsto}(t)\right)$$

in which both $V_{Cn\text{-}npnsto}(t)$ and $V_{Cp\text{-}npnsto}(t)$ are discharging voltages respectively on the C_n and C_p capacitors (that is $\frac{d}{dt}\left(V_{Cn-npnsto}(t)\right) < 0$ and $\frac{d}{dt}\left(V_{Cp-npnsto}(t)\right) < 0$).

10 Modeling of the dead time after the NPN storage time phase

During the phase concerning the dead time after the NPN storage time both complementary pairs of bipolars are inactive and their B-C and B-E junctions are reverse biased. So, in order to model this phase, the following circuital scheme in which the B-C and B-E junctions are represented by the respective junction capacitances charging or discharging according to the working condition, respectively, of the NPN and PNP device is considered.

Figure 25. Driving network modeling for the simulation of the dead time phase after the NPN bipolar storage time phase



Neglecting the currents I_{CEBn} and I_{CBEp} of the reverse biased B-E junction capacitances of the two bipolars, the following conditions are obtained:

Equation 23

$$I_{CEBn}, I_{CBEp} \cong 0 \Rightarrow I_{Bnpn} \cong I_{CCBn}\ , I_{Bpnp} \cong I_{CBCp} \text{ and } I_{CS} \cong I_{LP}$$

where:

- $I_{CCBn} = C_{CBnpn} \cdot \frac{d}{dt}(V_{CCBn}(t))$ on the charge phase of the (variable) NPN base-collector junction capacitance C_{CBnpn};
- $I_{CBCp} = -C_{BCpnp} \cdot \frac{d}{dt}(V_{CBCp}(t))$ on the discharge phase of the (variable) PNP collector-base junction capacitance C_{BCpnp}.

Then, imposing the previous assumptions, combining, with each other, the equations of the *System of equations 5*, describing the working conditions of the NPN bipolar during this

phase, the following system of two first order linear differential equations is valid on all the $[t_5,t_6]$ time interval with $C=C_n=C_p$:

System of equations 19

$$\begin{cases} \frac{d}{dt}\left(V_{Cn-npndead}(t)\right) = -\frac{1}{C}\cdot\left(\frac{1}{R_S}+\frac{1}{R_b}\right)\cdot V_{Cn-npndead} - \frac{1}{C\cdot R_b}\cdot V_{Cp-npndead} + \frac{1}{C}\cdot I_{CBCp} + \frac{V_S}{C\cdot R_S} + \frac{V_{CEBn}}{C\cdot R_S} \\ \frac{d}{dt}\left(V_{Cp-npndead}(t)\right) = \frac{1}{C}\cdot\left(\frac{1}{R_S}-\frac{1}{R_b}\right)\cdot V_{Cn-npndead} - \frac{1}{C\cdot R_b}\cdot V_{Cp-npndead} - \frac{1}{C}\cdot I_{CCBn} - \frac{V_S}{C\cdot R_S} - \frac{V_{CEBn}}{C\cdot R_S} \\ V_{Cn-npndead}(t_{5+}) = V_{Cn-npnsto}(t_{5-}) \\ V_{Cp-npndead}(t_{5+}) = V_{Cp-npnsto}(t_{5-}) \end{cases}$$

in which $V_{BEn}= -V_{CEBn}<0$ and $V_{EBp}= -V_{CBEp}<0$ is an opportunely modeled signal complying with the following function:

Equation 24

$$V_{CEBn} = \left(\frac{I_{CCBn}}{C_{CBnpn}} - \frac{I_{CS}}{C_S}\right)\cdot t + \psi_1$$

in which ψ_1 is a constant depending on the initial value of the V_{CEBn} voltage at $t=t_{5-}$. The length of this dead time interval fixed for the simulation, in which the V_{Cn} and V_{Cp} voltage functions are determined through the ODE45 simulator, is imposed to be given by the following formula in which $T_{npnsto}=t_5-t_4$, $T_{npncon}=t_4-t_2$ and $T_{npnric}=t_2-t_0$:

Equation 25

$$T_{npndead} = t_6 - t_5 = \frac{1}{2f} - T_{npnsto} - T_{npncon} - T_{npnric}$$

This last working operation phase described completes the resonant driving network modeling with reference to the variation over a one-half period of the voltage signal V(s) across the filter capacitor and in particular concerning the time intervals, in sequence, shortly before (re-circulating phase), during (conduction phase) and afterwards (dead time) the NPN bipolar device functional stage. In the second one-half period the voltage signal V(s) has an opposite polarity compared to the first one and an analytical procedure similar to the NPN device modeling technique is applied for the PNP bipolar device interested in being simulated during its sequential working condition phases, as subsequently shown.

11 Modeling of the re-circulating phase preliminary to the PNP conduction time phase

The re-circulating phase before the PNP bipolar conduction time is modeled taking into consideration the following circuital scheme in which I_{LP} signal represents the demagnetization current of the inductor Lp and ICBp is the PNP device collector-base diode junction forward biased current on the first re-circulating phase:

Figure 26. Driving network modeling for the simulation of the first re-circulating phase preliminary to the PNP bipolar conduction time phase

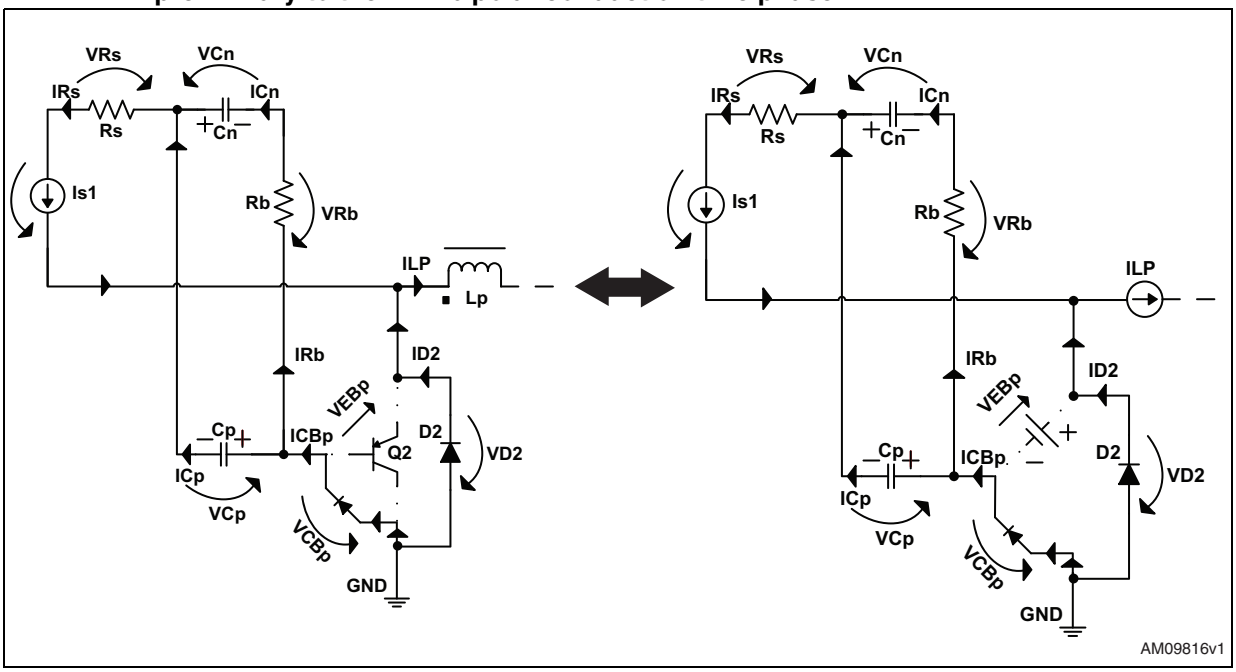
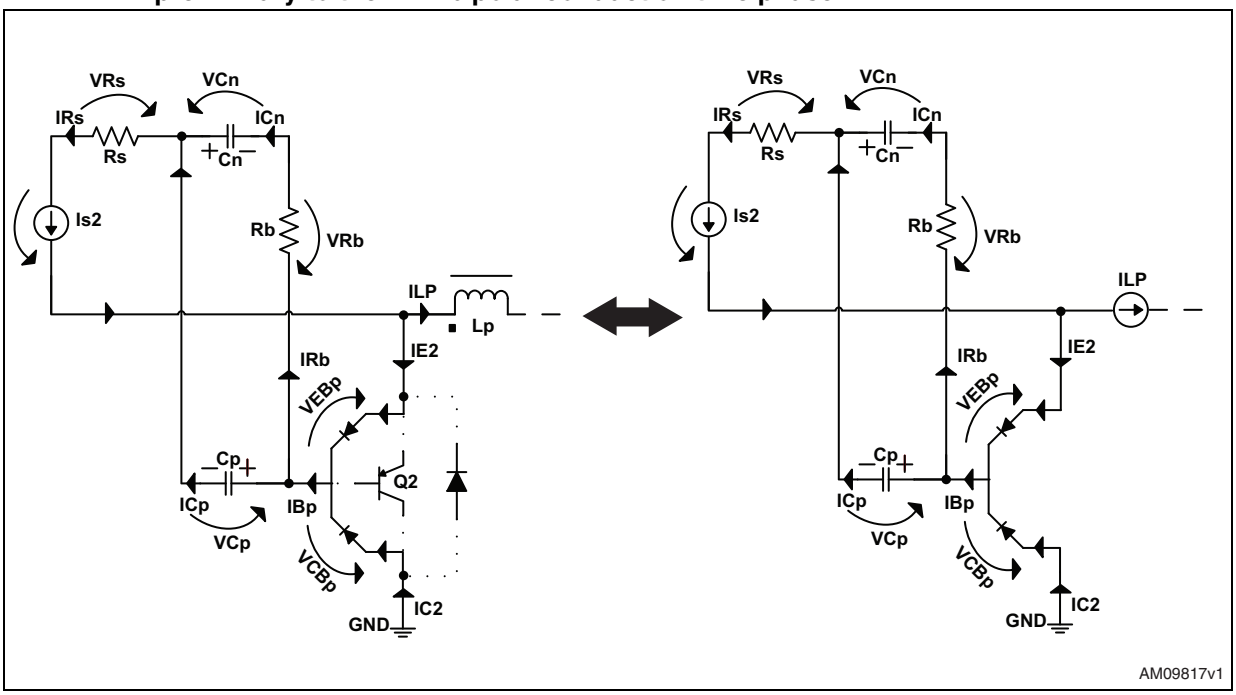


Figure 27. Driving network modeling for the simulation of the second re-circulating phase preliminary to the PNP bipolar conduction time phase



Equations in the *System of equations 6* and *System of equations 7*, describing the working conditions of the PNP bipolar during the re-circulating phase before the PNP bipolar conduction time, can be combined, with each other, in order to obtain the following system of two first order linear differential equations valid on all the $[t_6,t_8]$ time interval with $C=C_n=C_p$:

System of equations 20

$$\begin{cases} \frac{d}{dt}\left(V_{Cn-pnpric}(t)\right) = -\frac{1}{C \cdot R_b} \cdot V_{Cn-pnpric} - \frac{1}{C \cdot R_b} \cdot V_{Cp-pnpric} \\ \frac{d}{dt}\left(V_{Cp-pnpric}(t)\right) = -\frac{1}{C \cdot R_b} \cdot V_{Cn-pnpric} - \frac{1}{C \cdot R_b} \cdot V_{Cp-pnpric} + \frac{I_S}{C} \\ V_{Cn-pnpric}(t_{6+}) = V_{Cn-npndead}(t_{6-}) \\ V_{Cp-pnpric}(t_{6+}) = V_{Cp-npndead}(t_{6-}) \end{cases}$$

where:

System of equations 21

$$I_S = \begin{cases} I_{S1} = I_{RS} = I_{LP} - I_{D2} = I_{Cn} + I_{Cp} = I_{CBp} & \text{for } t6<t<t7; \\ I_{S2} = I_{RS} = I_{LP} + I_{E2} = I_{Cn} + I_{Cp} = I_{Bp} & \text{for } t7<t<t8; \end{cases}$$

During the simulation phase, solutions for the V_{Cn} and V_{Cp} voltage functions have been calculated with the ODE45 simulator in a time interval as large as the length of the forcing signal Is opportunely modeled in order to take into consideration the effect of demagnetization current for the inductor L_p.

For the PNP bipolar base current I_{Bpnp}, the following formula reported is valid during the whole re-circulating phase preliminary to the PNP conduction time:

Equation 26

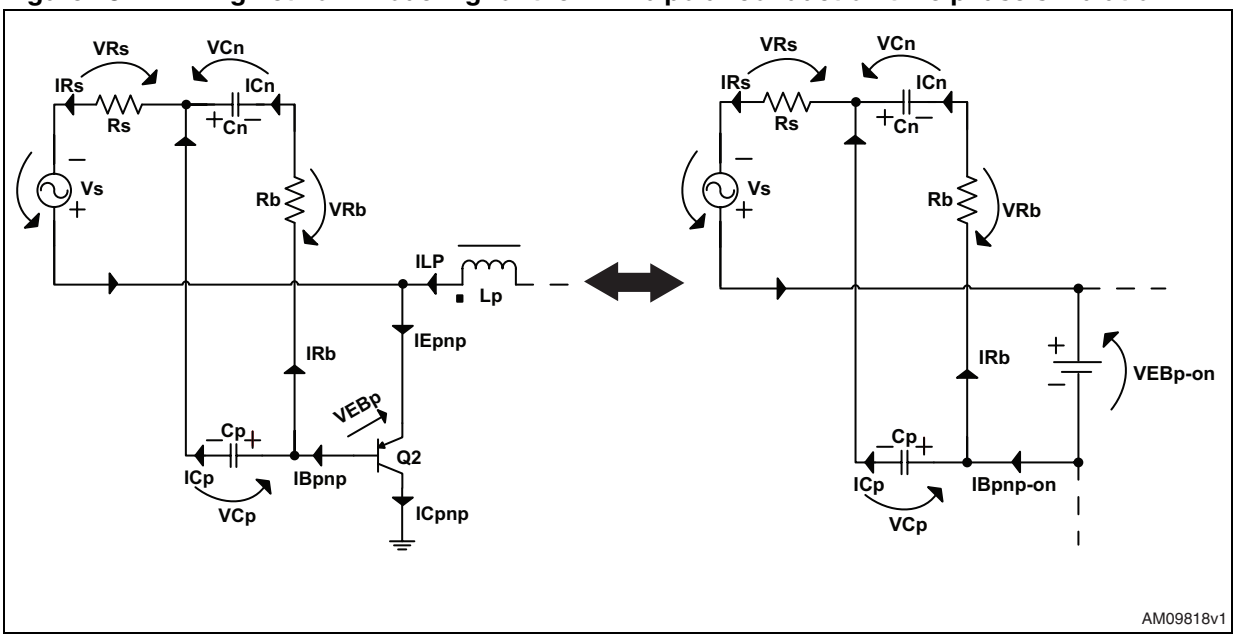
$$I_{Bpnp}(t) = I_{Cn-pnpric}(t) + I_{Cp-pnpric}(t) = -C \cdot \frac{d}{dt}\left(V_{Cn-pnpric}(t)\right) + C \cdot \frac{d}{dt}\left(V_{Cp-pnpric}(t)\right)$$

in which $V_{Cn\text{-}pnpric}(t)$ is a discharging voltage on the C_n capacitor (that is $\frac{d}{dt}\left(V_{Cn-pnpric}(t)\right) < 0$).

12 PNP conduction phase modeling

The PNP conduction time phase is modeled taking into consideration the following circuital scheme in which the VEBp voltage is constant:

Figure 28. Driving network modeling for the PNP bipolar conduction time phase simulation



By combining, with each other, the circuital equations of the previous *System of equations 8*, describing the working conditions of the PNP bipolar during the conduction time phase, the following system of two first order linear differential equations is obtained valid on all the $[t_8,t_{10}]$ time interval in which the signal $V_S(t) = -A \cdot sen(2\pi ft - \pi)$ has the polarity shown in the previous figure and imposed $C=C_n=C_p$:

System of equations 22

$$\begin{cases} \frac{d}{dt}\left(V_{Cn-pnpcon}(t)\right) = -\frac{1}{C \cdot R_b} \cdot V_{Cn-pnpcon} - \frac{1}{C \cdot R_b} \cdot V_{Cp-pnpcon} \\ \frac{d}{dt}\left(V_{Cp-pnpcon}(t)\right) = -\frac{1}{C \cdot R_b} \cdot V_{Cn-pnpcon} - \frac{1}{C} \cdot \left(\frac{1}{R_S} + \frac{1}{R_b}\right) \cdot V_{Cp-pnpcon} + \frac{V_S}{C \cdot R_S} - \frac{V_{EBp}}{C \cdot R_S} \\ V_{Cn-pnpcon}(t_{8+}) = V_{Cn-pnpric}(t_{8-}) \\ V_{Cp-pnpcon}(t_{8+}) = V_{Cp-pnpric}(t_{8-}) \end{cases}$$

After that the two V_{Cn} and V_{Cp} functions have been obtained by resolving the previous system, the PNP bipolar base current $I_{Bpnp\text{-}on}$ is directly given by the following formula:

Equation 27

$$I_{Bpnp-on}(t) = I_{Cn-pnpcon}(t) + I_{Cp-pnpcon}(t) = -C \cdot \frac{d}{dt}\left(V_{Cn-pnpcon}(t)\right) + C \cdot \frac{d}{dt}\left(V_{Cp-pnpcon}(t)\right)$$

in which $V_{Cn\text{-}pnpcon(t)}$ is a discharging voltage on the C_n capacitor

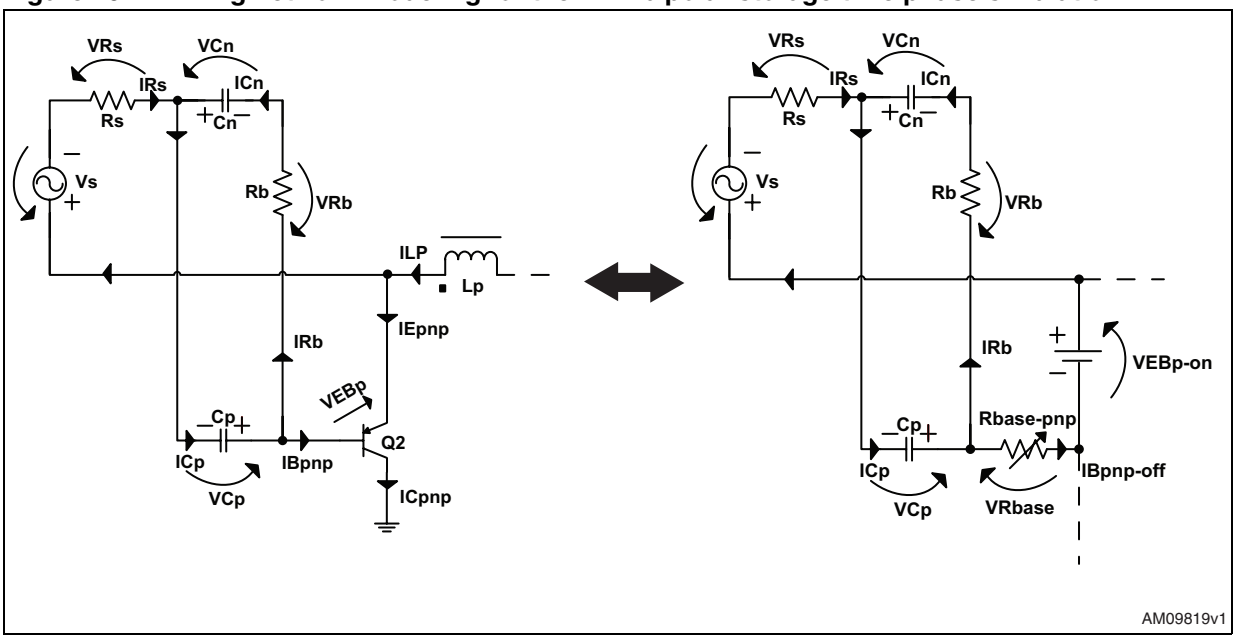
(that is $\frac{d}{dt}\left(V_{Cn-pnpcon}(t)\right) < 0$).

After having determined, through the ODE45 simulator, in a rather large time interval (one half of the total working period), the V_{Cn} and V_{Cp} voltage functions that resolve the *System of equations 22*, a research of the maximum value for the V_{Cp} function was imposed in order to determinate the final instant of the PNP conduction time t_{10}.

13 PNP storage time phase modeling

During the PNP storage time phase the emitter-base voltage does not change from its forward bias value ($V_{EBp\text{-}on}$=$V_{EBp\text{-}sat}$) due to the excess minority carriers stored in the base region. A negative base current starts removing this excess carrier at a rate determined by the base driving network. PNP bipolar working condition during this phase is modeled by the following circuital scheme in which $R_{base\text{-}pnp}$ is an opportunely sized variable resistor that takes into consideration the effect of the base resistance modulation (increase) due to the removal of the excess carriers:

Figure 29. Driving network modeling for the PNP bipolar storage time phase simulation



By combining, with each other, the equations of the *System of equations 9*, describing the working conditions of the PNP bipolar during the PNP bipolar storage time phase, the following system of two first order linear differential equations valid on all the [t_{10},t_{11}] time interval in which the signal

$V_S(t) = -A \cdot sen(2\pi ft - \pi)$ has the polarity shown in the previous figure and imposed $C=C_n=C_p$:

System of equations 23

$$\begin{cases} \frac{d}{dt}\left(V_{Cn-pnpsto}(t)\right) = -\frac{1}{C \cdot R_b} \cdot V_{Cn-pnpsto} - \frac{1}{C \cdot R_b} \cdot V_{Cp-pnpsto} \\ \frac{d}{dt}\left(V_{Cp-pnpsto}(t)\right) = -\frac{1}{C \cdot R_b} \cdot V_{Cn-pnpsto} - \frac{1}{C \cdot R_b} \cdot \left(1 + \frac{R_b}{R_S + R_{Base-pnp}}\right) \cdot V_{Cp-pnpsto} + \\ + \frac{V_S}{C \cdot \left(R_S + R_{Base-pnp}\right)} - \frac{V_{EBp}}{C \cdot \left(R_S + R_{Base-pnp}\right)} \\ V_{Cn-pnpsto}(t_{10+}) = V_{Cn-pnpcon}(t_{10-}) \\ V_{Cp-pnpsto}(t_{10+}) = V_{Cp-pnpcon}(t_{10-}) \end{cases}$$

in which V_{EBp} is a constant voltage and $R_{Base\text{-}pnp}(t)$ is imposed to have the same increasing variability law as the $R_{Base\text{-}npn}(t)$ variable resistance:

Equation 28

$$R_{Base-pnp}(t) = \alpha_2 \cdot t^p \quad \text{with} \quad 0 \le t \le \Delta_{pnp}$$

in which α_2 and p (this last integer number) coefficients are determined so that $R_{Base\text{-}pnp}(t)$ has a fixed and constant mean value $R_{Base\text{-}pnp\text{-}mean}$ during the PNP storage time period of length equal to Δ_{pnp} seconds:

Equation 29

$$R_{Base-pnp-mean} = \frac{1}{\Delta_{pnp}} \cdot \int_0^{\Delta_{pnp}} R_{Base-pnp}(t)dt \Rightarrow \alpha_2 = \frac{R_{Base-pnp-mean} \cdot \Delta_{pnp} \cdot (p+1)}{\Delta_{pnp}^{(p+1)}} =$$

$$(\text{by imposing } \Delta_{pnp} = T_{Storage-pnp} = t_{11} - t_{10}) = \frac{R_{Base-pnp-mean} \cdot (p+1)}{(t_{11} - t_{10})^p}$$

Then, as already determined for the NPN storage time calculation, once the two parameters σ_{pnp} (or time constant directly connected to the lifetime of the minority carriers (holes) in the transistor base) and $T_{on\text{-}pnp}$ (obtained from the simulation of the previous PNP bipolar conduction period) are fixed and well-known , a function of two independent variables is defined for the calculation of the PNP storage time as follows:

Equation 30

$$f(T_{storage-pnp}, \varepsilon_{pnp}) = T_{storage-pnp} - \sigma_{pnp} \cdot \ln\left[1 + \frac{1}{T_{on-pnp}} \cdot \frac{T_{storage-pnp}}{\varepsilon_{pnp}}\right]$$

in which ε_{pnp} parameter, depending on the recombination phenomenon of a share of the amount of charges in base, is given by:

Equation 31

$$\varepsilon_{pnp} = \frac{A_{storage-pnp}}{A_{on-pnp}}$$

Therefore, varying the parameter ε_{pnp} from a minimum to a maximum value, imposed in base to the recombination characteristics of the minority carriers in base of the bipolar examined, the value $T_{storage\text{-}pnp}$, that determines the storage time final instant t_{11}, can be obtained finding the zeroes of the functions $f(T_{storage\text{-}pnp}, \varepsilon_{pnp})$ for each fixed ε_{pnp} value and effectuating a mean operation among the $T_{storage\text{-}pnp}$ values so obtained.

After having found, with the ODE45 simulator, in the calculated time interval $T_{storage\text{-}pnp}$, the solutions of the *System of equations 23* for the V_{Cn} and V_{Cp} voltage functions, then the NPN bipolar base current IBpnp-off is given by the following formula:

Equation 32

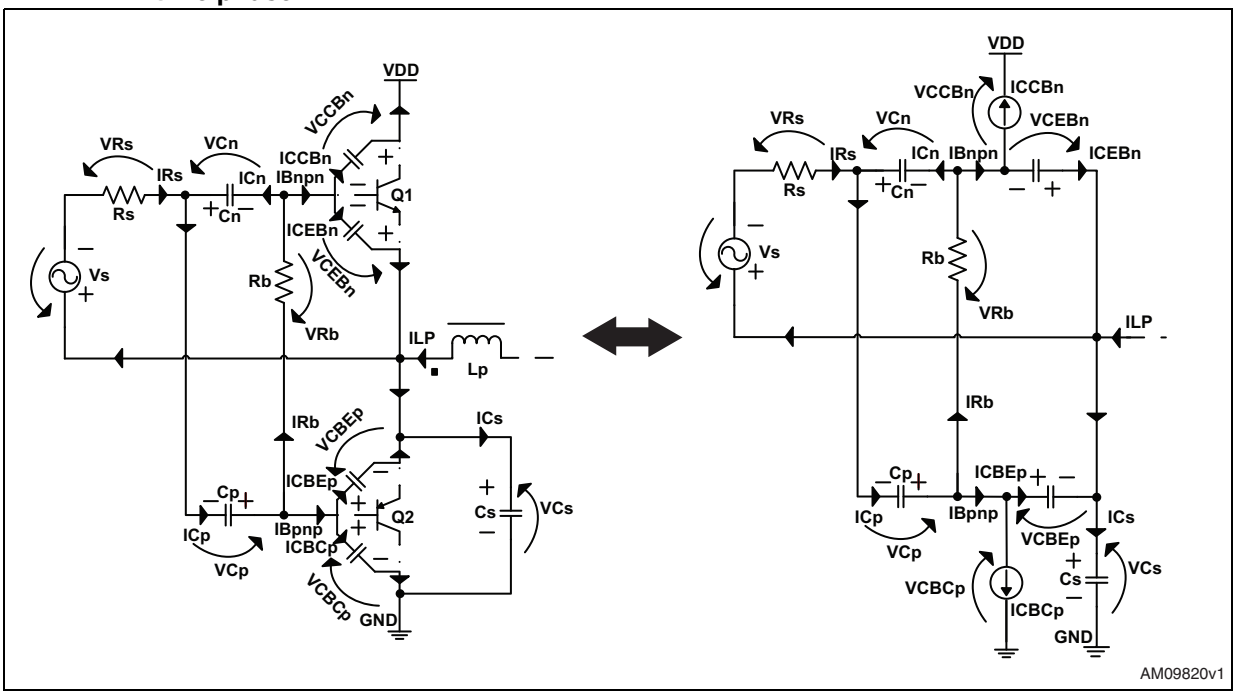
$$I_{Bpnp-off}(t) = I_{Cp-pnpsto}(t) - I_{Cn-pnpsto}(t) = -C \cdot \frac{d}{dt}\left(V_{Cp-pnpsto}(t)\right) + C \cdot \frac{d}{dt}\left(V_{Cn-pnpsto}(t)\right)$$

in which both $V_{Cn\text{-}pnpsto}(t)$ and $V_{Cp\text{-}pnpsto}(t)$ are discharging voltages respectively on the C_n and C_p capacitors (that is $\frac{d}{dt}\left(V_{Cn-pnpsto}(t)\right) < 0$ and $\frac{d}{dt}\left(V_{Cp-pnpsto}(t)\right) < 0$).

14 Modeling of the dead time after the PNP storage time phase

During the phase concerning the dead time after the PNP storage time both complementary pairs of bipolars are already inactive and their B-C and B-E junctions are reverse biased. So, in order to model this phase, the following circuital scheme in which the B-C and B-E junctions are represented by the respective junction capacitances charging or discharging according to working condition respectively of the PNP and NPN device, is considered.

Figure 30. Driving network modeling for the simulation of the dead time after the PNP storage time phase



Neglecting the currents I_{CEBn} and I_{CBEp} of the reverse biased B-E junction capacitances of the two bipolars, the following conditions are obtained:

Equation 33

$$I_{CEBn}, I_{CBEp} \cong 0 \Rightarrow I_{Bnpn} \cong I_{CCBn}\ , I_{Bpnp} \cong I_{CBCp} \text{ and } I_{CS} \cong I_{LP}$$

where:

- $I_{CCBn} = -C_{CBnpn} \cdot \frac{d}{dt}(V_{CCBn}(t))$ on the discharge phase of the (variable) NPN base-collector junction capacitance C_{CBnpn};
- $I_{CBCp} = C_{BCpnp} \cdot \frac{d}{dt}(V_{CBCp}(t))$ on the charge phase of the (variable) PNP collector-base junction capacitance C_{BCpnp}.

Then, after having imposed the previously listed assumptions, combining, with each other, the equations of the *System of equations 10*, describing the working conditions of the PNP bipolar during this phase, the following system of two first order linear differential equations has validity on all the $[t_{11},t_{12}]$ time interval in which the signal $V_S(t) = -A \cdot sen(2\pi ft - \pi)$ has

the polarity shown on the previous figure and imposed $C=C_n=C_p$:

System of equations 24

$$\begin{cases} \frac{d}{dt}\left(V_{Cn-pnpdead}(t)\right) = -\frac{1}{C \cdot R_b} \cdot V_{Cn-pnpdead} + \frac{1}{C} \cdot \left(\frac{1}{R_S} - \frac{1}{R_b}\right) \cdot V_{Cp-pnpdead} - \frac{1}{C} \cdot I_{CBCp} - \frac{V_S}{C \cdot R_S} - \frac{V_{CBEp}}{C \cdot R_S} \\ \frac{d}{dt}\left(V_{Cp-pnpdead}(t)\right) = -\frac{1}{C \cdot R_b} \cdot V_{Cn-pnpdead} - \frac{1}{C} \cdot \left(\frac{1}{R_S} + \frac{1}{R_b}\right) \cdot V_{Cp-pnpdead} + \frac{1}{C} \cdot I_{CCBn} + \frac{V_S}{C \cdot R_S} + \frac{V_{CBEp}}{C \cdot R_S} \\ V_{Cn-pnpdead}(t_{11+}) = V_{Cn-pnpsto}(t_{11-}) \\ V_{Cp-pnpdead}(t_{11+}) = V_{Cp-pnpsto}(t_{11-}) \end{cases}$$

in which $V_{BEn}= -V_{CEBn}<0$ and $V_{EBp}= -V_{CBEp}<0$ is an opportunely modeled signal complying with the following function:

Equation 34

$$V_{CBEp} = \left(\frac{I_{CBCp}}{C_{BCpnp}} - \frac{I_{CS}}{C_S}\right) \cdot t + \psi_2$$

in which Ψ_2 is a constant depending on the initial value of the V_{CBEp} voltage at $t=t_{11-}$.

The length of this dead time interval fixed for the simulation, in which the V_{Cn} and V_{Cp} voltage functions are determined through the ODE45 simulator, is imposed to be given by the following formula in which $T_{pnpsto}=t_{11}-t_{10}$, $T_{pnpcon}=t_{10}-t_8$ and $Tpnpric=t_8-t_6$:

Equation 35

$$T_{pnpdead} = t_{12} - t_{11} = \frac{1}{f} - T_{pnpsto} - T_{pnpcon} - T_{pnpric} - T_{npndead} - T_{npnsto} - T_{npncon} - T_{npnric}$$

This last working operation phase described completes the resonant driving network modeling with reference to the variation over the whole period of the voltage signal V(s) across the filter capacitor and covering the time intervals, relating to the re-circulating, conduction and dead time phases for both NPN and PNP bipolar devices in their functional stages.

The accuracy of the modeling technique proposed is verified by comparing the simulation results obtained using the Matlab tool with experimental results of the driving network circuital implementation response in steady-state working condition for the bipolar devices.

15 Experimental results

Two commercially available power bipolar junction transistors, that find application in electronic lamp ballasts, were chosen for the experimental acquisition on the board tested. In particular, a complementary pair of ST power bipolar transistors, the NPN device STX83003 and PNP device STX93003 (in TO-92 package), respectively, were employed on the common emitter half bridge section to supply a 15 W CFL board in order to verify their compatibility on the resonant driving circuit solution. Values of the components used on the half bridge voltage fed topology optimized board setting and the main datasheet electrical specifications of the above mentioned devices are the following.

15.1 Applicative parameters

- Setting of the driving network components (see *Figure 1*):
  - $D_1, D_2, D_3, D_4 = 1N4007 ; D_5, D_6 = BA159$
  - $C_1 = 4.7\mu F / 400V ; C_2 = 47nF / 100V ; C_3 = C_4 = 100nF ; C_5 = 1.2nF$
  - $C_6 = 4.7nF / 630V ; C_7 = C_8 = 100nF / 250V$
  - $R_{fuse} = 8.2\Omega ; R_2 = 8.2\Omega ; R_3 = 330k\Omega ; R_4 = 330\Omega ; R_5 = 470k\Omega$
  - $L_1 = 100\mu H$
  - $T1A = 2.3mH ; N_{T1B} = 3$ turns.
- Power bipolar transistors specifications:
  - Q1 $\rightarrow$ High voltage fast-switching NPN power bipolar transistor STX83003 in TO-92 package with Ic=1 A, BV_{ceo}=400 V and BV_{ces}=700 V; V_{CESAT}=1 V@I_C=350 mA, I_B=50 mA and h_{FE} = 25 (TYP) @ I_C= 350 mA and V_{CE}=5 V.
  - Q2 $\rightarrow$ High voltage fast-switching PNP power bipolar transistor STX93003 in TO-92 package with I_C=-1 A, BV_{ceo}=-400 V and BV_{ces}= -500 V; V_{CESAT}=-500 mV @ I_C= -350 mA, I_B =-50 mA and h_{FE} = 25 (TYP) @ I_C= -350 mA and V_{CE}=-5 V.

An evaluation of switching performances of the devices during the normal working operation was made in “open board” (at 25 °C ambient temperature) conditions with 230 V input voltage values and 50 Hz frequency. In particular, the following images depict the functionality of the high side NPN bipolar transistor in steady-state operation.

Figure 31. STX83003 (NPN) bipolar transistor during steady-state operation with 230 V input voltage: base current (I_{B1}), collector current (I_{C1}), base-emitter voltage (V_{BE1}) and collector-emitter voltage (V_{CE1}) signals acquired

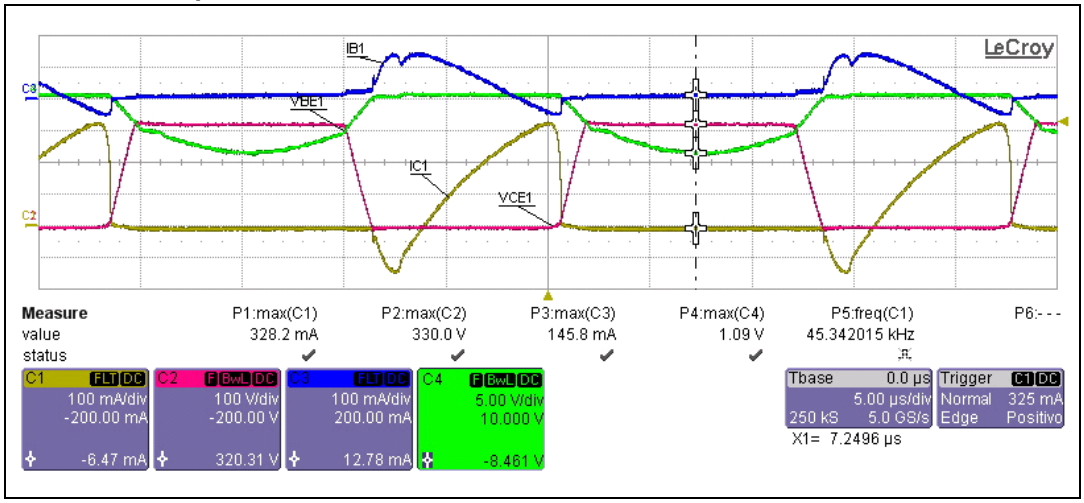


Figure 32. STX83003 (NPN) bipolar transistor during steady-state operation with 230 V input voltage: base current (I_{B1}), collector current (I_{C1}), voltage on base series capacitor C_n (V_{CN}) and voltage on base series capacitor C_p (V_{CP}) signals acquired

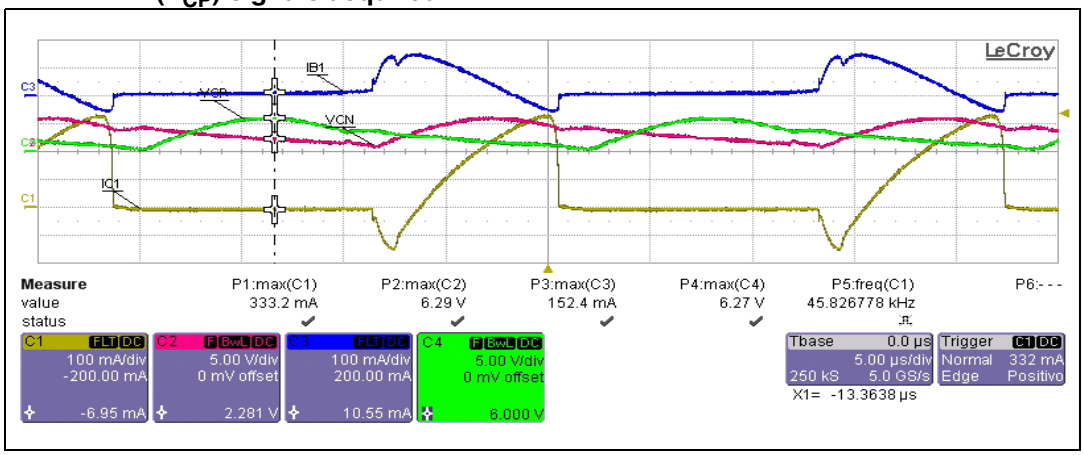


Figure 33. STX83003 (NPN) bipolar transistor during steady-state operation with 230 V input voltage: base current (I_{B1}), collector current (I_{C1}), voltage on filter capacitor C2 (V_C) and voltage on driving resistance R2 (V_{RS}) signals acquired

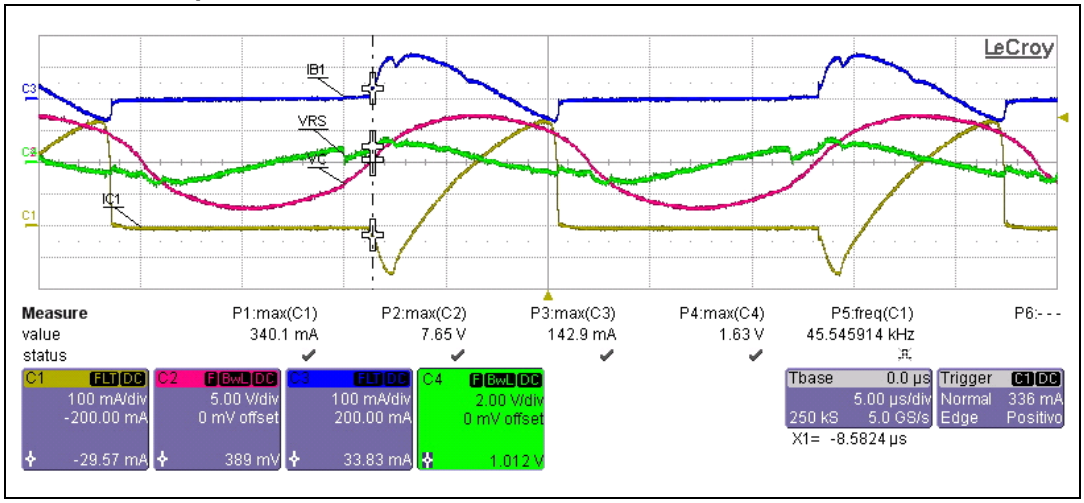
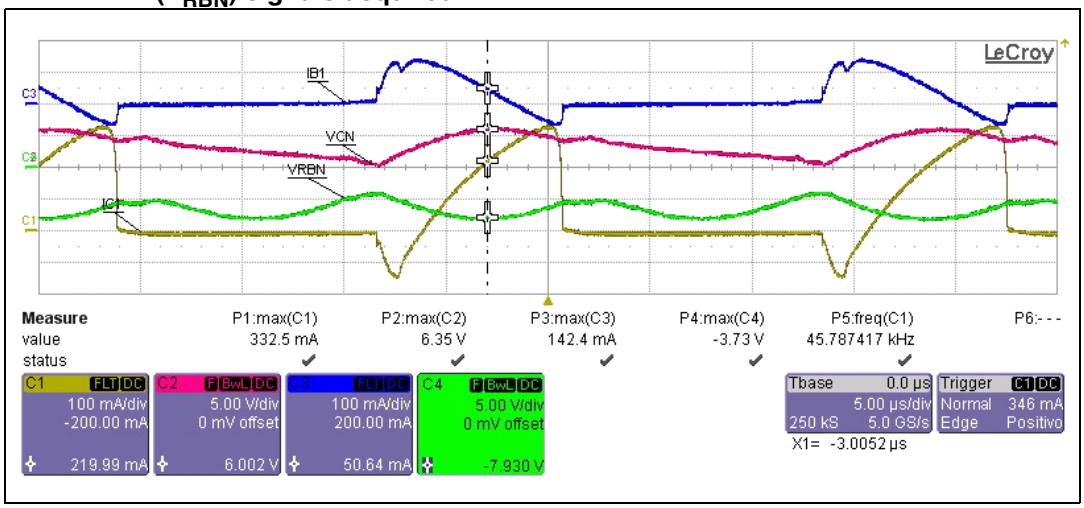


Figure 34. STX83003 (NPN) bipolar transistor during steady-state operation with 230 V input voltage: base current (I_{B1}), collector current (I_{C1}), voltage on base series capacitor C3 (V_{CN}) and voltage on breakdown resistance R4 (V_{RBN}) signals acquired



As previously seen, experimental waveforms acquired on the 15 W CFL optimized setting board show a close similarity with the theoretical waveforms discussed during the description of the self-oscillating operation principle (see *Figure 2*, *3*, *4*, *5* and *6*). Images related to the steady-state situation (*Figure 31*-*32*-*33* and *34*) show basically a regular behavior of half bridge section NPN bipolar transistor during the open board normal working operation at 230 Vac without highlighting any critical electrical condition that could cause bipolar case overheating phenomena.

In the following images, switching particulars during turn-on and turn-off transients respectively for both NPN and PNP bipolar transistors are reported in open board steady-state working operation with V_{main} equal to 230 V.

Figure 35. STX83003 (NPN) bipolar transistor during turn-on particular in steady-state operation with 230 V input voltage: base current (I_{B1}), collector current (I_{C1}) and collector-emitter voltage (V_{CE1}) signals acquired

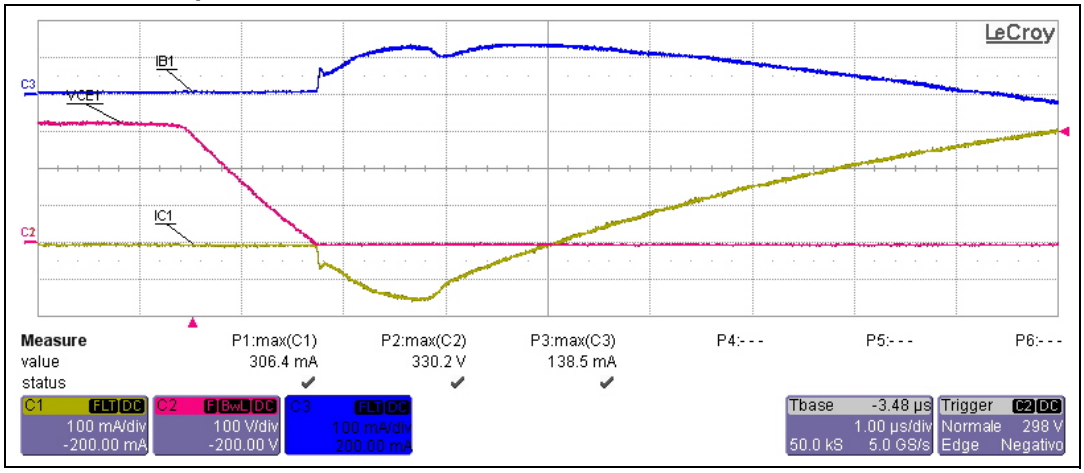


Figure 36. STX83003 (NPN) bipolar transistor during turn-off particular in steady-state operation with 230 V input voltage: base current (I_{B1}), collector current (I_{C1}) and collector-emitter voltage (V_{CE1}) signals acquired

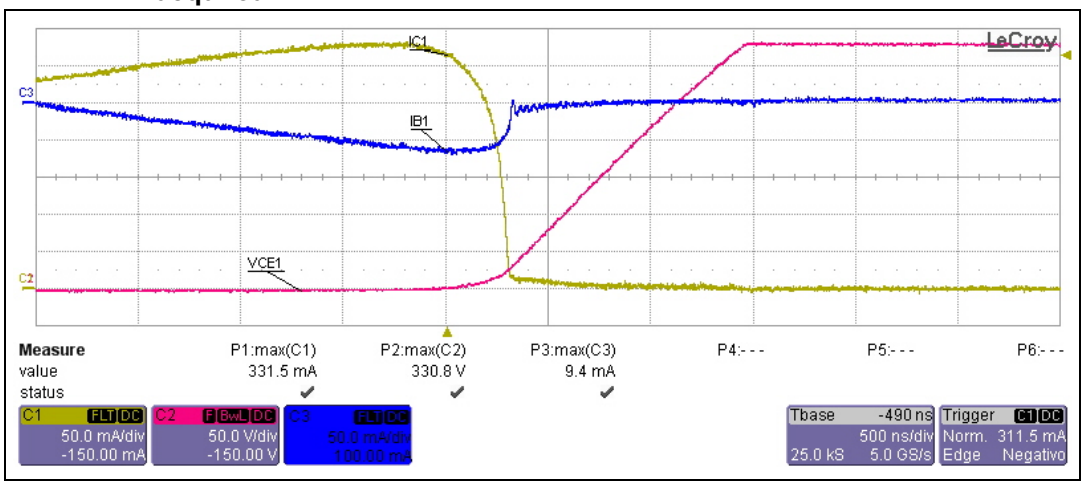


Figure 37. STX93003 (PNP) bipolar transistor during turn-on particular in steady-state operation with 230 V input voltage: base current (I_{B2}), collector current (I_{C2}) and emitter-collector voltage (V_{CE2}) signals acquired

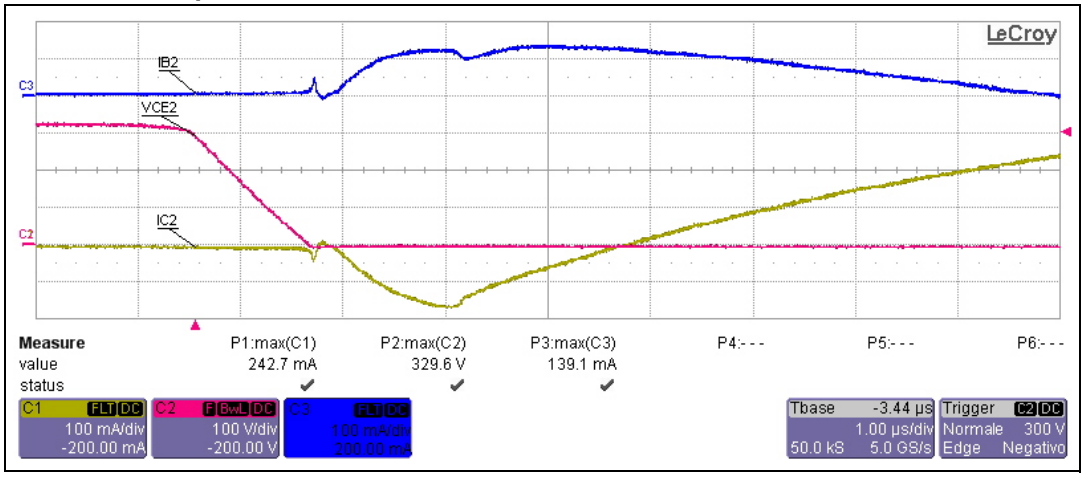
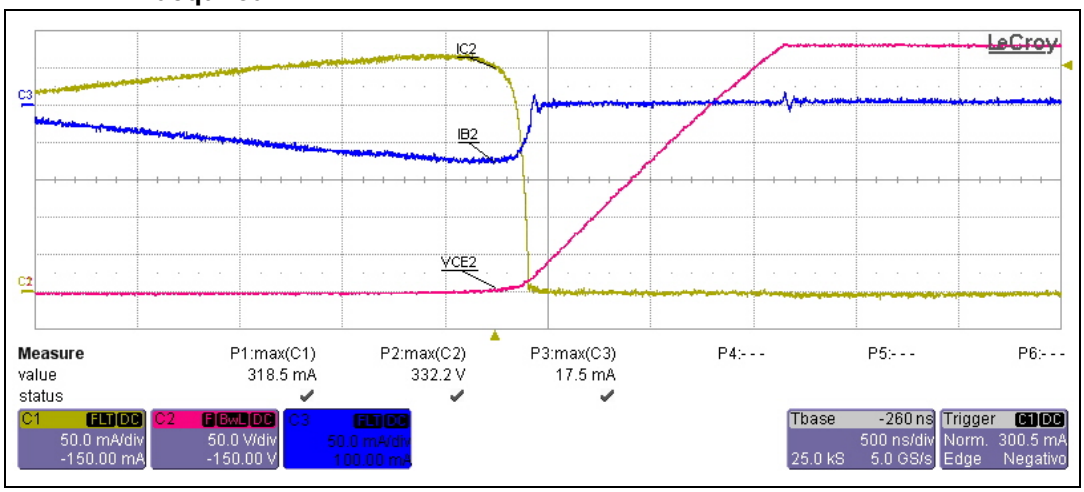


Figure 38. STX93003 (PNP) bipolar transistor during turn-off particular in steady-state operation with 230 V input voltage: base current (I_{B2}), collector current (I_{C2}) and emitter-collector voltage (V_{CE2}) signals acquired



As can be seen when observing the previous waveforms, ST transistors fit this application very well in terms of switching characteristics and power dissipation. In fact, no thermal problems due to a bad driving or behavior of the devices were found for the two bipolars under test in normal working conditions. Switching during the turn-off times is good as the cross-over points Ic-Vce are acceptably low (within around 25 mA-25 V values at 230 Vac) and, consequently, the amounts of energy dissipated by the bipolars (proportional to the areas subtended to the Ic-Vce signals) are quite limited. Also measurements performed in “closed board” conditions point to a satisfactory functionality for the two complementary ST bipolars with case temperatures reaching values of around 64 °C-68 °C and working frequencies of around 46 kHz while the absorbed input power (Pin) is fixed at around 15 W at 230 Vac main voltage.

16 Simulation results with the Matlab tool

In order to evaluate the reliability of the modeling method described and relating to a complementary pair solution of bipolar transistors driven by a resonant network, results of the simulative analysis, implemented with the Matlab tool, have been compared with the applicative results obtained while testing the 15 W CFL optimized board. Therefore, the following listed conditions and assumptions have been imposed so as to perform the comparison.

16.1 Simulative parameters

- Forcing signal generator:

$$V_S(t) = A \cdot \text{sen}(2\pi ft) \text{ with } A = 7.65V \text{ and } freq = f = 45kHz \text{ for } 0 < t < \frac{1}{f}.$$

- $Cap = C = C_n = C_p = 100nF$; $C_S = 1.2nF$; $R_S = 8.2\Omega$; $R_b = 330\Omega$

Re-circulating phase preliminary to the NPN bipolar conduction time phase (t_0<t<t_2)

- $V_{Cn-npnric}(t_0) = \gamma_0 = 1V$, $V_{Cp-npnric}(t_0) = \vartheta_0 = 3.9V$ (initial values fixed)

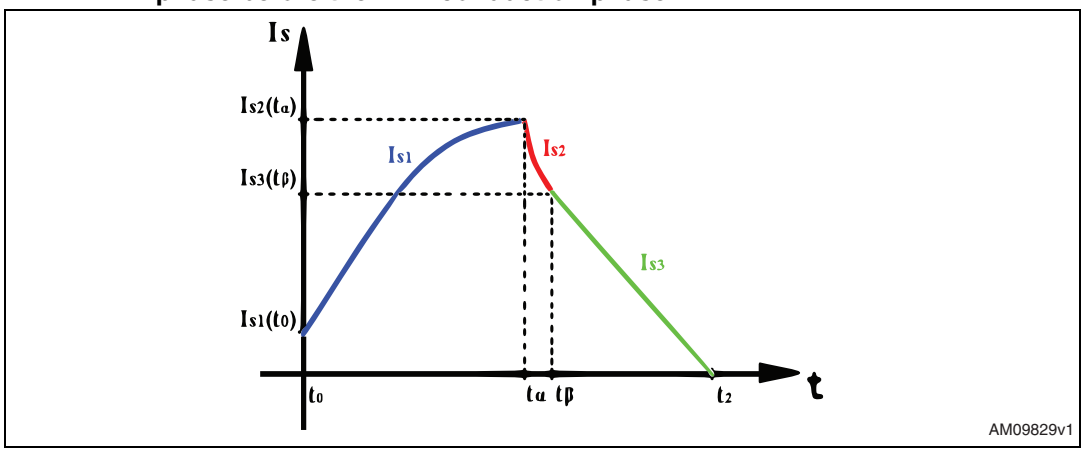
- $V_{BEn} = \frac{V_{BEn-on}}{2} = 0.5V$

- Signal I_S modeled in the re-circulating interval $t_0<t<t_2$ with $T_{recn}=t_2-t_0=2.35$ µsec as:

System of equations 25

$$I_S(t) = \begin{cases} I_{S1}(t) = 1 - \exp\left(-\frac{t}{\alpha_1}\right) + \beta_1 \text{ for } t_0 \le t \le t_\alpha \text{ with } \alpha_1, \beta_1 > 0 \text{ and } t_\alpha = 55\%(t_2 - t_0) \\ I_{S2}(t) = -1 + \exp\left(-\frac{t}{\alpha_2}\right) + \beta_2 \text{ for } t_\alpha < t \le t_\beta \text{ with } \alpha_2, \beta_2 > 0 \text{ and } t_\beta = 60\%(t_2 - t_0) \\ I_{S3}(t) = -\gamma_1 \cdot t + \beta_3 \text{ for } t_\beta < t \le t_2 \text{ with } \gamma_1, \beta_3 > 0 \end{cases}$$

Figure 39. Current source signal Is modeling for the simulation on the re-circulating phase before the NPN conduction phase



NPN conduction time phase ($t_2<t<t_4$)

- $V_{BEn} = 1V$

NPN storage time phase ($t_4<t<t_5$)

- $V_{BEn} = 1V$
- Applicative analysis provides the following results:
  - $T_{steadystate-period-applicative} = \frac{1}{f} = \frac{1}{45000} \Rightarrow T_{storage-applicative} = 11\% \cdot T_{steadystate-period-applicative} =$

$$= 0.11 \cdot \frac{1}{45000} \approx 2.44 \cdot 10^{-6} s = 2.44 \mu s$$

  - $I_{Bnpn-on-max} = 150 \cdot 10^{-3} A$ and $\left|I_{Bnpn-off-max}\right| = 55 \cdot 10^{-3} A$

so σ_{npn} is experimentally calculated by the *Equation 13* as:

Equation 36

$$\sigma_{npn} = \frac{2.44 \cdot 10^{-6}}{\ln\left[1 + \frac{150 \cdot 10^{-3}}{55 \cdot 10^{-3}}\right]} \approx 1.8 \cdot 10^{-6} \sec$$

- $R_{Base-npn}(t) = \alpha_1 \cdot t^n$ with $\alpha_1 = \frac{R_{Base-npn-mean} \cdot (n+1)}{(T_{storage-applicative})^n}$ and $R_{Base-npn-mean} = 2\Omega, n = 3$
- $\varepsilon(i)_{npn}$ for $i = 1 \div m$ with $\varepsilon_{min-npn} \le \varepsilon(i)_{npn} \le \varepsilon_{max-npn}$ with:
  - $m = 100$
  - $\varepsilon_{min-npn} = 0.15$ and $\varepsilon_{max-npn} = 0.25$

Dead time after the NPN storage time phase ($t_5<t<t_6$)

- Applicative analysis result provides $I_{Cnpn\text{-}max}$=330 mA
- $V_{CEBn} = \left(\frac{I_{CCBn}}{C_{CBnpn}} - \frac{I_{CS}}{C_S} \right) \cdot t + \psi_1$ with:
  - $I_{CBCp}=I_{CCBn}$=10 mA
  - $I_{CS} = I_{Cnpn-max} \cdot 0.8 = 330mA \cdot 0.8 = 264mA$
  - $C_{CBnpn} = 45pF$ (meant as average capacity value)
  - Ψ_1=0.5

Re-circulating phase preliminary to the PNP bipolar conduction time phase ($t_6<t<t_8$)

- $V_{EBp} = \frac{V_{EBp-on}}{2} = 0.4V$
- Signal I_S modeled in the re-circulating interval $t_6<t<t_8$ as already done for the re-circulating interval $t_0<t<t_2$ with $T_{recp}=t_8-t_6$=2.35 µsec.

PNP conduction time phase ($t_8<t<t_{10}$)

- V_{EBp}=0.8 V

PNP storage time phase ($t_{10}<t<t_{11}$)

- V_{EBp}=0.8 V
- $\sigma_{npn}=\sigma_{pnp}$
- $R_{Base\text{-}npn}(t)=R_{Base\text{-}pnp}(t)$
- $\varepsilon(i)_{pnp}$ for $i = 1 \div m$ with $\varepsilon_{min-pnp} \le \varepsilon(i)_{pnp} \le \varepsilon_{max-pnp}$ with:
  - m=100
  - $\varepsilon_{min\text{-}pnp}$=0.15 and $\varepsilon_{max\text{-}pnp}$=0.25

Dead time after the PNP storage time phase ($t_{11}<t<t_{12}$)

- Applicative analysis result provides $I_{Cpnp\text{-}max}$=330 mA
- $V_{CBEp} = \left(\frac{I_{CBCp}}{C_{BCpnp}} - \frac{I_{CS}}{C_S} \right) \cdot t + \psi_2$ with
  - $I_{CBCp}=I_{CCBn}$=10 mA
  - $I_{CS} = I_{Cpnp-max} \cdot 0.8 = 330mA \cdot 0.8 = 264mA$
  - $C_{BCpnp} = 45pF$ (meant as average capacity value)
  - Ψ_2=0.5

In the following images, the code developed with Matlab software and implementing the calculation for the resolution of the systems of differential equations that rule each working phase for the devices of the complementary pair in one period, is detailed having imposed the conditions reported below:

Equation 37

$$a = -\frac{1}{C \cdot R_b}; b = -\frac{1}{C} \cdot \left(\frac{1}{R_S} + \frac{1}{R_b} \right); c = a \cdot \left(1 + \frac{R_b}{R_S + R_{Base-npn}(t)} \right);$$

$$g = \frac{1}{C} \cdot \left(\frac{1}{R_S} - \frac{1}{R_b} \right); k = \frac{1}{C}; h = \frac{1}{C \cdot R_S}; z = \frac{1}{C \cdot \left(R_S + R_{Base-npn}(t) \right)}.$$

Figure 40. Re-circulating phase preliminary to the NPN conduction time phase

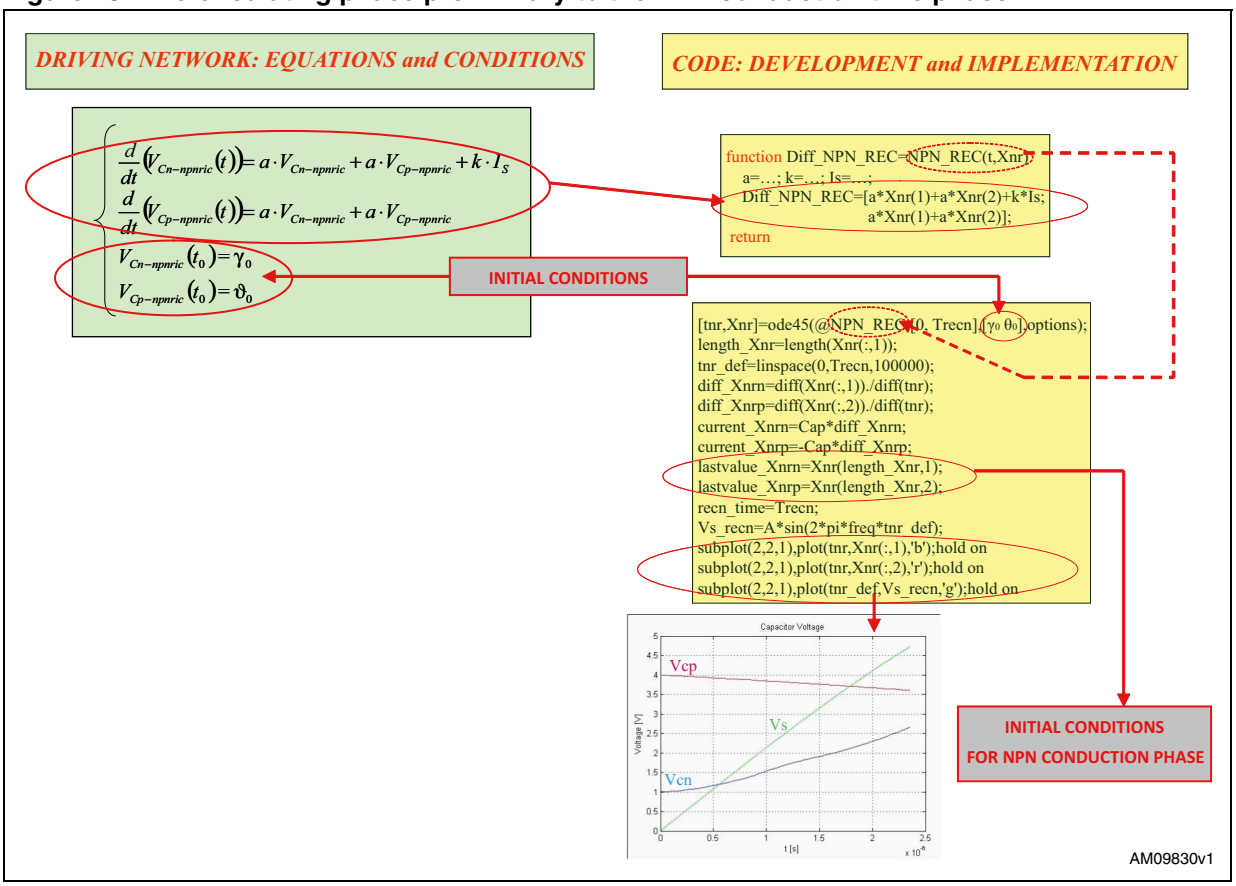


Figure 41. NPN conduction time phase

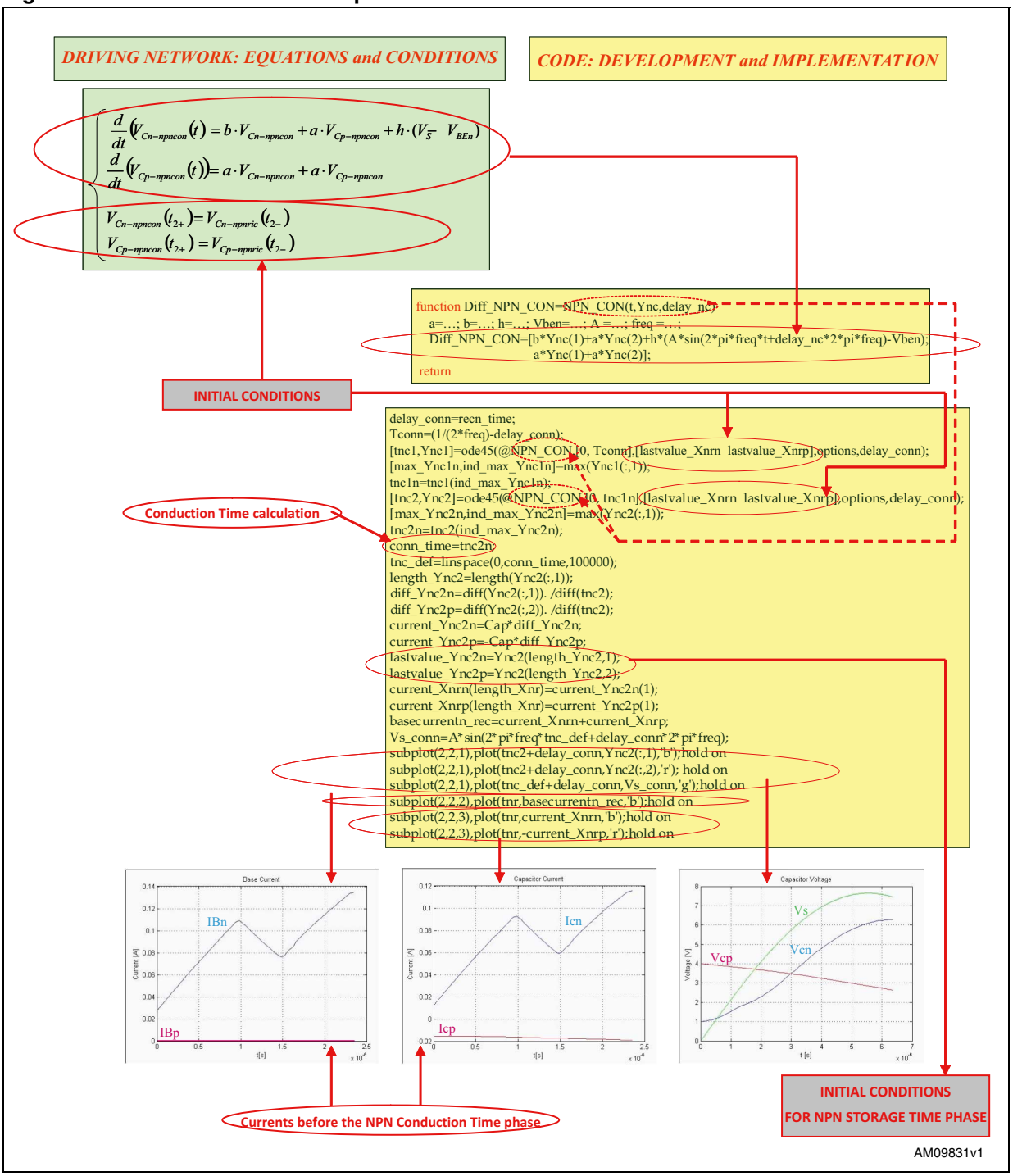


Figure 42. NPN storage time phase

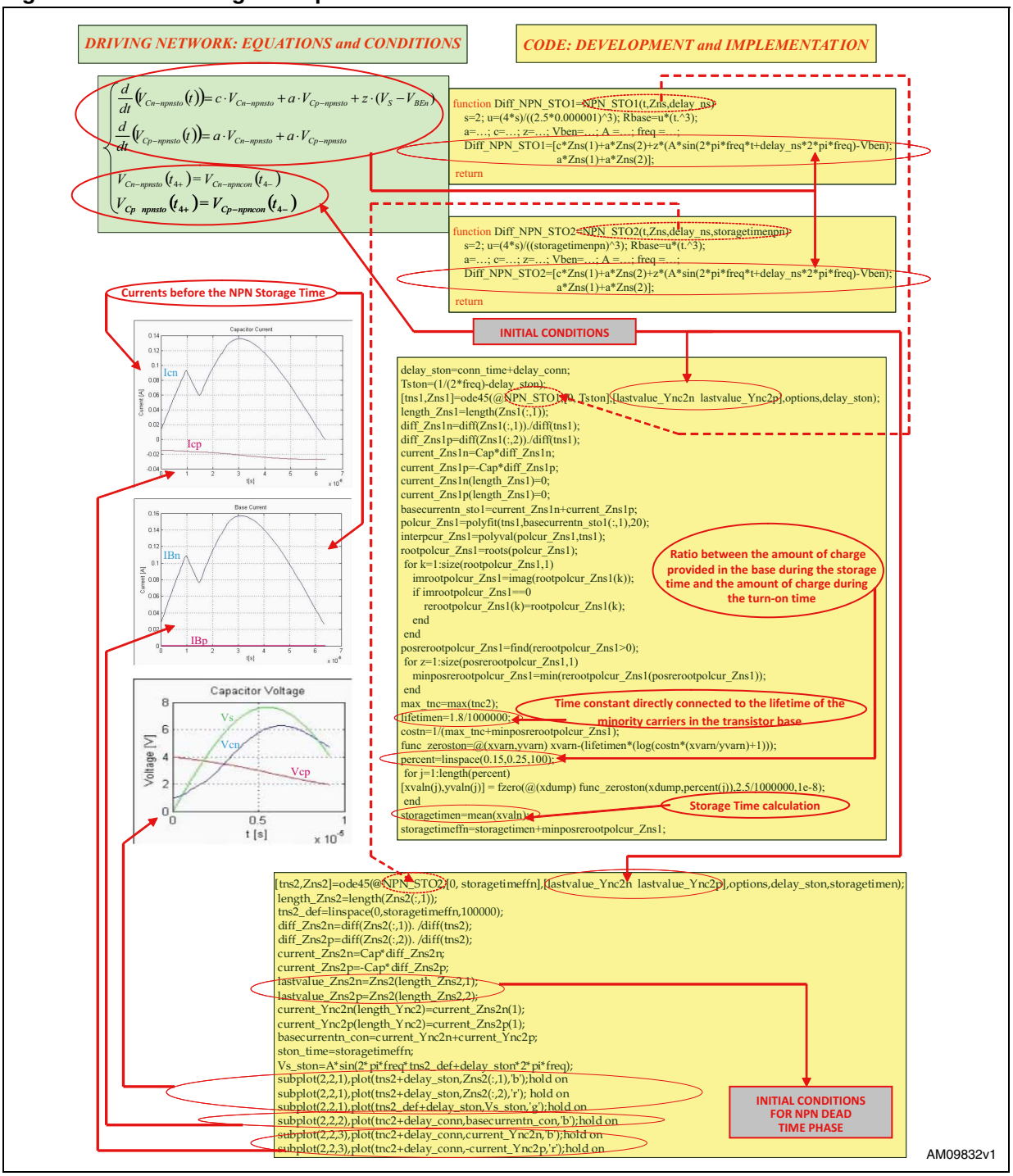


Figure 43. Dead time phase after the NPN storage time phase

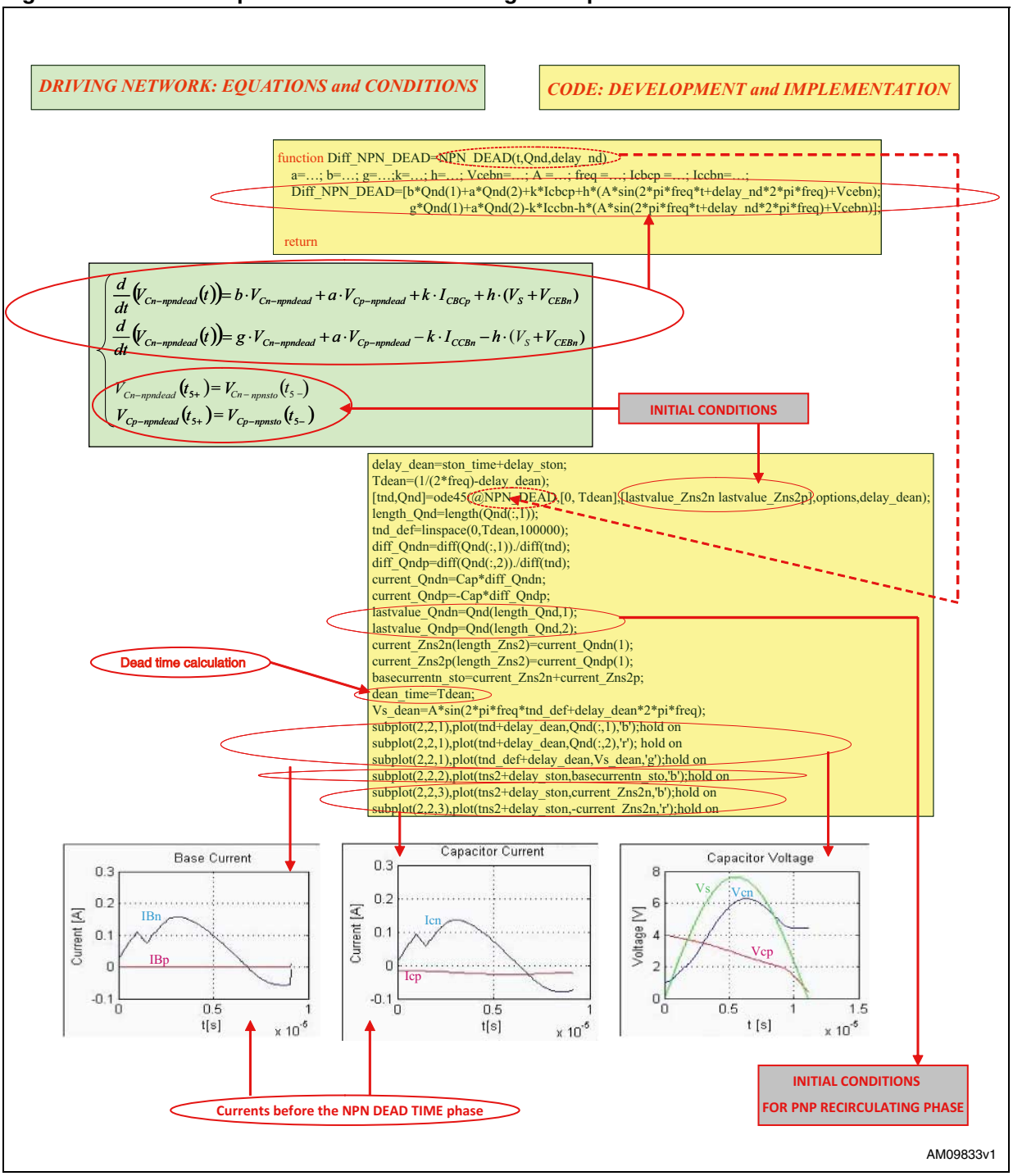


Figure 44. Re-circulating phase preliminary to the PNP conduction time phase

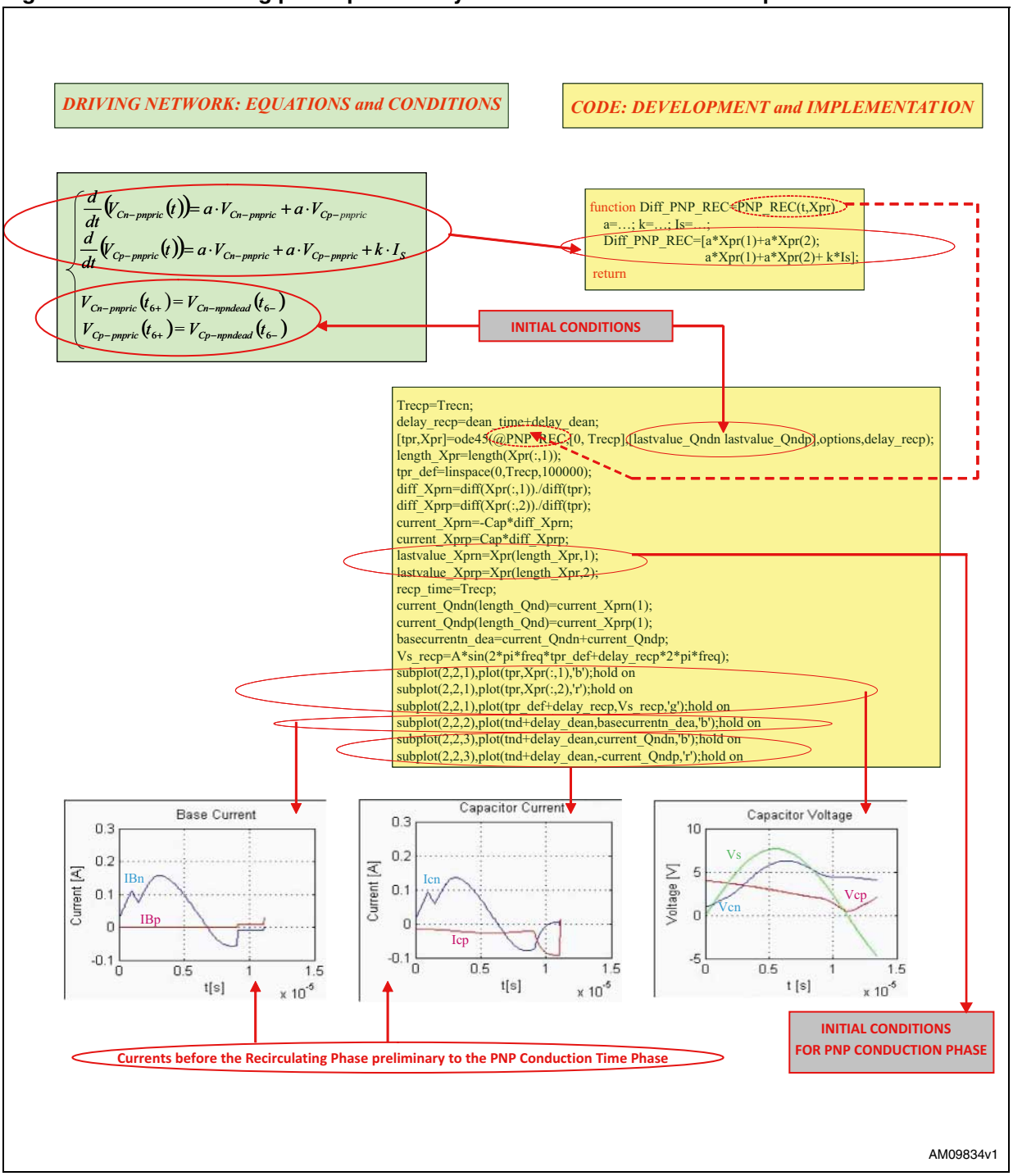


Figure 45. PNP conduction time phase

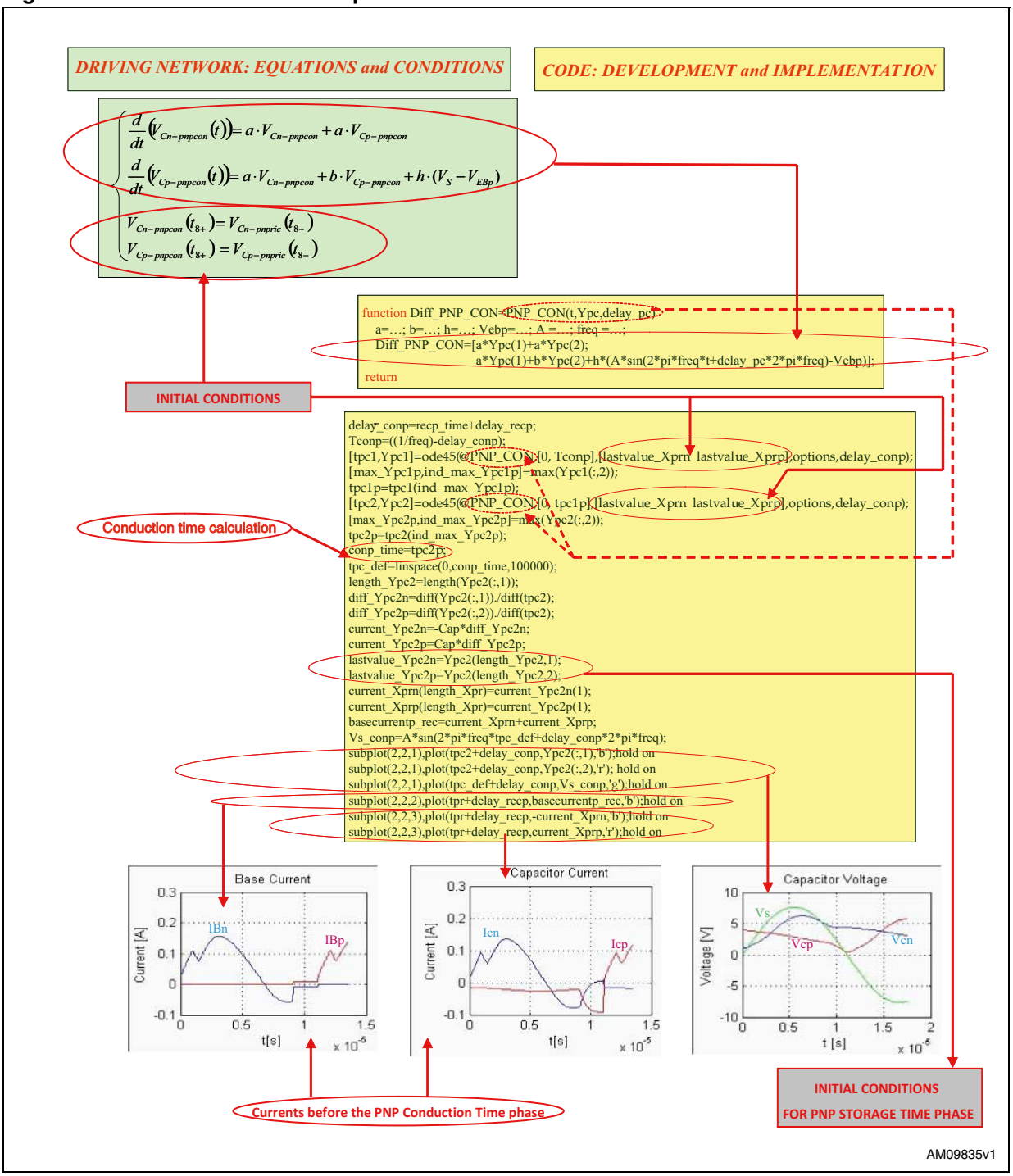


Figure 46. PNP storage time phase

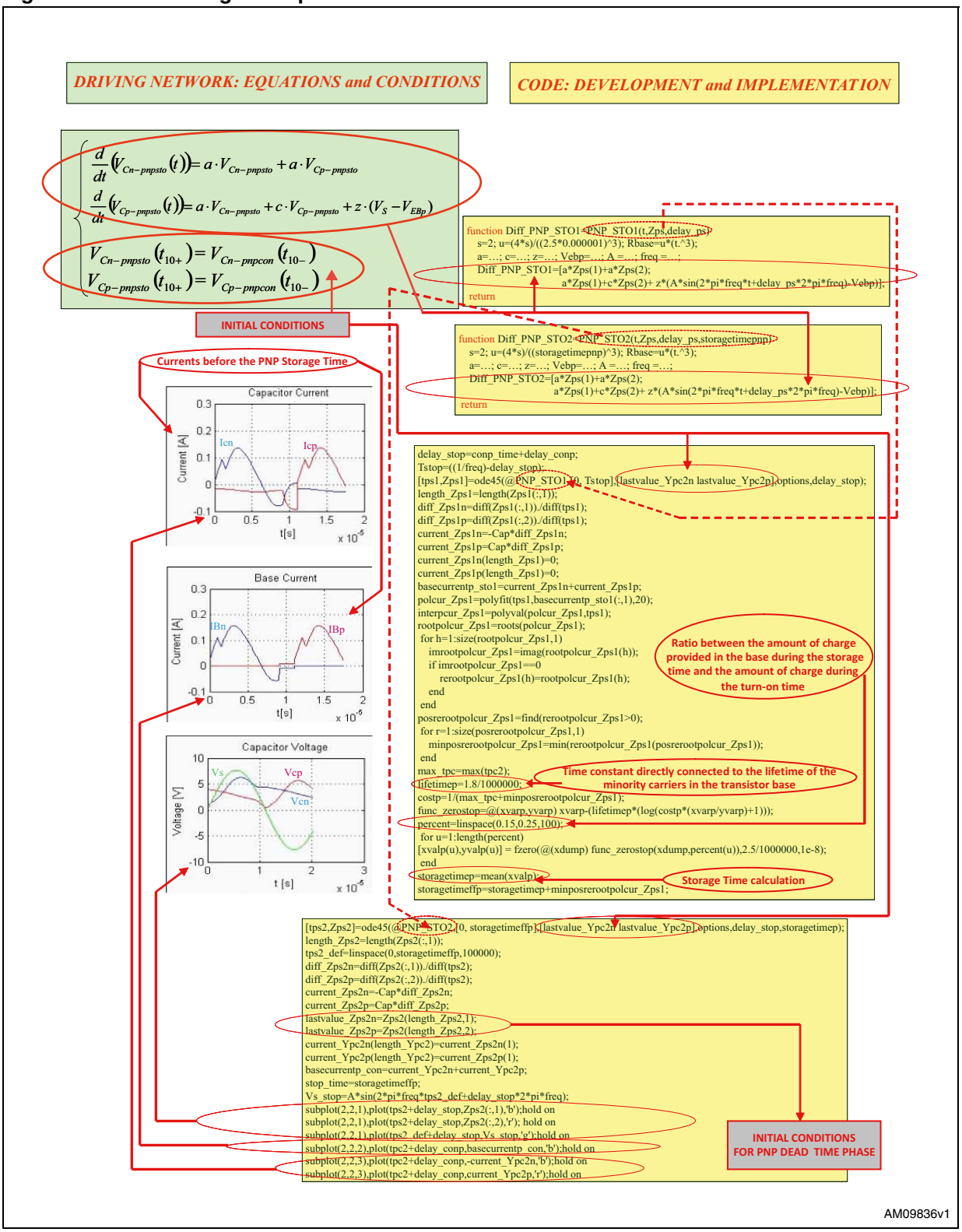
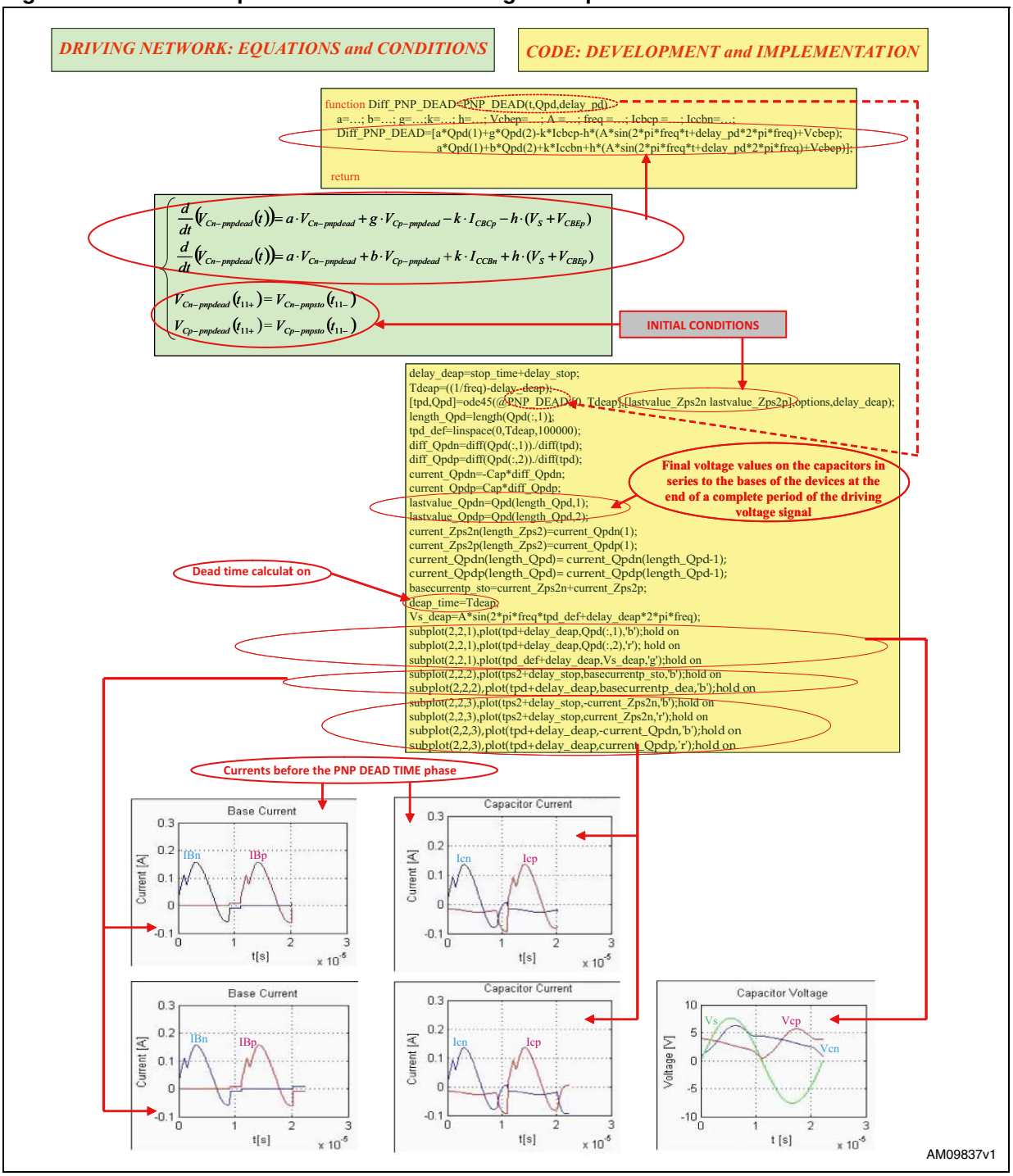


Figure 47. Dead time phase after the PNP storage time phase



The following images represent the results of the driving network simulation in Matlab environment. In particular, signals simulated refer respectively to the filter capacitor voltage signal (V_s), NPN base series capacitor voltage (V_{Cn}) and PNP base series capacitor voltage (V_{Cp}) depicted in *Figure 48*, NPN base current (I_{Bn}) and PNP base current (I_{Bp}) depicted in *Figure 49* and NPN base series capacitor current (I_{Cn}) and PNP base series capacitor current (I_{Cp}) depicted in *Figure 50*.

For a better overall visualization, the following complete graphs are been obtained simulating sequentially for two times the total cycle of the driving voltage signal so to plot only the last cycle in advance of a time period t_{antic} equal to:

Equation 38

$$t_{antic} = \frac{1}{freq} - T_{pnpdead}$$

in which $T_{pnpdead}$ is the duration of the dead time phase after the PNP storage time phase.

Moreover, the conduction time phase simulation for both devices is repeated iteratively for two consecutive times in order to restrict the integration interval and refine the maximum voltage value research in it.

Figure 48. Driving network simulation results: filter capacitor voltage signal (V_s), NPN base series capacitor voltage (V_{Cn}) and PNP base series capacitor voltage (V_{Cp}) signals simulated

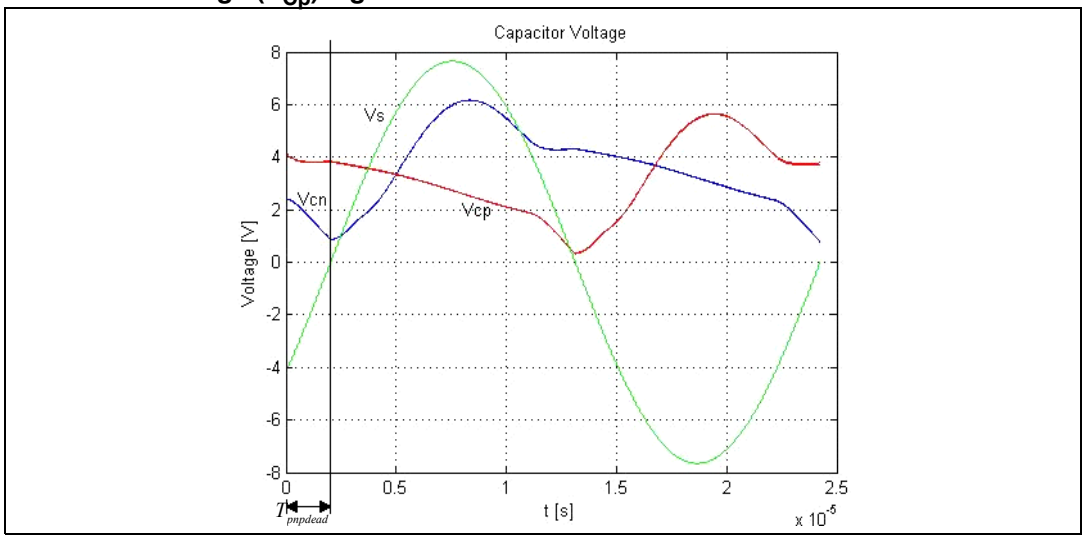


Figure 49. Driving network simulation results: NPN base current (I_{bn}) and PNP base current (I_{bp}) signals simulated

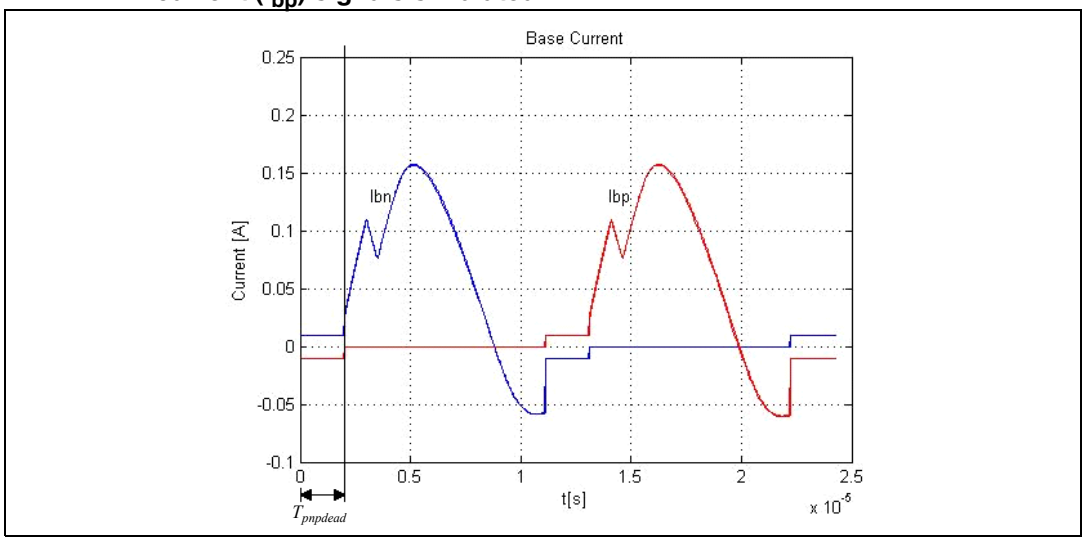
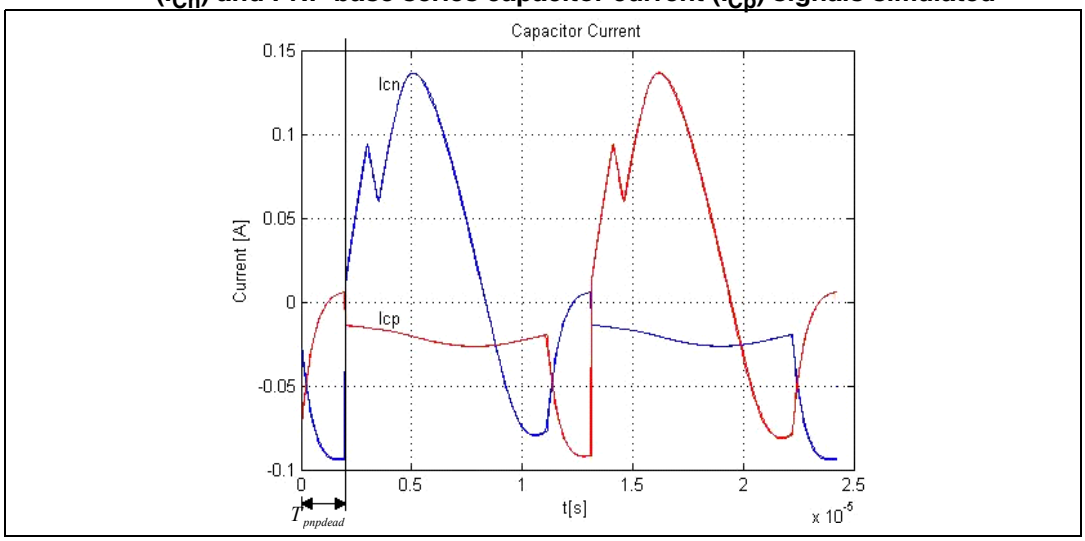


Figure 50. Driving network simulation results: NPN base series capacitor current (I_{Cn}) and PNP base series capacitor current (I_{Cp}) signals simulated



As can be seen from the comparison of the experimental acquisitions of the current/voltage signals on the 15 W CFL tested board with the results obtained using the Matlab tool, the modeling method developed for the complementary pair solution driving network simulation, with the conditions and assumptions imposed during each working operation stage of the bipolars, can be considered quite reliably because a good match is observed between the measured and the modeled results. In particular, the results of modeling observed to be in good correspondence with measured data are the following:

Equation 39

$$I_{Bon} \cong 150mA;\ I_{Boff} \cong -60mA;\ T_{Storage} \cong 2.3\mu sec$$

Previously reported simulation results can be viewed during the simulation and then exported to the Matlab workspace for subsequent offline analysis.

17 Conclusions

A comprehensive description of a self-oscillating resonant driving system for compact fluorescent lamps (CFL), using a complementary pair of bipolar transistors on the half bridge converter section was made using a stage-wise circuit analysis in steady-state working condition for the devices. An analytical model has been developed to describe both of the resonant driving network functional characteristics and the physics of the bipolar devices during each working operation phase in steady-state condition. Then, a simulation procedure of the corresponding behavior model in Matlab environment has been carried out in order to verify the correctness of the modeling technique proposed. Finally, the accuracy of this approach/method is verified by comparing the simulation results with experimental ones obtained by the driving network circuital implementation response. Two commercially available complementary ST power bipolar junction transistors in TO-92 package (respectively NPN device STX83003 and PNP device STX93003), which find application in electronic lamp ballast applications, were chosen for the experimental analysis on a 15 W CFL board prototype. From the comparison of the simulation results with the signals acquired on the 15 W CFL board tested, the measured data are observed to agree closely with those provided by Matlab software tool, therefore validating the modeling method developed for the resonant driving network. In particular, results of simulation observed to be in good correspondence with measured experimental data are the values of the parameters $I_{Bon} \cong 150mA$, $I_{Boff} \cong -60mA$ and $T_{Storage} \cong 2.3\mu$ sec , and for both devices.

18 References

1. “Resonant Driving Circuit with a Complementary Pair Of Power Bipolar Transistor For CFLs”, STMicroelectronics Catania.
2. “Resonant Driving System for a Fluorescent Lamp”, Patent No.:US6, 628,090 B1, Date of Patent: Sep.30, 2003
3. “The Determination of the Bipolar Transistor Commutation Time Components by Using a Virtual Circuit” Hyperion University of Bucharest, Faculty of Mathematics-Informatics, ROMANIA

19 Revision history

Table 1. Document revision history

Date	Revision	Changes
28-Nov-2011	1	Initial release.