AN3302
Application note

Monolithic power management for high definition ODD with true shutdown, reset, and programmable step-up voltage

Introduction

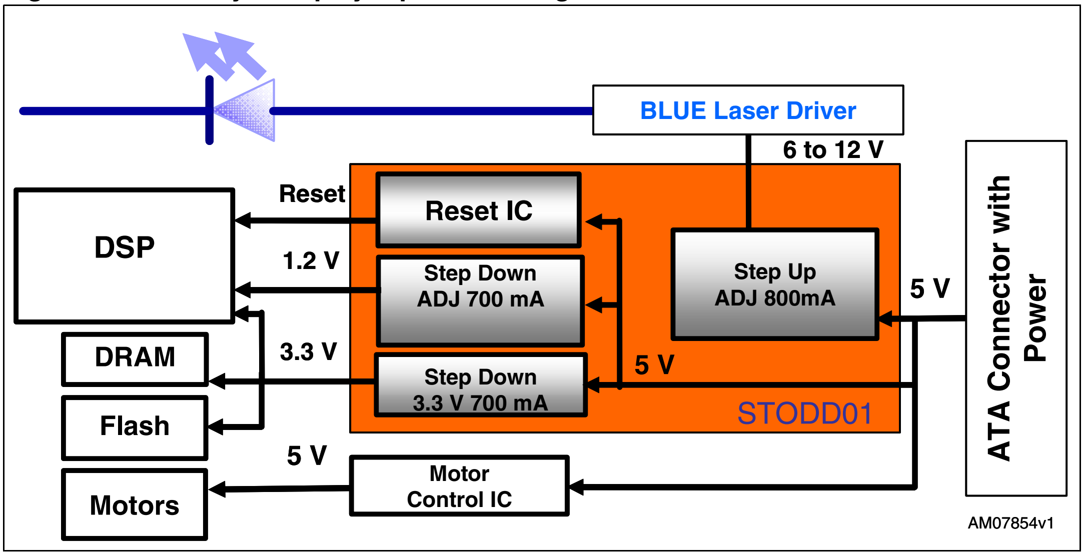
Blu-ray disc players have grown rapidly in popularity due to the increasing availability of digital services and high definition digital media content.

This application note describes how to use STODDO1, a complete power management for Blu-ray disc players, based on high density optical storage devices. It integrates two step-down converters and one step-up.

The step-down converters are optimized for powering low-voltage digital core, up to 0.8 A, in ODD applications and, generally, to replace a high current linear solution when the power dissipation may cause an overheating of the application environment.

The step-up provides the needed voltage for supplying the blue laser in mobile applications where only 5 V is available. The output voltage is programmable, by using S-wire protocol, in the range of 6.5 V to 14 V, with a current capability of 0.7 A.

Figure 1. Blu-ray disc player power management architecture based on STODD01



The integrated low R_{DSon}, for N-channel and P-channel MOSFET switches, contributes to obtaining high efficiency.

The enable function for the step-up section, and reset function for monitoring the input voltage, make the device particularly suitable for optical storage applications.

The high switching frequency (1.2 MHz typ.) allows the use of tiny surface-mounted components. Furthermore, a low output ripple is guaranteed by the current mode PWM topology and by the use of X7R or X5R and low ESR SMD ceramic capacitors.

The device includes soft-start control, thermal shutdown, and peak current limit, to prevent damage due to accidental overload.

Contents

1 Block diagram

Figure 2. Block diagram and reference circuit

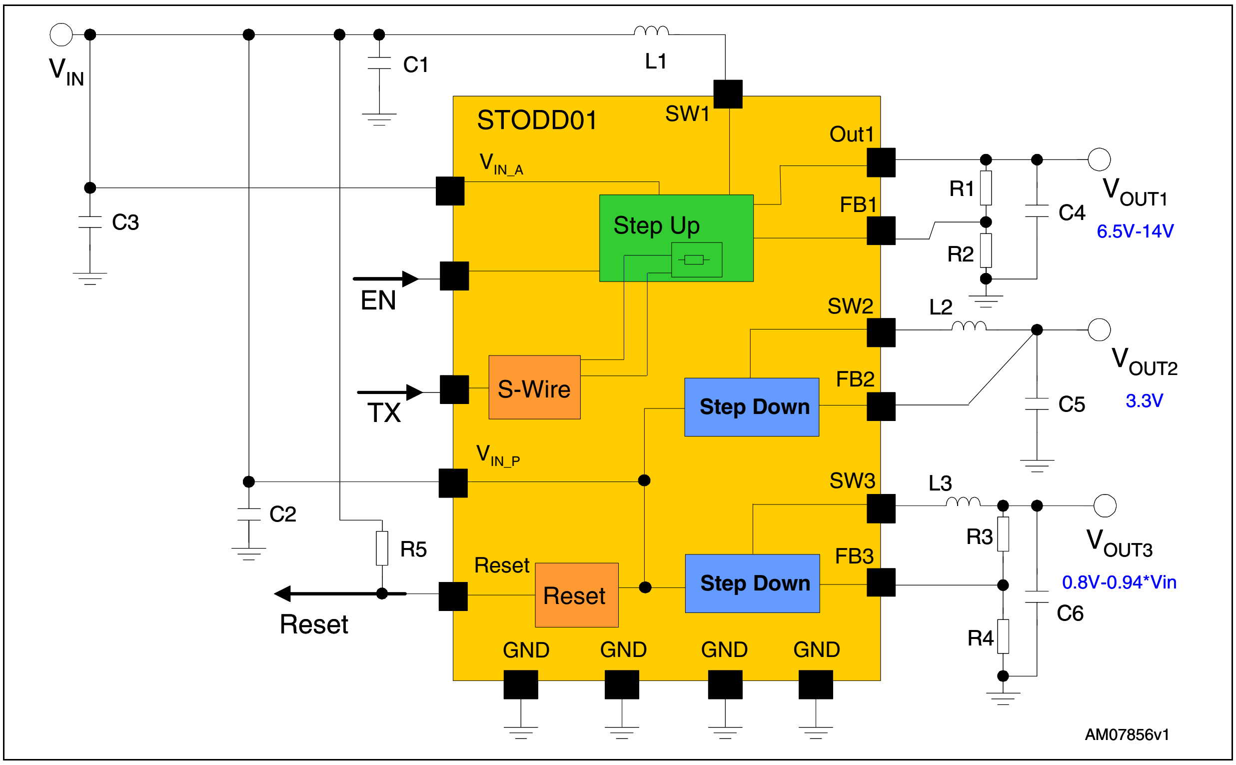


Table 1. List of external components [(1)]

Component	Manufacturer	Part number	Value	Size
C1, C2, C3	Murata	GRM21BR61A1O6KE19L	10 µF	0805
C4, C5, C6	Murata	GRM32ER61C226KE2OL	22 µF	1210
L1	Coilcraft	LPS6225-472MLB	4.7 µH	6 x 6 x 2.5
L2, L3	Coilcraft	LPS4O18-332MLB	3.3 µH	4.1 x 4.1 x 1.8
R1		33 kΩ (V_{OUT1} = 8.8 V)	(2)	0603
R2		3.3 kΩ		0603
R3		27 kΩ (V_{OUT3} = 1.2 V)	(3)	0603
R4		47 kΩ		0603
R5		100 kΩ	(4)	0603
If the S-wire function Is not used, the TX pin must be connected to GND. List of external components [(1)]				

1. Components listed above refer to a typical application. Operation of the STODD01 is not limited to the choice of these external components.
2. R_1 and R_2 are calculated according to the following formula: $R_1 = R_2 (V_{OUT1} / V_{FB1}-1)$

It is recommended to use resistors with values in the range of 1 kΩ to 50 kΩ.

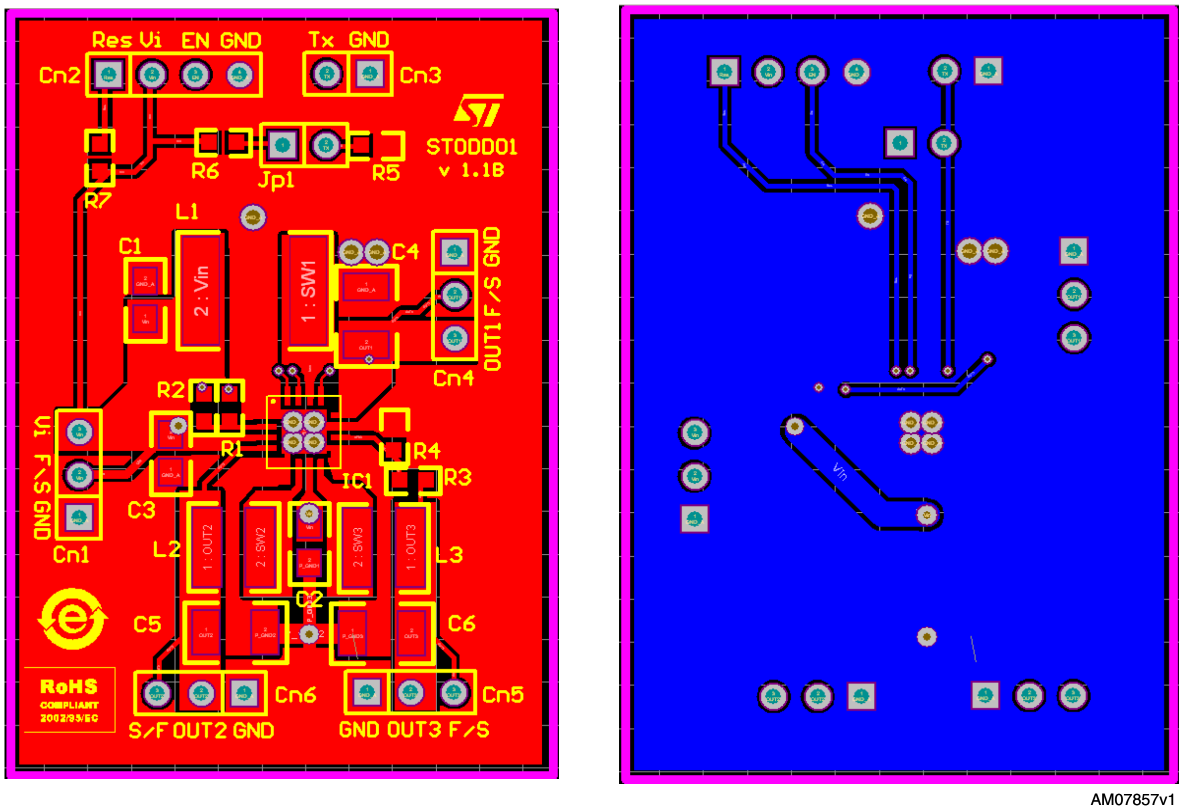
3. R_3 and R_4 are calculated according to the following formula: $R_3 = R_4 (V_{OUT3} / V_{FB3}-1)$

It is recommended to use resistors with values in the range of 1 kΩ to 50 kΩ.

4. It is recommended to use resistors with values in the range of 100 kΩ to 1 MΩ.

2 Recommended PCB layout

Figure 3. Recommended PCB layout



2.1 Layout considerations

The layout is an important design step for all switching power supplies due to the high switching frequency and peak current. If the layout is not performed carefully, important parameters such as efficiency and output voltage ripple may be out of specification.

Short, wide traces must be implemented for the main current and for power ground paths. The input capacitor must be placed as close as possible to the IO pins as well as the inductor and output capacitor.

The feedback pin (FB) connection to the external resistor divider is a high impedance node, so interference can be minimized by placing the routing of the feedback node as far as possible from the high current paths. To reduce pick-up noise, the resistor divider must be placed very close to the device.

A common ground node minimizes ground noise. The exposed pad of the package must be connected to the common ground node.

2.2 Programming the output voltage

The output voltage for the step-up (ch1) can be adjusted from 6.5 V up to 14 V by connecting a resistor divider between the V_{OUT1} and GND, the middle point of the divider must be connected to the FB1 pin, as shown in *Figure 2*.

The resistor divider should be chosen according to the following equation:

Equation 1

$$V_{OUT1} = V_{FB1} \cdot \left(\frac{R_1}{R_2} + 1 \right)$$

where V_{FB1} is programmable, by using S-wire protocol, in the range of 0.8 V to 1.25 V (see *Figure 11*).

It is recommended to use a resistor with a value in the range of 1 kΩ to 50 kΩ. Lower values may also be suitable, but increase current consumption.

For ch2 the device integrates the resistor divider needed to set the correct output voltage (3.3 V). This allows to save 2 external components. The FB2 pin must be connected directly to V_{OUT2}.

The output voltage for ch3 can be adjusted from 0.8 V up to 94 % of the input voltage value by connecting a resistor divider between the V_{OUT3} and GND, the middle point of the divider must be connected to the FB3 pin, as shown in *Figure 2*.

The resistor divider should be chosen according to the following equation:

Equation 2

$$V_{OUT3} = V_{FB3} \cdot \left(\frac{R_3}{R_4} + 1 \right)$$

It is recommended to use a resistor with a value in the range of 1 kΩ to 50 kΩ. Lower values may also be suitable, but increase current consumption.

3 Test results

Figure 4. Inrush current of step-up

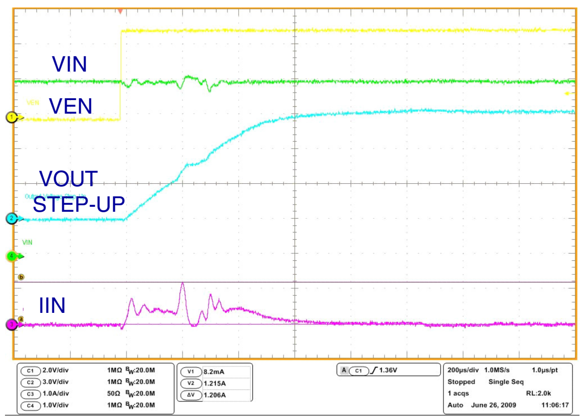


Figure 5. Enable startup time of step-up

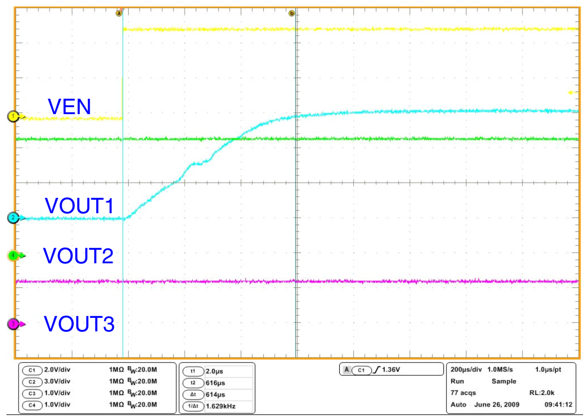


Figure 6. Efficiency ch1 step-up

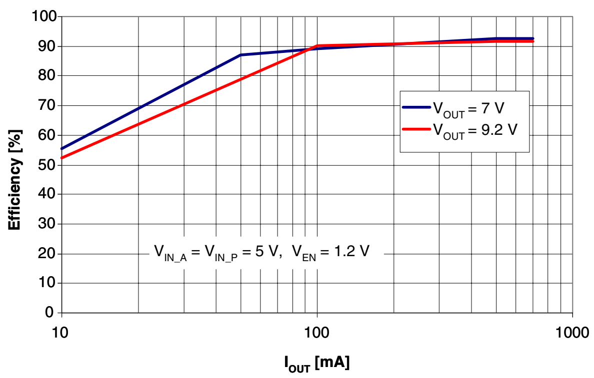


Figure 7. Efficiency ch2-ch3 step-down

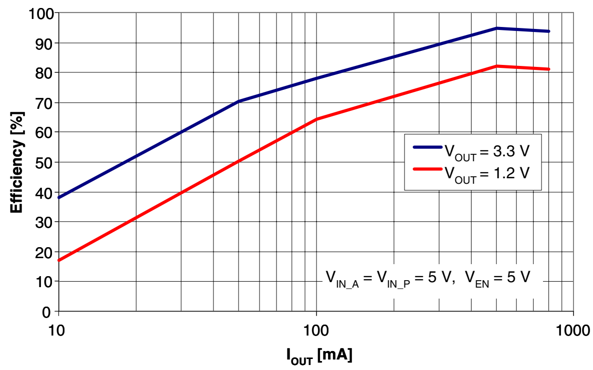
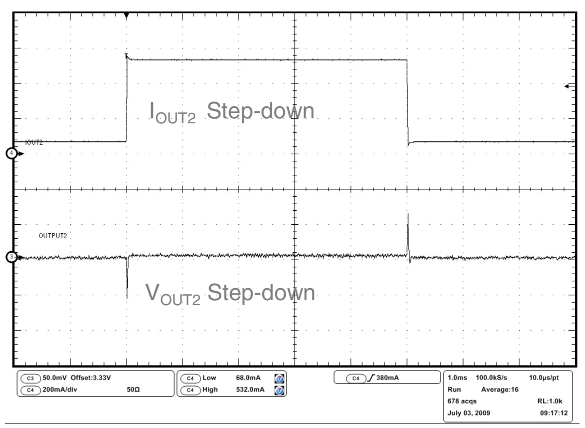
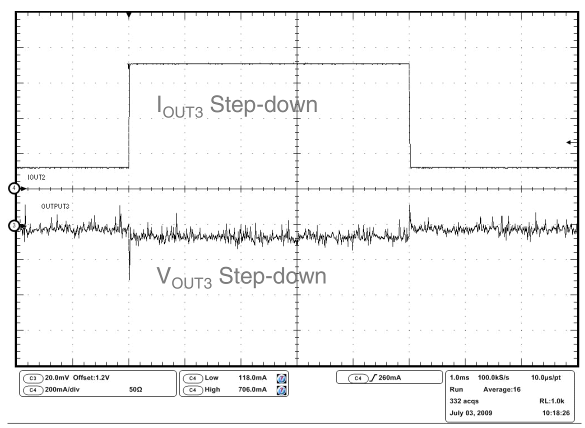


Figure 8. Step-down load transient OUT2



$V_{IN\_A} = V_{IN\_P}$ = 5 V, V_{EN} from 0 to 5 V, V_{OUT2} = 3.2 V, I_{OUT2} = 100-700 mA, $C_{IN1,2,3}$ = 10 µF, $C_{OUT1,2,3}$ = 22 µF, L_1 = 4.7 µH, $L_2 = L_3$ = 3.3 µH, $T_{rise} = T_{fall}$ = 1 µs

Figure 9. Step-down load transient OUT3

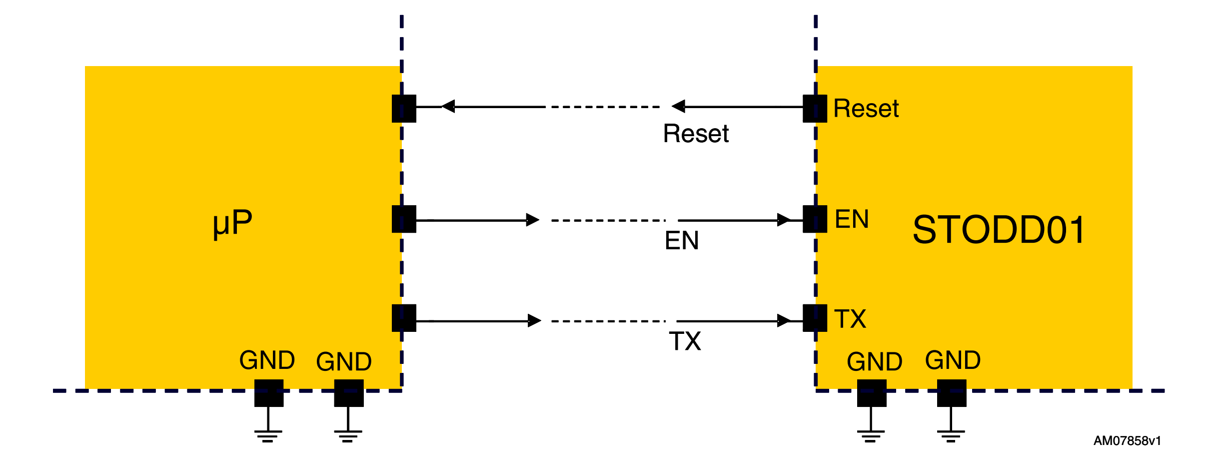


$V_{IN\_A} = V_{IN\_P}$ = 5 V, V_{EN} from 0 to 5 V, V_{OUT3} = 1.2 V, I_{OUT3} = 100-700 mA, $C_{IN1,2,3}$ = 10 µF, $C_{OUT1,2,3}$ = 22 µF, L_1 = 4.7 µH, $L_2 = L_3$ = 3.3 µH, $T_{rise} = T_{fall}$ = 1 µs

3.1 S-wire protocol

The device implements an S-wire bus communication that uses one control signal coming from the microprocessor to program the STODD01 output voltage (see *Figure 10*).

Figure 10. Wire connection



S-wire protocol allows to change the feedback voltage of the step-up section from 0.8 to 1.25 V, with steps of 15 mV. This feature allows complete and easy control of the laser diode power during read and write operation.

If this function isn't used, the TX pin must be connected to GND.

Table 2. Feedback one voltage level

S-wire pulses	V_{FB1} (V)	S-wire pulses	V_{FB1} (V)	S-wire pulses	V_{FB1} (V)
0 (Default Value)	0.800	11	0.965	22	1.130
1	0.815	12	0.980	23	1.145
2	0.830	13	0.995	24	1.160
3	0.845	14	1.010	25	1.175
4	0.860	15	1.025	26	1.190
5	0.875	16	1.040	27	1.205
6	0.890	17	1.055	28	1.220
7	0.905	18	1.070	29	1.235
8	0.920	19	1.085	30	1.250
9	0.935	20	1.100		
10	0.950	21	1.115		

The TX pin must be set to '1' after programming. If TX is programmed with 0 S-wire pulses, the V_{FB1} is programmed to 0.8 V.

Figure 11. Single wire programming

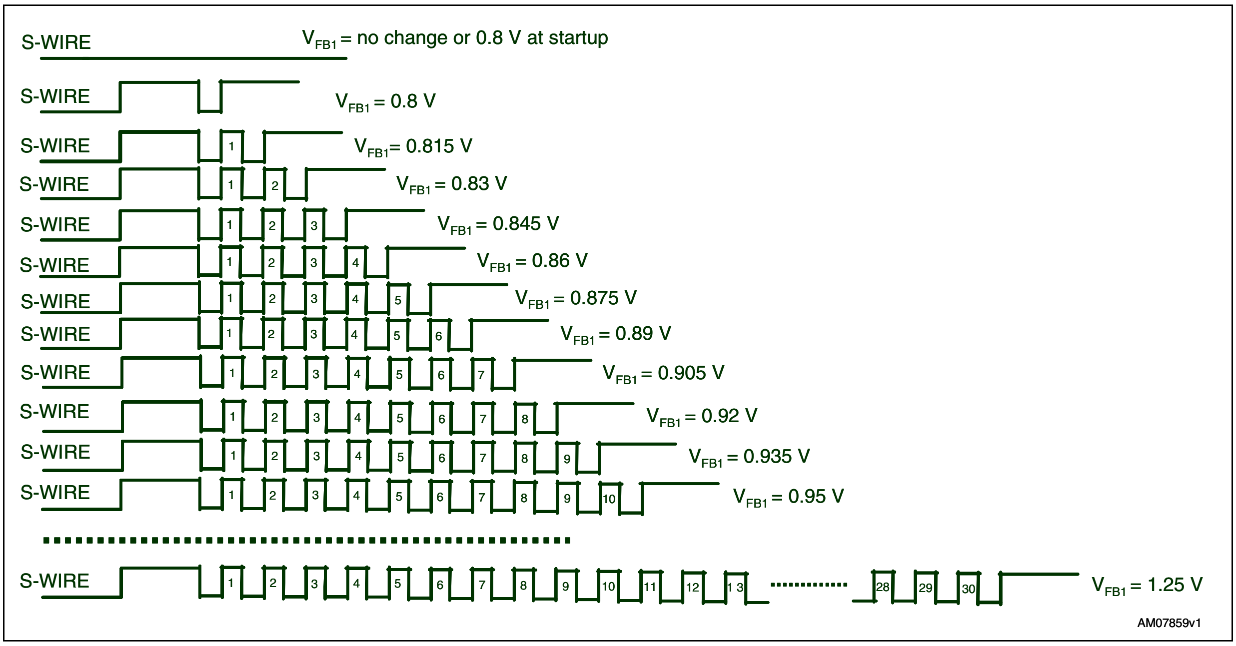
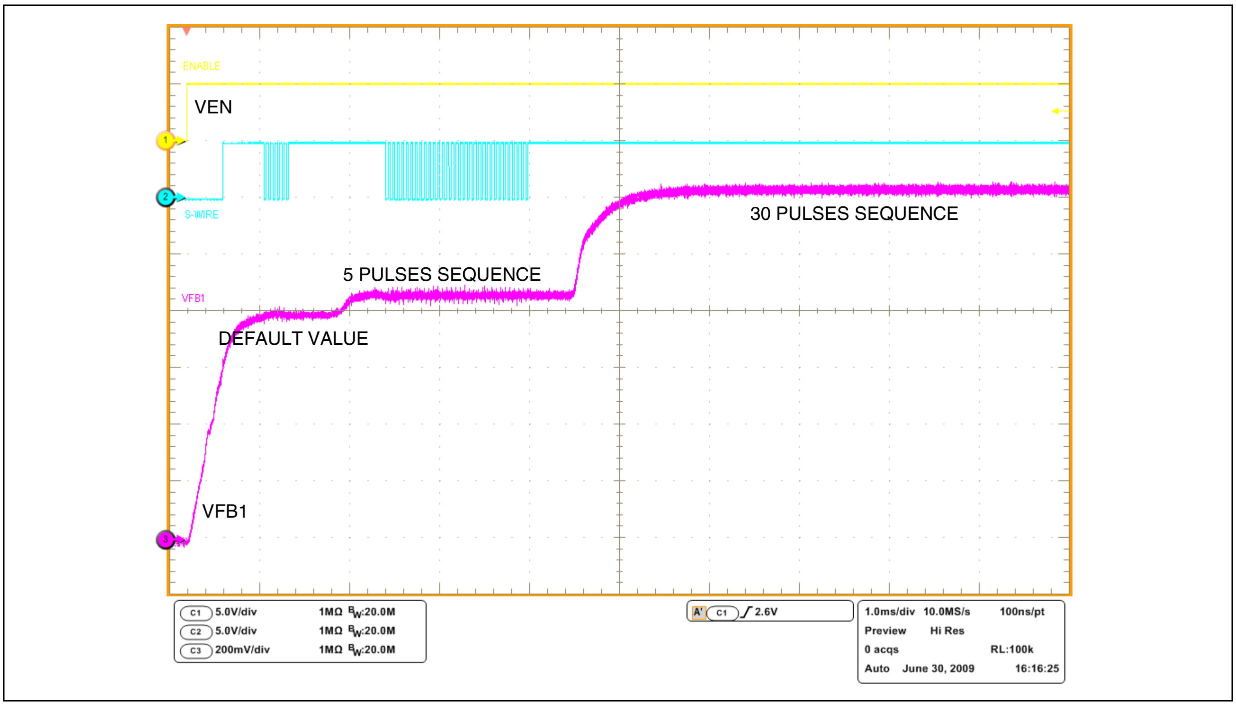


Figure 12. Example of S-wire programming



3.2 Inductor selection

The inductor is the key passive component for switching converters. The inductor selection must take the boundary conditions in which the converter works into consideration; for the buck, the maximum input voltage, and for the boost, the minimum input voltage. The critical inductance values are then obtained according to the following formulas:

for the step-down:

Equation 3

$$L_{MIN} = \frac{V_{OUT} \cdot (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \cdot F_{SW} \cdot \Delta I_L}$$

and for the step-up:

Equation 4

$$L_{MIN} = \frac{V_{IN\_MIN} \cdot (V_{OUT} - V_{IN\_MIN})}{V_{OUT} \cdot F_{SW} \cdot \Delta I_L}$$

where:

F_{SW}: switching frequency.

ΔI_L = the peak-to-peak inductor ripple current. As a rule of thumb, the peak-to-peak ripple can be set at 20 % - 40 % of the output current for the step-down and can be set at 20 % - 40 % of the input current for the step-up.

The peak current of the inductor must be calculated as:

Equation 5

$$I_{PEAK-STEP-DOWN} = (I_{OUT}/0.8) + \frac{V_{OUT} \cdot (V_{IN\_MAX} - V_{OUT})}{2 \cdot V_{IN\_MAX} \cdot F_{SW} \cdot L}$$

Equation 6

$$I_{PEAK-STEP-UP} = \left(\frac{V_{OUT} \cdot I_{OUT}}{\eta \cdot V_{IN\_MIN}}\right) + \frac{V_{IN\_MIN} \cdot (V_{OUT} - V_{IN\_MIN})}{2 \cdot V_{OUT} \cdot F_{SW} \cdot L}$$

In addition to the inductance value, in order to avoid saturation, the maximum saturation current of the inductor must be higher than that of the I_{PEAK}.

3.3 Input and output capacitor selection

It is recommended to use ceramic capacitors with X5R or X7R dielectric and low ESR as input and output capacitors in order to filter any disturbance present in the input line and to obtain stable operation. The output capacitor is very important to satisfy the output voltage ripple requirement.

The output voltage ripple (V_{OUT_RIPPLE}) in continuous mode, for the step-down channel, must be calculated as:

Equation 7

$$V_{OUT\_RIPPLE} = \Delta I_L \cdot \left[ESR + \frac{1}{8 \cdot C_{OUT} \cdot F_{SW}} \right]$$

where: ΔI_L is the ripple current and F_{SW} is the switching frequency.

The output voltage ripple (V_{OUT_RIPPLE}) in continuous mode, for the step-up channel, is:

Equation 8

$$V_{OUT\_RIPPLE} = I_{OUT} \cdot \left[ESR + \frac{(V_{OUT} - V_{IN})}{V_{OUT} \cdot C_{OUT} \cdot F_{SW}} \right]$$

where F_{SW} is the switching frequency.

The use of ceramic capacitors with voltage ratings in the range higher than 1.5 times the maximum input or output voltage is recommended.

Figure 13. Inductor with high I_{SAT} current

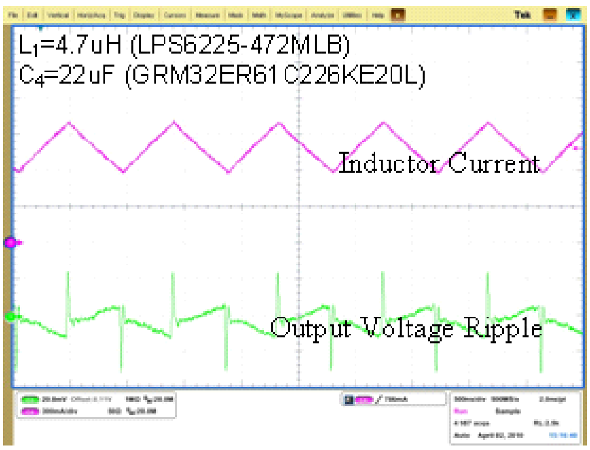
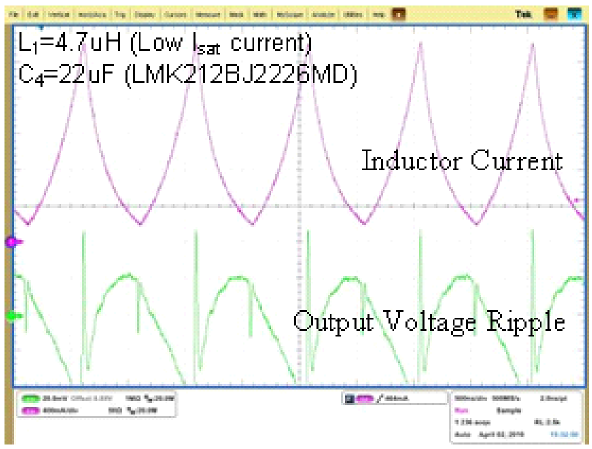


Figure 14. Inductor with low I_{SAT} current



The inductors with low saturation current dramatically increase the inductor peak current value; as shown, using an inductor with low saturation current, the inductor current is higher than 2.4 A. With the LPS6225-472MLB inductor (I_{SAT} = 3 A) the peak current value is about 1 A.

Figure 15. Efficiency

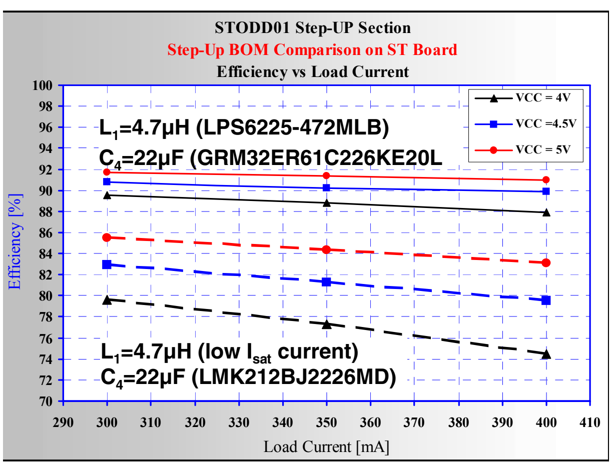
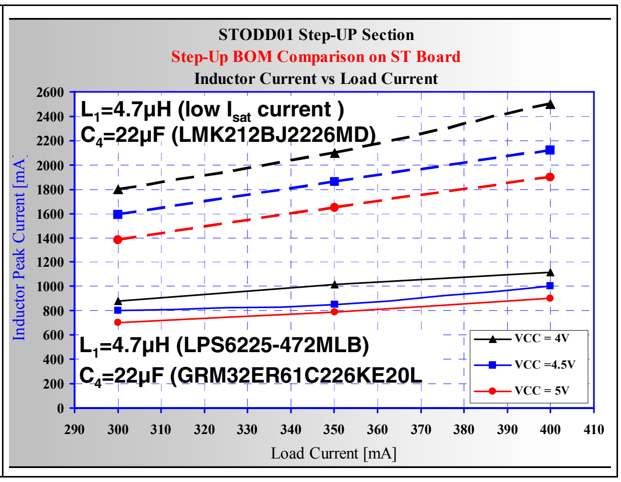


Figure 16. Inductor peak current



The resistance R_{DC} and low saturation current of this inductor have a strong impact on efficiency and output voltage ripple.

Figure 17. Capacitive change vs. voltage C4 GRM32ER61C226KE20L

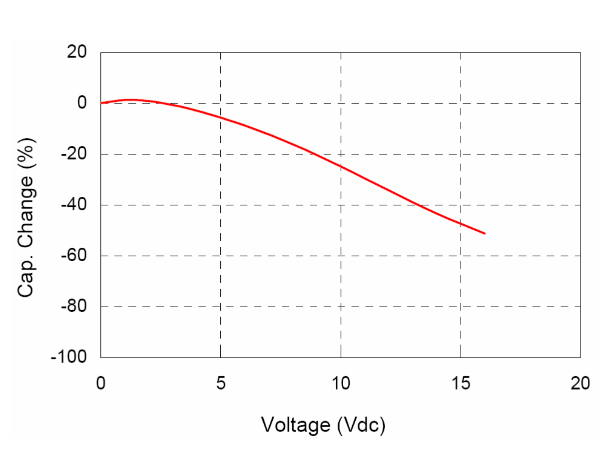
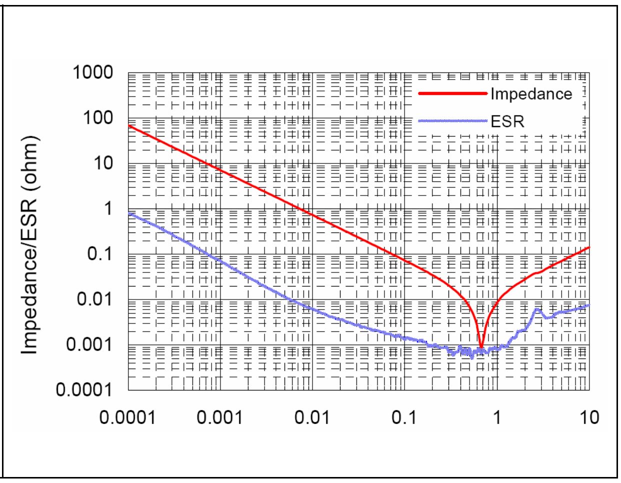


Figure 18. Impedance/ESR characteristics C4 GRM32ER61C226KE20L



Output voltage ripple depends on output capacitor ESR and by increasing the voltage rating of the capacitor, as suggested by the BOM list, the switching ripple is minimized.

4 Revision history

Table 3. Document revision history

Date	Revision	Changes
03-Jan-2011	1	Initial release.