AN3271
Application note

Using the STM6600, STM6601 smart push-button on/off controller

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Introduction

This application note provides a detailed description of the primary applications and benefits of the STM6600-STM6601. These devices allow easy and safe control of applications run with one or two push-buttons by securely starting or powering down a system and also resetting the processor or disabling power in case of a non-responding application (e.g. code in a dead loop). This makes the STM660x devices suitable for a broad spectrum of applications such as terminals, audio and video players, smartphones, PDAs, PCs, or any portable device.

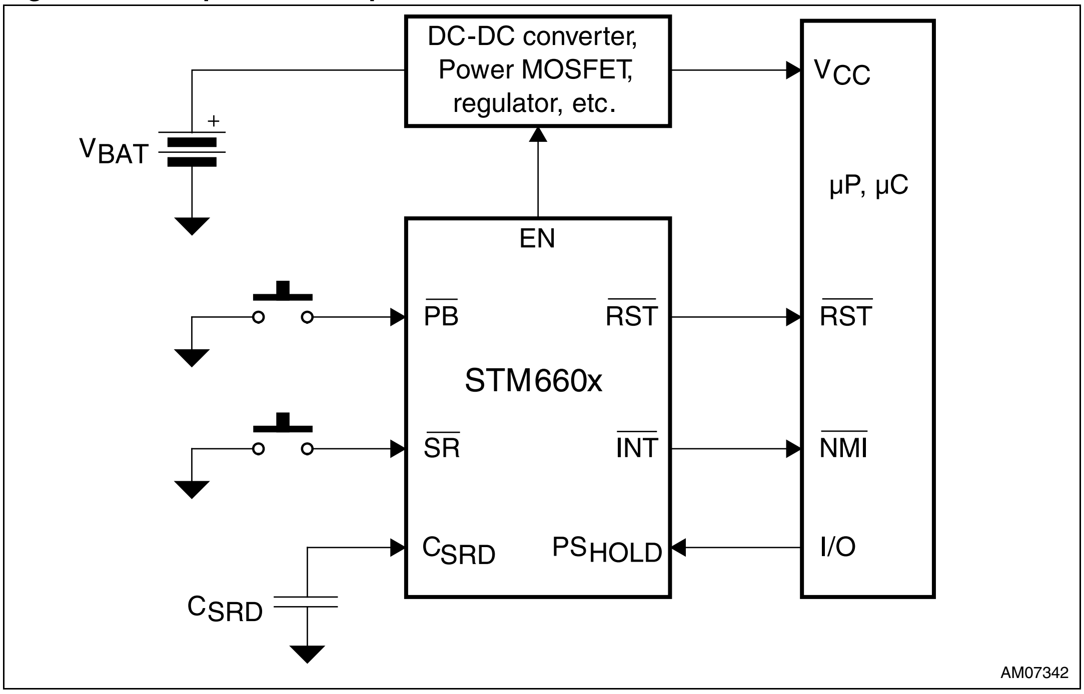
A smart on/off controller monitors the state of the connected push-button(s) as well as ensures sufficient supply voltage. An enable output controls the power for the application through a MOSFET transistor, DC-DC converter, regulator, etc. (see *Figure 1*).

The device also offers additional features such as a precise 1.5 V voltage reference with very tight accuracy of ±1%, which can be used as a reference for A/D and D/A conversion.

The current consumption is a very low 6 µA during normal operation and only 0.6 µA current during standby.

The STM660x is available in the tiny TDFN12 package and is offered with several optional features such as selectable threshold, hysteresis, timeouts, output types, etc. (see datasheet for available part options).

Figure 1. Simplified hookup



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1 Basic functionality

1.1 Safe power-up

If the system is off, press the $\overline{PB}$ button to safely power up. EN output is asserted and power for the application is enabled. Proper power-up has to be confirmed from a processor by PS_{HOLD} assertion, otherwise EN is deasserted.

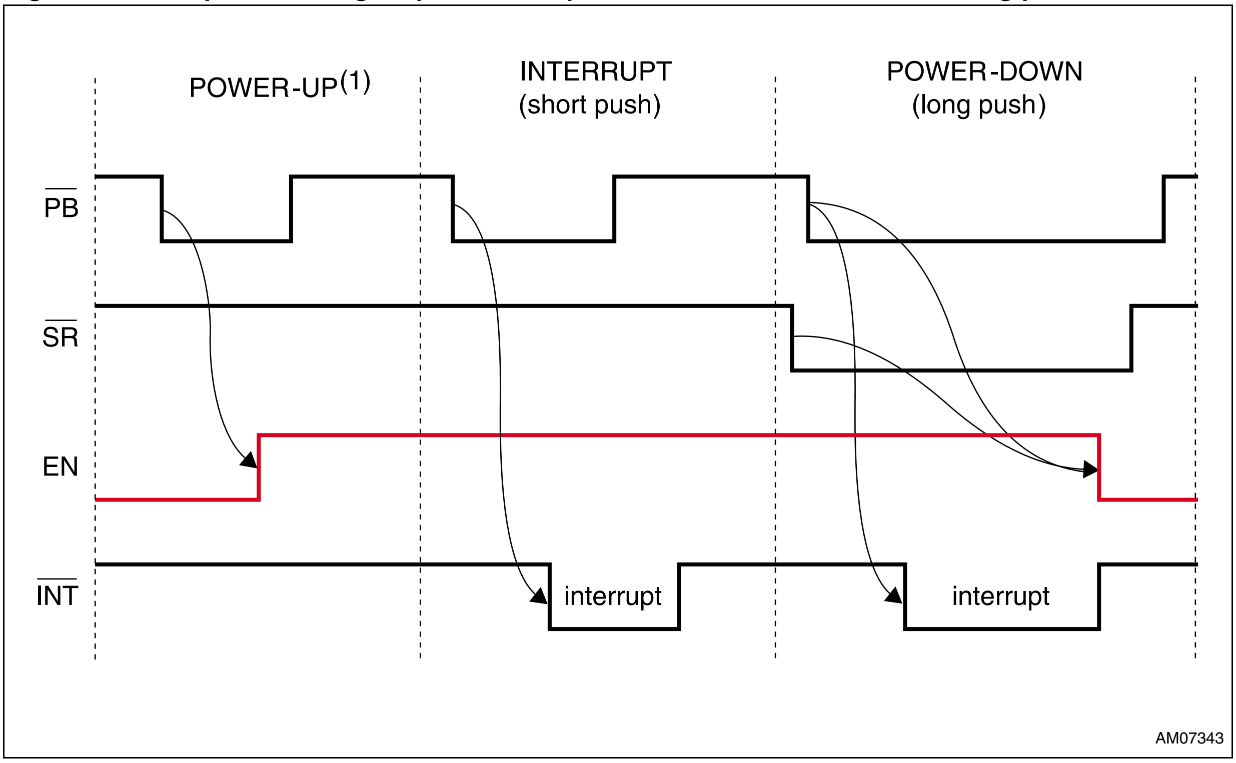
1.2 Interrupt assertion

If the device is on, press the $\overline{PB}$ button to assert an interrupt to the processor. The processor can then perform backup routines and prepare the application for shutdown, reset, display the menu, etc.

1.3 Power-down after long push (optional)

If the application is not responding to the interrupt (e.g. program freezes), press the $\overline{PB}$ button and $\overline{SR}$ button simultaneously to power down the application regardless of processor response. The time needed for both buttons to be held is adjustable by external capacitor C_{SRD}.

Figure 2. Simplified timing sequence for option "enable deasserted after long push"

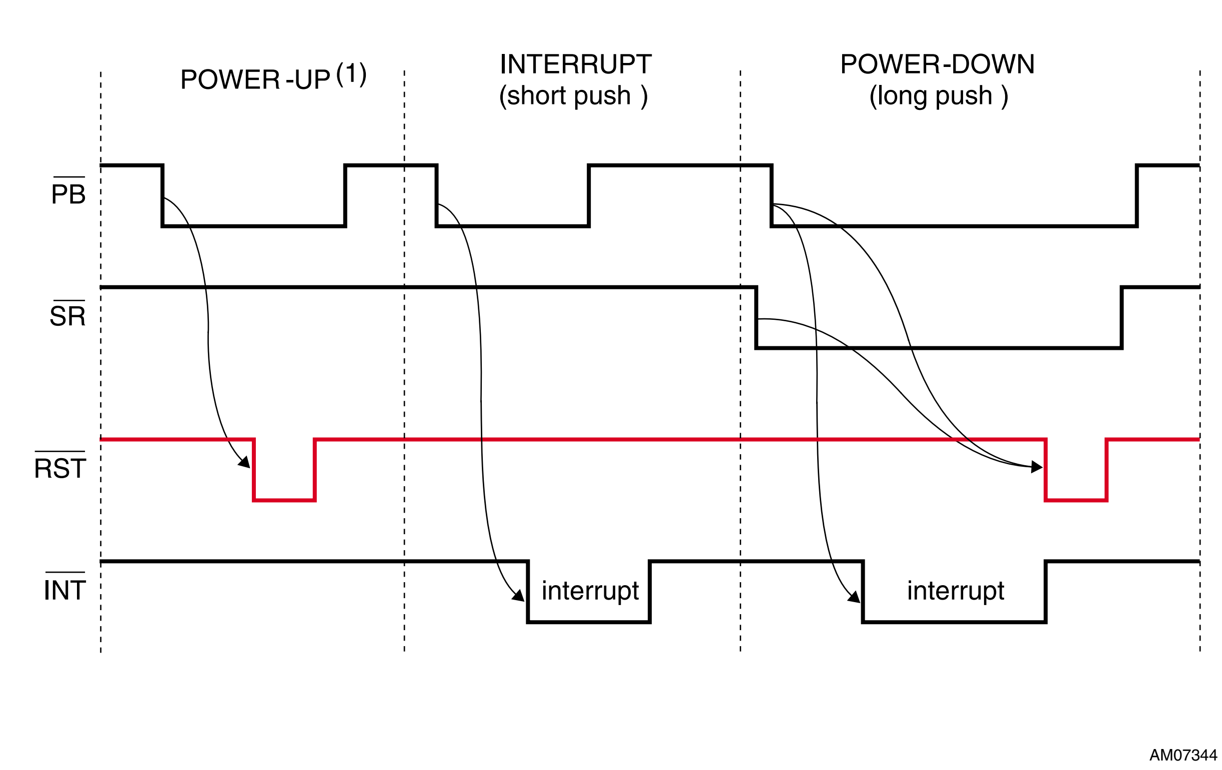


1. For successful power-up the battery voltage has to be above V_{TH+} threshold.

1.4 Reset after long push (optional)

Holding the $\overline{PB}$ and $\overline{SR}$ buttons simultaneously asserts a reset regardless of processor response - i.e. if the application is not responding to an interrupt (e.g. program freezes) (see *Figure 3*). The time needed for both buttons to be held is adjustable by an external capacitor (C_{SRD}).

Figure 3. Simplified timing sequence for option "reset asserted after long push"



1. For successful power-up the battery voltage has to be above V_{TH+} threshold.

2 Pin descriptions and typical application hookup

V_{CC} - power supply input is monitored at startup and during operation to have sufficient voltage.

$\overline{\textbf{PB}}$ - push-button input is used to start an application or assert an interrupt during normal operation or possibly power down the application.

$\overline{\textbf{SR}}$ - Smart Reset button, when pressed together with $\overline{PB}$, can either power down the application or reset the device regardless of system response.

EN ($\overline{\textbf{EN}}$) - active high or active low enable output (device ordering option) can drive various power switches from PMOS to DC-DC converters, regulators, etc. and therefore switch power for the application. It is asserted by a $\overline{PB}$ button press and confirmed by PS_{HOLD} assertion (V_{CC} has to be above threshold the whole time). Enable output can be deasserted by the following events:

- Startup is not properly confirmed by PS_{HOLD} assertion
- PS_{HOLD} is deasserted (driven low) during operation
- Undervoltage condition is detected
- Long push of $\overline{PB}$ and $\overline{SR}$ buttons is detected (valid only for devices with option “EN deasserted by long push”)
- PS_{HOLD} is not asserted after reset invoked by a long push of $\overline{PB}$ and $\overline{SR}$ buttons (valid only for devices with option “$\overline{RST}$ deasserted by long push”)

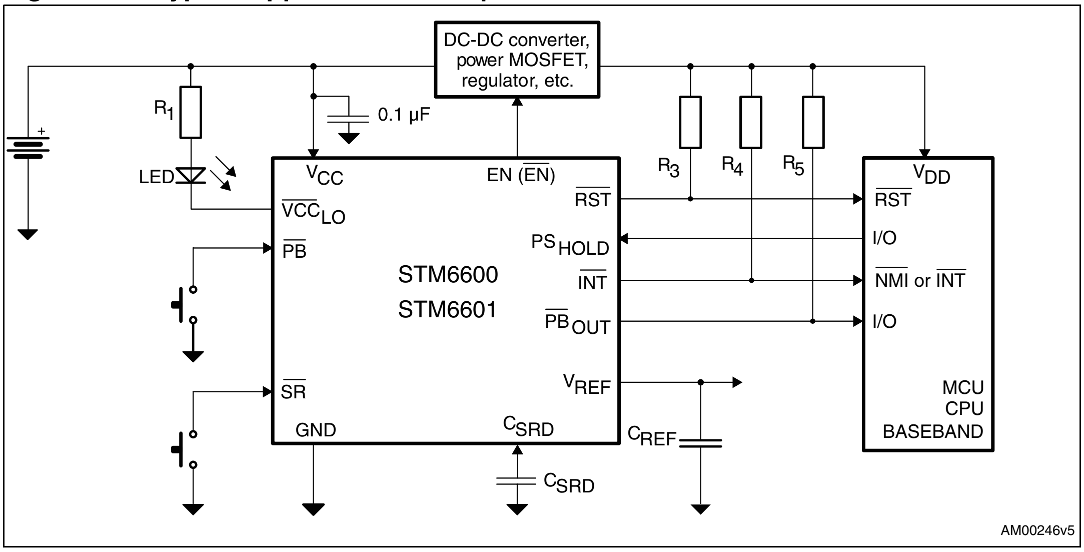
$\overline{\textbf{RST}}$ - system reset, output is asserted during power-up or after a long push of $\overline{PB}$ and $\overline{SR}$ buttons simultaneously (device option).

PS_{HOLD} - assertion of the input confirms proper power-up, deassertion disables power for the application.

C_{SRD} - external capacitor connected to C_{SRD} pin determines how long the $\overline{PB}$ and $\overline{SR}$ buttons must be held in order to recognize a long push and either reset the system or disable the system power (based on option used), the constant is 10 s / µF.

V_{REF} - highly precise 1.5 V voltage reference output with ±1% accuracy (can be used as a reference for analog-digital converters, for example). A 1 µF C_{REF} capacitor on the output is mandatory.

Figure 4. Typical application hookup



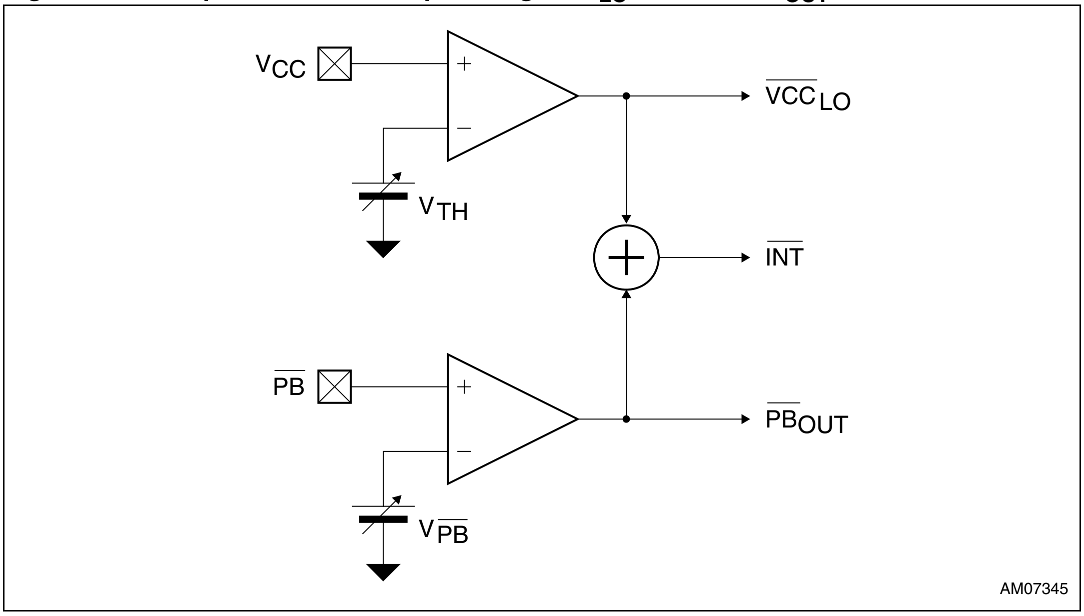
$\overline{VCC_{LO}}$ - output signal is asserted if the battery voltage is insufficient, an LED indicates low battery voltage.

$\overline{INT}$ - interrupt output indicates either low battery voltage or a press of the $\overline{PB}$ button during operation. After asserting an interrupt, the processor should prepare the system for power-down.

$\overline{PB}_{OUT}$ - output is asserted if the $\overline{PB}$ button is pressed. The primary cause of $\overline{INT}$ assertion can be easily derived from this signal.

The relationship among $\overline{VCC}_{LO}$, $\overline{INT}$ and $\overline{PB}_{OUT}$ is clear from the simplified block diagram in *Figure 5*.

Figure 5. Simplified relationship among $\overline{VCC}_{LO}$, $\overline{INT}$ and $\overline{PB}_{OUT}$



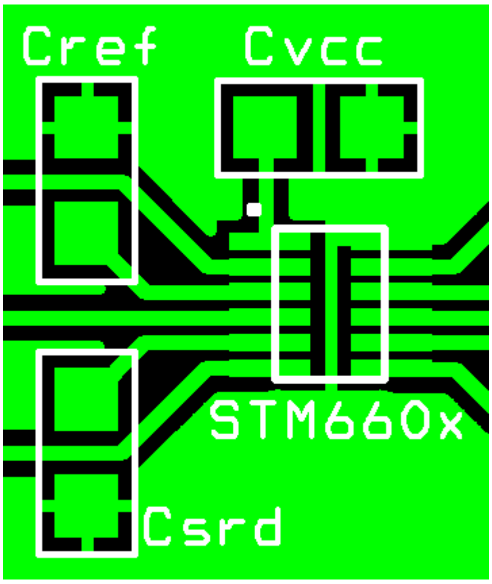
3 Timing accuracy note

External capacitor-adjusted timings and environmental considerations

There are several external factors to be considered that may affect the accuracy of the timing related to the Smart Reset^{TM} delay time t_{SRD}. The timing specification found in the datasheet applies solely to the STM660x devices (i.e. it does not include an ideal timing capacitor, external tolerances, temperature dependencies nor leakages).

The STM660x device is designed to meet strict requirements for the lowest possible current consumption and to maintain the basic timing constant of 10 s / µF, therefore the constant current used to charge the external timing capacitor is low, in the order of 100 nA. Any external leakage due to poor quality timing capacitors or excessive humidity (especially if the dew point is exceeded and moisture condenses on the PCB tracks) may cause a significant leakage current which is deducted from the constant charging current that the device provides. This results in a reduction of the charging current of the real external timing capacitor which increases the Smart Reset delay (t_{SRD}). To minimize this effect, the PCB tracks between the C_{SRD} pin and its respective timing capacitor should be as short as possible, properly covered with solder mask and isolated from other tracks (especially V_{SS}) by as great a distance as possible (see *Figure 6* for recommended layout). Also, low-leakage timing capacitors (ceramic or film capacitor) should be used.

Figure 6. Recommended layout



4 STM660x advantages over alternative solutions

4.1 Using a microprocessor

Some applications use a processor for monitoring the push-buttons. This solution however has some disadvantages compared to the STM660x.

Disadvantages of monitoring using a microprocessor

- If the processor is frozen, the control of the buttons is lost
- Processor can NOT go into standby mode as it must continuously monitor the push-buttons
- Additional load on the processor (I/O pins are needed, the software has to monitor the push-buttons)
- Noise sensitivity

Advantages of monitoring with the STM660x

- Functionality independent from the processor
- Push-buttons monitored even if power for the system is disabled and the STM660x is in standby mode (negligible current consumption of 0.6 µA)
- Glitch immunity - glitches shorter than 32 ms are ignored
- High ESD protection of the inputs

4.2 Discrete solution

Other applications try to replicate STM660x functionality by using a discrete solution.

Disadvantages of a discrete solution

- Significant space on the PCB is needed
- High current consumption
- Sensitivity to accuracy of discrete components
- Noise sensitivity

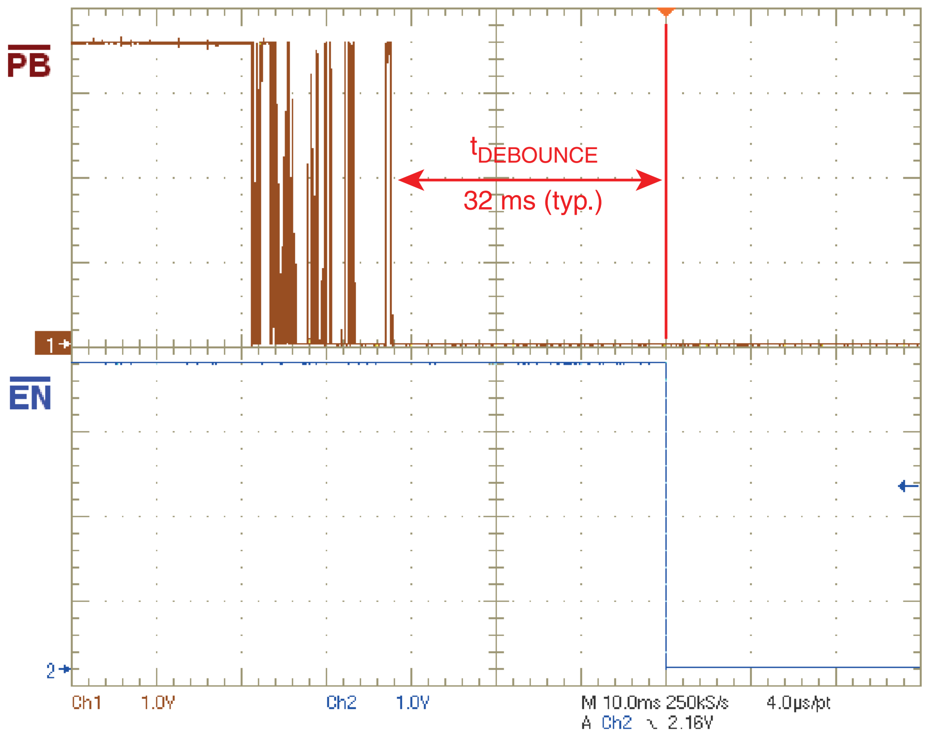
Advantages of using the STM660x

- Compact solution, which needs a tiny fraction of PCB space compared to a discrete solution (at least 20 discrete components are needed to reproduce only a basic functionality of the STM660x devices which are available in a tiny TDFN12 - 2 x 3 mm package)
- Low current consumption of 6 µA and only 0.6 µA in standby mode
- Push-buttons monitored even if power for the system is disabled and the STM660x is in standby mode (negligible current consumption of 0.6 µA)
- Glitch immunity - glitches shorter than 32 ms are ignored
- High ESD protection of the inputs

5 Push-button input glitch immunity

A mechanical push-button connected to $\overline{PB}$ or $\overline{SR}$ input can produce a quite noisy signal during switching. The STM660x ignores all the glitches and asserts an enable output (EN or $\overline{EN}$) only if the push-button input stays low for the debounce time period $t_{DEBOUNCE}$ (typically 32 ms).

Figure 7. Push-button noise immunity

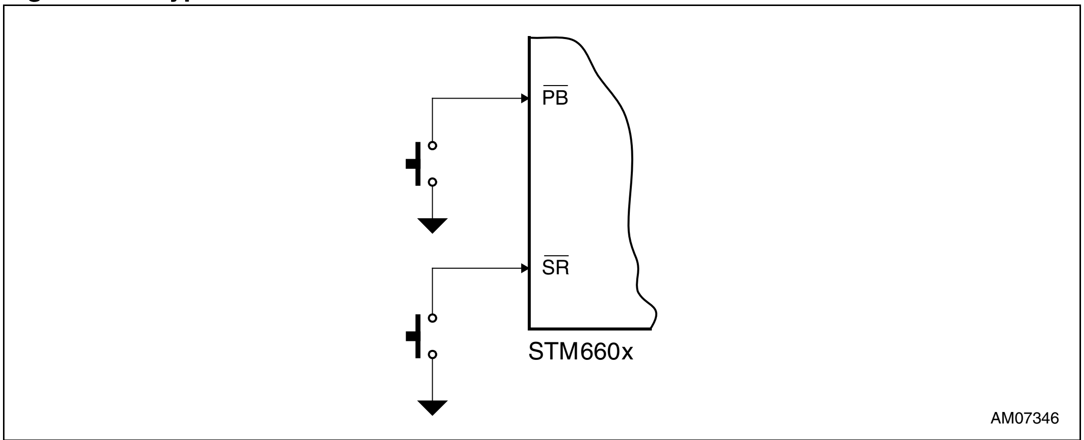


$\overline{PB}$ and $\overline{SR}$ inputs are also equipped with high ESD protection of ±8 kV (human body model).

6 Various connections of push-buttons

The $\overline{PB}$ and $\overline{SR}$ inputs are usually controlled by two separate push-buttons (see *Figure 8*), however both inputs can be connected to a single push-button as shown in *Figure 9*.

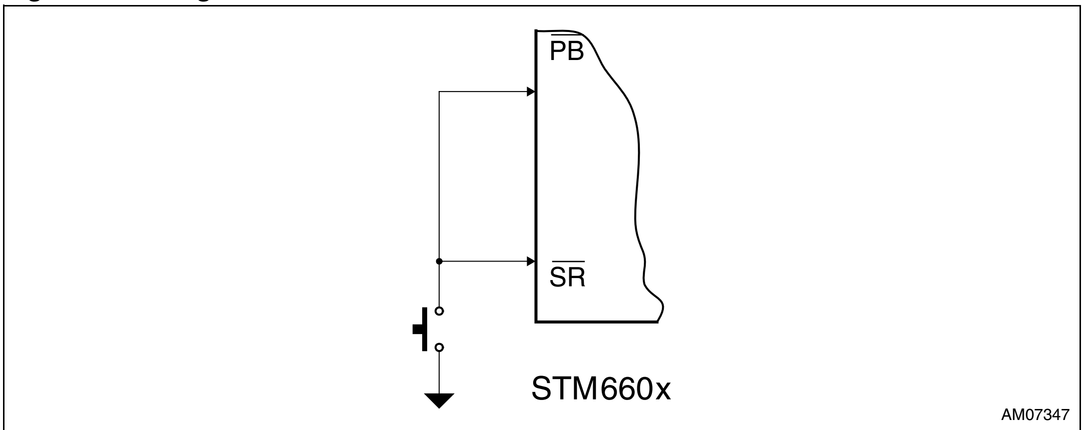
Figure 8. Typical connection of $\overline{PB}$ and $\overline{SR}$ buttons



6.1 Single button control

- If the device is off, press the push-button to power up.
- If the device is on, press the push-button to power down.
- If the application is not responding, press and hold the push-button to power down or reset the application regardless of processor response.

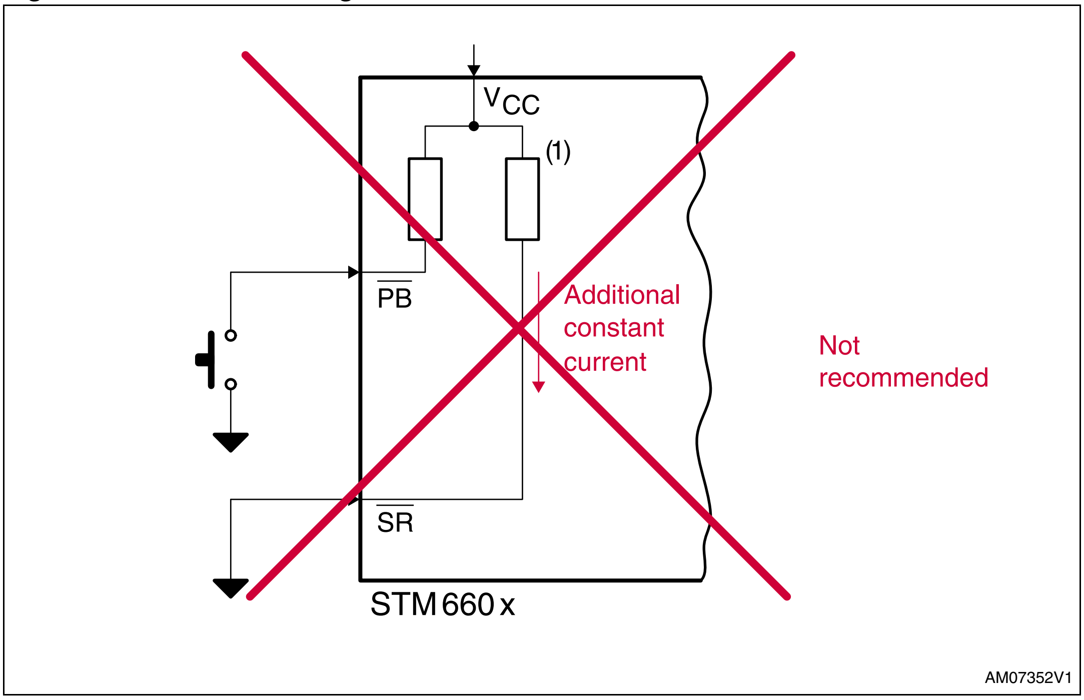
Figure 9. Single button control



6.2 Alternative single button control

The hookup in *Figure 10* might suggest identical functionality compared to hookup in *Figure 9*. However $\overline{SR}$ input is monitored for falling edge after power-up and must not be grounded permanently. In addition some flavors have internal pull-up resistor connected to $\overline{SR}$ input, which would create additional current. Therefore hookup in *Figure 9* is recommended for single button control.

Figure 10. Alternative single button control



1. Internal pull-up resistor is available on STM660xA, STM660xB, STM660xC and STM660xD.

6.3 Multiple button control

- $\overline{PB}$ and $\overline{SR}$ inputs can be controlled by mechanical or electrical switches connected in series or in parallel (see *Figure 11* and *Figure 12*).
- A reset circuitry with active low and open drain output is used as an example of an electrical switch. This reset can monitor supply voltage other than V_{CC} and trigger power-down of an application if it drops below the voltage threshold.

Note: Any output connected to $\overline{PB}$ or $\overline{SR}$ input must be open drain.

Figure 11. Multiple button control

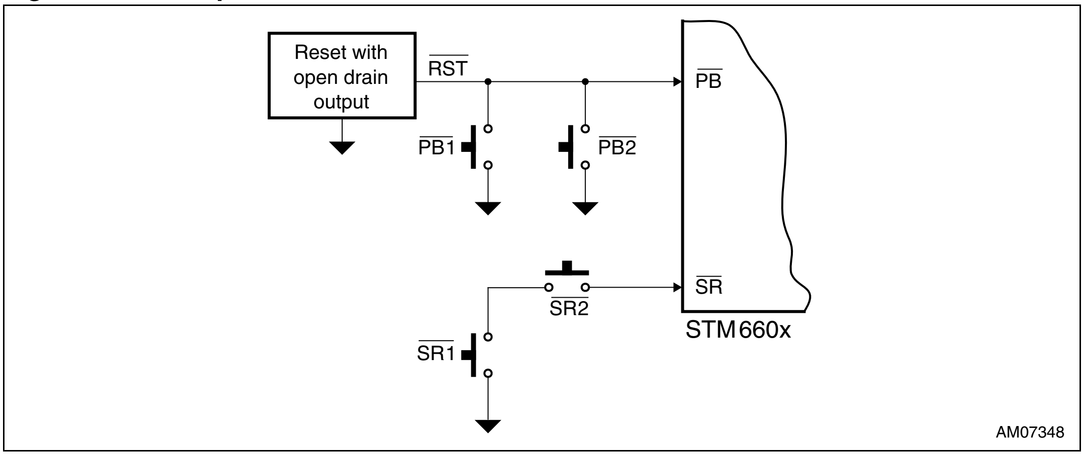
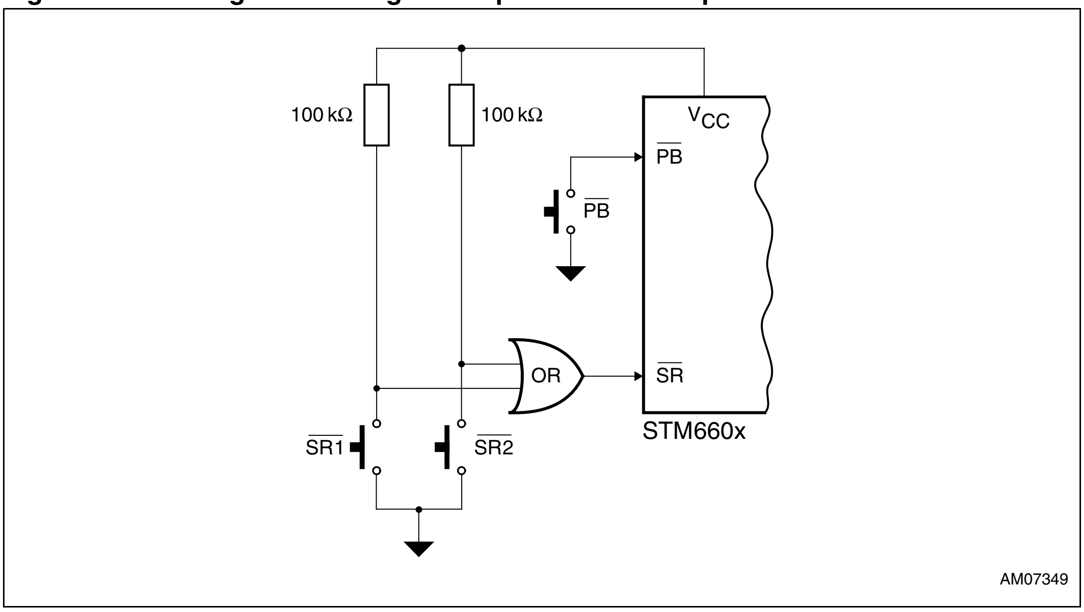


Figure 11 shows how two switches can be wired together to implement the AND function requiring that both $\overline{SR1}$ and $\overline{SR2}$ be pressed to drive $\overline{SR}$ low.

In some applications, switches are packaged such that they share a common ground pin and cannot be connected in that manner. *Figure 12* shows how such switches can be used to implement this active low AND function. In this case, a conventional OR gate is used. When both its inputs are low, its output drives $\overline{SR}$ low.

Figure 12. Adding external logic to implement more inputs



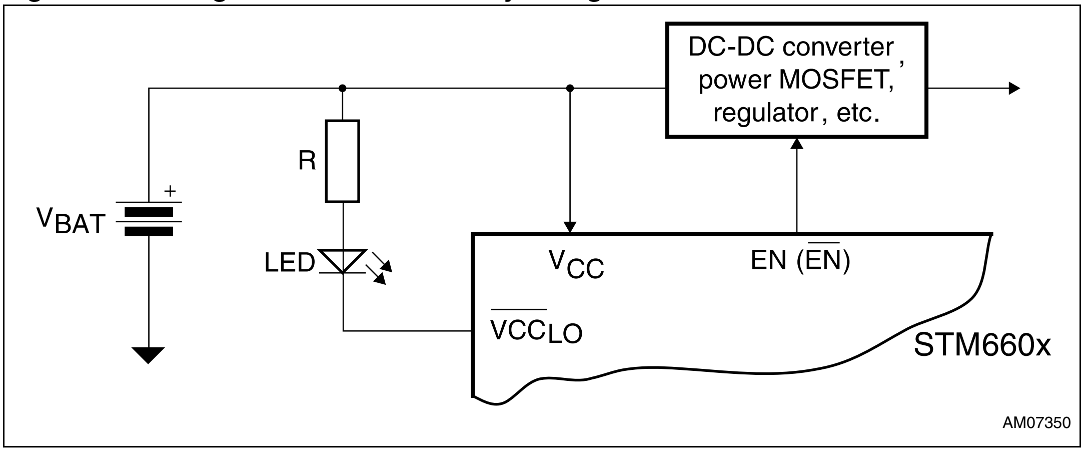
7 Low battery detection

The LED in *Figure 13* is ON if:

- $\overline{PB}$ button is pressed for power-up and low battery voltage is detected (i.e. $V_{CC} < V_{TH+}$).
- Application is powered (i.e. EN or $\overline{EN}$ is asserted) and undervoltage is detected.

Thus the user can be easily informed of the undervoltage condition. $\overline{VCC}_{LO}$ is an open drain output.

Figure 13. Using an LED for low battery voltage detection

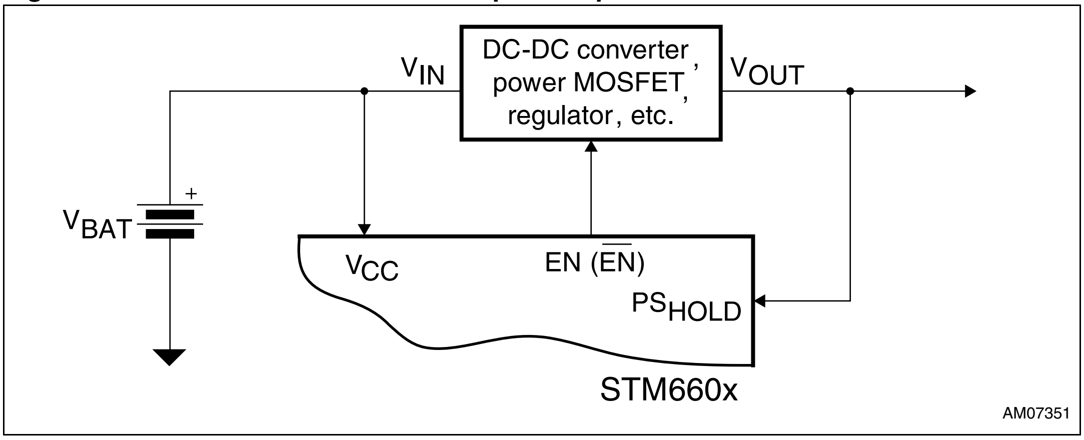


8 Automatic confirmation of power-up

Connect PS_{HOLD} directly to the output voltage V_{OUT} in order to enable automatic confirmation of power-up (see *Figure 14*). This allows immediate power-up but does not guarantee proper startup of the application.

The enable signal EN ($\overline{EN}$) is asserted immediately after pushing the $\overline{PB}$ button, thus enabling V_{OUT}. Since PS_{HOLD} is connected directly to V_{OUT}, power-up is confirmed immediately and EN ($\overline{EN}$) stays asserted. Please note that a small delay can be caused by capacitors connected between ground and V_{OUT} elsewhere in the application.

Figure 14. Automatic confirmation of power-up

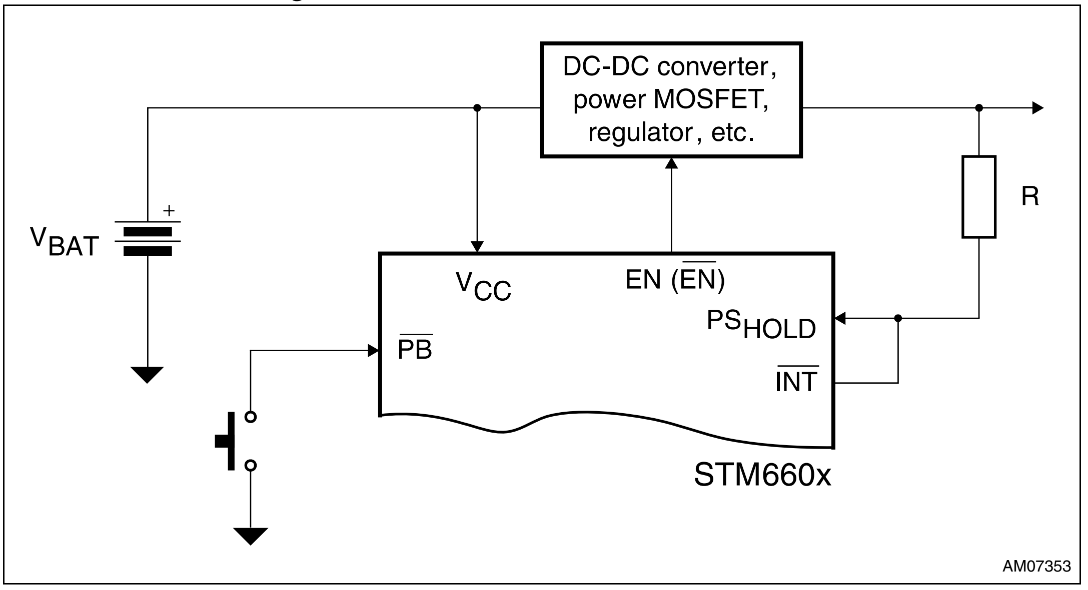


9 Automatic confirmation of power-up + immediate shutdown after $\overline{PB}$ button press or undervoltage

In addition to automatic power-up confirmation, power can be disabled immediately after a $\overline{PB}$ button press or undervoltage detection. In this way the application does not service the interrupt, which decreases its complexity. However as there is no time for data backup and since the application no longer controls power-down, this solution might be considered as less secure in some cases.

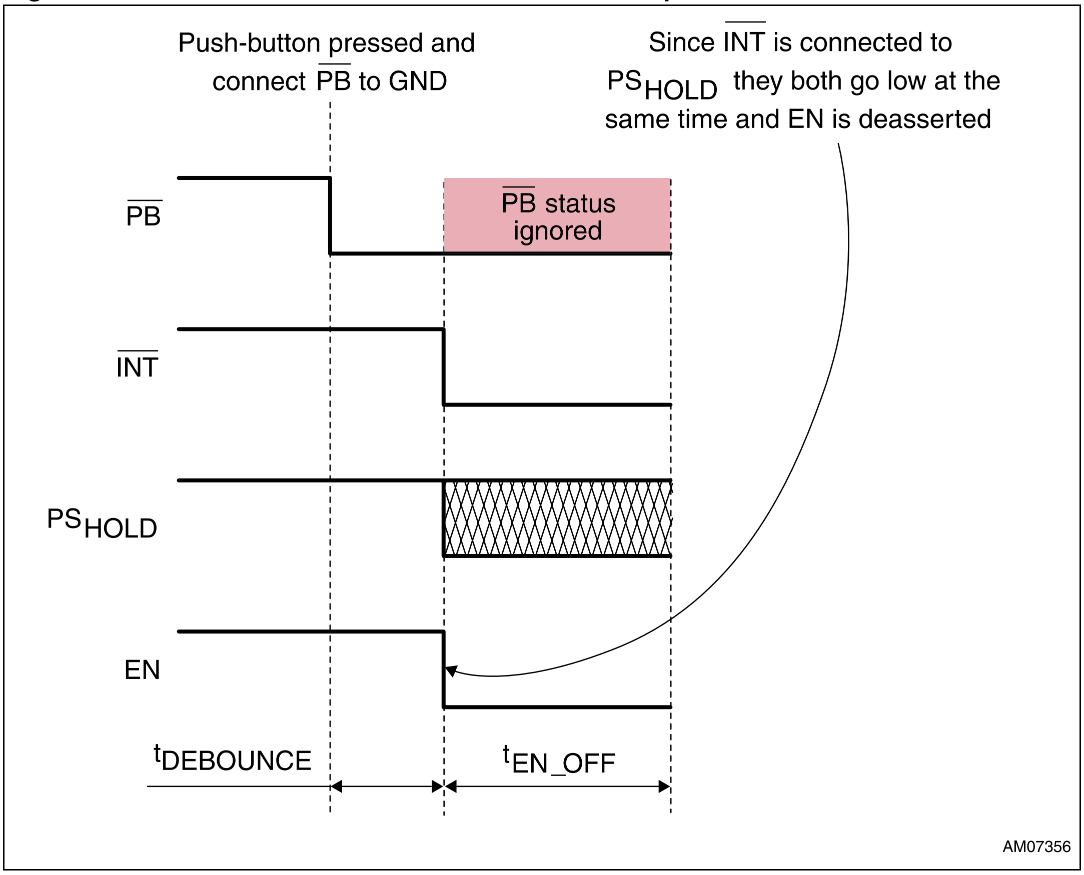
If $\overline{INT}$ is connected to the PS_{HOLD} signal, the power for the application is disabled immediately after pressing the $\overline{PB}$ button or undervoltage detection (see *Figure 15*).

Figure 15. Automatic power-up confirmation + shutdown after $\overline{PB}$ button press or undervoltage



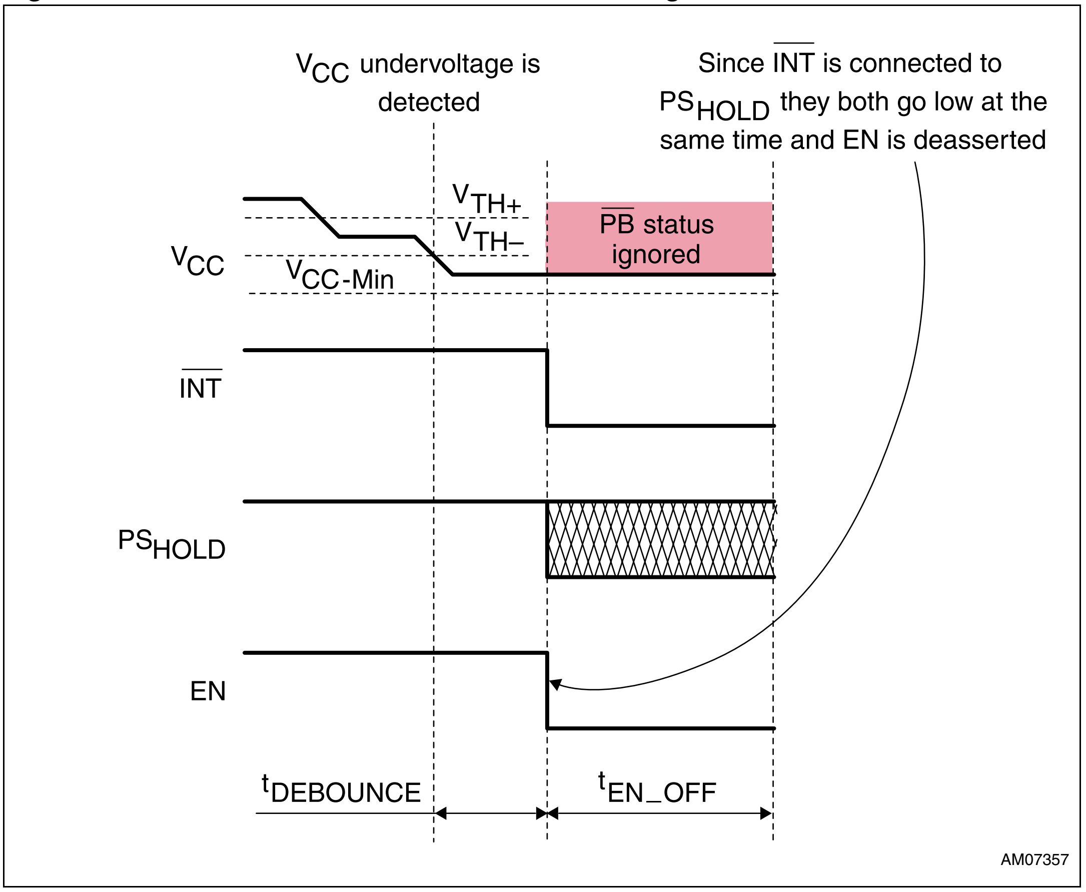
A push-button ($\overline{PB}$) press always asserts the interrupt ($\overline{INT}$). Since $\overline{INT}$ is connected to PS_{HOLD} they both go low at the same time, EN output is deasserted, and therefore power for the application is turned off (see *Figure 16*).

Figure 16. Waveform for shutdown after $\overline{PB}$ button press



The mechanism is similar during undervoltage detection. If the supply voltage (V_{CC}) goes below the threshold (V_{TH-}), the $\overline{INT}$ signal is asserted, PS_{HOLD} goes low and power for application is turned off (see *Figure 17*).

Figure 17. Waveform for shutdown after undervoltage detection

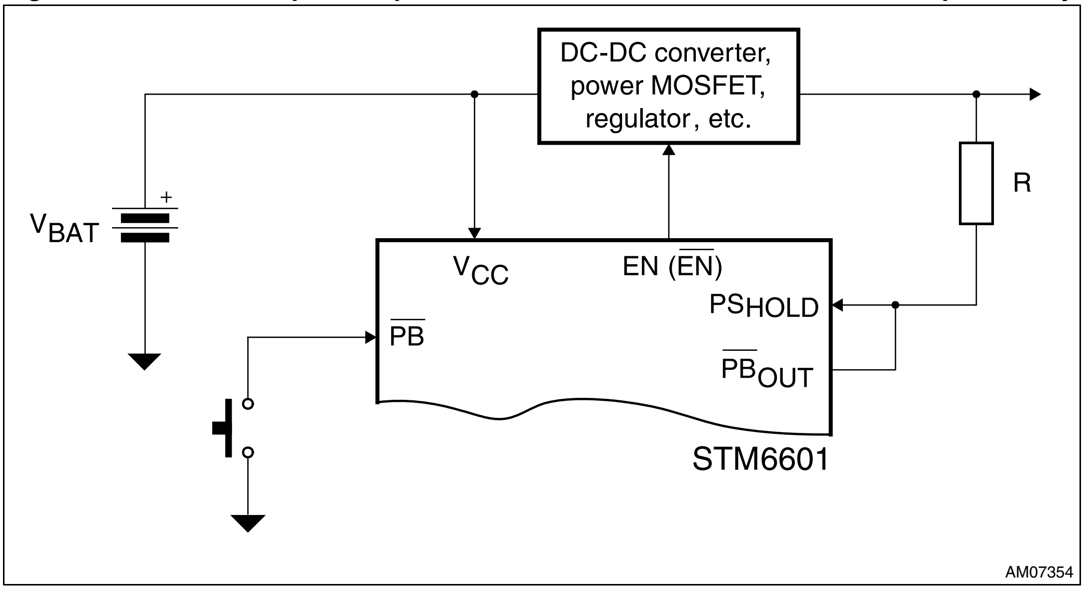


10 Automatic confirmation of power-up + immediate shutdown after $\overline{PB}$ button press only

If $\overline{PB}_{OUT}$ is connected to the PS_{HOLD} signal, power for the application is disabled **only after pressing the $\overline{PB}$ button** (see *Figure 18*).

This hookup only applies to the STM6601 device. For the STM6600, the PS_{HOLD} state is checked after releasing the $\overline{PB}$ button. Since PS_{HOLD} is held low by $\overline{PB}_{OUT}$, the STM6600 would never start.

Figure 18. Automatic power-up confirmation + shutdown after $\overline{PB}$ button press only



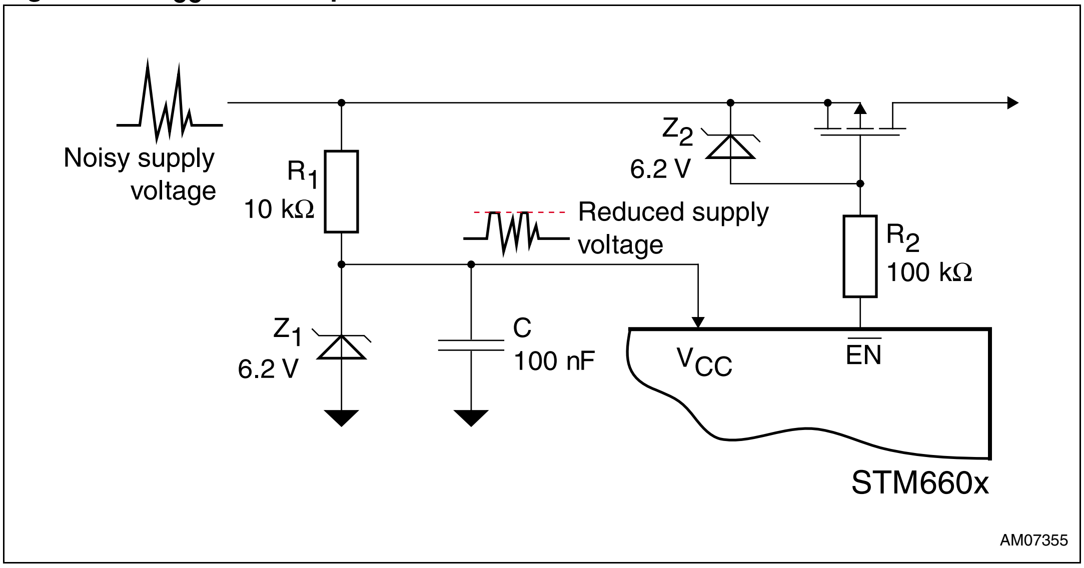
Note: This hookup is not suitable for the STM6600.

11 V_{CC} transient protection

The absolute maximum supply voltage of the STM660x is 7 V. The immunity of high voltage transients can be improved by using a Zener diode Z_1 and current limiting resistor R_1 (see *Figure 19*). The Zener diode does not draw any current within the operating V_{CC} voltage range (V_{CC} specified from 1.6 V to 5.5 V).

A possible PMOS transistor can be protected by Zener diode Z_2 similarly (see *Figure 19*). The diode should have a breakdown voltage smaller than the PMOS gate-source breakdown voltage.

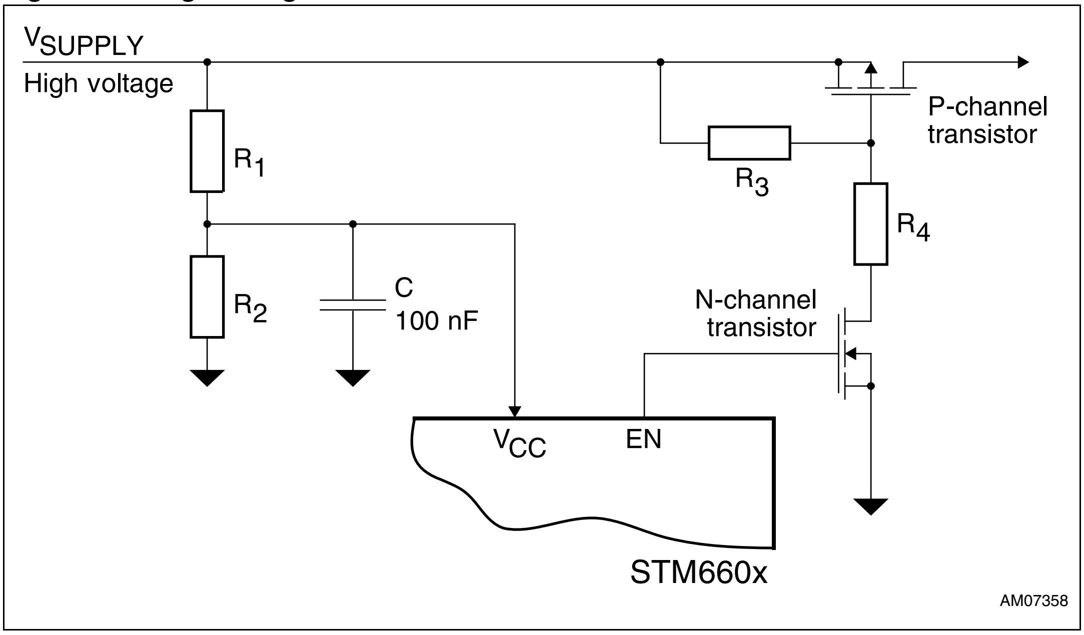
Figure 19. V_{CC} transient protection



12 High voltage connection

Even if the maximum operating voltage of STM660x is 5.5 V, high voltage can be also monitored based on the hookup shown in *Figure 20*. This extends the application scope to devices such as notebooks, printers, network storages, etc. The supply voltage of the application is limited by the maximum drain-source voltage of the P-channel transistor.

Figure 20. High voltage connection



The STM660x device has active high enable output (EN).

The monitored voltage threshold is determined by resistors R_1 and R_2. The STM660x current consumption has to be negligible compared to current through R_1 and R_2 in order to not influence the monitored threshold (approx. 100 µA is recommended). The threshold accuracy decreases with greater R_1 and R_2 resistors. With lower resistor values the accuracy improves, but the overall current consumption increases.The value of resistors R_1 and R_2 can be calculated according to the following equation:

Equation 1

$$R_1 = \frac{V_{SUPPLY-TH} - V_{TH-}}{I_{12}}$$

where

R_1 is the first resistor of the voltage divider,

$V_{SUPPLY-TH}$ is the monitored threshold of the high voltage power supply,

V_{TH-} is the undervoltage threshold of the STM660x,

I_{12} is the current through the R_1/R_2 divider.

Equation 2

$$R_2 = R_1 \frac{V_{TH-}}{V_{SUPPLY-TH} - V_{TH-}}$$

where

R_2 is the second resistor of the voltage divider.

The tolerance of resistors R_1 and R_2 affects the precision of the $V_{SUPPLY\text{-}TH}$ threshold.

R_3 / R_4 ratio has to guarantee a secure open and close of the P-channel transistor. It is possible to use for example dual N-channel / P-channel transistor STS8C5H30L in a tiny SO8 package, which can switch voltages up to 30 V and currents up to 5 A.

The absolute maximum gate-source voltage V_{GS} has to be considered, therefore:

Equation 3

$$R_4 = \frac{V_{SUPPLY-MAX} - V_{GS}}{I_{34}}$$

where

R_4 is the resistor between the P-channel transistor and N-channel transistor,

$V_{SUPPLY-MAX}$ is the possible maximum of V_{SUPPLY} voltage,

V_{GS} is the absolute maximum gate-source voltage or lower,

I_{34} is the current through the R_3 and R_4 resistors.

Equation 4

$$R_3 = \frac{V_{GS}}{I_{34}}$$

where,

R_3 is the resistor between the gate and source of the P-channel transistor.

Example

Let's use STM6600ES24DM6F, which has active high EN output and undervoltage threshold V_{TH-} = 3.2 V.

We would like to monitor the supply voltage V_{SUPPLY} for 18 V, the current through the resistor divider R_1/R_2 is I_{12} = 100 µA and therefore:

Equation 5

$$R_1 = \frac{V_{SUPPLY-TH} - V_{TH-}}{I_{12}} = \frac{18 - 3.2}{100 \times 10^{-6}} = 148k\Omega$$

The closest resistor value from the E6 series is R_1 = 150 kΩ

Equation 6

$$R_2 = R_1\frac{V_{TH-}}{V_{SUPPLY-TH} - V_{TH-}} = 150000\frac{3.2}{18 - 3.2} = 32.43k\Omega$$

The closest resistor value from the E6 series is R_2 = 33 kΩ

The monitored threshold is slightly different due to the E6 series resistors:

Equation 7

$$V_{SUPPLY-TH} = R_1 \times I_{12} + V_{TH-} = 150 \times 10^3 \times 100 \times 10^{-6} + 3.2 = 18.2V$$

If using R_1 = 150 kΩ and R2 = 33 kΩ, the monitored high voltage threshold is 18.2 V. The tolerance of resistors R_1 and R_2 affects the precision of the $V_{SUPPLY\text{-}TH}$ threshold.

Let's use dual N-channel / P-channel transistor STS8C5H30L, which has an absolute maximum gate-source voltage of 16 V. In order to keep some margin, let's use V_{GS} = 15 V for the calculation. The maximum supply voltage is 30 V (it can't be higher than the maximum drain-source voltage of the P-channel transistor). The current through resistors R_3 and R_4 is 100 µA.

Resistor R_4 is:

Equation 8

$$R_4 = \frac{V_{SUPPLY-MAX} - V_{GS}}{I_{34}} = \frac{(30 - 15)}{100 \times 10^{-6}} = 150k\Omega$$

And resistor R_3 is:

Equation 9

$$R_3 = \frac{V_{GS}}{I_{34}} = \frac{15}{100 \times 10^{-6}} = 150k\Omega$$

The maximum gate threshold voltage of the P-channel transistor is $V_{GS(th)\text{-}MAX}$ = 2.5 V, therefore the P-channel transistor is securely driven for supply voltages down to:

Equation 10

$$V_{SUPPLY-MIN} = V_{GS}\frac{R_3 + R_4}{R_3} = 2.5\frac{150 \times 10^3 + 150 \times 10^3}{150 \times 10^3} = 5V$$

13 Demonstration boards, promotion tools

A complete set of demonstration/promotion tools is available for various purposes, from easy high-level application functional demonstration down to tools for detailed testing (see below). Please contact a local ST sales office for availability.

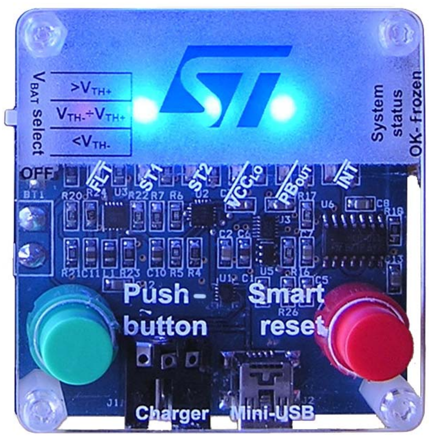
13.1 STM660x demonstration board

The board allows demonstration of the following STM660x features:

- Push-button and Smart Reset application control;
- Hardware power-down of a non-responding application;
- Undervoltage protection with safe application power-down.

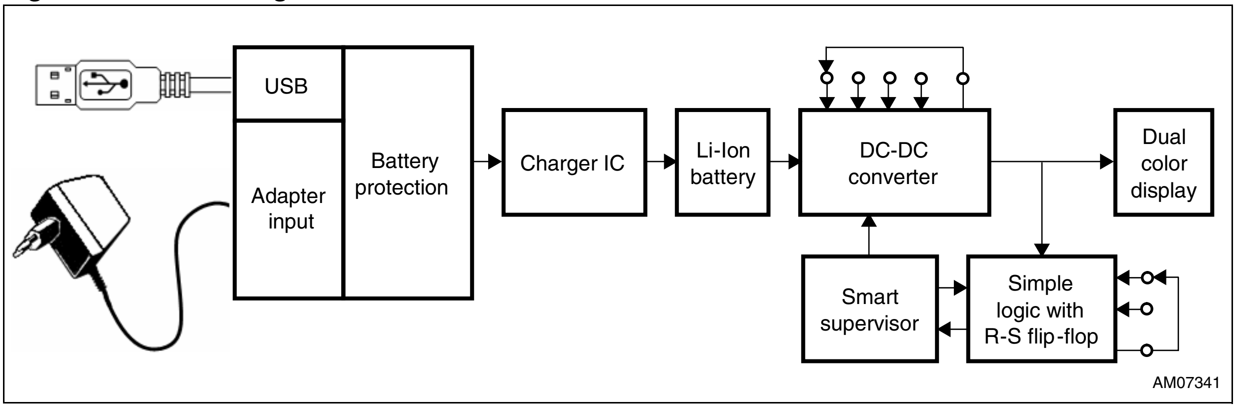
Various states can be easily simulated by push-buttons and slide switches. Operating modes are indicated by LEDs and changing the display backlight.

Figure 21. STM660x demonstration board



The demonstration board consists of battery protection provided by the STBP120, which protects the battery from undervoltage and overvoltage. The L6924D is used for proper battery charging. The STBB1 converts battery voltage based on a preset slide switch position and switching power on/off for the application. The STM660x smart supervisor controls power management based on the position of both slide switches. A dual color display indicates either proper functionality (blue backlight) or a frozen application (red backlight). See also the block diagram in *Figure 22*.

Figure 22. Block diagram of STM660x demonstration board



13.2 Interposer

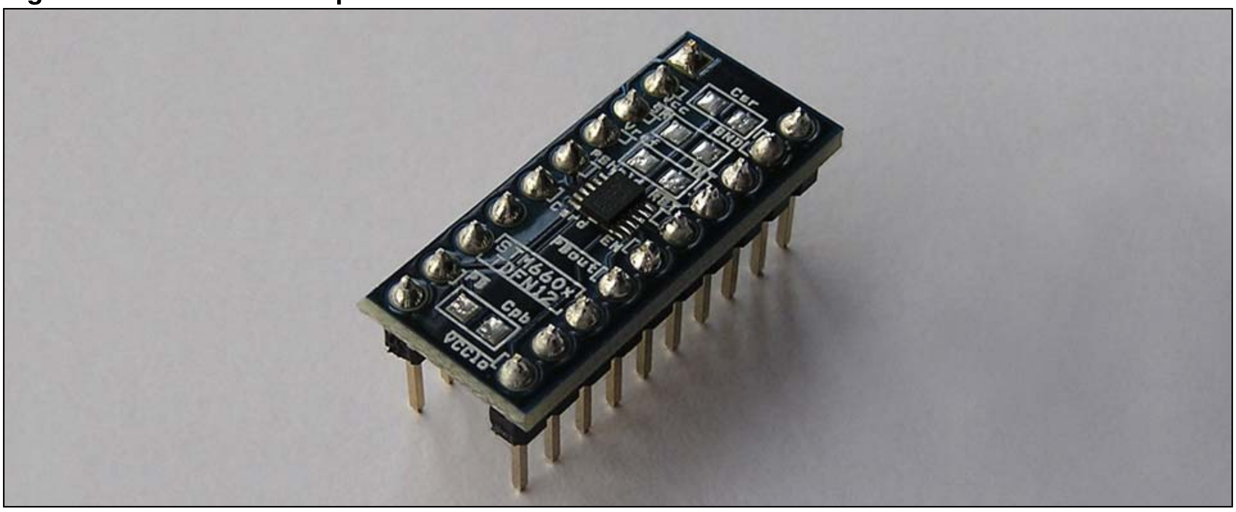
An interposer with the STM660x part can be easily plugged into a breadboard, soldered, or effectively used with an evaluation board (see below), etc.

A breadboarded interposer can be easily measured or connected to the rest of the application.

It is also much easier to solder wires to an interposer for any necessary external connection.

An interposer combined with an evaluation board provides flexibility, allowing various parts to be changed quickly in the socket.

Figure 23. STM660x interposer

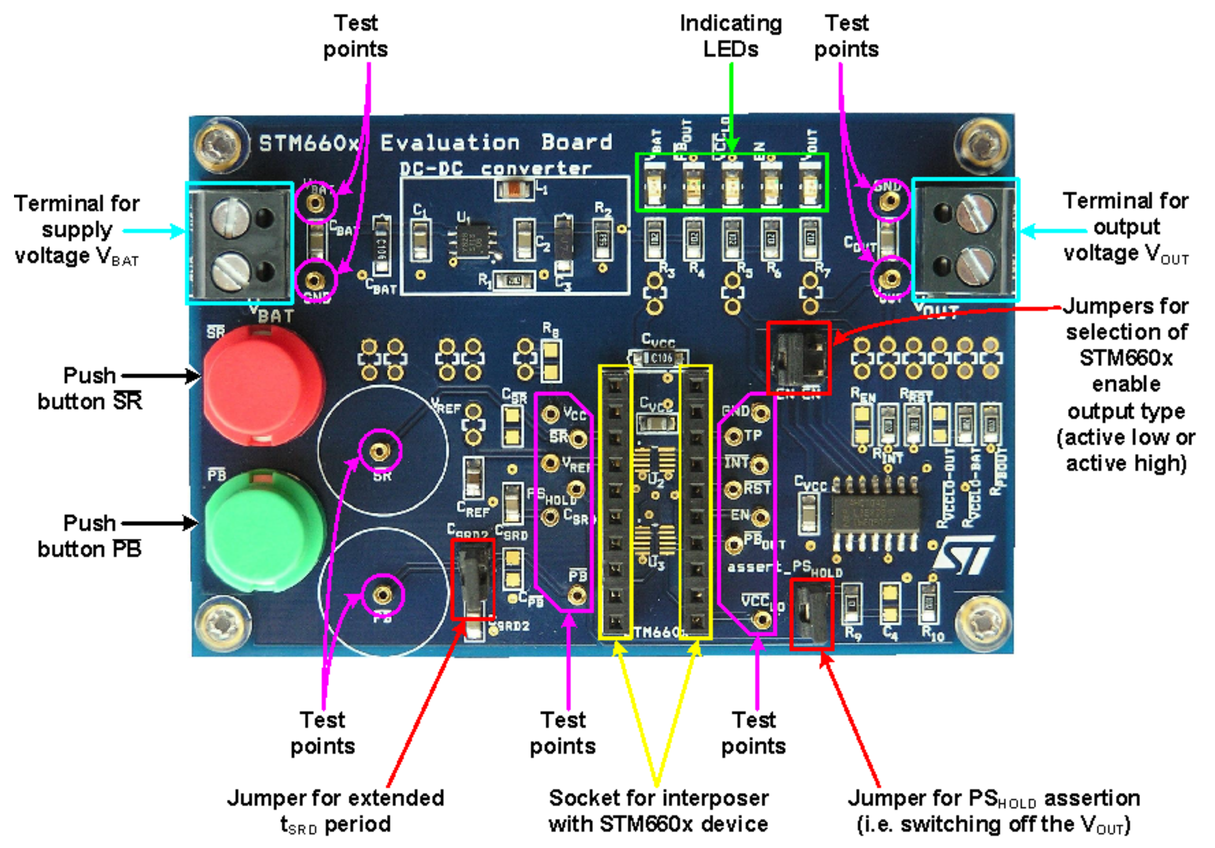


13.3 Demonstration board

The board can be connected to all of the STM660x pins through test points and has terminals for the connection of supply voltage V_{BAT} and switched output voltage V_{OUT}. Two push-buttons are used to assert the $\overline{PB}$ and $\overline{SR}$ signals and five LEDs indicate the status of V_{BAT}, $\overline{PB}_{OUT}$, $\overline{VCC}_{LO}$, EN, and V_{OUT}. Any STM660x part soldered on the interposers can be easily replaced.

Other functionalities of the board include deassertion of output voltage using jumper assert_PS_{HOLD}, selection of EN output (active low or active high), and optional adjustment of the Smart Reset delay t_{SRD} using jumper C_{SRD2}.

Figure 24. STM660x demonstration board for evaluation



14 Conclusion

The STM660x provides an easy solution for safe control of application power management and simultaneously offers adaptability to a broad spectrum of applications. It can be used in complex systems, where each step is controlled by a processor, but also as a simple connection without the need for additional parts. For easy evaluation and demonstration purposes, a variety of tools are available.

15 Links

For additional information about the STM660x, please visit the **Power Path Management web page at:** *www.st.com/powerpath* or attend our online video seminar on the same page.

16 Revision history

Table 1. Document revision history

Date	Revision	Changes
16-Dec-2010	1	Initial release.
26-Jun-2012	2	Updated *Section 6.2: Alternative single button control* and *Section 15: Links*.