AN3267
Application note

Impact of power MOSFET V_{GS} on buck converter performance

Introduction

DC-DC buck converters are widely used in the computer and peripherals industry due to their high efficiency and simple electrical topology. In synchronous buck converter design and semiconductor device choice, converter efficiency maximization and switching behavior immunity to voltage stresses and fast transients are mandatory.

This document presents the simulation and experimental test results on a single-phase synchronous buck converter, highlighting the power MOSFET gate driving voltage impact on converter power management and switching behavior. In the latest generation of microprocessors for desktops and mobile equipment, ever increasing switching frequency and output current delivered to the CPU have become necessary.

These features push converter and system designers to critical choices for overall performance optimization. In fact, fast transients, together with high load currents, may degrade the converter thermal and power management. Therefore, a deep and accurate fine tuning of the main electrical parameters is mandatory. In this document, based on the single-phase synchronous buck converter topology, the impact of different power MOSFET gate-source voltages on converter efficiency and waveforms of main circuit nodes is thoroughly analyzed through OrCAD® simulations and bench test results, highlighting a perfect match between these two experiments.

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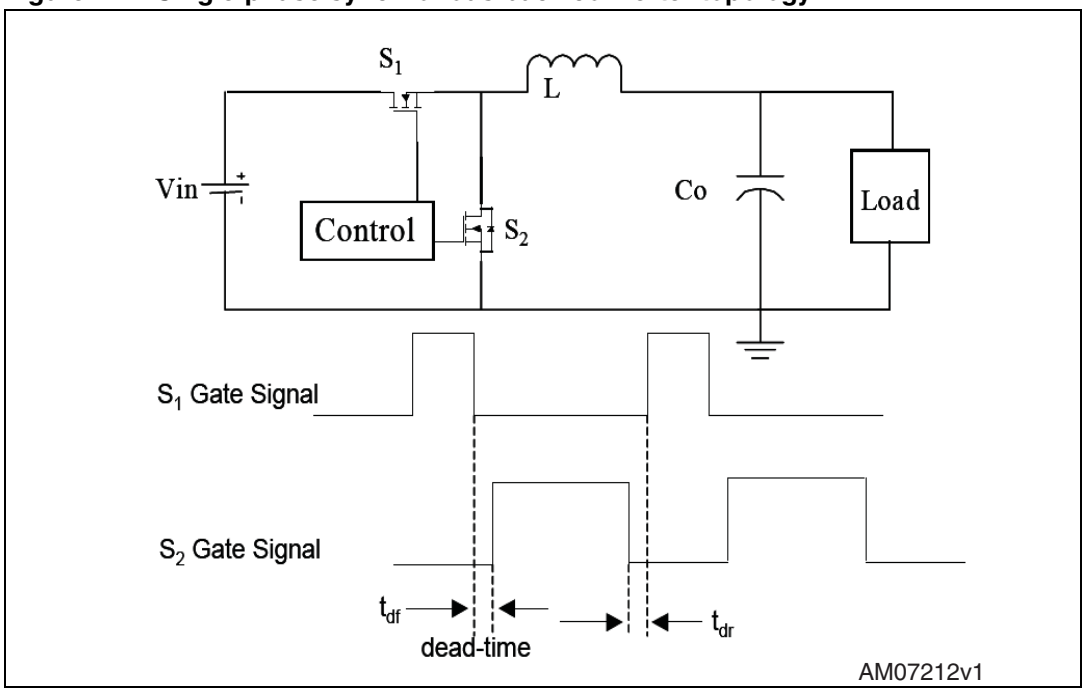
1 Synchronous buck converter basic principles

The synchronous buck converter is the most common electrical topology used for DC-DC converters which supply a CPU. In *Figure 1*, the basic schematic is depicted, where:

- S1 is the control FET (or high side FET)
- S2 is the synchronous FET (or low side FET).

In *Figure 1* it is also possible to see that the power MOSFET's gate signals are provided by the "control unit" in a synchronous way: S1 and S2 cannot be in an on-state simultaneously, avoiding the creation of a low-resistance path between the input voltage (V_{IN}) and GND (shoot-through or cross-conduction), and generating a spurious power dissipation which worsens overall efficiency.

Figure 1. Single-phase synchronous buck converter topology



L and Co form the output filter (low-pass filter), which generates a DC voltage from a square-wave signal on the low side drain (so-called phase node). The synchronous buck converter is a closed-loop topology as the output voltage is compared firstly with a reference voltage, producing an error signal; this voltage is then compared to a sawtooth signal, at the desired switching frequency (f_{sw}) (integrated in the control unit) to switch the power MOSFETs on and off. In this way, the output voltage is stable when line or load changes occur.

Together with the output voltage regulation, the control unit provides complete logic control and various protections such as overcurrent, overvoltage, undervoltage, etc.

When S1 is ON, the current in the output coil increases linearly ($dI/dt = (V_{IN}-V_{OUT})/L$ and $VL = V_{IN} - V_{OUT}$. During dead time (t_{df}), the energy store in L discharges through the body-drain diode of S2 until its gate-source signal becomes high. Therefore, the load current diverts from the body-drain diode to the channel ($V_{DS,ON} << V_{F, DIODE}$). Finally, both gate signals are low and the body-drain diode is forward-biased, allowing the load current flow.

During dead time and before HS turn-on, the LS device must remove the charge stored in the LS body-drain diode (reverse recovery charge process) before sustaining drain-source voltage. Therefore, the body-drain characteristics, in terms of reverse recovery current and charge, heavily impact the power MOSFET's switching behavior and converter power losses, especially when the converter switching frequency rises.

In a synchronous buck converter, the low side drain is subjected to fast positive/negative slopes and high voltage spikes, which can exceed the low side absolute maximum voltage, degrading power MOSFET reliability up to its failure. For this reason, the right power MOSFET choice and system configuration, placing of the device on the board and the optimization of the stray inductances and parasitic, allow important phase node spike reduction, improving converter performance.

The input-output relationship of a buck converter is given by:

Equation 1

$$V_{OUT} = DV_{IN}$$

D is the converter duty cycle, defined as the ratio between the ON time of the HS and the switching period.

2 Power MOSFET gate driving voltage requirements in real applications

In common synchronous buck converter topologies, two different solutions are widely used for the power MOSFET gate signal generation: driver and PWM logic controller integration in a single package or separately mounting the PWM logic controller and power MOSFET driver to turn the power switches on and off. The main controller suppliers provide a large number of products for both solutions.

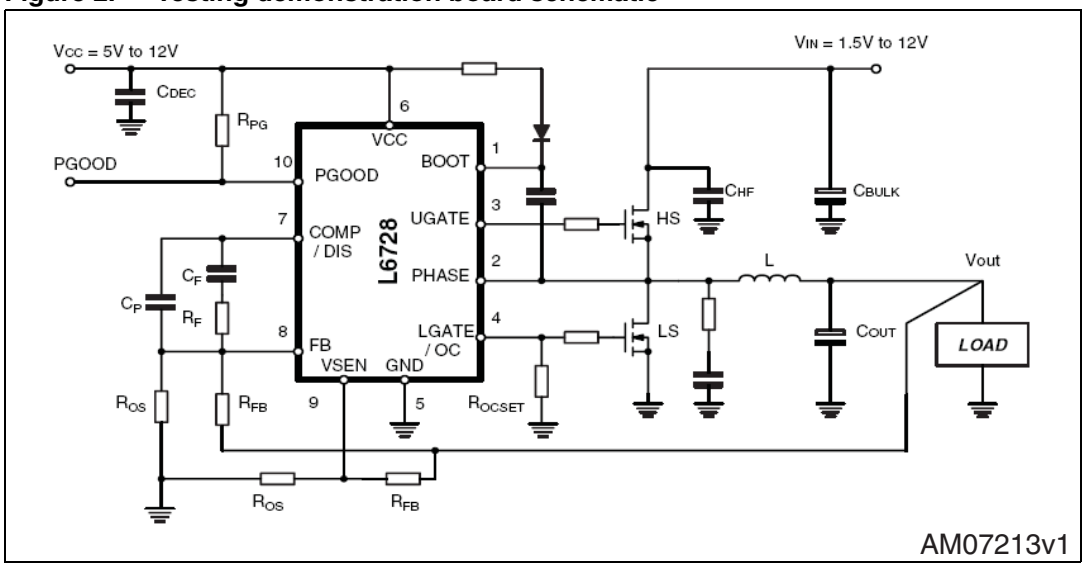
The gate-source voltages, needed to turn the high side and low side devices on and off, are generated by the driver section, formed by a common push-pull circuit. Typically, these voltages are chosen in the range of 5 V to 10 V, depending on application features: switching frequency, converter efficiency target, maximum load current, power MOSFET number and electrical characteristics, driver DC power consumption minimization, and system power limitations. Typically, desktop applications need 10 V as the power MOSFET gate driving voltage, because currents delivered to the load are high and the output voltage becomes lower and lower (up to 1 V). In these operating conditions, low side devices are in the on-state for the majority of a switching period, so the conduction losses must be minimized to improve the system power management: lower on-state losses mean lower $R_{DS(on)}$ and higher V_{GS} (up to 10-12 V).

It is the contrary in the mobile segment, 5 V power MOSFET gate-source voltage choice is due to 5 V supply rail availability (it also feeds USB and HDD sections). In fact, the input voltage, which varies from 8 V to 19 V, is not suitable for driving power MOSFETs, while other voltages in the system are lower than 3.3 V and so cannot switch the devices on and off. In this way, the power MOSFET gate driving voltage is obtained “free”, without additional active and passive components.

3 Synchronous buck converter testing demonstration board

The test vehicle is a synchronous buck converter, which lowers the input voltage (12 V) to 1.25 V as output; the converter switching frequency is 300 kHz (*Figure 2*), while the maximum output current is 20 A.

Figure 2. Testing demonstration board schematic



The power MOSFETs are driven by an L6728 single-phase PWM controller with integrated driver ($I_{HS,SRC}$ = 1.5 A, $R_{HS,SINK}$ = 1.1 Ω, $I_{LS,SRC}$ = 1.5 A, $R_{LS,SINK}$ = 0.65 Ω). The main advantage for this analysis is the availability of both the physical board and the full PSpice® model of the converter (including driver and MOSFETs). Based on the same schematic, with identical passive and semiconductor devices, it is possible to use the converter PSpice model for testing various operating conditions, validating and explaining the experimental results. Furthermore, the simulation data are very helpful to evaluate the power MOSFET currents, because on the real board they cannot be measured by current probes.

As shown in *Figure 2*, through a different external DC power supply, it is possible to provide different voltages as the input voltage (V_{IN}) and driver supply voltage (V_{CC}): adjusting V_{CC}, the impact of the power MOSFET's gate driving voltage on the converter performance is thoroughly analyzed, evaluating the power MOSFET switching behavior and thermal management. The power MOSFETs mounted on the board have the following electrical characteristics:

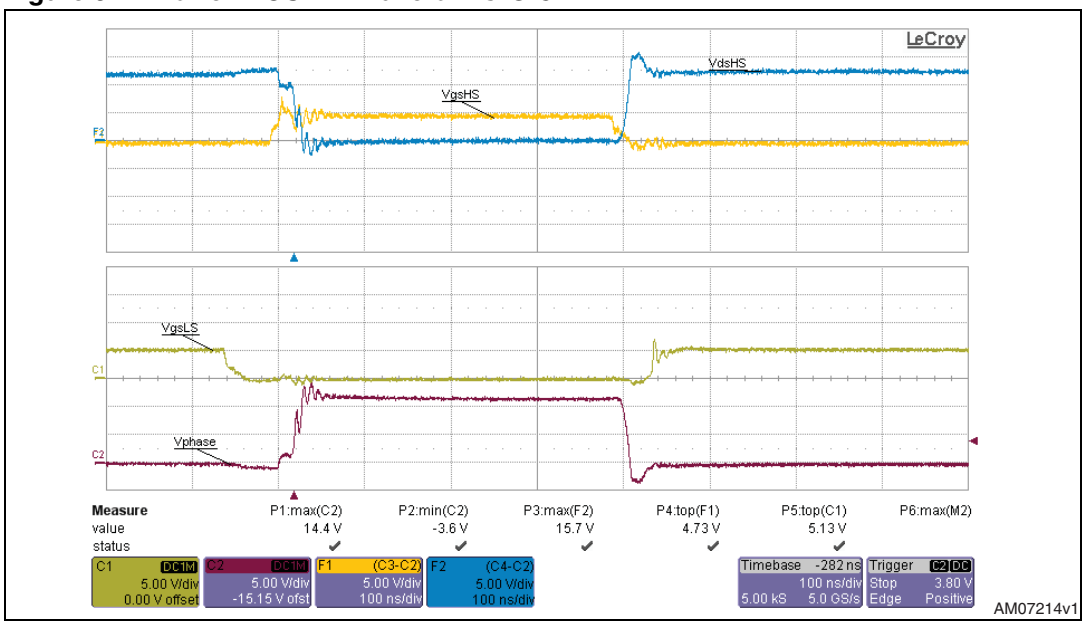
Table 1. Power MOSFET electrical characteristics

Type	BV_{DSS} @ 250 µA (V)	V_{SD} @ 25 mA (mV)	V_{th} @ 250 µA (V)	$R_{DS(on)}$ @ 10 V typ. (mΩ)	C_{iss} @ 15 V (pF)	C_{rss} @ 15 V (pF)	C_{oss} @ 15 V (pF)	R_g (Ω)
STD60N3LH5	30	N.A.	N.A.	7.3	1450	62	285	1.2
STD95N3LLH6	33.8	576	1.55	3.7	2040	271	511	1.2

3.1 HS/LS switching behavior evaluation and phase node spike measurements

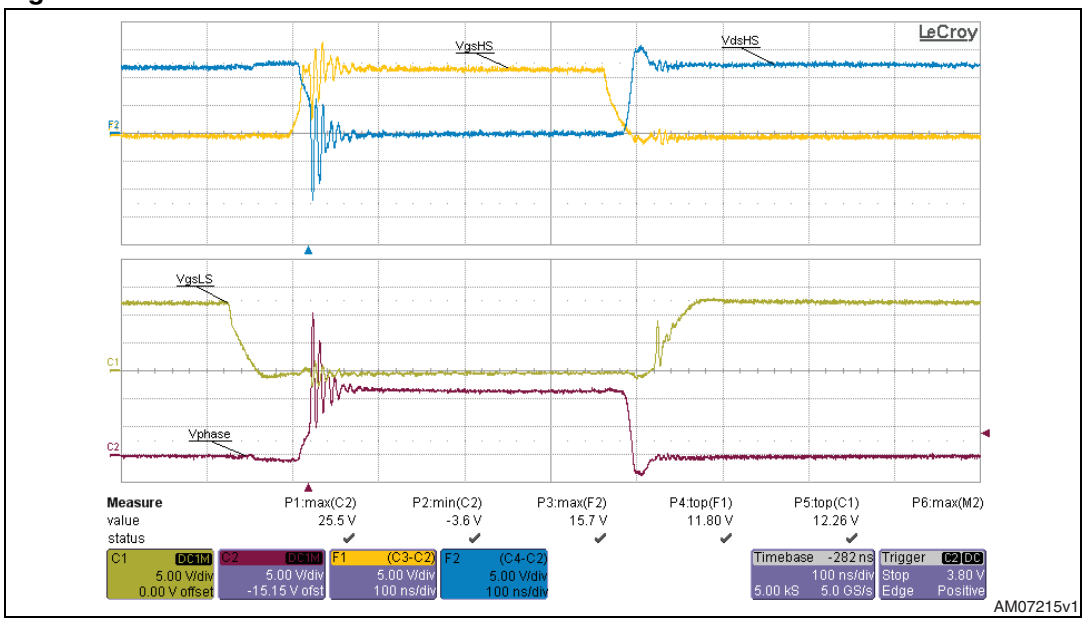
Firstly, the HS/LS switching behavior is analyzed by capturing the relevant MOSFET waveforms. The maximum output current is fixed at 20 A by an electronic DC load; the waveforms are captured at maximum load. The MOSFET gate driving voltage is adjusted at 5 V by an external DC power supply.

Figure 3. Power MOSFET waveforms @ 5 V



The blue and orange traces show HS drain-source and gate-source signals, while the yellow and purple ones are the LS waveforms. The maximum phase node spike is 14.4 V.

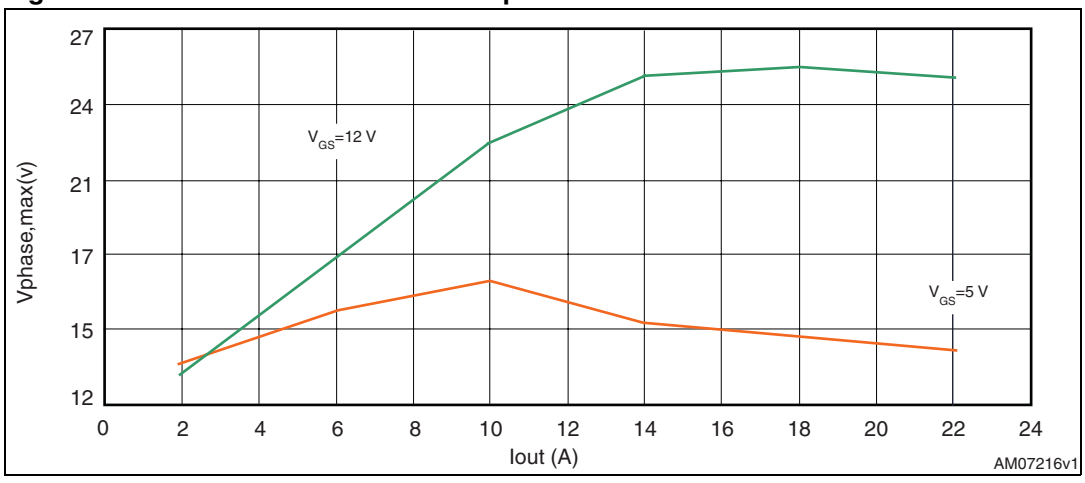
Figure 4. Power MOSFET waveforms @ 12 V



Increasing the external driver DC supply, the MOSFET's gate driving voltage rises to 12 V. The relevant waveforms are shown in *Figure 4*.

It is easy to see that the phase node spike overshoot has increased strongly, reaching 25.5 V. Obviously, the converter is working in safe mode because the power MOSFET's breakdown voltage is 30 V. Increasing the output current from 0 A to 20 A, with 4 A as step, both for V_{GS} = 5 V and V_{GS} = 12 V, it is possible to link the phase node spike overshoot to the output current, see *Figure 5*.

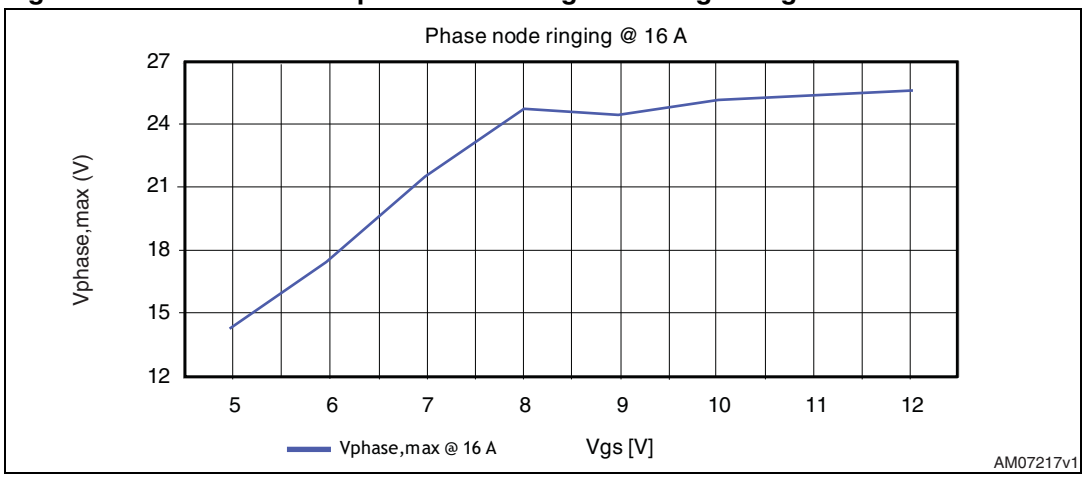
Figure 5. Phase node overshoot comparison



In the whole current range, driving the power MOSFETs at 5 V, the phase node spike is strongly reduced, with a maximum value of 16.3 V at 10 A.

By fixing the output current (i.e. 16 A) and varying the power MOSFET's gate-source voltage, the chart shown in *Figure 6* is obtained.

Figure 6. Phase node vs. power MOSFET gate driving voltage



For V_{GS} higher than 8 V, the power MOSFET gate driving impact on the phase node spike is not great, while at lower voltages the overshoot reduction is more evident. In other words, lower power MOSFET gate voltages are helpful to reduce phase node voltage stress, improving the power MOSFET reliability and robustness.

Now, the power MOSFET waveforms at two different driving voltages (5 V and 12 V) are inserted in the same chart to compare them and highlight the main differences. In *Figure 7*, the phase node waveforms are compared at the two different operating conditions, while in *Figure 8*, HS/LS G-S and phase node signals are given.

Figure 7. Phase node @ 5 V / 12 V

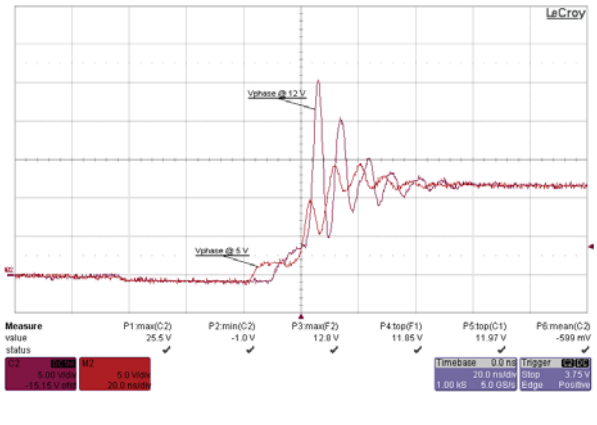
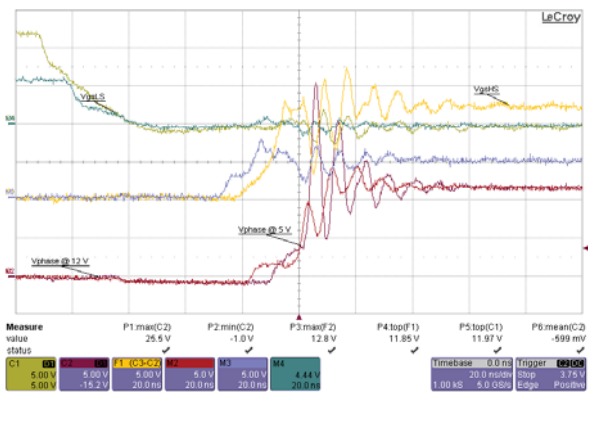


Figure 8. HS / LS signal comparison



Some relevant differences are easily observed at V_{GS} = 5 V. First, looking at the phase node signal, the “plateau” after the body diode conduction is relatively longer and the maximum spike is strongly reduced. Comparing the phase node waveforms, it seems that the LS body-drain diode is in the on-state for a shorter time, therefore the dead time has less duration (around 10 ns) and the charge stored in the body-drain diode during the reverse recovery process (Q_{rr}) decreases, reducing the voltage stress on the phase node and the reverse recovery current that adds up to the load current.

The simulation tools can validate these assertions on phase node spike minimization at lower gate driving voltage. Two different simulations are performed by the full OrCAD model

of the testing board. The only changing parameter is the driver supply voltage, 5 V and 12 V. In *Figure 9* and *10*, the waveforms at HS turn-on for both operating conditions are shown.

Figure 9. HS turn-on waveform @ 12 V

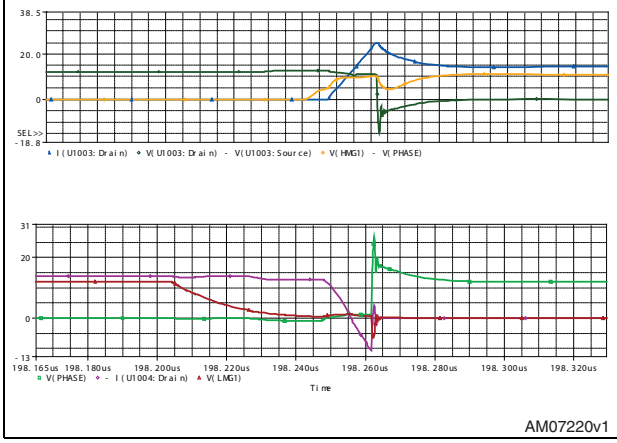
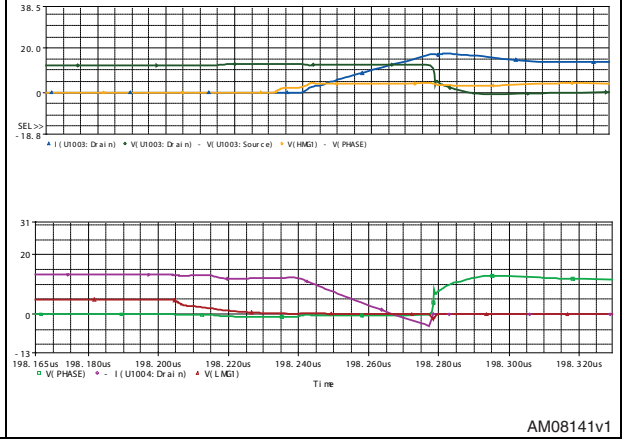


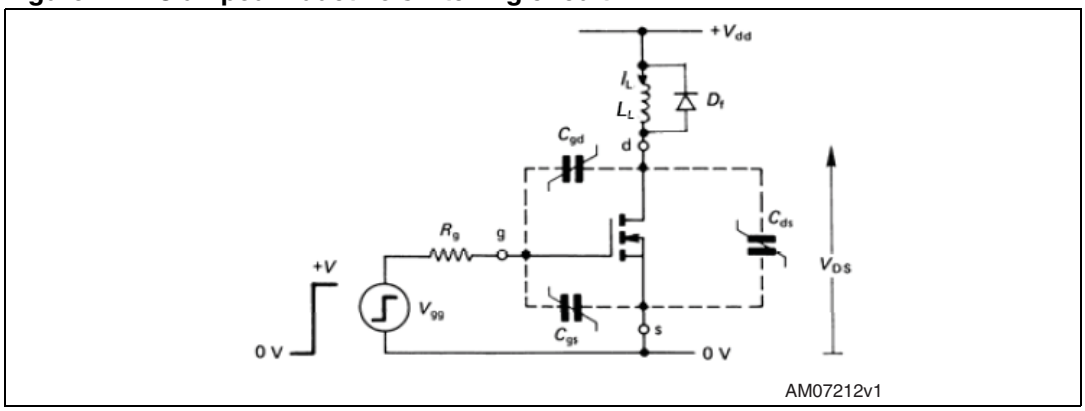
Figure 10. HS turn-on waveform @ 5 V



With OrCAD simulations, the principle advantage is the availability of the current waveforms. It is clear that all the values provided by these simulations are not exact due to real device-PSpice model mismatch.

During the HS turn-on process (*Figure 9* and *10*, HS V_{GS} and I_D are shown in orange and blue traces, respectively), the inductive load can be modeled as a constant DC current (I_L, load current) in parallel with the LS body-drain diode. The equivalent circuit is, therefore, a classic clamped power switching circuit (*Figure 9*).

Figure 11. Clamped inductive switching circuit



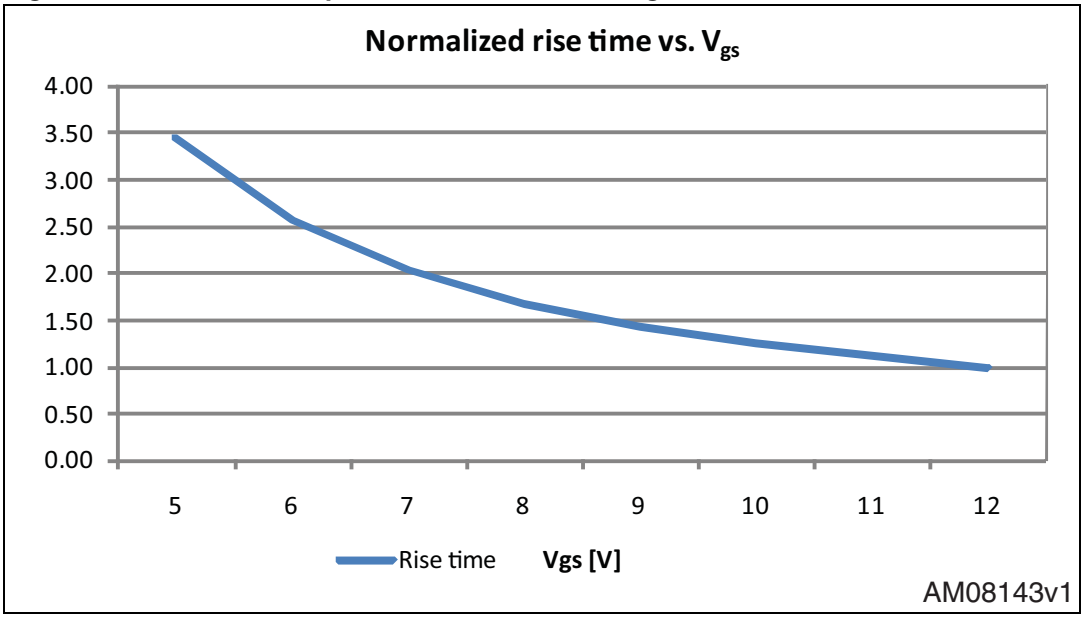
The drain current rise time, neglecting the parasitic effects caused by the stray inductances, is given by *Equation 2:*

Equation 2

$$t_{ri} = R_G \cdot C_{ISS} \cdot \ln\left(\frac{g_{fs} \cdot (V_{GG} - V_{TH})}{g_{fs} \cdot (V_{GG} - V_{TH}) - I_L}\right)$$

Varying the gate drive voltage from 5 V to 12 V, using typical power MOSFET electrical parameters, the normalized power MOSFET rise time is linked to the V_{GS} (*Figure 12*):

Figure 12. Rise time vs. power MOSFET G-S voltage



Driving the power MOSFET at a lower gate voltage, the device switching speed is appreciably reduced, while the drain current slope, in HS and LS, becomes less steep, as clearly shown in *Figure 9* and *10*. Focusing on the LS device, the current slope ($dI_{D,LS}/dt$) decrease causes reverse recovery time (t_{rr}) enlarging and a far more marked reduction of maximum reverse recovery current (I_{rrm}). The body-drain diode reverse recovery charge (Q_{rr}) is given, with good approximation, by:

Equation 3

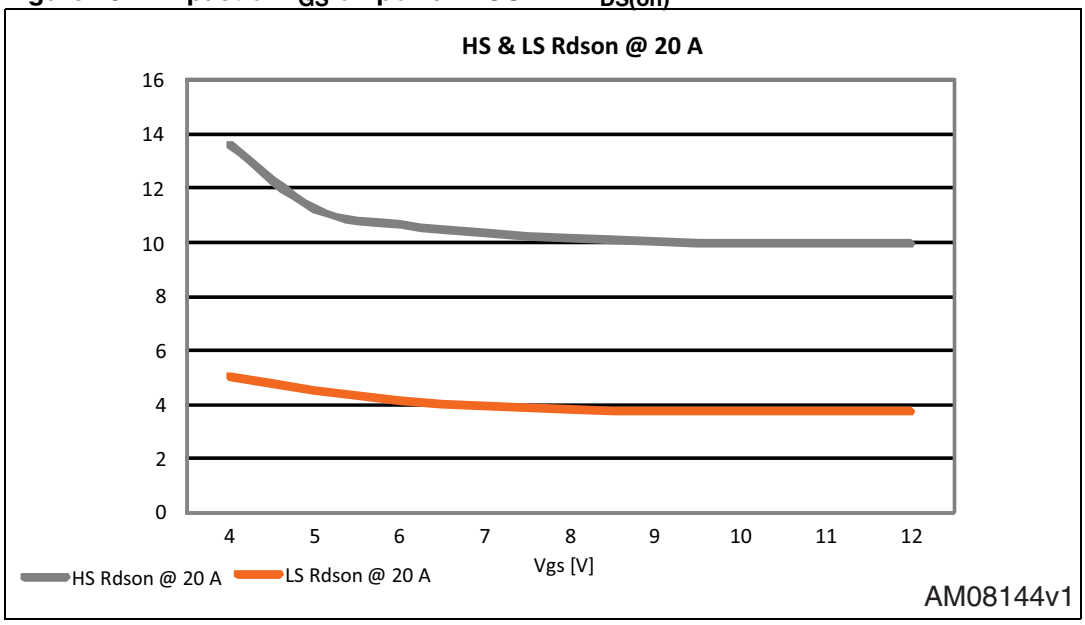
$$Q_{rr} \cong 0.5 \cdot t_{rr} \cdot I_{rrm}$$

Q_{rr} values are 20.9 nC (V_{GS} = 5 V) and 34 nC (V_{GS} = 12 V). The stored charge to be removed before body diode off-state decreases with the power MOSFET gate drive voltage; as a consequence, the current stress on the HS device and the phase node spike become less critical. Referring to *Figure 9* and *10*, with V_{GS} = 12 V, $V_{PHASE,MAX}$ is 27.1 V whereas, it is 14.5 with V_{GS} = 5 V.

3.2 Converter efficiency calculation

The impact of the power MOSFET gate driving voltage on the converter efficiency is analyzed in this section. As already known, the gate-source voltage controls the power MOSFET channel, so by increasing the power MOSFET's V_{GS}, the possible drain current is higher with a lower $R_{DS(on)}$. In other words, driving the power MOSFET gate in the range of 10-12 V optimizes device behavior and efficiency at high currents. In *Figure 13*, for the devices mounted on the board, the $R_{DS(on)}$ values at different V_{GS} are shown.

Figure 13. Impact of V_{GS} on power MOSFET $R_{DS(on)}$



At V_{GS} = 5 V, the HS and LS on-state resistances are respectively 11.2 mΩ and 4.5 mΩ Increasing gate-source voltage up to 12 V, the relative $R_{DS(on)}$ is 9.9 mΩ and 3.7 mΩ; $R_{DS(on}$ improvements with higher V_{GS} are in the range of [10% - 20%]. Therefore, the conduction (on-state) losses, for the LS device, are given by the following formula:

Equation 4

$$P_{COND,\ LS} = (1 - D) \cdot R_{DS(on)}(T) \cdot I_{D,}{}^{2}{}_{L}$$

The higher the V_{GS}, the lower the LS conduction losses, maximizing converter efficiency. For low D values (in this case, $D = V_{OUT}/V_{IN} = 1.25/12 = 10.4\%$), this power loss is the most relevant for the whole converter. Higher V_{GS} values also reduce HS conduction losses, given by:

Equation 5

$$P_{COND,\ HS} = D \cdot R_{DS(on)}(T) \cdot I_{D,\ HS}^{2}$$

Even though this contribution is less important, due to low D values.

Another two power loss contributions linked to the power MOSFET gate-source voltage are the gate drive power losses (P_{GATE}) and the HS switching losses. The first are given by:

Equation 6

$$P_{GATE} = N_{FET} \cdot Q_g \cdot V_{GG} \cdot f_{sw}$$

where:

- N_{FET} is the power MOSFET paralleled number (in HS or LS position)
- Q_g is the total gate charge
- V_{GG} is the power MOSFET gate driving voltage
- f_{sw} is the switching frequency.

The HS switching losses are:

Equation 7

$$P_{SW,HS} = \frac{1}{2} \cdot (Q_{GS2} + Q_{GD}) \cdot \left(\frac{R_{TOT,P-UP}}{V_{CCDRV} - V_{PLAT}} + \frac{R_{TOT,P-DW}}{V_{PLAT}} \right) \cdot V_{IN} \cdot I_{OUT} \cdot f_{SW}$$

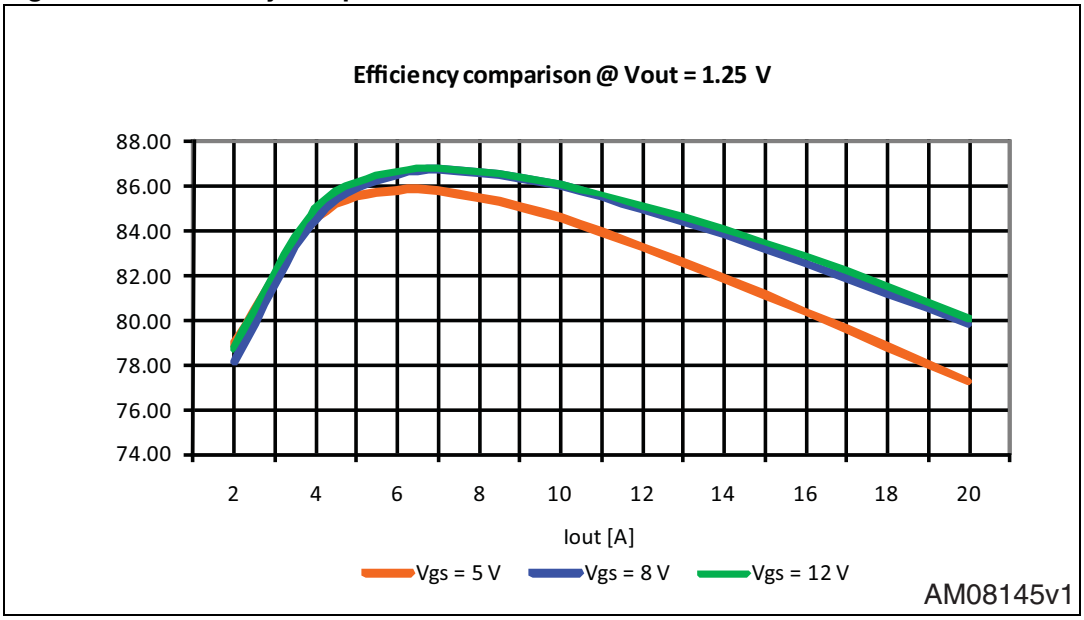
where:

- Q_{GS2} and Q_{GD} are the gate-source after the threshold and gate-drain charges
- $R_{TOT,P-UP}$ and $R_{TOT,P-DW}$ the total HS gate resistance at turn-on and turn-off
- V_{PLAT} the plateau voltage.

Driving the power MOSFETs at 5 V, the gate charge needed to switch the devices on and off is lower, causing a reduction in P_{GATE}. Obviously, at low switching frequency this benefit is not significant, but becomes important in high frequency converters.

However, the lower the V_{CCDRV} is (and therefore HS $V_{GS)}$, the higher the $P_{SW,HS}$ is.

Figure 14. Efficiency comparison



Now, the converter efficiency at three different power MOSFET gate-source voltages (5 V, 8 V, and 12 V) is calculated, stepping up the load current from 0 to 20 A without airflow. The curves are shown in *Figure 14*.

Regarding *Figure 14*, at low currents the curves are very similar, due to the balance of the above mentioned loss contributions. Therefore, the V_{GS} impact is not evident at light load. At full load, the gap between 12 V and 5 V curves is conspicuous (2.8% at 20 A), whereas 8 V and 12 V are very similar both at low and high currents. In fact, according to *Figure 11*, $R_{DS(on)}$ curve enters "flat zone" for V_{GS} higher than 8 V; consequently, there are no strong variations in the conduction losses or major power losses at full load.

Finally, device temperature at 80% (16 A) of maximum load is measured, after the converter reaches the thermal equilibrium (around 15-20 min), without airflow. In *Figure 15*, a thermal photo captured by a thermo-camera is depicted. In *Table 2*, the temperature values for the power MOSFET's driver and output coil are shown. At V_{GS} = 5 V, the power MOSFET's, driver and output coil have the hottest temperatures, due to higher losses, while the other two drive conditions show similar values.

Figure 15. Thermal capture @ 16 A

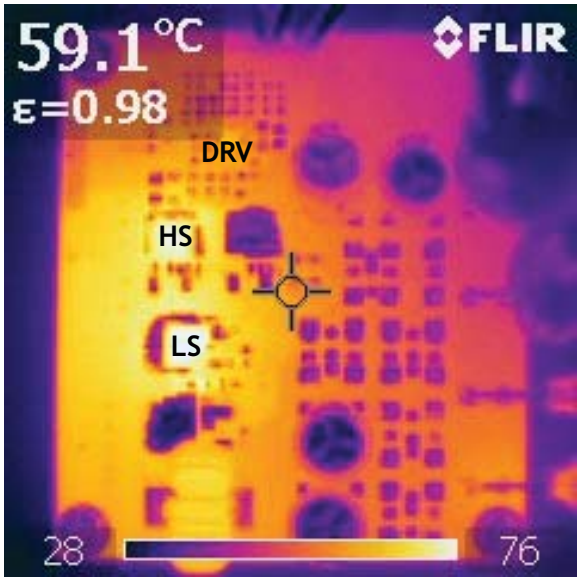


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Table 2. Temperature measurements @ 16 A

	T_{HS} (°C)	T_{coil} (°C)	T_{LS} (°C)	T_{DRV} (°C)
V_{GS} = 5 V	87.9	69.1	85.2	60.8
V_{GS} = 8 V	77.3	67.1	79	61.4
V_{GS} = 12 V	75.5	66.3	77.9	61.9

4 Conclusions

Through bench tests and OrCAD simulations, the impact of the power MOSFET gate drive voltage on device and converter performance has been thoroughly analyzed. In particular, the MOSFET immunity to high voltage stress on the phase node is higher at low V_{GS} values (i.e. 5 V). Slowing down the power MOSFET switching speed, the body diode reverse recovery process is less critical in these operating conditions. On the contrary, the higher the V_{GS} the bigger the reverse recovery charge, causing higher spike on the phase node.

However, when lower voltages are applied to the power MOSFET gate, some power loss contributions (gate drive, conduction, HS switching losses, etc.) increase, worsening the overall efficiency. Therefore, the power MOSFET and converter power and thermal management is optimized at high V_{GS} (typically, higher than 8 V), because of the power MOSFET conduction losses minimization at heavy load conditions.

The right V_{GS} choice, according to overall system requirements, allows a good trade-off between phase node spike reduction and efficiency improvement to be reached.

The OrCAD simulations provide a useful tool for understanding and validating the experimental results. Please consider that the devices' PSpice models are quite accurate but not precise, so a mismatch with the experimental results is understandable.

5 References

1. AN-6005 - Synchronous buck converter losses calculations with Excel model, J. Klein, Fairchild Semiconductor, 2006
2. L6728 datasheet, STMicroelectronics
3. Power Electronics Handbook, Muhammad H. Rashid, 2001

6 Revision history

Table 3. Document revision history

Date	Revision	Changes
25-Aug-2011	1	Initial release.