AN3115
Application note

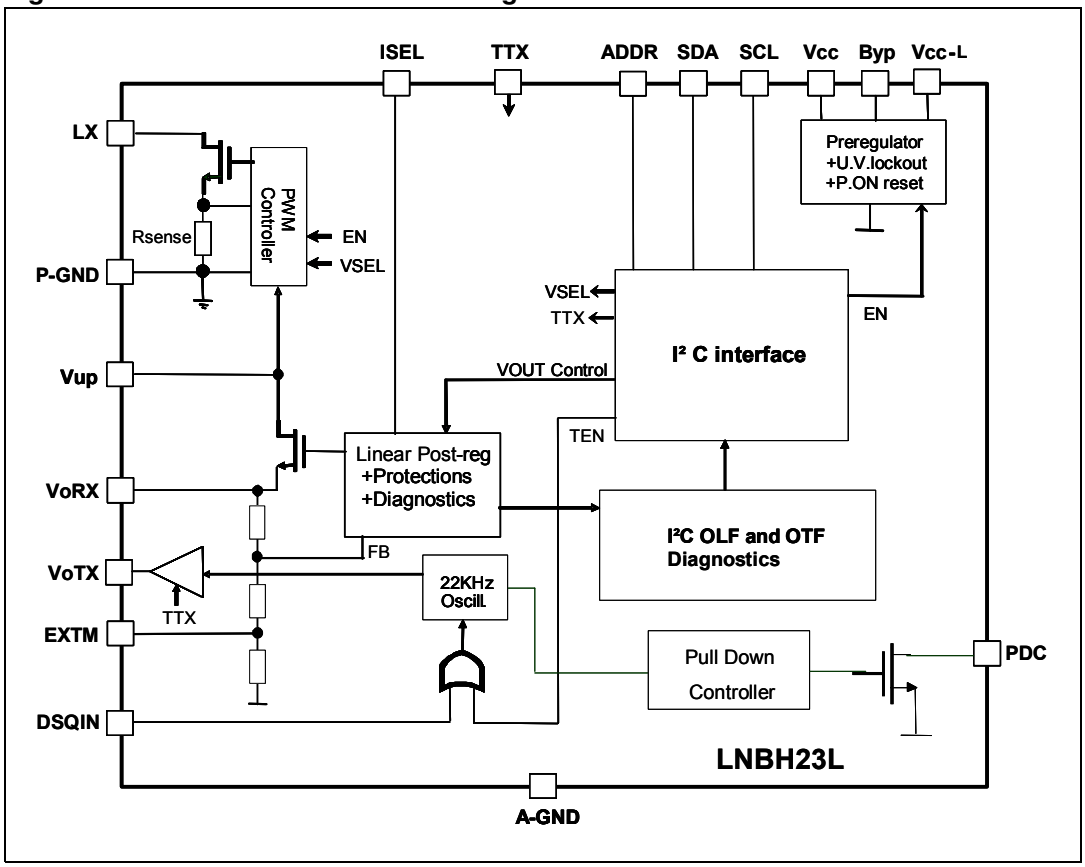
LNB power supply based on the LNBH23L supply and control IC with step-up and I²C interface

Introduction

This application note is intended to provide additional information and suggestions for the correct use of the LNBH23L device. All waveforms shown are based on the demonstration board order code STEVAL-CBL007V1 described in *Section 3*.

The LNBH23L is an integrated solution for supplying/interfacing satellite LNB modules. It gives good performance in a simple and cheap way, with minimum external components necessary. It includes all functions needed for LNB supplying and interfacing, in accordance with international standards. Moreover, it includes an I²C bus interface and, thanks to a fully integrated step-up DC-DC converter, it functions with a single input voltage supply ranging from 8 V to 15 V.

Figure 1. LNBH23L internal block diagram



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1 Block diagram and pin function description

The internal blocks of the LNBH23L are described in the following paragraphs:

1.1 Step-up controller

The LNBH23L features a built-in step-up DC-DC converter that, from a single supply source ranging from 8 V to 15 V, generates the voltages that allow the linear post-regulator to work with minimum power dissipation. The external components of the DC-DC converter are connected to the L_X and V_{UP} pins (see *Figure 6*). No external power MOSFET is needed.

1.2 Pre-regulator block

This block includes a voltage reference connected to the BYP pin, an undervoltage lockout circuit, intended to disable the whole circuit when the supplied V_{CC} drops below a fixed threshold (6.7 V typ), and a power-on reset that sets all the I²C registers to zero when the V_{CC} is turned on and rises from zero above the “on” threshold (7.3 V typ).

1.3 I²C interface and diagnostic

The main functions of the device are controlled via the I²C bus by writing 5 bits on the system register (SR bits in write mode). In the same register there are 5 bits that can be read back (SR bits in read mode) and provide 2 diagnostic functions, whereas the other 3 bits are for internal usage (TEST1, TEST2, and TEST3).
Two bits report the diagnostic status of the two internal monitoring functions:

- OTF: over temperature flag. If an overheating occurs (junction temperature exceeds 150 °C), the OTF I²C bit is set to “1”.
- OLF: overload flag. If the output current required exceeds the current limit threshold or a short circuit occurs, the OLF I²C bit is set to “1”.

Moreover, three bits report the last output voltage register status (EN, VSEL, LLC) received by the I²C. The LNBH23L I²C interface address can be selected from two different addresses by setting the voltage level of the dedicated ADDR pin according to *Table 1*:

Table 1. LNBH23L I²C addresses

Pin Set-up	Write (HEX)	Read (HEX)
ADDR=Low or floating	0x14	0x15
ADDR=High	0x16	0x17

1.3.1 Reserved I²C address

The device has another I²C address reserved only for internal usage, see *Table 2*.

Table 2. LNBH23L other I²C addresses

Pin Set-up	Write (HEX)	Read (HEX)
ADDR=Low/High or floating	0x10	0x11

1.4 DiSEqC™ 1.X implementation through EXTM pin

The EXTM pin is an analog input to generate the 22 kHz tone superimposed to the V_{oRX} DC output voltage. If the EXTM pin is used, the internal 22 kHz generator must be kept OFF (TTX pin or TTX bit set LOW). A cheaper circuit must be used to couple the modulating signal source to the EXTM pin (see *Figure 2*).

The EXTM pin modulates the V_{oRX} voltage through the series decoupling capacitor, so that:

V_{oRX} (AC) = V_{EXTM} (AC) x G_{EXTM}

Where:

- V_{oRX} (AC) and V_{EXTM} (AC) are, respectively, the peak to peak voltage on the V_{oRX} and EXTM pin

- G_{EXTM} is the voltage gain from EXTM to V_{oRX}.

In order to avoid the 22 kHz tone distortion, a dummy output load may be necessary, strictly dependent on the output bus capacitance.

Table 3. Output load

Output bus capacitance	Output load
< 50 nF	10 mA
250 nF (EUTELSAT spec.)	30 mA
750 nF (DIRECT TV spec.)	80 mA

For the correct DiSEqC implementation, during tone transmission, it is most important that the DiSEqC_out pin of the 22 kHz IC controller, is set in low impedance and vice versa, during no-tone transmission, it must be set in high impedance.

Figure 2 shows an example circuit as an appropriate solution with a 22 kHz IC controller to drive the EXTM pin for the DiSEqC implementation.

Figure 2. EXTM example of use with 22 kHz IC controller

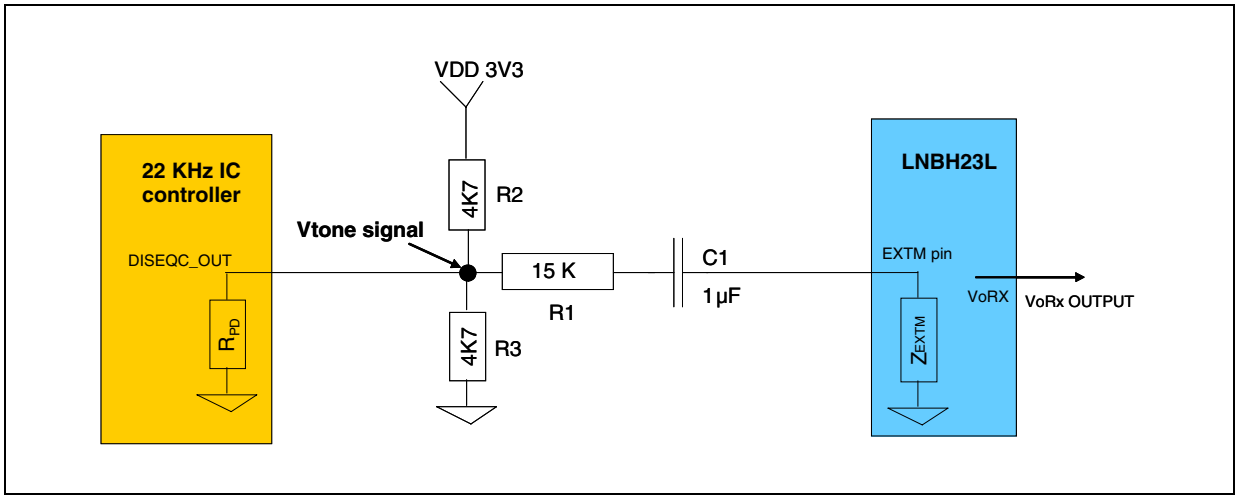
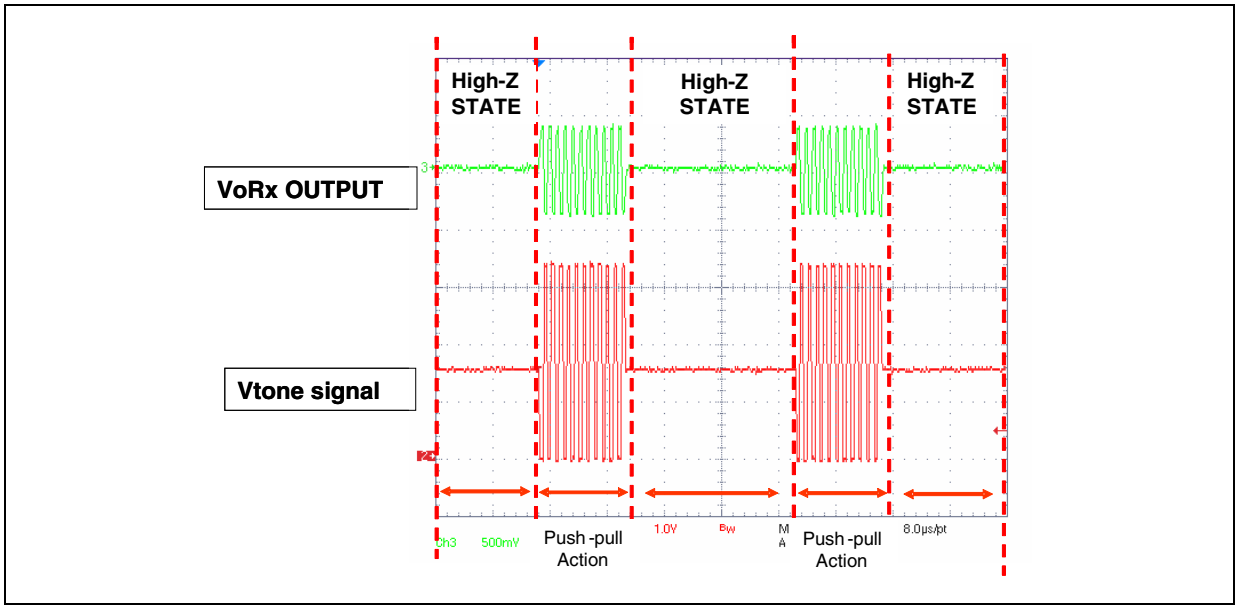


Figure 3. DiSEqC 1.X tone burst with 22 kHz IC controller



1.5 DiSEqC 1.X Implementation through V_{oTX} and EXTM

If an external 22 kHz tone source is not available, it is possible to use the internal 22 kHz tone generator signal available through the V_{oTX} pin to drive the EXTM pin. In this way the V_{oTX} 22 kHz signal is superimposed to the V_{oRX} DC voltage to generate the LNB output 22 kHz tone (see *Figure 6*). The internal 22 kHz tone generator, available through the V_{oTX} pin, must be activated during the 22 kHz transmission by the DSQIN pin or by the TEN bit. The DSQIN internal circuit activates the 22 kHz tone on the V_{oTX} output with 0.5 cycles ± 25 µs delay from the TTL signal present on the DSQIN pin, and it stops with 1 cycle ± 25 µs delay after the TTL signal is expired. The V_{oTX} pin internal circuit must be preventively set ON by the TTX function. This can be controlled both through the TTX pin and the I²C bit. As soon as the tone transmission is expired, the V_{oTX} must be disabled by setting the TTX to LOW. The 13 / 18 V power supply is always provided to the LNB from the V_{oRX} pin.

1.6 PDC optional circuit for DiSEqC 1.X applications using V_{oTX} signal on to EXTM pin and 22 kHz tone controlled by DSQIN pin

In some applications, at light output current (< 50 mA) having a heavy LNB output capacitive load, the 22 kHz tone can be distorted. In this case it is possible to add the “Optional” external components described on *Section 2.7*.

1.7 22 kHz oscillator

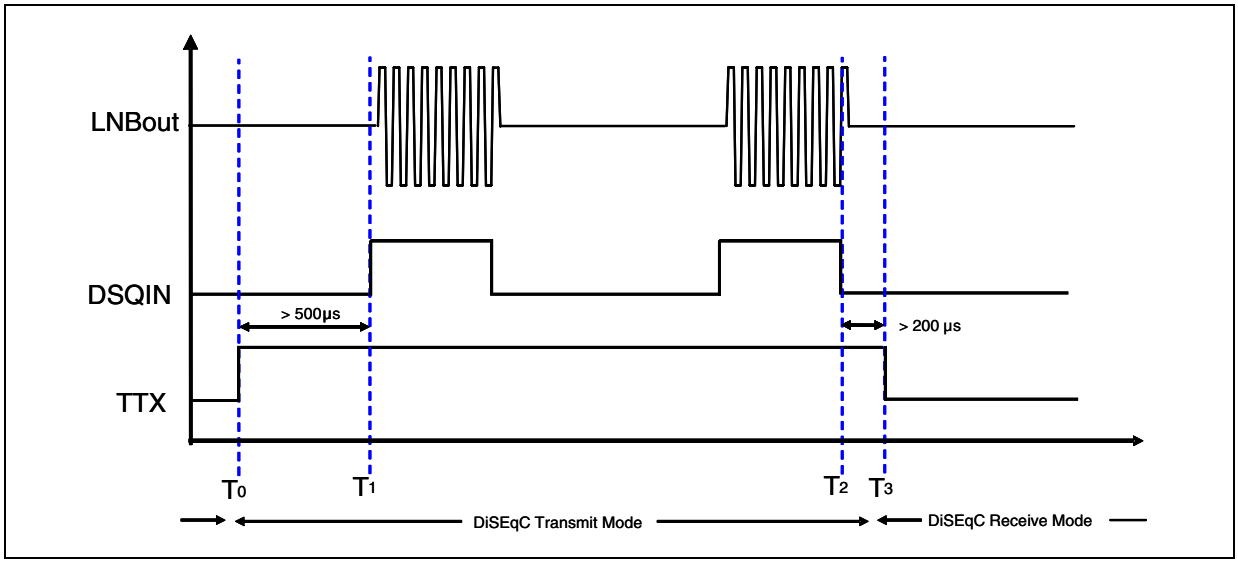
The internal 22 kHz tone generator is factory-trimmed in accordance with current standards and can be selected by the I²C interface TTX bit (or TTX pin) and controlled by the DSQIN pin (TTL compatible), which allows immediate DiSEqC data encoding. If the 22 kHz tone presence is requested in continuous mode, the internal oscillator can be activated by the I²C

interface TEN bit. The rise and fall edges are controlled to be in the 5 µs to 15 µs range, 8 µs typ for 22 kHz. The Duty cycle is 50 % typ., it modulates the DC output with a 0.650 V_{PP} (typ.) amplitude as well as the DSQIN pin.

1.8 DiSEqC communication

The following steps must be taken to ensure the correct implementation of the DiSEqC communication:

Figure 4. DiSEqC timing control



- T0: Before starting the DiSEqC transmission. The TTX function must be activated (through the TTX pin or TTX I²C bit);
- T1: After 500 µs minimum, the IC is ready to receive the DiSEqC code through the DSQIN pin (or, alternatively, the TEN I²C bit can be set to HIGH to activate the 22 kHz burst);
- T2: When the transmission is elapsed, the TTX function is set to LOW (through the TTX pin or TTX I²C bit) not earlier than 200 µsec after the last falling edge of the DiSEqC code.

1.9 Linear post-regulator, modulator and protection

The output voltage selection and the current selection commands join this block, which manages the LNB output function. This block gives feedback to the I²C interface from the diagnostic block, regarding the status of the thermal protection, over current protection, and output settings.

1.10 Pin description

The LNBH23L is available in an exposed pad QFN-32 package for surface mount assembly. *Figure 5* shows the device pin-out and *Table 4* briefly summarizes the pin function.

Figure 5. LNBH23L pin configuration

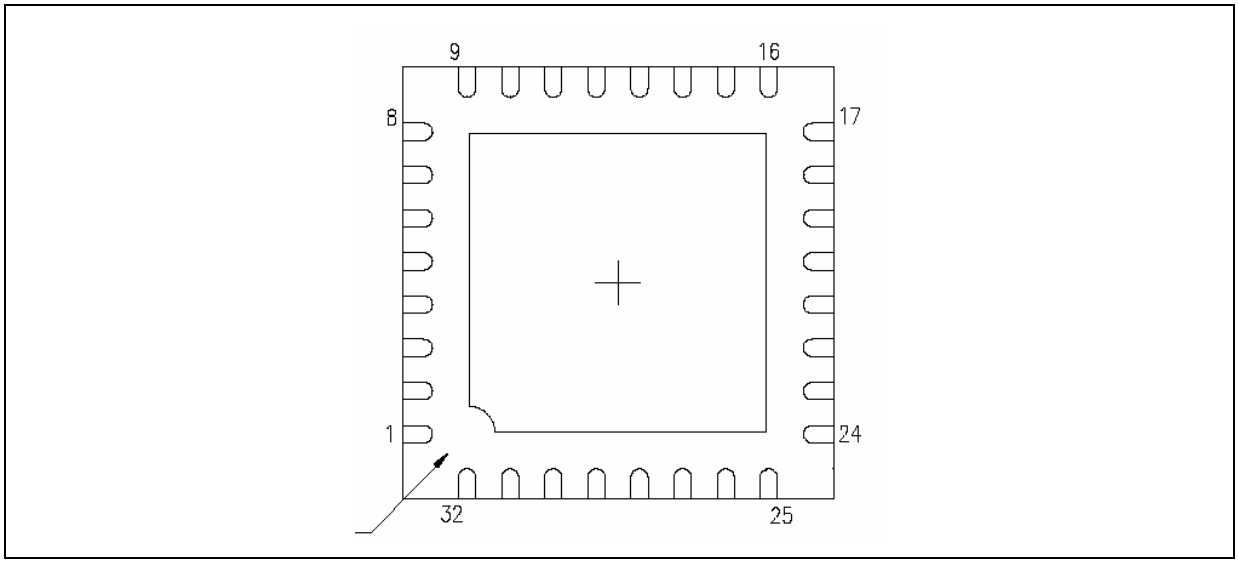


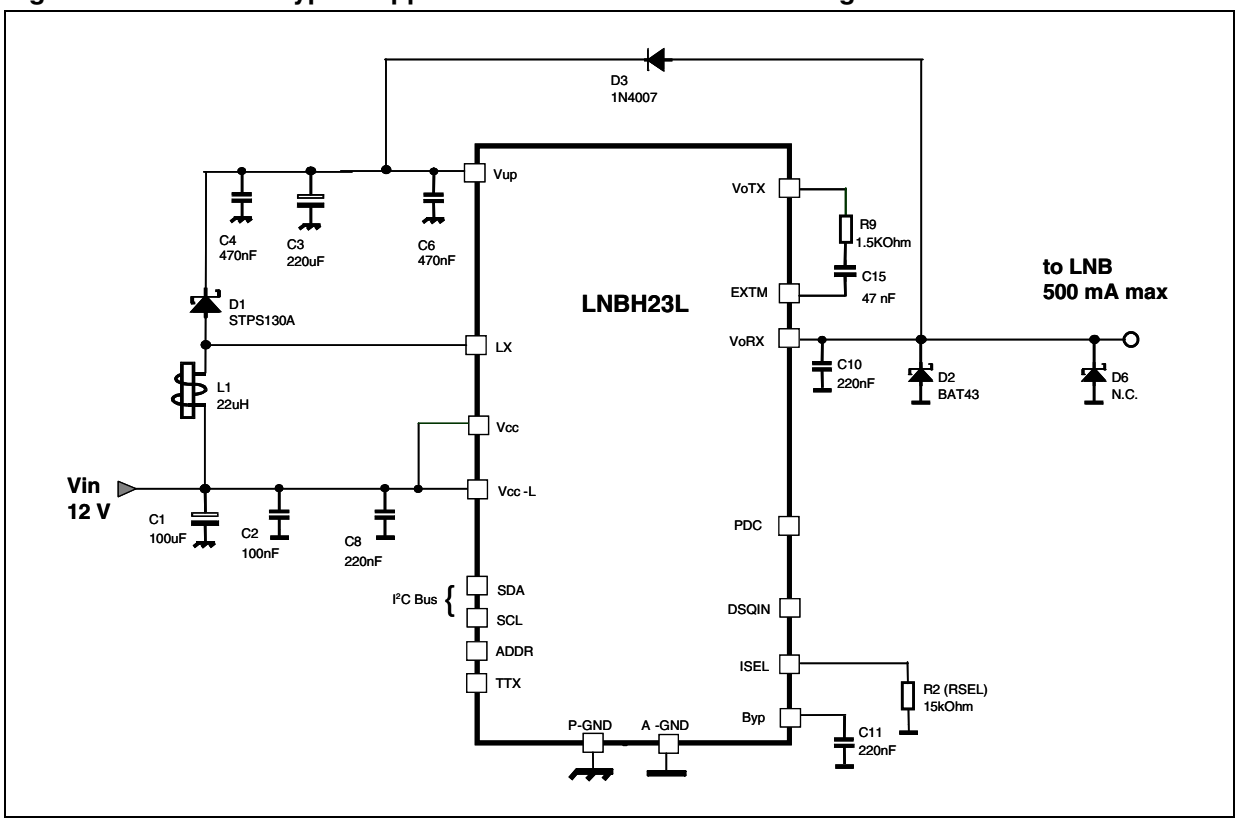
Table 4. LNBH23L pin description

QFN 5x5 pin n°	Symbol	Name	Pin function
19	V_{CC}	Supply input	8 to 15 V IC DC-DC power supply
18	V_{CC}_L	Supply input	8 to 15 V analog power supply
4	LX	NMos drain	Integrated N-channel Power MOSFET Drain
27	V_{UP}	Step-up voltage	Input of the linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor.
21	V_{oRX}	LDO output port	Output of the linear post-regulator
22	V_{oTX}	Output port during 22 kHz tone TX	TX Output to the LNB
6	SDA	Serial data	Bi-directional data from/to the I²C bus
9	SCL	Serial clock	Clock from the I²C bus
12	DSQIN	DiSEqC input	This pin accepts the DiSEqC code from the main microcontroller. The LNBH23L uses this code to modulate the internally-generated 22 kHz carrier. Set this pin to ground if not used.
14	TTX	TTX enable	This pin, as well as the TTX I²C bit of the system register, is used to control the TTX function enable before starting the 22 kHz tone transmission. Set this pin floating or to GND if not used.
29	Reserved	Reserved	To be connected to GND
11	PDC	Pull-down control	To be connected to the external NPN transistor base to reduce the 22 kHz tone distortion in case of heavy capacitive load at light output current. If not used it can be left floating.
13	EXTM	External modulation	External Modulation Input acts on V_{oRX} linear regulator output to superimpose an external 22 kHz signal. Needs DC decoupling to the AC source. If not used it can be left floating.
5	P-GND	Power ground	DC-DC converter power ground to be connected directly below the ePad of the PCB top GND layer.
ePad	ePad	ePad	On the bottom side of the QFN-32 package. It must be connected with power ground and to the ground layer through vias to dissipate heat.
20	A-GND	Analog ground	Analog circuits ground
15	BYP	Bypass capacitor	Needed for internal preregulator filtering. The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to an external current or voltage sources may cause permanent damage to the device.
10	ADDR	Address setting	Two I²C bus addresses available by setting the ADDR pin voltage level.
28	ISEL	Current selection	The resistor RSEL connected between ISEL and GND defines the linear regulator current limit threshold by the equation: I_{MAX} (typ.)=10000/ RSEL.
30	Reserved	Reserved	To be left floating. Do not connect to GND
1, 2, 3, 7, 8, 16, 17, 23, 24, 25, 26, 31, 32	N.C.	Not connected	Not internally connected pins

2 Component selection guidelines

The LNBH23L application schematic in *Figure 6* shows the typical configuration for a single LNB power supply.

Figure 6. LNBH23L typical application circuit with internal tone generator



Note: TVS D6 diode to be used if surge protection is required (see Section 2.4).

Table 5. LNBH23L demo-board BOM list

Index	Quantity	Reference	Value / generic part number	Package
1	1	R2	15 kΩ 1/8 W (*see Section 2.2*)	1206
2	1	R5	2.2 kΩ 1/8 W (*see Section 2.7*)	1206
3	1	R7	22 Ω 1/2 W (*see Section 2.7*)	1206
4	1	R8	150 Ω 1/2 W (*see Section 2.7*)	1206
5	1	R9	1.5 kΩ 1/8 W (*see Section 2.8*)	1206
6	3	C8, C10, C11	0.22 µF	1206
7	1	C15	47 nF	1206
8	1	C14	1 nF	1206
9	2	C4, C6	0.47 µF (*See Section 2.5*)	1206
10	1	C1	100 µF > 25 V ESR = 150 mΩ ÷ 350 mΩ Higher value is suitable (*see Section 2.6*)	El.Al. Radial
11	1	C3	220µF > 25 V ESR = 150 mΩ ÷ 350 mΩ (*see Section 2.5*)	El.Al. Radial
12	1	L1	22 µH Inductor with $I_{SAT} > I_{PEAK}$ (see *Section 2.1*)	Radial
13	1	D1	STPS130A (*see Section 2.3*)	SMB
14	1	D2	BAT43 (or any Schottky diode with $I_{F(AV)} > 0.2$ A, $V_{RRM} > 25$ V) or BAT30, BAT54, TMM BAT43, 1N5818 (*See Section 2.9*)	DO-35
15	1	D3	1N4001/1N4007 or equivalent	DIODE-0.4
16	1	IC1	LNBH23L	QFN32
17	1	TR1	BC817	SOT23-3L
18	1	D8	1N4148	SMD
19	2	CN3, CN4	Strip 4p M	HDR1X4
20	2	CN2, CN5	Strip 3p M	HDR1X3
21	3	JP1, 3.3V, CN1	Strip 2p M	HDR1X2

2.1 DC-DC converter inductor (L1)

The LNBH23L operates with a standard 22 µH inductor for the entire range of supply voltages and load current. The Inductor saturation current rating (where inductance is approximately 70 % of zero current inductance) must be greater than the switch peak current ($I_{SAT} > I_{PEAK}$) calculated at:

- maximum load (I_{OUTmax});
- minimum input voltage (V_{INmin});
- maximum DC-DC output voltage ($V_{UPmax} = V_{OUTmax}$ + 0.75 V typ.)

In this condition the switch peak current is calculated using the formula in *Equation 1*:

Equation 1

$$Ipeak = \frac{VUP\,\max * IOUT\,\max}{Eff * VIN\,\min} + \frac{VIN\,\min}{2LF}\left(1 - \frac{VIN\,\min}{VUP\,\max}\right)$$

where:

- Eff is the efficiency of the DC-DC converter (93 % typ. at highest load)
- L is the inductance (22 µH typ.)
- F is the PWM frequency (220 kHz typ.)

Example:

Application conditions:

V_{OUTmax} = 19.2 V (supposing EN=VSEL=1, LLC=0)

V_{INmin} = 11 V

$V_{UPmax} = V_{OUTmax} + V_{DROP}$ = 19.2 V + 0.75 V = 19.95 V

I_{OUTmax} = 500 mA

Eff = 90 % (worst-case in these conditions)

Based on Equation 1 and the preceding application conditions, I_{PEAK} is:

$$\text{Ipeak} = \frac{19.95 * 0.5}{0.9 * 11} + \frac{11}{2 * 22 * 10^{-6} * 220 * 10^{3}}\left(1 - \frac{11}{19.95}\right) = 1.52\text{A}$$

Then, in this example, an inductor with saturation current > 1.52 A should be recommended.

Several inductors suitable for the LNBH23L are listed in *Table 6*, although there are many other manufacturers and devices that can be used. Consult each manufacturer for more detailed information and for their entire selection of related parts, since many different shapes and sizes are available. Ferrite core inductors should be used to obtain the best efficiency. Choose an inductor that can handle at least the I_{PEAK} current without saturating, and ensure that the inductor has a low DCR (copper wire resistance) to minimize power losses and, consequently, to maximize the total efficiency.

Table 6. Recommended Inductors

Vendor	Part number	I_{SAT} (A)	DRC (m?)	Mounting type
Sumida	CD104-220MC	1.6	67	SMD
	RHC110-220M	2.4	88	Through-hole
Toko	822LY-220K	1.3	70	Through-hole
	824LY-220K	1.72	76	Through-hole
	A671HN-220L	2.44	21	Through-hole
	A814LY-220M	2.0	75	SMD
Panasonic	ELC08D220E	1.8	51	Through-hole
	ELC10D220E	3.2	40	Through-hole
Coilcraft	DC1012-223	2.5	46	Through-hole
	PVC-0-223-03	3	35	Through-hole
	DO3316P-223	2.6	85	SMD

2.2 Output current limit selection (R2-RSEL)

The linear regulator current limit threshold can be set through an external resistor connected to the I_{SEL} pin. The resistor value defines the typical output current threshold limit by the equation:

Equation 2

$$\mathrm{Im}\,ax(A) = \frac{10000}{Rsel}$$

Where R_{SEL} is the resistor connected between ISEL and GND. The highest selectable current limit threshold is 0.650 A typ. with R_{SEL} = 15 kΩ

To set the current limitation, ±15 % tolerance, referred to the typical I_{max} current value, must be considered. At this tolerance the tolerance of the R_{SEL} resistor must be added.

For example:

R_{SEL} resistor = 15 kΩ ± 1 %

$$\mathrm{Im\,ax(typ)} = \frac{10000}{15000} = 666\,\mathrm{mA}$$

To calculate the Imax(min) and Imax(max) values:

$$\mathrm{TotToleran\,ce} = 15\% + 1\% = 16\%$$

Where:

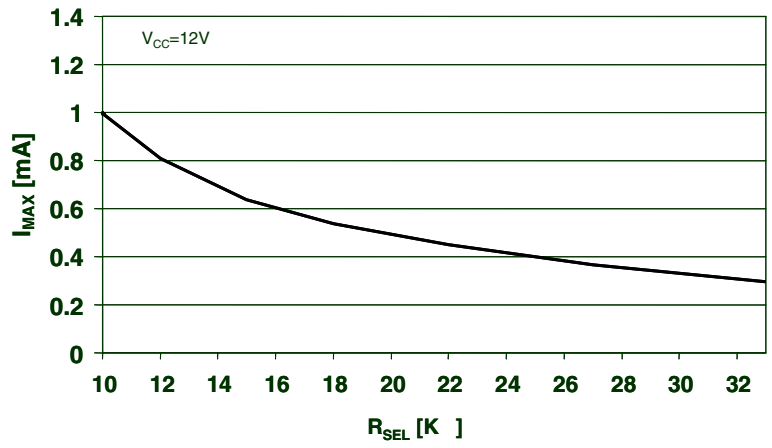
– 15 % is the LNBH23L tolerance
– 1 % is the R_{SEL} tolerance

And then:

$$Imax(min) = 666mA - 16\% = 559mA$$

$$Imax(min) = 666mA + 16\% = 772mA$$

Figure 7. Typical output current limiting vs. R_{SEL}



The formula below allows correct dimensioning of the R_{SEL} total power dissipation:

$$Rsel(I) = \frac{1V}{Rsel(\Omega)}$$

Supposing:

R_{SEL} resistor = 15 kΩ

$$Rsel(I) = \frac{1V}{15000(\Omega)} = 66\mu A$$

$W_{RSEL} = R_{SEL(I)}^2 \times R_{SEL}$ = (66 µA) 2 x 15000 = 65 µW

2.3 DC-DC converter schottky diode (D1)

In typical application conditions it is beneficial to use a 1 A Schottky diode which is suitable for the LNBH23L DC-DC converter. Taking into account that the DC-DC converter Schottky diode must be selected depending on the application conditions (V_{RRM} > 25 V), in general a Schottky diode such as the STPS130A is suitable.

The average current flowing through the Schottky diode is lower than I_{PEAK} and can be calculated by *Equation 3*. In worst-case conditions, such as low input voltage and higher

output current, a Schottky diode capable of supporting the I_{PEAK} should be selected. I_{PEAK} can be calculated using *Equation 1*.

Equation 3

$$Id = Iout \times \frac{Vout}{Vin}$$

Table 7. Recommended Schottky diode

Vendor	Part number	I_F (av)	V_F (max)
STMicroelectronics	1N5818	1 A	0.50 V
	1N5819	1 A	0.55 V
	STPS130A	1 A	0.46 V
	STPS1L30A	1 A	0.30 V
	STPS2L30A	2 A	0.45 V
	1N5822	3 A	0.52 V
	STPS340	3 A	0.63 V
	STPS3L40A	3 A	0.5 V

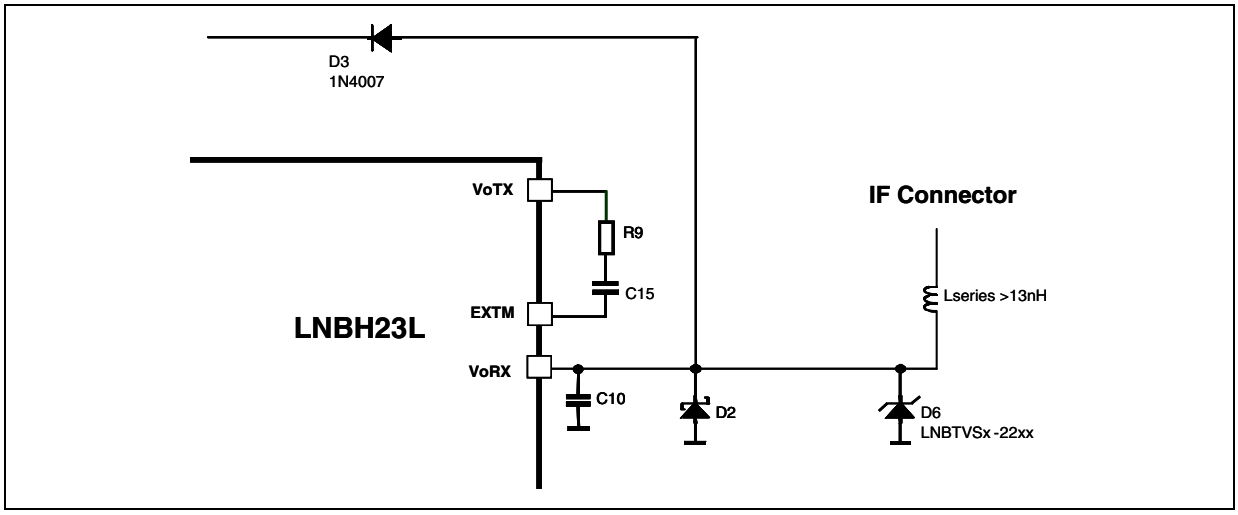
2.4 TVS diode (D6)

The LNBH23L device is directly connected to the antenna cable in a set-top box. Atmospheric phenomenon can cause high voltage discharges on the antenna cable causing damage to the attached devices. In applications where it is required to protect against lightning surges, transient voltage suppressor (TVS) devices like LNBTVSx-22xx can be used to protect the LNBH23L and the other devices electrically connected to the antenna cable.The LNBTVSx-22xx diodes, developed by STMicroelectronics, are dedicated to lightning and electrical overstress surge protection for LNBHxx voltage regulators. These protection diodes were designed to comply with the stringent IEC61000-4-5 standard with surges up to 500 A in a whole range of products.

Note: TVS diodes have intrinsic capacitance that attenuates the RF signal. For this reason, the LNBTVSx-22xx cannot be directly connected to the I_F (RX/TX) cable connector that carries the RF signals coming from the LNB. To suppress effects of the intrinsic capacitance, an inductance must be placed in series with the TVS diode (see Figure 6 example). The goal of the L series inductance added to the CLNBTVS is to be transparent at 22 kHz and to reject frequencies higher than 900 MHz.

The value of the series inductance is usually >13 nH, with a current capability higher than the I_{PP} (peak pulse current) expected during the surge.

Figure 8. Example of LNBTVS diode connection



The selection of the TVS diode must be based on the maximum peak power dissipation that the diode is capable of supporting.

Table 8. Recommended LNBTVS

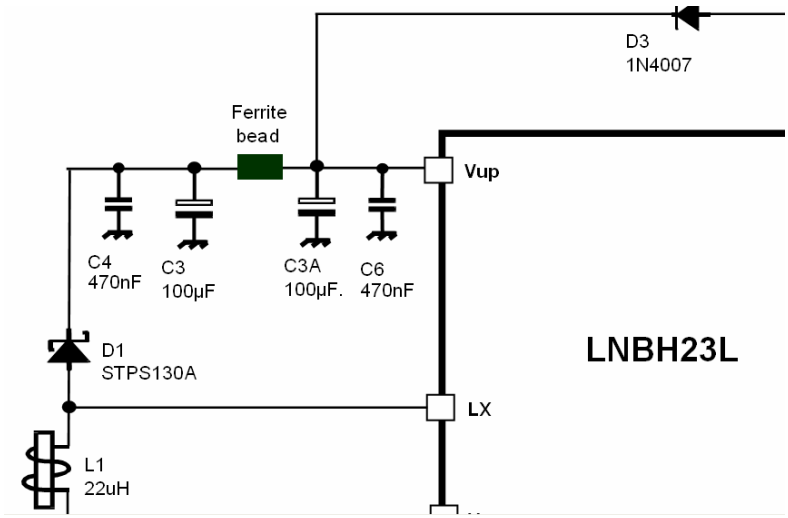
Vendor	Part number	VBR_{TYP} (V)	Ipp (A) 8/20 µs
STMicroelectronics	LNBTVS4-220S	23.1	334
	LNBTVS4-221S	23.1	334
	LNBTVS4-222S	23.1	334
	LNBTVS6-221S	23.1	500

Select the TVS diode which is capable of supporting the required Ipp (A) value indicated in *Table 8*.

2.5 DC-DC output capacitors (C3, C4, C6) and ferrite bead

An electrolytic low cost capacitor is needed on the DC-DC converter output stage (C3 in *Figure 6*). Moreover, two ceramic capacitors are recommended to reduce the high frequency switching noise. The switching noise is due to the voltage spikes of the fast switching action of the output switch, and to the parasitic inductance of the output capacitors. To minimize these voltage spikes, special low-inductance ceramic capacitors can be used, and their lead lengths must be kept short and as close as possible to the IC pins (C4 and C6 in *Figure 9*). In case of high switching noise, it is possible to increase the C6 capacitor up to 4.7 µF, 2.2 µF is a good compromise to reduce the switching noise.

Figure 9. DC-DC converter output stage with ferrite bead



The most important parameter for the DC-DC output electrolytic capacitors is the effective series resistance (ESR). The DC-DC converter control loop circuit has been designed to work properly with low-cost electrolytic capacitors which have ESR in the range of 200 mΩ.

A 220 µF with ESR between 100 mΩ and 350 mΩ is a good choice in most application conditions. In case it is requested to further reduce the switching noise, a ferrite bead with a current rating of at least 2 A and impedance higher than 60 Ω at 100 MHz could be used.

In this case It is recommended to use two electrolytic capacitors of 100 µF (see C3 and C3A in *Figure 9*) with ESR between 150 mΩ and 350 mΩ adding the ferrite bead in accordance to *Figure 9*.

The DC-DC capacitor's voltage rating must be at least 25 V, but higher voltage capacitors are recommendable.

2.6 Input capacitors (C1)

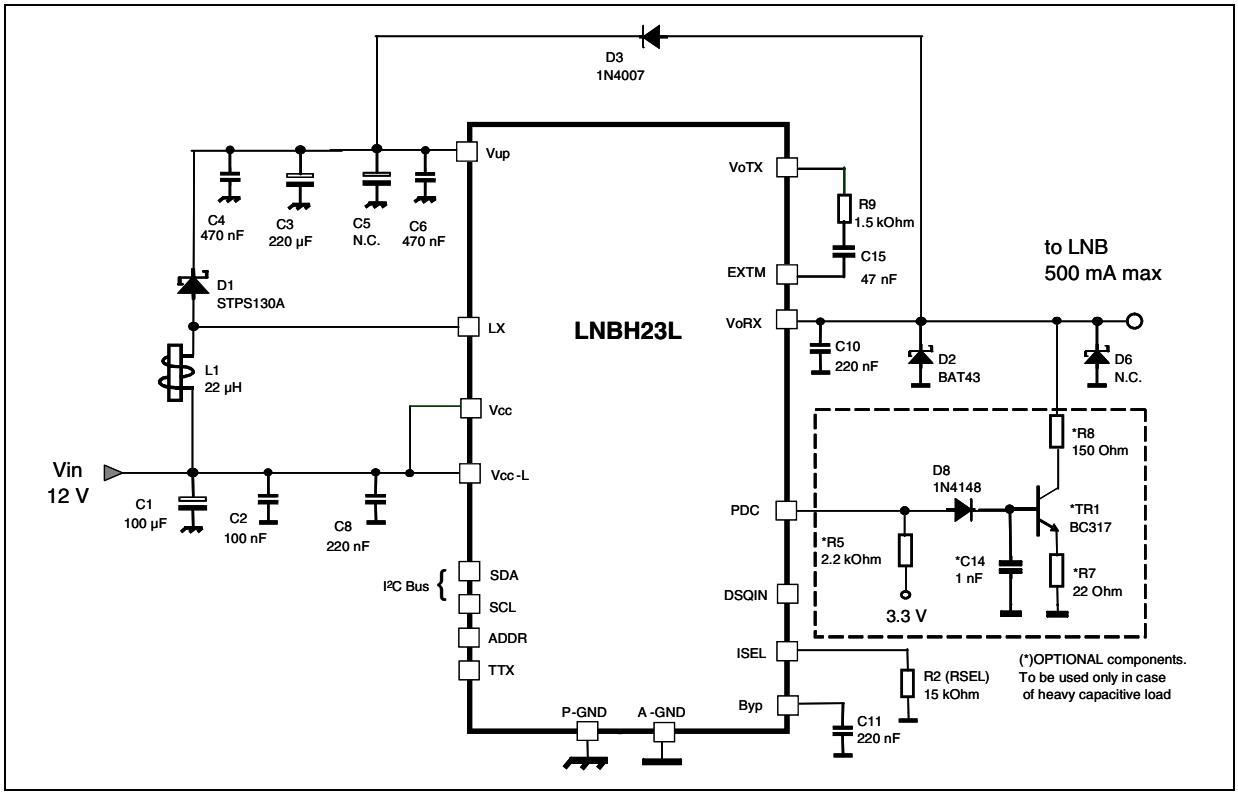
An electrolytic bypass capacitor (C1 in *Figure 6*) between 100 µF and 470 µF, located close to the LNBH23L, is needed for stable operation. In any case, a ceramic capacitor (C2 in *Figure 6*) between 100 nF and 470 nF is recommended to reduce the switching noise at the input voltage V_{CC} pins.

2.7 PDC optional external circuit

This optional circuit, internally controlled by the PDC output pin, acts as an active pull-down discharging the output capacitance only when the internal 22 kHz tone is activated (TEN=TTX=1 or DSQIN=1).

This optional circuit is not needed in standard applications having I_{OUT} > 50 mA and capacitive load up to 250 nF where the PDC pin can be left floating.

Figure 10. Application circuit with PDC optional solution



The formula to calculate the transistor I_C current with PDC circuit is:

Equation 4

$$I_C = \frac{V_{BYP} - V_D - V_{BE}}{R_7 + \frac{R_5}{TR1hfe}}$$

The current flows through R8, TR1 and R7 during fall time of 22 kHz tone and the power dissipated by these passive components is 1/3 because the D.C. is 30 % (see *Figure 11*).

Figure 11. PDC optional circuit load calculation

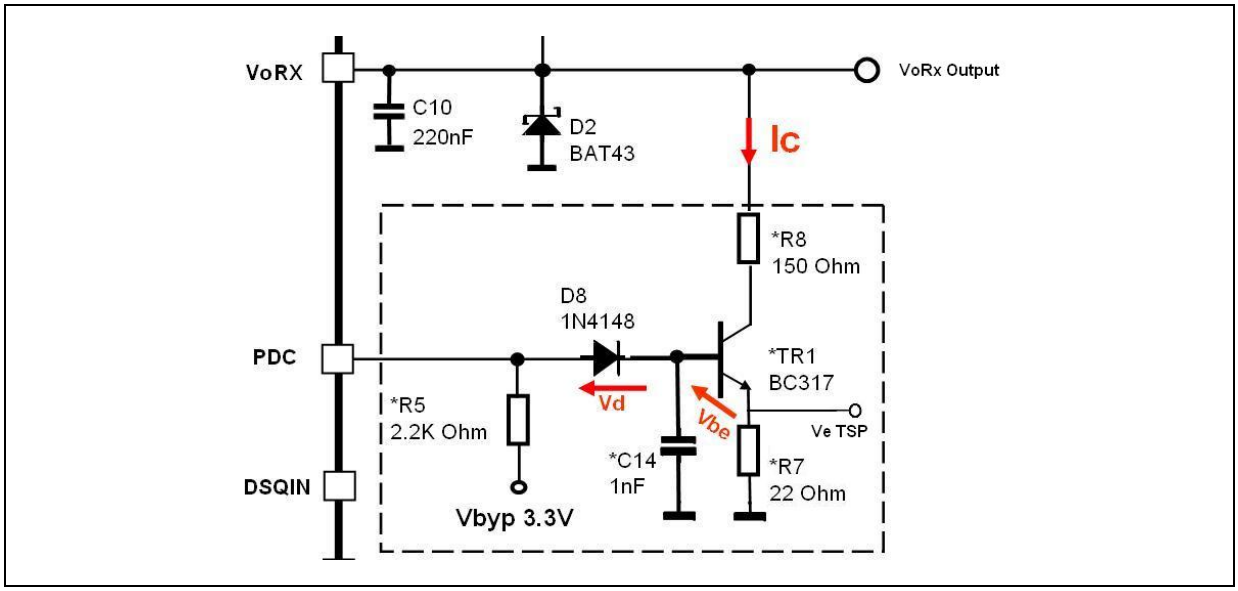
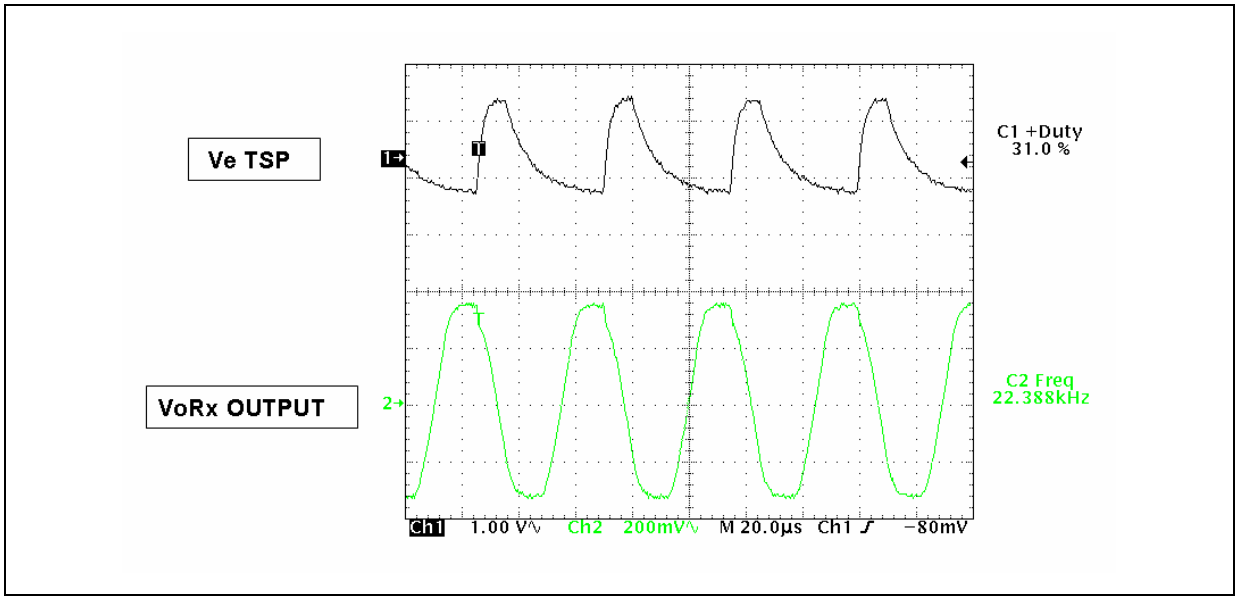


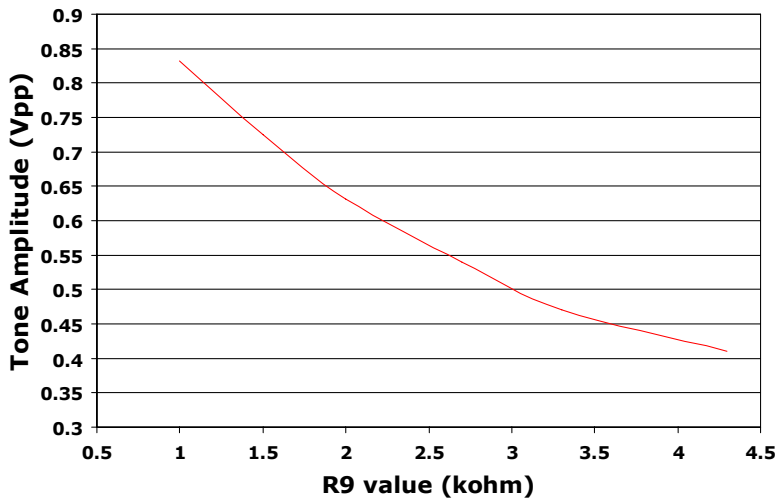
Figure 12. PDC circuit waveform



2.8 EXTM-V_{OTX} resistor (R9)

The LNBH23L device offers the possibility to customize the output tone amplitude through the R9 resistor variation. According to the graph in *Figure 13*, the R9 resistor can be slightly modified to change the output tone amplitude when the internal 22 kHz tone generator is used. Values between 1 kΩ and 2.7 kΩ are recommended.

Figure 13. Tone amplitude vs. R9 value



2.9 Undervoltage protection diode (D2)

During a short-circuit event on the LNB output, negative voltage spikes may occur on the V_{oRX} pin. To prevent reliability problems, a low-cost Schottky diode with low V_F clamping voltage is used between this pin and GND (see D2 in Figure 6). It is recommended to place the protection diode cathode as close as possible to the V_{oRX} pin.

3 Layout guidelines

Due to high current levels and fast switching waveforms, which radiate noise, a proper printed circuit board (PCB) layout is essential. Sensitive analog grounds can be protected by using a star ground configuration. Also, lead lengths should be minimized to reduce stray capacitance, trace resistance, and radiated noise. Ground noise can be minimized by connecting GND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Place input bypass capacitors (C1, C2 and C8) as close as possible to V_{CC} and GND, and the DC-DC output capacitors (C3, C4 and C6) as close as possible to V_{UP}. Excessive noise at the V_{CC} input may falsely trigger the undervoltage protection circuitry, resetting the I²C internal registers. If this occurs, the registers are set to zero and the LNBH23L is put into shutdown mode.

An LNB power supply demonstration board is available.

3.1 PCB layout

Any switch-mode power supply requires a good PCB layout in order to achieve maximum performance. Component placement, and GND trace routing and width, are the major issues. Basic rules commonly used for DC-DC converters for good PCB layout should be followed. All traces carrying current should be drawn on the PCB as short and as thick as possible. This should be done to minimize resistive and inductive parasitic effects, and increase system efficiency. White arrows indicate the suggested PCB (ring) ground plane to avoid spikes on the output voltage (this is related to the switching side of the LNBH23L). Good soldering of the ePad helps on this issue.

Figure 14. PBC top layer

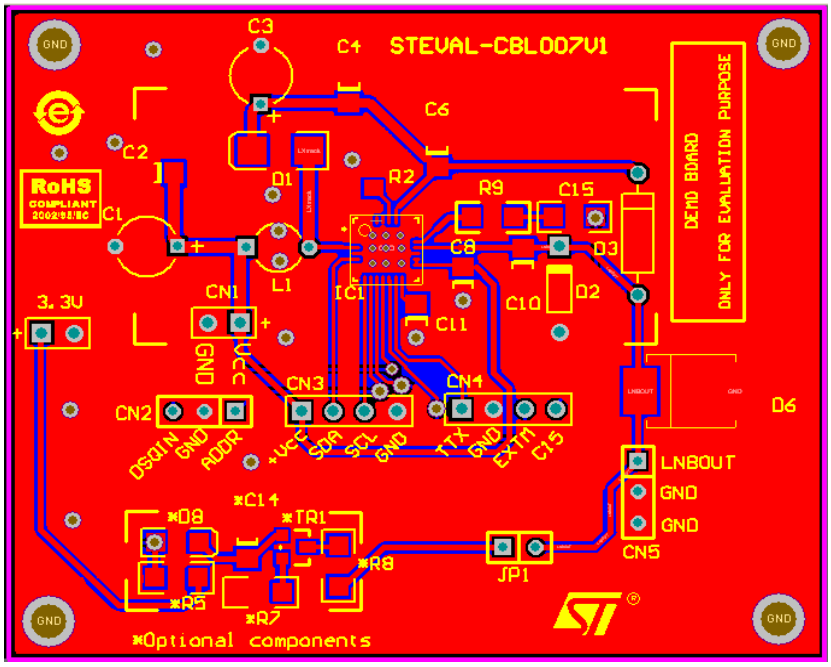


Figure 15. PBC bottom layer

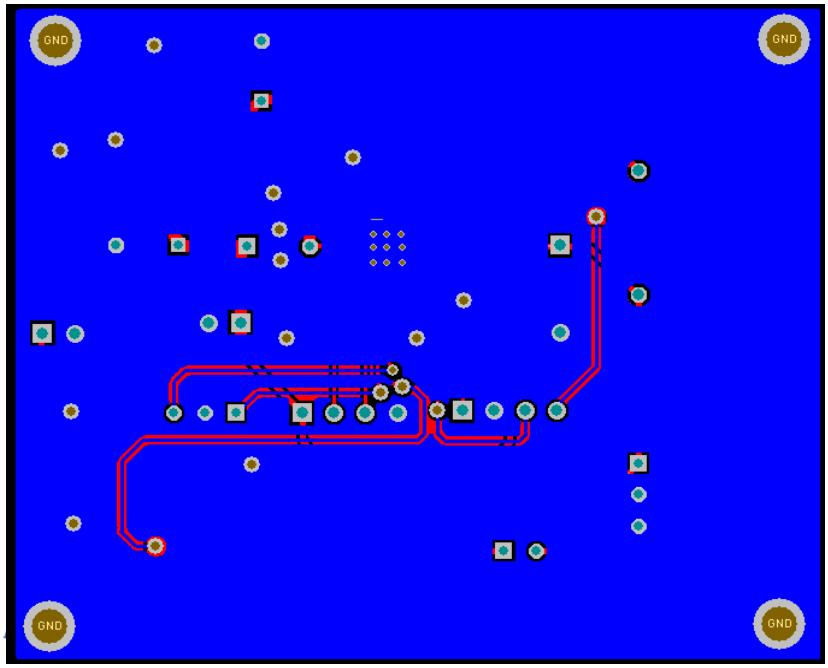
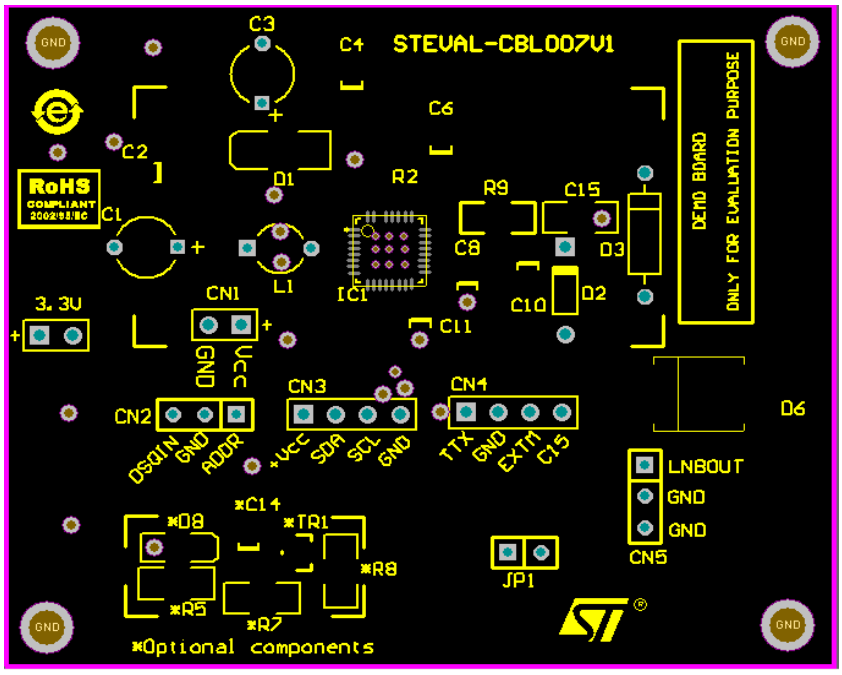


Figure 16. PCB components layout



3.2 PCB Thermal managing

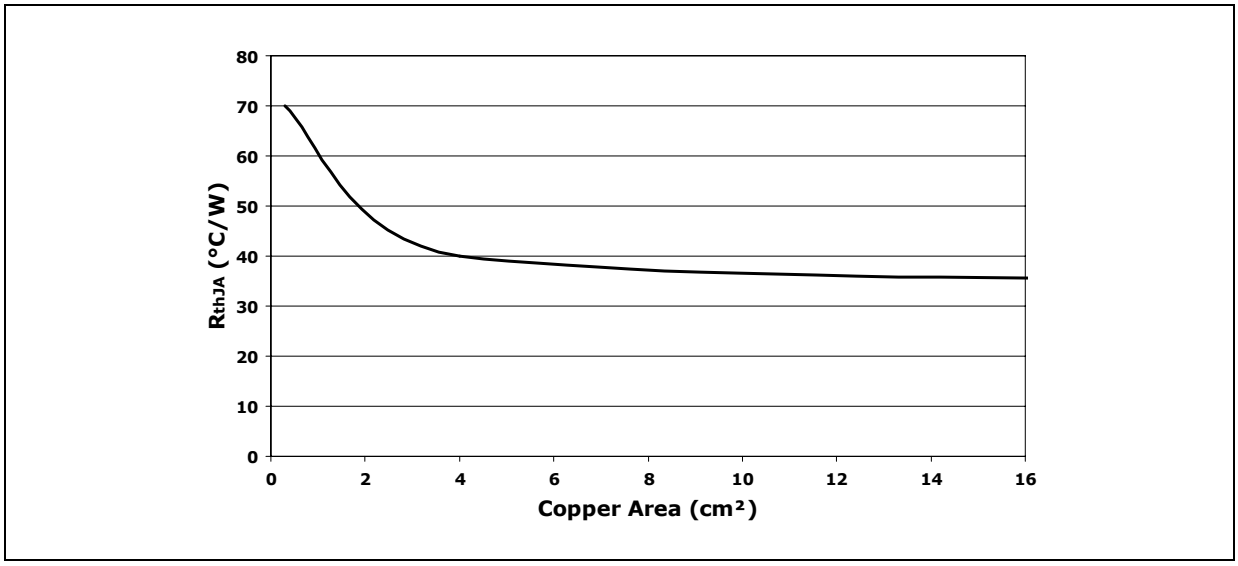
The LNBH23L power dissipation inside the IC is mainly due to the DC-DC integrated MOSFET power loss plus the linear regulator power dissipation. The total power dissipation calculated, considering both the DC-DC and linear regulator power loss at the maximum output current (500 mA) with 18 V for LNB output and V_{IN} = 11 V, is around 1 W. The heat generated due to this power dissipation level requires a suitable heat-sink to keep the junction temperature below the over temperature protection threshold at the rated ambient temperature inside the set-top box.

For example: assuming a 70 °C max for the ambient temperature inside the STB case and a 125 °C maximum junction temperature for the LNBH23L, the total R_{thJA} is less than 50 °C/W.

The R_{thJA} for the QFN32 package used for the LNBH23L can be as low as 35 °C/W. Based on thermal resistance tests performed on the LNBH23L ST demonstration board, this result is achievable with a minimum of a 4x4 cm² copper area placed just below the IC body (see *Figure 17*). Better performance with a smaller copper area may be achievable using four layers (2s2p) PCB.

Usually the copper area is obtained by using the ground layer of a multi-layer PCB soldered below the IC exposed pad. In *Figure 14* an example of a layout for the QFN32 package with a dual layer PCB is shown, where the IC exposed pad is connected to the ground layer and the square dissipating area is thermally connected through 9 via holes filled by solder.

Figure 17. Typical junction to ambient thermal resistance with dual layer PCB, 1oz, 9 thermal vias



The best thermal and electrical performance can be achieved when an array of copper vias barrel plating is incorporated in the land pattern at 1.2 mm grid. It is also recommended that the via diameter should be 0.30 mm to 0.33 mm with 1 oz copper via barrel plating.

If the copper plating does not plug the vias, a solder mask material must be used to cap the vias with a dimension equal to the via diameter + 0.1 mm minimum. This prevents the solder from not being well spread through the thermal via and potentially creating a solder void between the package bottom and the ground plane of the PCB.

Taking into account that the solder mask diameter should be at least 0.1 mm larger than the via diameter.

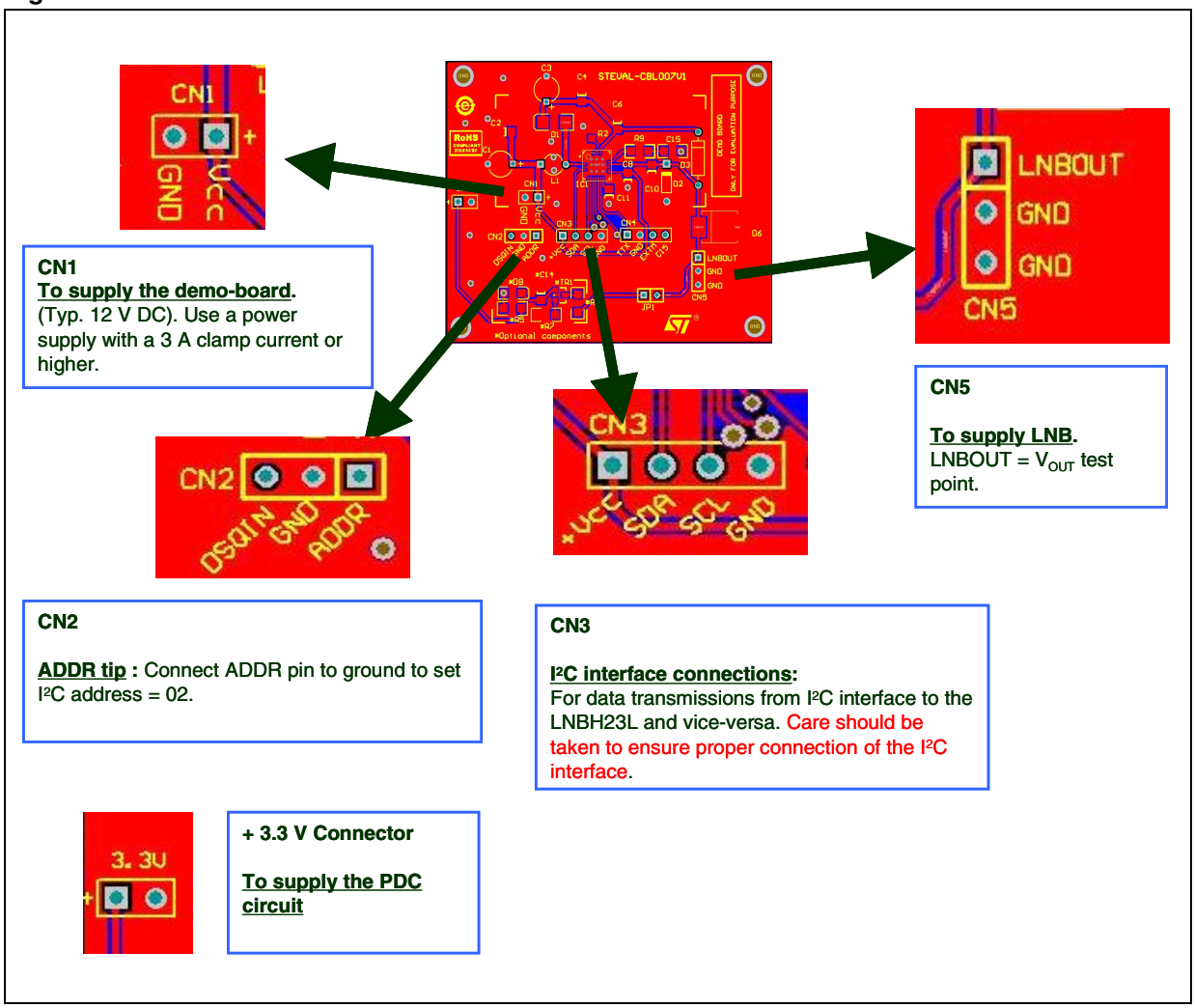
However, different layouts are also possible. Basic principles suggest keeping the IC and its ground exposed pad approximately in the middle of the dissipating area; to provide as many vias as possible; to design a dissipating area having a shape as square as possible and not interrupted by other copper traces.

4 Startup procedure

Testing the demonstration board requires a PC with a parallel port (ECP printer port), an I²C bus interface, software (LNBxx control suite), a dual-output power supply (3 A clamp current or higher) and an electronic load.

- Step 1: Install the LNBxx control suite software (Software installation)
- Step 2: Plug the I²C connector on CN3.
- Step 3: Supply the demo-board through CN1.
- Step 4: Manage the demo-board through LNBxx control suite software

Figure 18. PCB connector



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Oct-2010	1	Initial release
29-Nov-2010	2	Modified *Section 1.3.1: Reserved I²C address on page 5*.
28-Jan-2011	3	Modified R7 value *Table 5 on page 12*.