AN303
Application note

Thyristors and TRIACs: latching current

Introduction

The purpose of this note is to familiarize TRIAC or thyristor (SCR) users with the latching current I_L.

The importance of this parameter is illustrated with some typical examples. Procedures are given for measurement of I_L. The variation of I_L with operating conditions and device sensitivity are described.

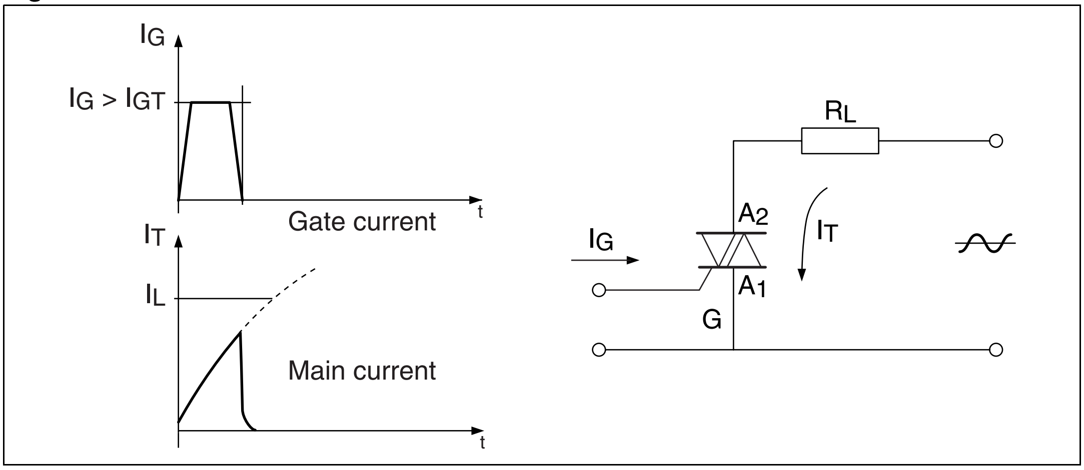
This application note presents only the TRIAC case. However, the concepts are valid for SCRs (except for the various conduction modes).

Definition

The latching current (I_L) of a TRIAC is the minimum value of the load current (current flowing between electrodes A_2 and A_1) that keeps the device conducting when the gate signal is removed (see *Figure 1*).

Figure 1 below shows the latching current and the gate current pulse. After the TRIAC triggering, a current (I_T) flows through the TRIAC. If the gate current (I_G) is removed while the current I_T is lower than the latching current I_L, the TRIAC switches off.

Figure 1. Blocked TRIAC



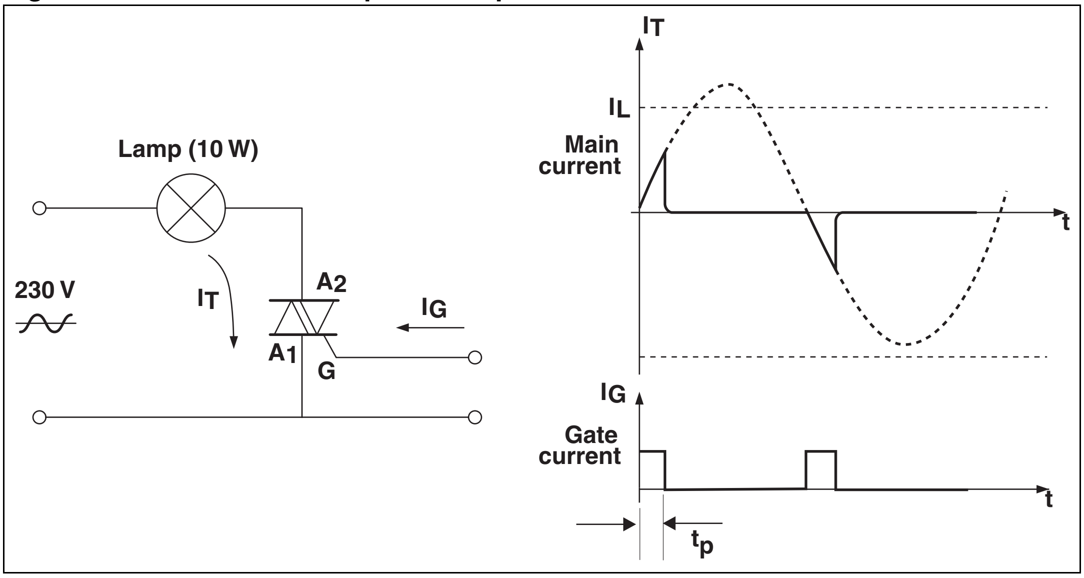
1 Application examples

The importance of the latching current is highlighted by the following application examples.

1.1 Example 1: low power lamp control

In the application circuit shown in *Figure 2* a TRIAC is used to control a 10 W signaling light. For the European mains (V_{rms} = 230 V), the peak load current is about 61 mA. A Z01 device could be used to control this load current, but the maximum latching current is specified as 50 mA if a Z0110 device is used in quadrant II. The peak load current is then very close to the maximum latching current given in the datasheet. The device will turn off if the gate current pulse is too short.

Figure 2. Control of a low-power lamp



Thus, a TRIAC could not remain on if its latching current is higher than the load current at the moment the gate current is removed (refer to *Figure 2*). For correct operation, a continuous gate current should be applied or a longer gate current pulse should be applied. For example, for a sinusoidal load current ($I_{(t)} = I_{peak} \times \sin(\omega t)$), the pulse width is given by the following equation (refer to AN302 for a complete definition of I_H[a]):

$$tp > \frac{1}{\omega} \cdot \arcsin\left(\frac{I_{HMAX}}{I_{peak}}\right) + \frac{1}{\omega} \cdot \arcsin\left(\frac{I_{LMAX}}{I_{peak}}\right)$$

To reduce the pulse width duration, a more sensitive TRIAC could be used (for example, for the Z0103 I_L max is 15 mA in QII).

a. The minimum current that keeps a TRIAC conducting is called the hypostatic or holding current I_H.

1.2 Example 2: inductive load control

When a TRIAC controls an inductive load (L), the rise of the load current I_T is slowed down. The approximate load current slope dI_T/dt is given by:

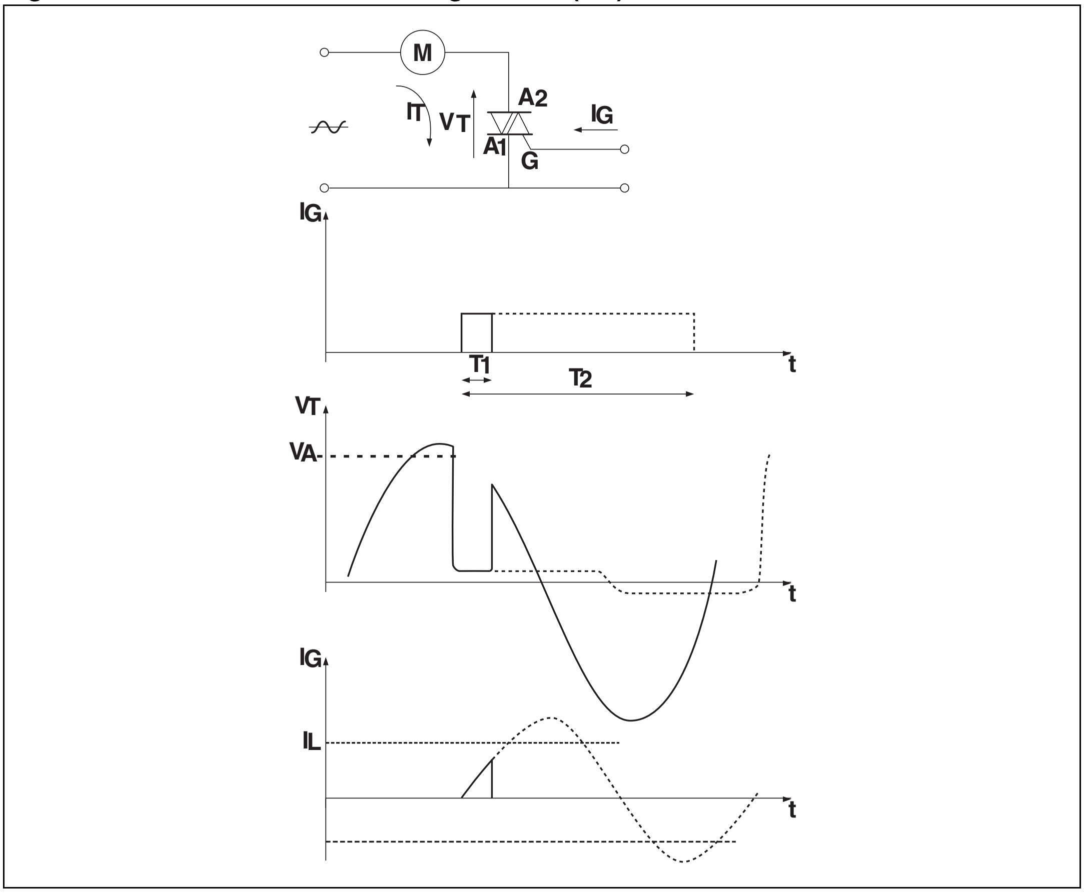
$$\frac{dI_T}{dt} \cong \frac{V_A}{L}$$

where V_A is the mains voltage when the gate signal is applied.

In *Figure 3* the impact of the gate pulse width on the TRIAC conduction is shown.

- **In continuous lines**: A short gate signal (T1) is applied. The TRIAC doesn't remain in the on state because the load current I_T doesn't reach the TRIAC latching current level before the gate current removal.
- **In dotted lines:** A longer gate signal (T2) is applied. In this case, the TRIAC turns on and remains in the on state. The TRIAC turns off when the load current reaches zero after the gate current removal.

Figure 3. Control of an alternating current (AC) motor



For correct operation a gate current has to be applied until the load current reaches the TRIAC latching current. The control mode shown in *Figure 3* is a square pulse.

Another TRIAC control mode is to apply a gate pulse train. Application note AN308 offers some TRIAC control circuits specially designed to work with inductive loads.

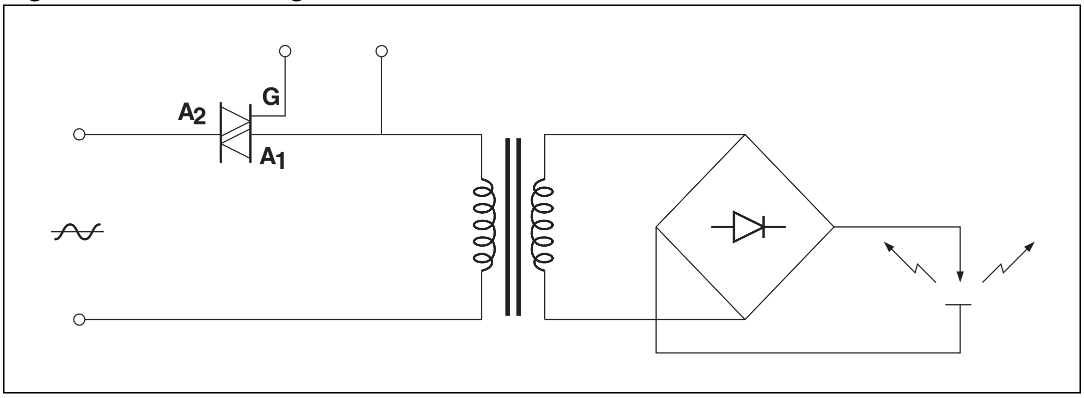
1.3 Example 3: varying power load control

For most applications, the load power is controlled by the TRIAC conduction time. For arc welding (see *Figure 4*), the controlled power can be subjected to considerable variations. The device current rating is chosen and validated for full-wave and full load operation. The application operation is then ensured in the worst case but, for low power loads, a TRIAC triggering issue could occur.

In the case of an open load operation, the load current equals the transformer magnetizing current, which is much lower than full load current. The load current could even be below the TRIAC latching current in one triggering quadrant. Thus, the TRIAC could turn on properly in one quadrant but could not turn on in another quadrant, for which the latching current is higher. An unbalance then occurs and induces a direct current (DC) through the transformer, which heats its coils and can cause transformer failure.

For correct circuit design, the TRIAC operation should be validated in full load and also in open load. (See AN308 for a schematic circuit diagram dedicated to this welding application.)

Figure 4. Arc welding control



2 Latching current – the details

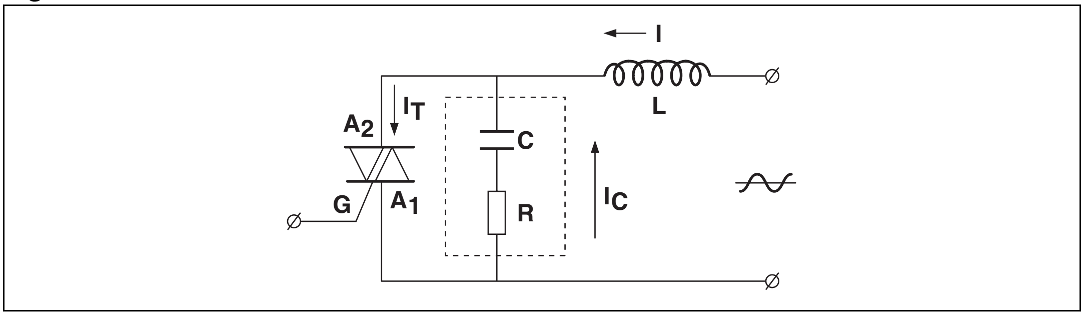
The three examples in the previous section illustrate the importance of the latching current parameter and the different issues considered in taken into account the latching current requirements.

In STMicroelectronics' datasheets for all types of TRIACs or SCRs the latching current (I_L) is specified as a maximum value for a 25 °C junction temperature. Then corrections have to be made according to temperature variations.

2.1 Effect of RC snubber circuit at turn on

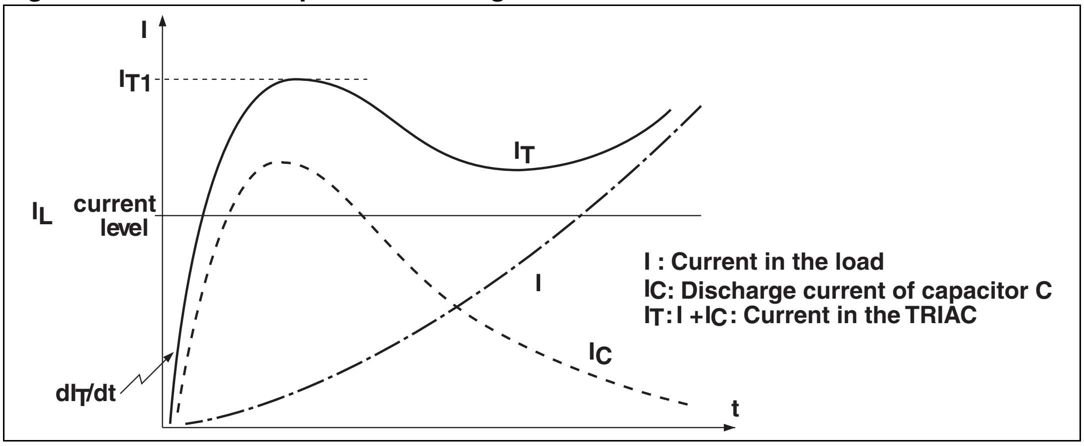
For most applications, an RC snubber across TRIAC A2 and A1 terminals is used to improve TRIAC immunity to fast transient voltages and also, in the case of inductive loads, to ensure appropriate TRIAC turn off. (Refer to *Figure 5* and AN437 for RC snubber circuit design for TRIACs.)

Figure 5. RC snubber circuit.



In the case of inductive loads, an RC snubber has another advantage at TRIAC turn on. The energy stored in the snubber capacitor C, during the TRIAC off state, is fed back through the TRIAC at turn on. The TRIAC current slope during the capacitor discharge is proportional to the capacitor voltage before the TRIAC turn on and inversely proportional to the series inductances of the board and the snubber resistor. Thus, the TRIAC current rise is faster than the load current and reaches the device latching current in a shorter time (see *Figure 6*).

Figure 6. Snubber capacitor discharge at TRIAC turn on



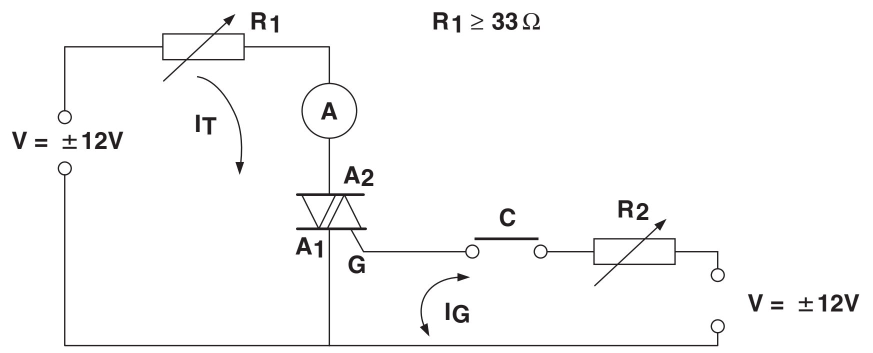
Note: To limit the rate of current rise at turn on (dI_T/dt) during the capacitor discharge, the value of the resistor (R) must be higher than a minimum value (typically 47 ohms for most TRIACs). A higher dI_T/dt than the dI/dt specified in the datasheet may damage the device. The TRIAC peak current (I_{T1}) is approximately the quotient of the capacitor voltage and the snubber resistance.

2.2 Latching current measurement

In *Figure 7*, push button C is used to trigger the TRIAC. The value of the gate current I_G is set to a higher value than the gate current specified in the datasheet ($I_G = 1.2 \times I_{GT}$). Decreasing the resistance R causes the TRIAC current I_T to increase. The value of the latching current I_L is the value of the TRIAC current I_T when the TRIAC remains on without a gate current.

Sensitive SCRs, that is, those with a gate triggering current I_{GT} of 200 µA or less, are measured with a 1 kΩ resistor connected between gate and cathode.

Figure 7. Circuit for the measurement of the latching current (I_L)



For repeatable results, the TRIAC should be appropriately turned on. The following guidelines must be applied:

- The pulse width of the gate current must be at least equal to 1 ms.
- The applied gate current (I_G) must by higher than the specified triggering gate current (I_{GT}) of the device measured. An I_G / I_{GT} ratio higher than or equal to 1.2 is recommended.

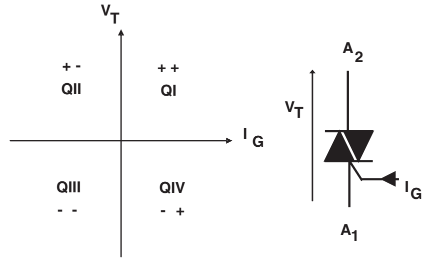
There are four different latching current levels; corresponding to the four triggering quadrants (refer to *Figure 8*). These quadrants are defined according to V_T polarity (V_T is positive if A2 is set to a higher bias voltage than A1) and gate polarity (I_G is positive if it is sourced to the gate, so it circulates from G to A1):

- Quadrant I (QI): $V_T > 0$ and $I_G > 0$
- Quadrant II (QII): $V_T > 0$ and $I_G < 0$
- Quadrant III (QIII): $V_T < 0$ and $I_G < 0$
- Quadrant IV (QIV): $V_T < 0$ and $I_G > 0$

I_L in QIV is not specified for devices only controlled in the three first quadrants, as Snubberless^{TM}, logic level and high temperature TRIACs.

TM: Snubberless is a trademark of STMicroelectronics

Figure 8. TRIAC triggering quadrants



2.3 Variation of the latching current

2.3.1 Typical variation of I_L with device sensitivity and quadrant

The latching current I_L is related to the triggering current, I_{GT}. The I_L/I_{GT} ratio also depends on the triggering quadrant as shown in *Table 1*.

Table 1. Approximate ratio between I_L and I_{GT} for sensitive and standard TRIACs

	$\frac{I_L(QI)}{I_{GT}(QI)}$	$\frac{I_L(QII)}{I_{GT}(QII)}$	$\frac{I_L(QIII)}{I_{GT}(QIII)}$	$\frac{I_L(QIV)}{I_{GT}(QIV)}$
Sensitive TRIAC 12 A rms (TW type)	3	6	3.5	N.A.
Standard TRIAC 12 A rms (C type)	1.5	4.5	1	0.5

Example

With a BTA/BTB12-600TW, I_{GT} (QI) = 1 mA (measured),

then I_L (QI) ≈ 3 mA, I_L (QII) ≈ 6 mA and I_L (QIII) ≈ 3.5 mA.

With a BTA/BTB12-600C, I_{GT} (QI) = 15 mA (measured),

then I_L(Q1) ≈ 22.5 mA, I_L (QII) ≈ 67.5 mA, I_L (QIII) ≈ 15 mA and I_L (QIV) ≈ 7.5 mA.

In the case of TRIACs (as opposed to the SCRs), it is important to note that the current I_L (QII), is much higher than the I_L current in the other quadrants. So, in the data sheets, two maximum values are specified: one value for quadrants I, III and IV (if specified) and one value for quadrant II.

2.3.2 Typical variation between I_L and I_H

The holding current value I_H (refer to AN302 for holding current) is linked to the latching current value I_L. For the most TRIACs (rated current lower than 40 A), the I_L value is higher than the I_H value. The I_L / I_H ratio is related to the TRIACs current rating, as shown *Table 2*.

Table 2. Approximate ratio between I_L and I_H according to devices current rating

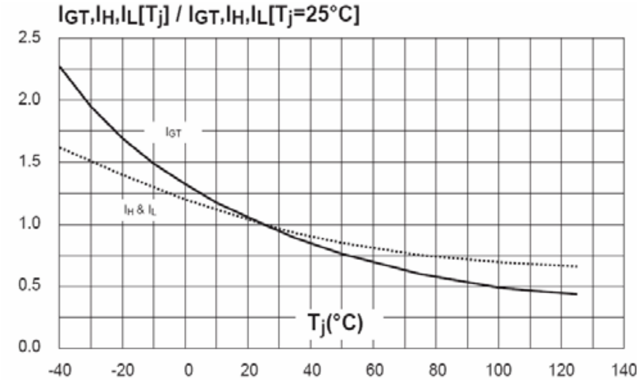
	Rating of TRIACs and SCRs	
	$I_{RMS} \le 6$ A	6 A $\le I_{RMS} \le 40$ A
I_L / I_H (1)	1.1 to 1.5	1.5 to 3

1. First quadrant in the case of TRIACs

2.3.3 Typical variation of I_L with junction temperature

The latching current is physically related to the triggering gate current I_{GT}. These two parameters vary with the junction temperature as shown in *Figure 9*.

Figure 9. Relative variation of I_L with the junction temperature T_j



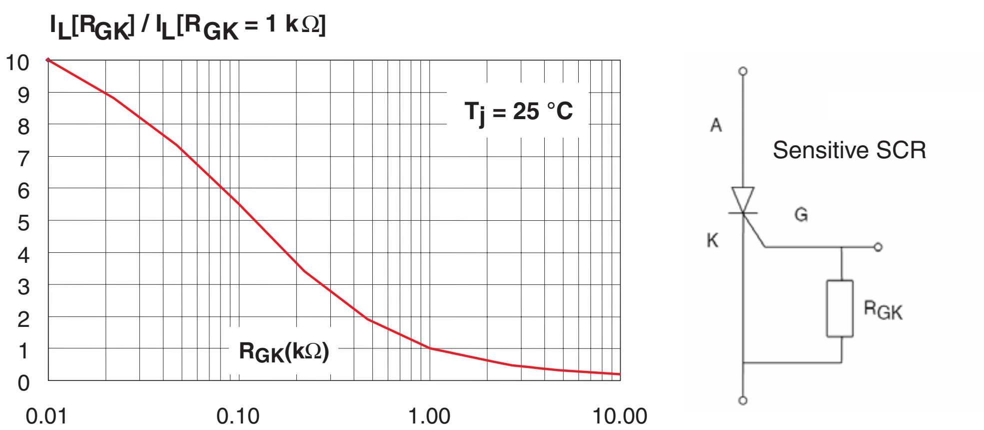
Example

With a BTA12-600C,
I_L (QI) = 20 mA (measured) at T_j = 25 °C, then I_L (QI) ≈ 32.5 mA at T_j = – 40 °C.

2.3.4 Influence of the external gate-cathode resistor

In some applications, an R_{GK} resistor is connected between the gate and the cathode of the component. This resistor either improves device behavior under fast transient voltages (by-pass for A2-G leakage current) in the case of sensitive SCRs or forms part of the triggering circuit. The value of this resistor, as well as the sensitivity of the component, affects the latching current as shown in *Figure 10*.

Figure 10. Variation of I_L, for a sensitive SCR with R_{GK}



Note: The latching current of sensitive SCRs is always specified with a 1000 ohm gate-cathode resistor.

Sensitive SCRs (I_{GT} < 200 µA)

For sensitive SCRs, R_{GK} has a large influence on the latching current as shown by *Figure 10*. Thus, in certain applications, the designer may want to use a high-impedance control circuit. The drawback will then be that the SCR sustainable dV/dt will be lower.

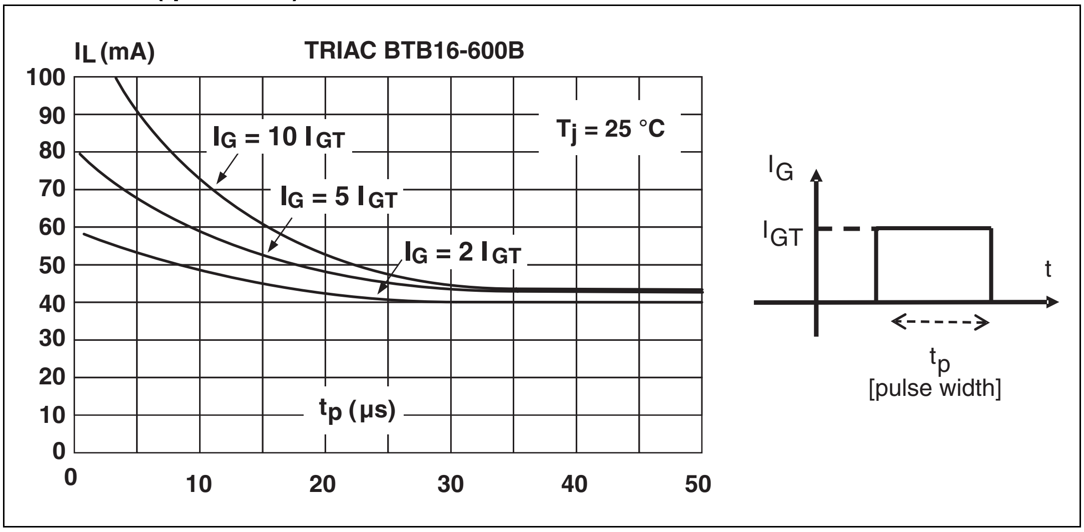
Standard SCRs, sensitive and standard TRIACs

R_{GK} greater than 20 Ω will have no significant effect on the latching. But values lower than 20 Ω are not used in practice as they will excessively increase the current applied by the control circuit to trigger the device.

2.3.5 Typical variation of the latching current I_L with the control signal

The latching current I_L varies with the amplitude and the pulse width t_p of the gate current I_G. With a constant triggering pulse width (< 50 µs), the I_G amplitude increase will lead to the I_L amplitude increase. And vice versa, if the I_G amplitude is kept constant, the t_p decrease will lead to the I_L amplitude increase (refer to *Figure 11*).

Figure 11. Variation of I_L with the width t_p and the amplitude I_G of the gate pulse (quadrant I)



The latching current varies also according to the gate current pulse shape. The latching current can:

- Increase if a negative gate current is applied at the end of the pulse, as shown in *Figure 12*.
- Decrease if the decreasing slope of the gate current is low (compared to dashed line), as shown in *Figure 13*. For a decreasing slope of the gate current lower than 0.5 A/µs, the I_L value is typically closed to the I_H value.

Figure 12. Gate current pulse with negative current at the end of the pulse

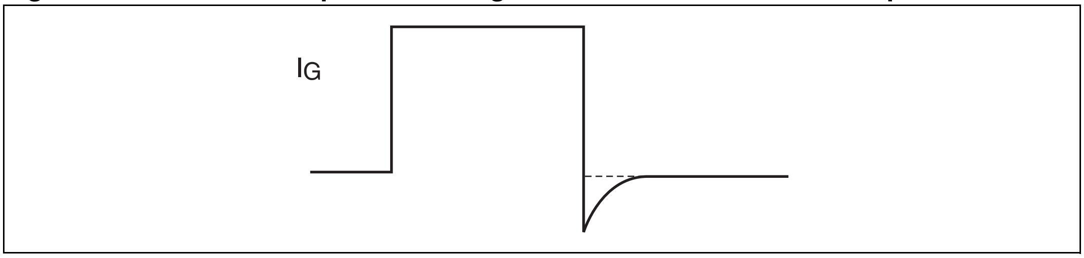
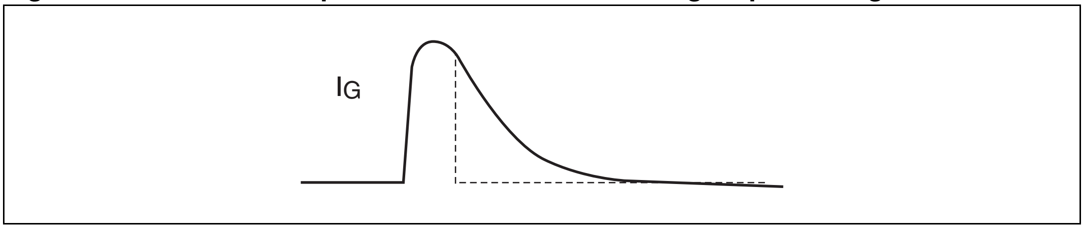


Figure 13. Gate current pulse with smooth decreasing slope of the gate current



To ensure a suitable device triggering, an I_G amplitude of 1.2 times the specified I_{GT} (calculated for the minimum application ambient temperature, see *Figure 9*) and an I_G pulse width as high as possible are recommended. A control pulse with decreasing slope of the gate current, and without reverse current, allows the latching current to decrease.

3 Conclusion

The SCR or TRIAC choice does not depend only on the voltage, the rated current and the sensitivity. Other parameters must be taken into account to ensure appropriate operation. Among them, the latching current, I_L, plays an important role in many circuits.

The value of this parameter varies with

- gate current pulse (amplitude, shape and width)
- temperature
- control circuit (in the case of sensitive SCRs)
- direction of current flow

TRIAC and SCR applications, involving highly inductive loads or loads with considerable power variations, are the main applications for which the latching current must be given particular consideration.

Taking into account these aspects, the designer can obtain satisfactory operation of the circuit in industrial applications.

4 Revision history

Table 3. Document revision history

Date	Revision	Changes
Apr-1995	1	First issue.
15-May-2004	2	Style sheet update. No content change.
24-Apr-2009	3	Reformatted to current standards. Complete technical update for current devices.