# AN2941
# Application note

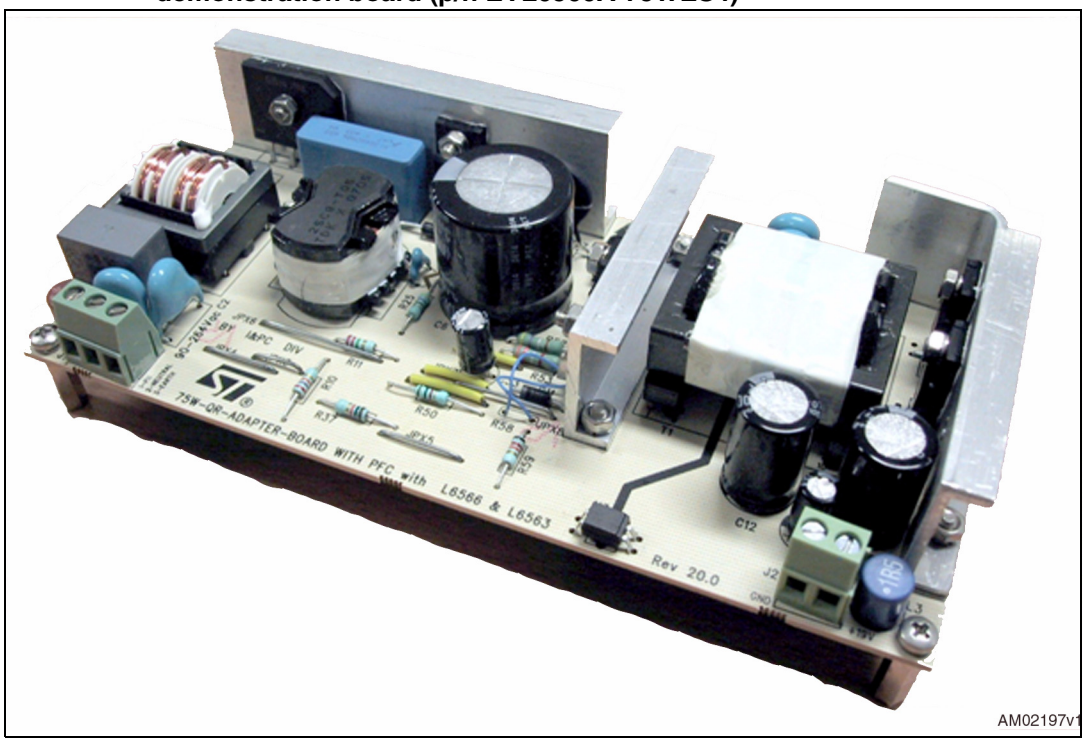
## 19 V - 75 W SMPS compliant with latest ENERGY STAR® criteria using the L6563S and the L6566A

## Introduction

This application note describes the characteristics and the features of a 75 W reference board (p/n EVL6566A-75WES4), tailored on specifications of a typical high-end portable computer power supply. The peculiarities of this design are the very high efficiency at light load and the excellent global efficiency for a two-stage architecture. The high efficiency at high load is achieved by not using synchronized rectification at the secondary side and therefore offering a very cost-effective solution.

Efficiency during active-load and light-load operation are compliant with ENERGY STAR® eligibility criteria for both external (EPA rev. 2.0 EPS) and computer integrated (EPA rev. 4.0 computers) power supply. In addition this design is even compliant with the latest computer document (EPA rev. 5.0 computers) whose effective date is July 2009.

**Figure 1. L6566A and L6563S-75W ENERGY STAR® compliant adapter demonstration board (p/n EVL6566A-75WES4)**



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# 1 Main characteristics and circuit description

The main features of the SMPS are listed as follows:

- Universal input mains range: 90÷264 Vac - frequency 45 ÷ 65 Hz
- Output voltage: 19 V at 4 A continuous operation
- Mains harmonics: according to EN61000-3-2 Class-D or JEITA-MITI Class-D
- Standby mains consumption: < 0.14 W at 230 Vac
- Active load average efficiency: better than 87% without synchronous rectification
- EMI: according to EN55022-Class-B
- Safety: according to EN60950
- Dimensions: 78 x 170 mm, 25 mm maximum height of components
- PCB: Single-side, 70 µm, CEM-1, mixed PTH/SMT

The circuit is composed of two stages: a front-end PFC using the L6563S and a flyback converter based on the L6566A. The CV/CC controller TSM1014 allows the correct current limitation on the secondary side. The flyback stage works as master and it is dedicated to control the circuit operation including the standby and protections. Additionally, it switches on and off the PFC stage by means of a dedicated pin (VCC_PFC), thus helping to achieve an excellent efficiency even at light load, with low complexity.

### PFC stage

The main function of the PFC is to keep the current absorbed from the power line tracking the line voltage to comply with the EN61000-3-2 or other similar regulations and to regulate the output voltage of the boost stage powering the downstream converter. Therefore, it is necessary to sense the PFC output voltage as well as the input coming from the mains and feed these two signals to the controller. The simplest way to implement these functions is to sense both input and output voltage through two resistor dividers as shown in *Figure 2.*

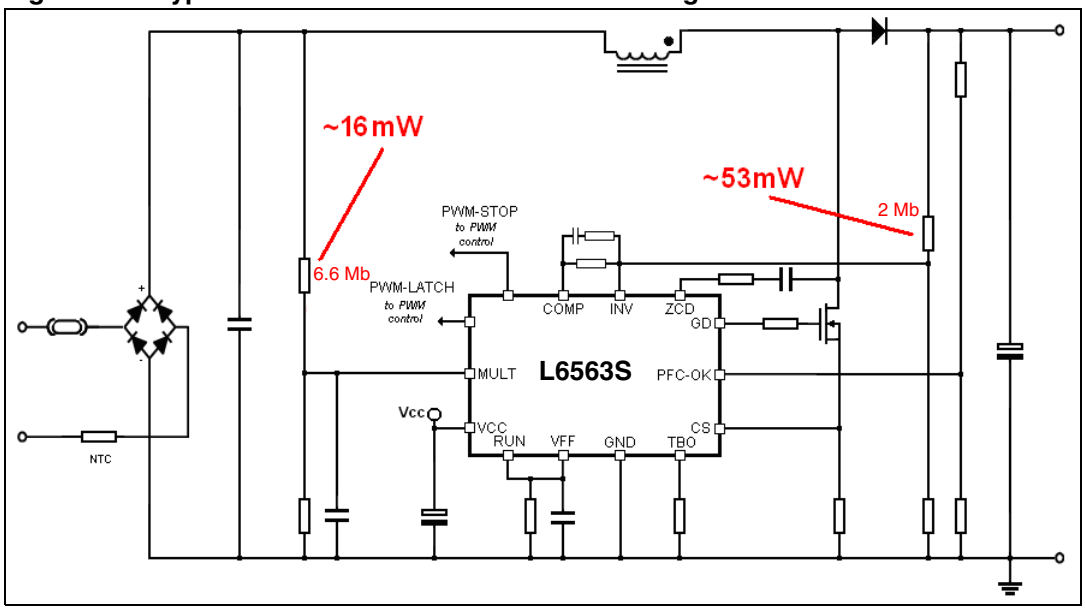
These resistors are in the MΩ range (6.6 MΩ for the input divider and 2 MΩ for the output divider of the example in the figure), however their power dissipation, which is negligible at full load, becomes significant at light load. Even if the PFC is turned off at light load, the power dissipation of the two dividers is always there. Additionally, at light load both the input and the output voltages become very close to the peak value of the rectified mains because the input and output capacitors act as peak detectors of the rectified mains voltage. Considering the worst case for power consumption, once the SMPS is working at european mains range, the power dissipation of these two dividers can be easily calculated as follows:

$$P_{MULT} = \frac{V_{IN}^2}{R_{MULT}} = \frac{\left(230V \cdot \sqrt{2}\right)^2}{6.6M\Omega} = 16mW$$

$$P_{FB} = \frac{V_{OUT}^2}{R_{MULT}} = \frac{\left(230V \cdot \sqrt{2}\right)^2}{2M\Omega} = 53mW$$

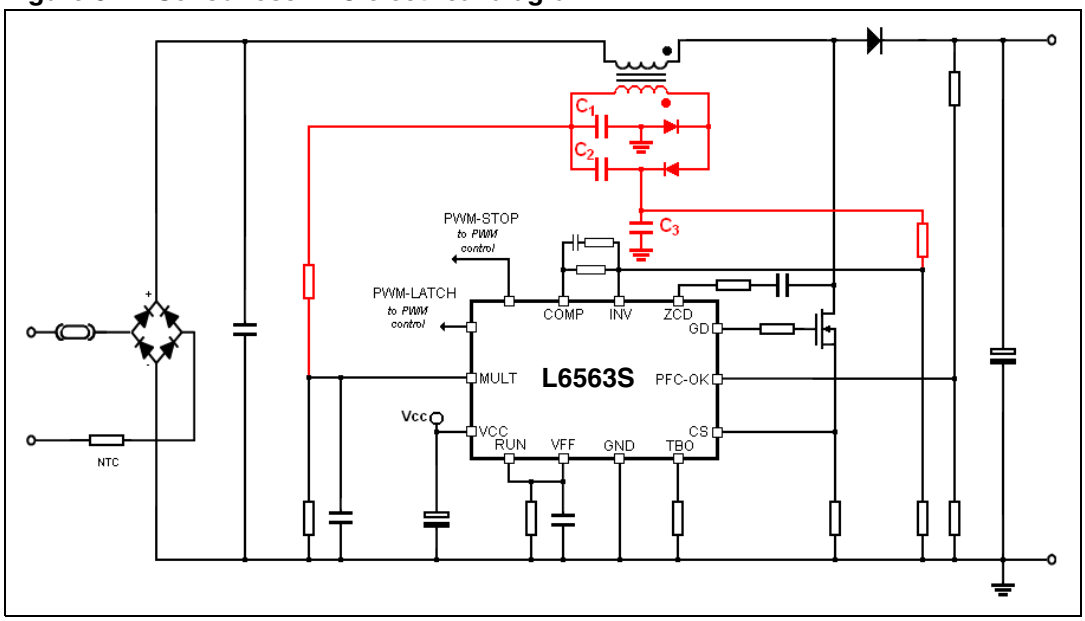
For example, if we calculate the impact of these losses with a 1 W output load, these two circuits affect the overall efficiency by about 7%.

**Figure 2. Typical transition mode PFC electrical diagram**




To overcome this problem, in this board a “sensorless” PFC solution has been implemented (*Figure 3*). The information relevant to input and output voltages is provided to the PFC controller L6563S by an auxiliary winding of the boost inductor.

**Figure 3. Sensorless PFC electrical diagram**



Operation of the “sensorless PFC” is explained as follows, referring to *Figure 4*:

a) During the MOSFET OFF-time the voltage applied across the boost inductance is the difference between the output and the input voltage. So $D_2$ is reverse biased and $C_2$ is charged via $D_1$ to:

$$V_2 = \frac{V_{out} - V_{in}}{n}$$

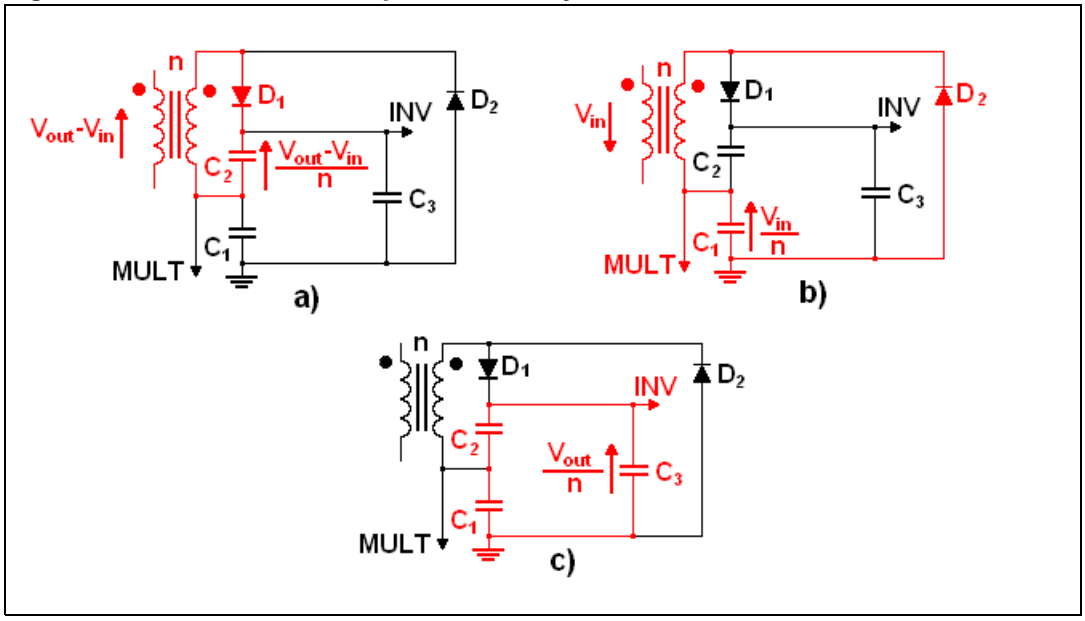
where n is the winding turns ratio.

b) During the MOSFET ON-time the voltage applied across the boost inductor is $V_{in}$ (with reversed polarity) so $D_1$ is reverse biased and the capacitor $C_1$ is charged via $D_2$ to a voltage equal to:

$$V_1 = \frac{V_{in}}{n}$$

Hence, properly selecting the time constant of the circuit, we can use the voltage across $C_1$ to feed the multiplier input of the L6563S because it is information about the instantaneous value of the input voltage which is needed by the control part to shape the input current.

**Figure 4. Sensorless PFC operation theory**




c) Because $C_3$ is in parallel to the series of $C_1$ and $C_2$, the voltage at which it is charged is proportional to the PFC output voltage and can be used to get the output voltage feedback signal:

$$V_3 = \frac{V_{out} - V_{in}}{n} + \frac{V_{in}}{n} = \frac{V_{out}}{n}$$

Of course the $C_3$ time constant has to be significantly longer than that of $C_1$ and $C_2$ in order to feed a stable feedback signal into the PFC controller error amplifier.

During light-load operation the PFC controller is stopped by the PWM controller, so the MOSFET doesn't switch and there is no reflected voltage on the auxiliary winding. $C_1$, $C_2$ and $C_3$ are no longer charged and discharged and so both the multiplier and the feedback networks do not dissipate.

The divider R3, R5, R11, R10 and R19, directly connected to the output voltage, is dedicated to protect the circuit in case of output overvoltage or open loop via pin PFC_OK (#7).

### Tracking boost option

To maximize overall efficiency the PFC makes use of the "Tracking Boost Option". With this function implemented the PFC DC output voltage changes proportionally to the mains voltage. The L6563S can implement this function by just adding a resistor (R30) connected to the dedicated pin (TBO, #6). Furthermore, the tracking boost option allows the use of a smaller (and cheaper) inductor. In this case a 400 µH inductor has been used while, with a fixed output voltage PFC working at similar operating frequency, a 700 µH inductor is needed.

### Fast voltage feed-forward

The voltage on the L6563S Vff pin (#5) is the peak value of the voltage on MULT pin (#3). The RC network (R34, C21) connected to Vff completes the peak-holding circuit. This signal is necessary to derive information from the RMS input voltage to compensate the loop gain that is mains voltage dependent.

Generally speaking, if the time constant is too small, the voltage generated is affected by a considerable amount of ripple at twice the mains frequency, causing distortion of the current reference (resulting in high THD and poor PF). If the time constant is too large there is a considerable delay in setting the right amount of feed-forward, resulting in excessive overshoot or undershoot of the pre-regulator's output voltage in response to large line voltage changes.

To overcome this issue, the L6563S implements the new fast Vff function. As soon as the voltage on the Vff pin decreases from a set threshold (40 mV typically), a mains dip is assumed and an internal switch rapidly discharges the Vff capacitor via a 10 kΩ resistor. Thanks to this feature it is possible to set an RC circuit with a long time constant, assuring a low THD, and keeping a fast response to the mains dip.

### Flyback power stage

The downstream converter, acting as the master stage, implements the ST L6566A (U6), a new dedicated current mode controller. The IC operates in quasi-resonant mode detecting the transformer demagnetization by pin ZCD (#11). R42 on pin OSC (#13) sets the maximum switching frequency at about 125 kHz. This value has been chosen to limit the switching losses.

Due to the fact that the maximum switching frequency is imposed, the converter operates in discontinuous conduction mode during light-load operation. Thanks to the L6566A valley skipping function, even in this condition, the flyback operates in valley switching, reducing switching losses. The MOSFET is a standard 800 V, STF7NM80, housed in the TO-220FP package, needing just a small heat sink. The transformer is layer type, using a standard ferrite size EER35. The transformer, designed according to EN60950, is manufactured by TDK. The flyback reflected voltage is ~130 V, providing enough room for the leakage inductance voltage spike with still margin for reliability of the MOSFET. The rectifier D8 and the transil D4 clamp the peak of the leakage inductance voltage spike at MOSFET turn-off.

The output rectifiers are two dual center tap Schottky diodes (D7 and D5) in parallel. They have been selected according to the maximum reverse voltage, forward voltage drop and power dissipation. The snubber made up of R14, R66 and C8 damps the oscillation produced by the diode capacitance and the leakage inductance. A small LC filter has been added on the output, filtering the high frequency ripple.

D17, R75÷R78, Q10 and Q15 implement an output voltage “fast discharge” circuit, discharging quickly the output capacitors when the converter is turned off. It has been implemented to quickly decrease the residual output voltage after the converter is turned off at no load.

### Startup sequence

The circuit is designed so that at startup the flyback starts first, then it turns on the PFC stage controlling the L6563S via the Vcc_PFC pin. Therefore, the flyback stage is designed to manage at startup the full output power over the entire input voltage range because it must guarantee the regulation of the output voltage even during load transitions when the load is increasing but the PFC is still not yet delivering the nominal output voltage. Of course this condition can be maintained only for a short time, typically tens of milliseconds, because the flyback is not designed to sustain this condition from a thermal point of view. The flyback controller L6566A pin #1 (HV) is directly connected to the bulk capacitor. At startup, an internal high voltage current source charges C32 and C33 until the L6566A turn-on voltage threshold is reached, then the high voltage current source is automatically switched off. As the IC starts switching it is initially supplied by C32 and C33, then the transformer auxiliary winding (pins 8-9) provide the voltage to power the IC. Afterwards, according to the load level monitored by the COMP pin, the L6566A activates the L6563S powering it via the Vcc_PFC pin.

Because the L6566A integrated HV startup circuit is turned off and therefore not dissipative during normal operation, it contributes significantly to reducing power consumption when the power supply operates at light load which in turn contributes significantly in meeting worldwide standby standards currently required.

### Brownout protection

Brownout protection prevents the circuit from working with abnormal mains levels. It can be easily achieved using pin #16 (AC_OK) of the L6566A. D6, Q3, C23, R7, R12, R26, R62 and R64 implement a circuit sensing the mains voltage peak value and feed it into L6566A pin #16. An internal comparator then enables the IC operations if the mains level is correct, within the nominal limits. If the input voltage is below 90 Vac the startup of the circuit is inhibited, while the turn-off voltage has been set at the voltage reached by the bulk capacitor after the hold-up time. The internal comparator has in fact a hysteresis allowing the L6566A turn-on and turn-off voltage to be set independently. Sensing the mains voltage before the input rectifier is a less dissipative solution with respect to sensing the bulk voltage. In addition it allows faster restart because there is no need to wait for the bulk capacitor to discharge.

The L6563S has a similar protection on the RUN pin (#10) but in this schematic it is not used because in this architecture it acts as slave, therefore the main controls are managed by the flyback stage.

### Output voltage feedback loop

The output regulation is done by means of two control loops, a voltage and a current loop working alternatively. A dedicated control IC, the TSM1014 (U5), has been used. It integrates two operational amplifiers (used as error amplifiers) and a precise voltage reference. The output signal of the error amplifiers drives an optocoupler SFH617A-4 (U3) to get the required insulation of the secondary side and modulating the voltage on COMP pin (#9) of the L6566A.

### L6566A current mode control and voltage feed-forward function

R52 and R53 sense the Q5 MOSFET current of the flyback and the signal is fed into pin #7 (CS) connected to the PWM comparator. This signal is compared with the COMP (pin #9) signal which is coming from the optocoupler.

The maximum power that the converter can deliver is set by a comparator limiting the peak of the primary current, comparing the CS and an internal threshold ($V_{CSX}$). If the current signal exceeds the threshold, the comparator limits the MOSFET duty cycle, hence the output power is also limited.

Because the maximum transferable power depends on both the primary peak current and the input voltage, in order to keep almost constant the overload set point that would change according to flyback input voltage, the L6566A implements a voltage feed-forward function via a dedicated pin. Hence, $V_{CSX}$ is modulated by the voltage on pin #15 ($V_{FF}$) sensing the bulk voltage by a resistor divider. A higher voltage causes a smaller $V_{CS,MAX}$ so that the maximum power can be kept almost constant at any input voltage.

### L6566A short-circuit protection

In case of short-circuit, an internal comparator senses the COMP pin after the soft-start at which time the COMP pin goes high, activating an internal current source that restarts charging the soft-start capacitor from the initial 2 V level. If the voltage on this pin reaches 5 V, the L6566A stops the operation and enters in the “hiccup mode”. The L6566A restarts with a startup sequence when the Vcc voltage drops below the $V_{CCrestart}$ level (5 V). Because of the long time needed by the $V_{CC}$ capacitor to drop to 5 V, the duration of the no-load operation increases, thus decreasing the power dissipation and the stress of the power components. This sequence is repeated until the short is removed following which normal operation of the converter is automatically resumed.

Another comparator, whose threshold is 1.5 V and dedicated to protecting the circuit in case of transformer saturation or secondary diodes short, is also provided. If the voltage on the CS pin (#7) exceeds this threshold two consecutive times, the IC immediately shuts down and latches off. This is intended to prevent spurious activation of the protection in case of temporary disturbances, for example during the immunity tests. Even in this case the IC operation is resumed as soon as the $V_{CC}$ voltage drops below 5 V. In this way a hiccup mode operation is still obtained, avoiding consequent failures due to overheating of the power components.

### Overvoltage protection

Pin #11 (ZCD) is connected to the auxiliary winding by a resistor divider. It implements the OVP against feedback network failures. When the ZCD pin voltage exceeds 5 V the IC is shut down. This protection can be set as latched or auto-restart by the user with no additional components. On the board it is set as latched, therefore operations can resume after a mains recycling.

### Overtemperature protection

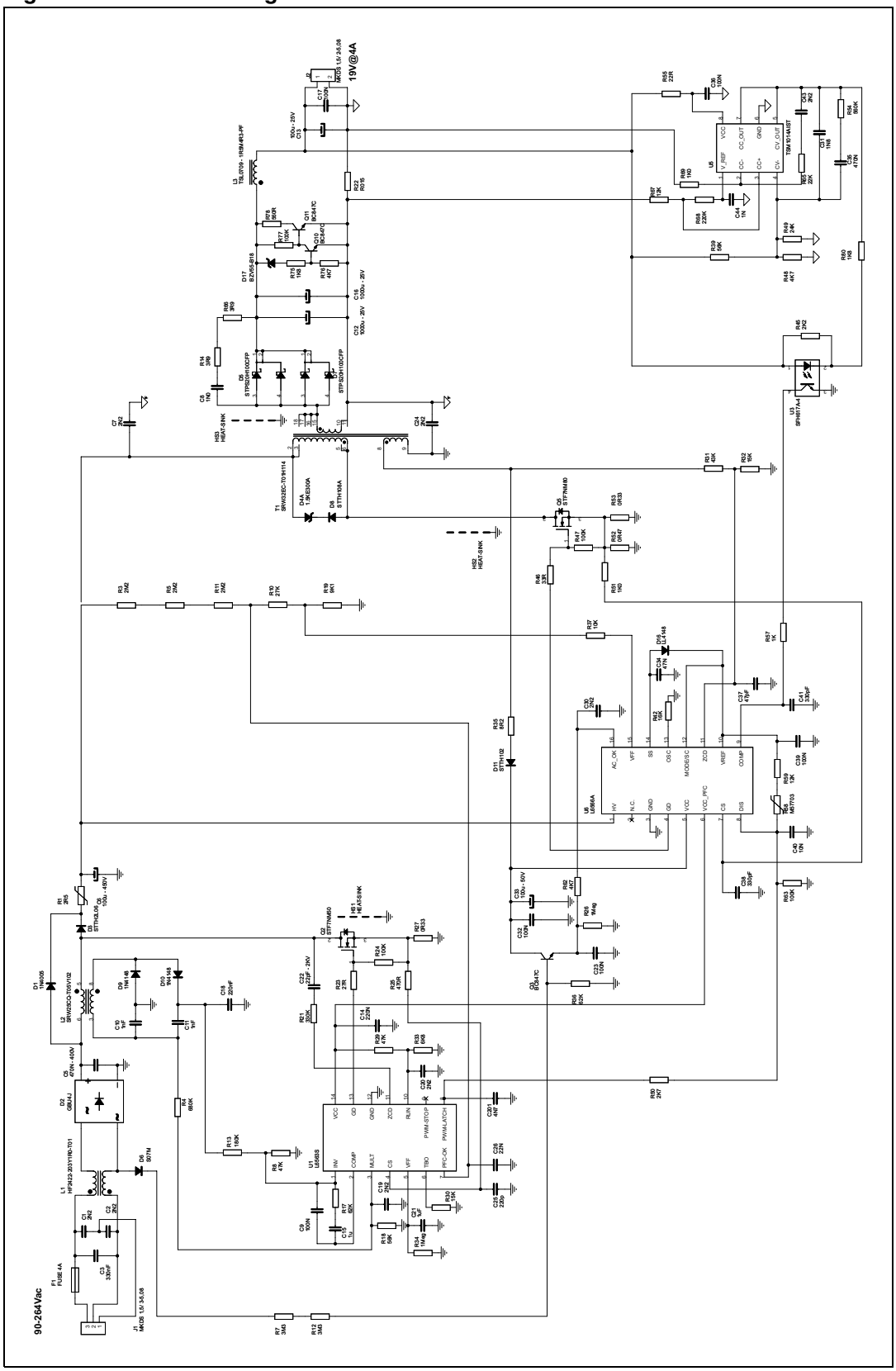
Thermistor R58, connected to L6566A DIS pin (#8), provides for a thermal protection of the flyback MOSFET (Q5). The L6563S PWM_LATCH pin (activated in case of PFC loop failures or PFC inductor saturation) is connected to L6566A DIS pin too. In case of PFC latching failure, the flyback converter activity is latched too. To maintain this state, an internal circuitry of the L6566A monitors the $V_{CC}$ and periodically reactivates the HV current source to supply the IC, while the L6563S remains inactive after latching because it is no longer powered via the Vcc_PFC pin that has been opened by the internal L6566A logic.

### Standby power savings

The L6566A implements a current mode control, thus it monitors the output power by pin COMP whose level is proportional to the load. Thus, when the voltage on pin COMP falls below an internal threshold, the controller is disabled and its consumption reduced. Normal operation restarts as soon as the COMP voltage rises again. In this way a low consumption burst mode operation is obtained.

On this board, because the flyback stage acts as master, it has been electrically designed to operate over the entire mains voltage range. This solution allows turning off the PFC controller during no-load operation, saving power. As soon as the COMP level falls below the burst mode threshold, the L6566A stops supplying the PFC controller, disabling VCC_PFC pin and reducing the PFC consumption to almost zero as already explained, minimizing the overall consumption of the converter.

**Figure 5. Electrical diagram**



# 2 Efficiency measurement

## EPA rev. 2.0 external power supply compliance

*Table 1* shows the no-load consumption and the overall efficiency, measured at the nominal mains voltages. As shown, these values are fully compliant with the EPA rev 2.0 external power supply limits, requiring an average efficiency higher than 87% for output load between 25% and 100% of the nominal load and no-load consumption lower than 500 mW.

In particular at no load the power consumption is very low, in fact at 230 Vac, it is just 136 mW and at 115 Vac it is 83 mW.

**Table 1. Overall efficiency compared to "EPA rev. 2.0 EPS"**

| Notes | 230 V-50 Hz | | | | | 115 V-60 Hz | | | | | EPA2 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Vout [V] | Iout [mA] | Pout [W] | Pin [W] | Eff. | Vout [V] | Iout [mA] | Pout [W] | Pin [W] | Eff. | | |
| No-load consumption | 19.08 | 0.00 | 0.00 | 0.136 | ------ | 19.09 | 0.00 | 0.00 | 0.083 | ------ | <0.5W | Pass |
| 25% load eff. | 19.12 | 980 | 18.73 | 22.37 | 83.7% | 19.10 | 983 | 18.76 | 21.50 | 87.3% | 87.0% | |
| 50% load eff. | 19.13 | 1960 | 37.50 | 42.87 | 87.5% | 19.11 | 1963 | 37.52 | 42.12 | 89.1% | 87.0% | |
| 75% load eff. | 19.16 | 2936 | 56.23 | 63.31 | 88.8% | 19.13 | 2942 | 56.26 | 63.33 | 88.8% | 87.0% | |
| 100% load eff. | 19.15 | 3917 | 75.01 | 84.07 | 89.2% | 19.14 | 3920 | 75.00 | 85.26 | 88.0% | 87.0% | |
| Average active load eff. | | | | | 87.3% | | | | | 88.3% | 87.0% | Pass |

## EPA rev. 4.0 computers power supply compliance

Different from the previous EPS regulation, the "EPA rev. 4.0 computers" requires a minimum efficiency higher than 80%, measured at 20%, 50% and 100% of nominal load. In *Table 2* the comparison of the overall efficiency measurements with the "EPA rev. 4.0 computers" requirements is given.

**Table 2. Overall efficiency compared to "EPA rev. 4.0 computers"**

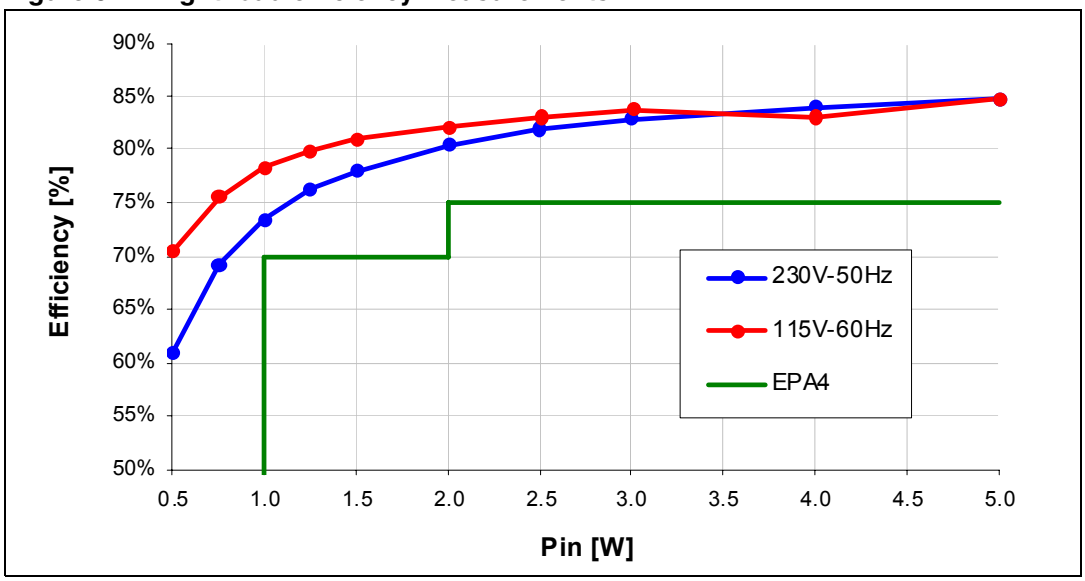
| Notes | 230 V-50 Hz | | | | 115 V-60 Hz | | | | | | EPA4 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Vout [V] | Iout [mA] | Pout [W] | Pin [W] | Eff. | Vout [V] | Iout [mA] | Pout [W] | Pin [W] | Eff. | | |
| 20% load Eff. | 19.12 | 785 | 15.02 | 18.17 | 82.6% | 19.10 | 785 | 14.99 | 17.39 | 86.2% | 80.0% | PASS |
| 50% load Eff. | 19.13 | 1960 | 37.50 | 42.87 | 87.5% | 19.11 | 1963 | 37.52 | 42.12 | 89.1% | 80.0% | PASS |
| 100% load Eff. | 19.15 | 3917 | 75.01 | 84.07 | 89.2% | 19.14 | 3920 | 75.00 | 85.26 | 88.0% | 80.0% | PASS |

Additionally, the "EPA rev.4.0 computers" document poses specific limitations to the maximum consumption of computers during standby mode, sleep mode and idle state but this is not sufficient to deduce the required power supply efficiency because the load applied during these states is not indicated. This information comes from computer manufacturer

requirements. The major computer manufacturers require efficiency higher than 70% from 1 W to 2 W input power and efficiency higher than 75% from 2 W to 3 W input power.

*Figure 6* shows the demonstration board's measured efficiency at light load, comparing it with requirements coming from the reference ENERGY STAR® document.

**Figure 6. Light-load efficiency measurements**




## EPA rev. 5.0 computers power supply compliance

As indicated in *Table 3*, this converter is also compliant with the newer, most stringent "EPA rev. 5.0 computers" limits for active-load efficiency.

**Table 3. Overall efficiency compared to "EPA rev. 5.0 computers"**

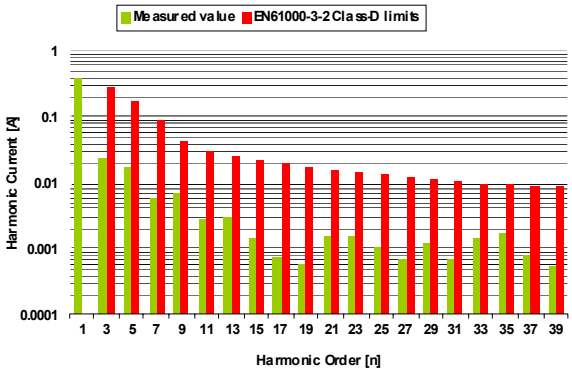
| Notes | 230V-50Hz | | | | | 115V-60Hz | | | | | EPA5 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Vout [V] | Iout [mA] | Pout [W] | Pin [W] | Eff. | Vout [V] | Iout [mA] | Pout [W] | Pin [W] | Eff. | | |
| 20% load eff. | 19.12 | 785 | 15.02 | 18.17 | 82.6% | 19.10 | 785 | 14.99 | 17.39 | 86.2% | 82.0% | PASS |
| 50% load eff. | 19.13 | 1960 | 37.50 | 42.87 | 87.5% | 19.11 | 1963 | 37.52 | 42.12 | 89.1% | 85.0% | PASS |
| 100% load eff. | 19.15 | 3917 | 75.01 | 84.07 | 89.2% | 19.14 | 3920 | 75.00 | 85.26 | 88.0% | 82.0% | PASS |

This latest ENERGY STAR® document, whose effective date is July 2009, introduces a new method of testing the energy performance of computers. It sets a limitation on typical energy consumption (TEC) of computers which is a value for typical annual electricity use, by measurements of average operational mode power levels scaled by an assumed typical usage model (duty cycle). This new approach, like the previous one, does not establish direct limits to the power supply minimum efficiency for each different state. In fact it depends on the actual load applied by computer itself. At the moment this application note has been written, not all the major computer manufacturers have produced specific requirements for EPA rev. 5.0 compliant designs. Anyway, the good margin achieved against the EPA rev. 4.0 limits proves that this board can be a viable solution even for upcoming EPA 5 computer designs.

# 3 Harmonic content measurement

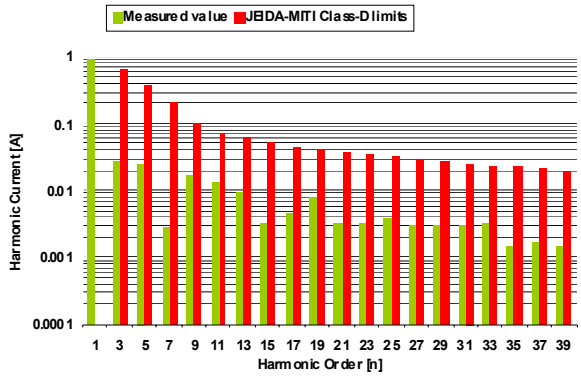
The board has been tested according to the european regulation EN61000-3-2 Class-D and Japanese regulation JEITA-MITI Class-D, at both the nominal input voltage mains. As shown in *Figure 7* and *8*, the circuit is able to reduce the harmonics well below the limits of both regulations.

**Figure 7. EVL6566A-75WES4 compliance to EN61000-3-2 standard at 230 Vac-50 Hz, full load**




THD = 5.95% - PF = 0.978

**Figure 8. EVL6566A-75WES4 compliance to JEITA-MITI standard at 100 Vac-50 Hz, full load**




THD = 4.52% - PF = 0.991

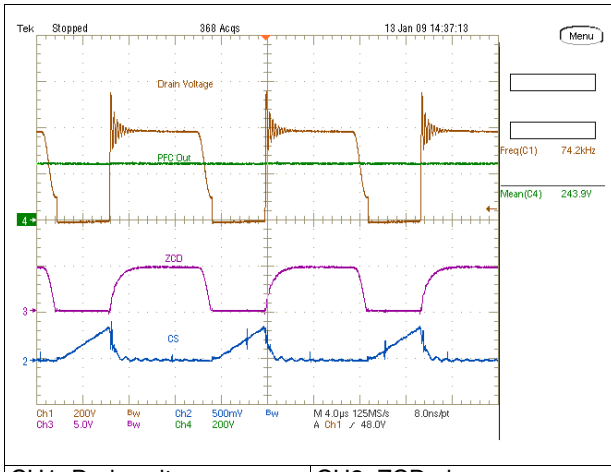
At the bottom of the diagrams the total harmonic distortion and power factor have been measured too. The values in all conditions give a clear idea of the correct function of the PFC.

# 4 Functional check

The following figures show some flyback waveforms during steady-state operation and the L6563S TBO function is depicted, setting different PFC output voltages according to the mains input voltage.

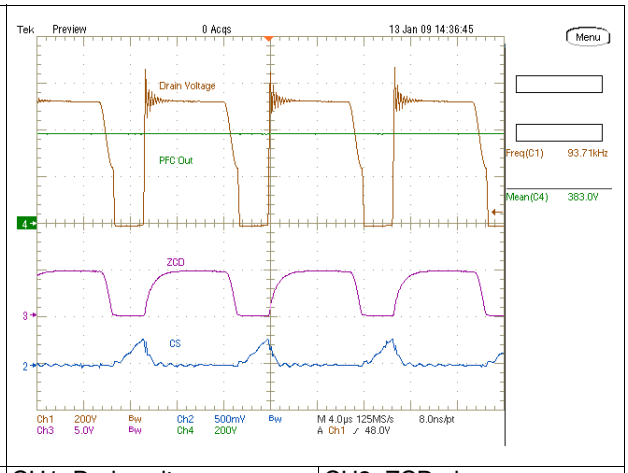
At nominal load conditions, in *Figure 9* and *Figure 10*, we note that the ZCD negative-going edge triggers the MOSFET's turn-on, allowing quasi-resonant operation.

**Figure 9. Flyback stage waveforms at 115 V-60 Hz - full load**




| | |
|---|---|
| CH1: Drain voltage<br>CH2: CS pin voltage | CH3: ZCD pin<br>CH4: PFC output |

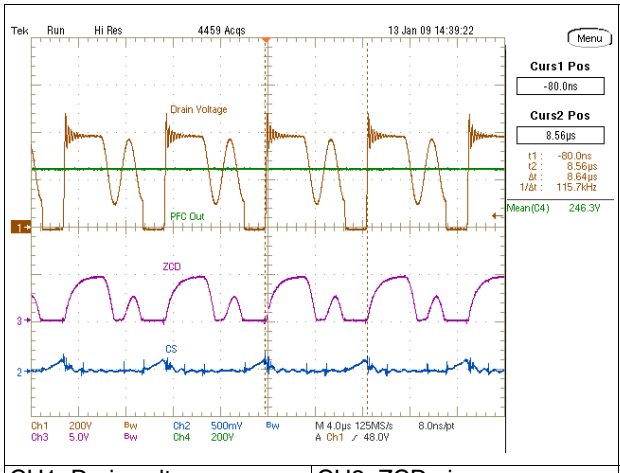
**Figure 10. Flyback stage waveforms at 230 V -50 Hz - full load**




| | |
|---|---|
| CH1: Drain voltage<br>CH2: CS pin voltage | CH3: ZCD pin<br>CH4: PFC output |

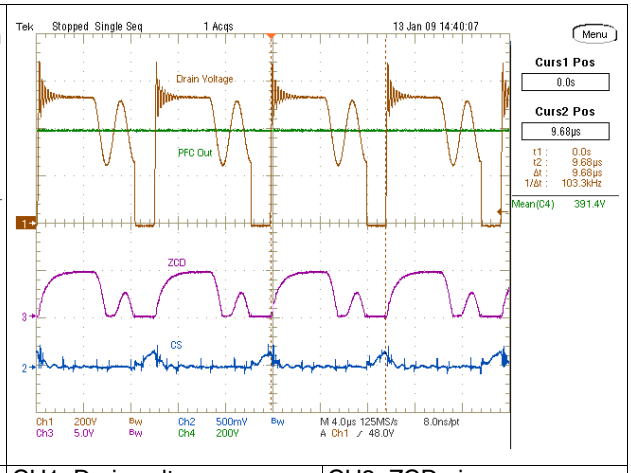
*Figure 11* and *Figure 12* show operation at 20 W. As indicated before, maximum switching frequency has been set at 125 kHz. For this reason, the L6566A skips the first valley signal on ZCD and switches on the MOSFET at the second negative-going edge.

**Figure 11. Flyback stage waveforms at 115 V-60 Hz - 20 W load**




| | |
|---|---|
| CH1: Drain voltage<br>CH2: CS pin voltage | CH3: ZCD pin<br>CH4: PFC output |

**Figure 12. Flyback stage waveforms at 230 V -50 Hz - 20 W load**

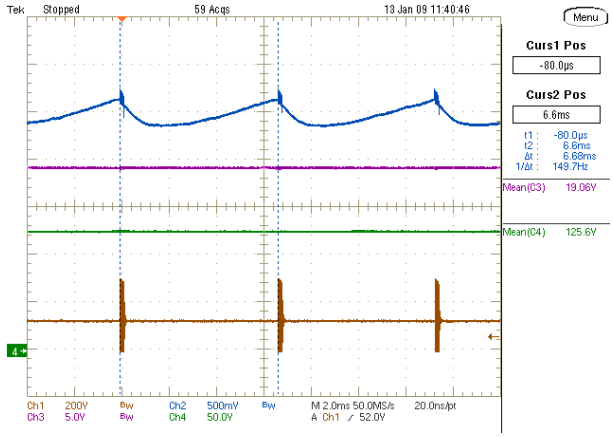



| | |
|---|---|
| CH1: Drain voltage<br>CH2: CS pin voltage | CH3: ZCD pin<br>CH4: PFC output |

### Standby and no-load operation

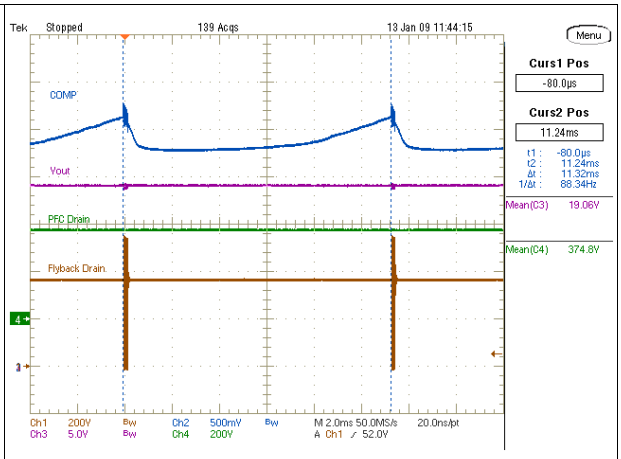
In *Figure 13* and *Figure 14*, some no-load waveforms are given. As shown, the L6566A works in burst mode. When the feedback voltage at pin COMP falls below 2.65 V (typical), the IC is disabled and its consumption is reduced. The chip is re-enabled as the voltage on pin COMP rises again over this threshold. Additionally, in order to get the best efficiency, during light-load operation the PFC stage is turned off. In fact when the voltage on pin COMP falls below the burst mode threshold, the L6566A pin #6 (Vcc_PFC) supplying the PFC controller, is opened. Thus the residual consumption of the PFC control circuitry is minimized to a negligible level. Whenever the IC is shut down, either latched or not, the Vcc_PFC pin is open as well.

**Figure 13. No-load operation at 90 V-60 Hz**




| | |
|---|---|
| CH1: Flyback drain<br>CH2: COMP pin | CH3: Output voltage<br>CH4: PFC drain |

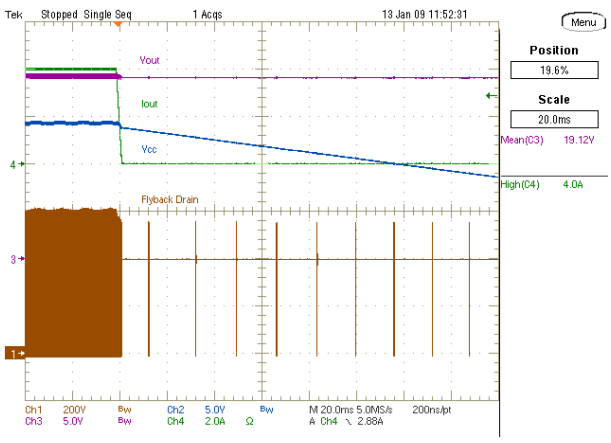
**Figure 14. No-load operation at 265 V-50 Hz**




| | |
|---|---|
| CH1: Flyback Drain<br>CH2: COMP pin | CH3: Output voltage<br>CH4: PFC drain |

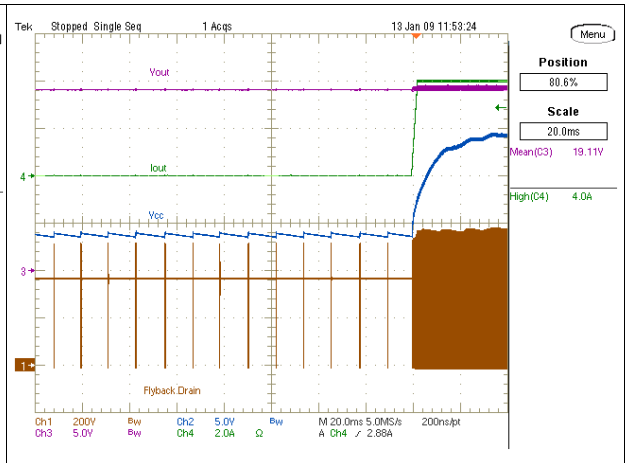
In *Figure 15* and *Figure 16* the transitions from full load to no load and vice versa at maximum input voltage have been checked. The maximum input voltage has been chosen because it is the most critical input voltage for transition. In fact at no load the burst pulses have lower repetition frequency and Vcc could drop, causing restart cycles of the controller. As visible in the graphs, both transitions are clean and there isn't any output voltage or Vcc dip.

**Figure 15. Transition full load to no load at 265 Vac-50 Hz**




| CH1: Drain voltage<br>CH2: Vcc | CH3: Output voltage<br>CH4: Output current |
|---|---|

**Figure 16. Transition no load to full load at 265 Vac-50 Hz**




| CH1: Drain voltage<br>CH2: Vcc | CH3: Output voltage<br>CH4: Output current |
|---|---|

## Overcurrent and short-circuit protection

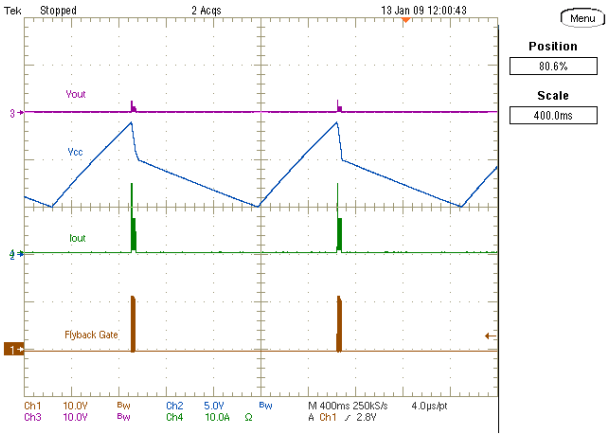
In this demonstration board the overcurrent is managed by TSM1014 (U5), a CC/CV controller. Inside the IC there are a voltage reference and two Or-ed operational amplifiers, one dedicated to act as the error amplifier of the voltage loop, the second is dedicated to act as the error amplifier of the current loop. During normal operation the voltage feedback loop is working while, in case the output current exceeds the programmed value, the current loop error amplifier takes over, thus keeping constant the output current.

In case of a dead-short, the current cannot be limited effectively by U5 because the output voltage drops so it is not powered, therefore the primary controller must manage the failure condition.

In case of output short, there are two different possible situations that the controller has to handle. If the coupling between the secondary winding and the auxiliary winding is good enough, as soon as the output voltage drops, the auxiliary voltage drops as well and the IC supply voltage falls below the undervoltage lockout threshold, causing the L6566A to disable. The controller stops switching and remains in the off-state until the voltage on the Vcc pin decreases below the Vcc restart threshold (5 V). Then, the HV startup turns on and charges the Vcc capacitor. As soon as the turn-on threshold is reached, the circuit restarts. If the short is still there, the circuit just attempts to restart but it stops in a few milliseconds. Restart attempts are repeated indefinitely, until the short is removed. This provides a very low frequency hiccup working mode (for this board 0.5 Hz), limiting the current flowing at secondary side (less than 1 Arms) preventing the power supply from overheating, which could destroy it.

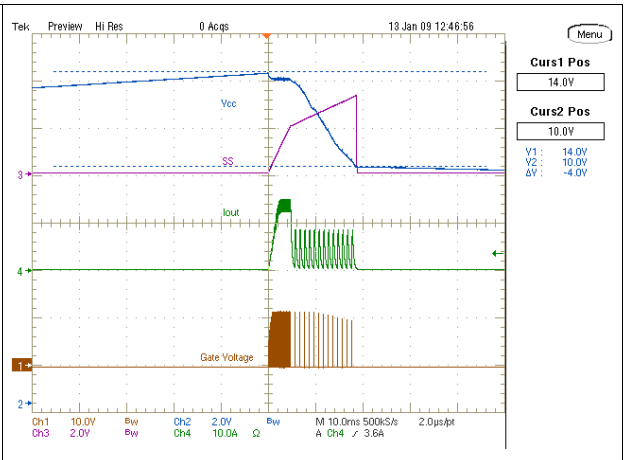
In case the leakage inductance between auxiliary and secondary winding is not negligible, some spikes on the auxiliary voltage could keep Vcc above the UVLO threshold for a time long enough to damage the converter. In this case L6566A detects a short-circuit monitoring the control pins. When the output voltage drops and consequently pin COMP saturates high, the soft-start capacitor is charged by an internal current source. When the Vss voltage reaches an internal disable threshold (5 V), the controller stops switching and starts operating in hiccup mode as described above.

**Figure 17. Short-circuit at full load and 230 Vac - 50 Hz**




| CH1: Gate voltage<br>CH2: Vcc | CH3: SS pin voltage<br>CH4: Output current |
|---|---|

**Figure 18. Short-circuit details at full load and 230 Vac - 50 Hz**




| CH1: Drain voltage<br>CH2:Vcc | CH3: SS pin voltage<br>CH4: Output current |
|---|---|

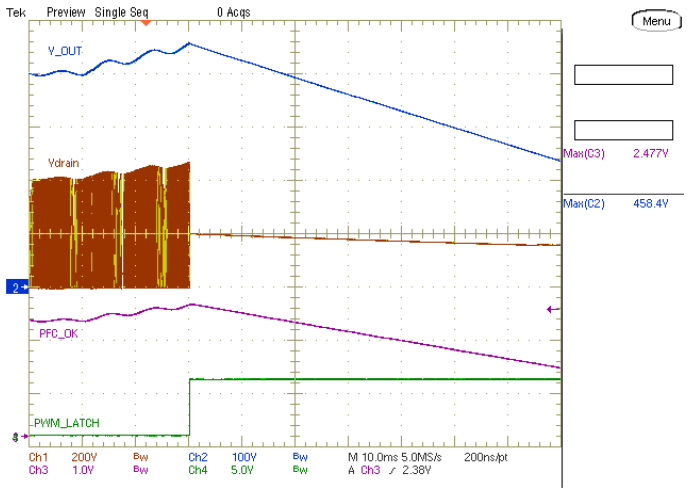
In *Figure 18* we can see that, in this case, the IC supply voltage drops to the UVLO threshold (10 V) causing controller turn-off before the SS pin signal attains the disable threshold (5 V). This happens because the transformer leakage inductance is very low and as soon as the output voltage drops, the auxiliary voltage drops immediately as well. Furthermore from the graph we can note that, during the SS voltage ramp-up, the transferred power is limited.

### Overvoltage and open loop protection

The EVL6566A-75WES4 board implements two different open loop protections, one for each stage.

The PFC controller L6563S is equipped with an OVP monitoring the output voltage by the PFC_OK (#7) pin with a resistor divider (R3, R5, R11 high, R10 and R19 low). This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value (455 V in this case). When this function is triggered, the gate drive activity is immediately stopped and it restarts as the voltage on the pin falls below 2.4 V. This function protects the bulk capacitor from voltage surges caused by abrupt load/line changes or startup overshoot. Because, in this case no failure occurred, the controller restarts as the output voltage falls below the overvoltage threshold. However, if the voltage on pin INV falls below 1.66 V (typ.) a feedback failure is assumed. In this case the device is latched off. Normal operation can be resumed only by cycling Vcc, bringing its value lower than 6 V, before moving up to turn-on threshold. At the same time the pin PWM_LATCH (pin #8) is asserted high. This pin is an open source output intended for tripping a latched shutdown function of the PWM controller IC in the cascaded DC-DC converter, so that the entire unit is latched off. On this board the PWM_LATCH is connected to the DIS pin of the L6566A.

**Figure 19. EVL6566-75WES4 PFC open loop at 115 Vac-60 Hz - full load**




| | |
|---|---|
| CH1: Drain voltage<br>CH2: PFC output voltage | CH3: PFC_OK pin voltage<br>CH4: PWM_LATCH pin voltage |

To restart the system the input power must be recycled.

Additionally, if the voltage on pin PFC_OK is tied below 0.23 V, the L6563S is shut down. In this case both PWM_STOP and PWM_LATCH keep their high impedance status. To restart the IC simply let the voltage at the pin go above 0.27 V. This function can be used as a remote on/off control input.

Note that this function offers a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. If either resistor of the PFC_OK divider fails short or opens or the PFC_OK (#7) pin is floating, this results in shutting down the L6563S and stopping the controller operation of the flyback stage.

The event of an open loop is given in *Figure 19*. We can notice the protection intervention stopping the operation of the L6563S and the activation of the PWM_LATCH pin that is connected to the L6566A pin #7 (DIS). This function of the L6566A is a latched device shutdown. Internally the pin connects a comparator that, when the voltage on the pin exceeds 4.5 V, shuts down the IC and brings its consumption to a value barely higher than before startup. The internal L6566A logic opens also the pin Vcc_PFC, therefore the L6563S remains inactive after latching because it is no longer powered.

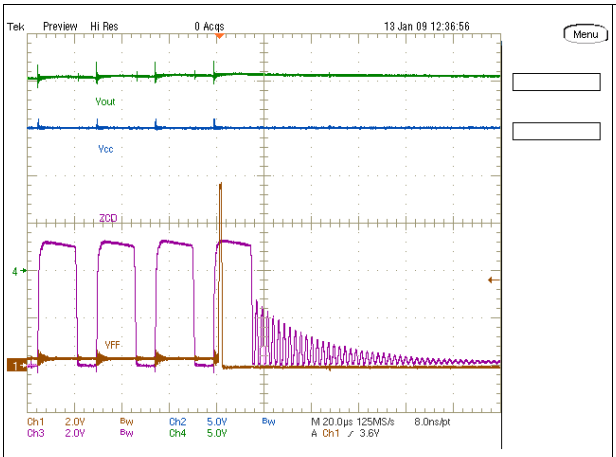
This state is latched and the input power must be recycled in order to restart the IC. The latch is removed as the voltage on the AC_OK goes below the brownout threshold.

The flyback stage is also protected against open loop conditions that lead to losing control of the output voltage.

The L6566A OVP function monitors the voltage on the ZCD pin (#11) during the MOSFET's off-time, during which the voltage generated by the auxiliary winding is proportional to the converter's output voltage. If the voltage on the pin exceeds an internal 5 V reference, an overvoltage condition is assumed and the device is shut down. An internal current generator is activated that sources 1 mA out of the VFF pin (#15). If the VFF voltage is allowed to reach 2 VBE over 5 V, the L6566A is latched off (*Figure 20*). As soon as the IC is latched, VCC starts decreasing until it reaches a value 0.5 V below the turn-on threshold. Then the

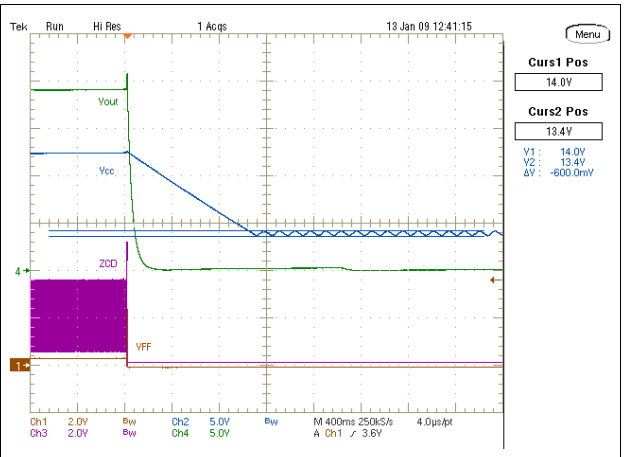
HV startup circuit turns on and begins to operate periodically in order to keep VCC between VCCON and VCCON-0.5 V (*Figure 21*) maintaining the IC latched.

**Figure 20. Flyback open loop at 230 V-50 Hz half load**




| | |
|---|---|
| CH1: VFF voltage<br>CH2: Vcc | CH3: ZCD voltage<br>CH4: Output voltage |

**Figure 21. Flyback open loop at 230 V-50 Hz half load**

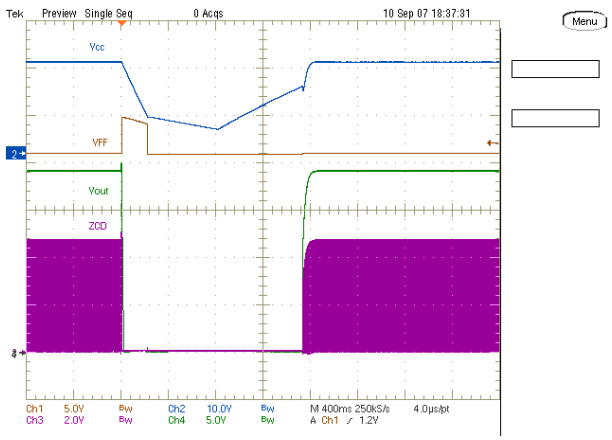



| | |
|---|---|
| CH1: VFF voltage<br>CH2: Vcc | CH3: ZCD voltage<br>CH4: Output voltage |

If R37 is shorted, the impedance externally connected to pin #15 (VFF) is lower and the voltage in case of OVP cannot reach the 5+2VBE threshold, so the L6566A restarts after VCC has dropped below 5 V (*Figure 22*). In case of L6566A OVP intervention, the L6563S operation is also stopped because the L6566A stops the PFC via the Vcc_PFC pin.

Additionally, to improve the immunity against temporary disturbances (needed for example in case of immunity tests), an internal logic activates the protection after the OVP has been detected for 4 consecutive switching cycles.

**Figure 22. Flyback open loop - restart option 230 Vac 50 Hz - half load**




| | |
|---|---|
| CH1: VFF voltage<br>CH2: Vcc | CH3: ZCD voltage<br>CH4: Output voltage |

In the following table the output voltage at OVP intervention are given. The measures therefore demonstrate that, as previously explained, the L6566A sensing technique provides a very stable OVP intervention threshold over the entire mains voltage and load ranges.

**Table 4. Output voltage at OVP intervention vs. input voltage and output power**

| Input voltage | Output power | Output voltage at OVP intervention |
|---|---|---|
| 115 V | 75 W | 20.45 V |
| 115 V | 35 W | 20.36 V |
| 115 V | 0 W | 20.74 V |
| 230 V | 75 W | 20.61 V |
| 230 V | 35 W | 20.55 V |
| 230 V | 0 W | 20.83 V |

# 5 Thermal map

In order to check the design reliability, a thermal mapping by means of an IR camera was done. *Figure 23* and *24* show the thermal measures of the board, component side, at nominal input voltage. Some pointers visible on the pictures have been placed across key components or components showing high temperature. The ambient temperature during both measurements was 27 °C.

All other components of the board are working within the temperature limits, assuring a reliable long-term operation of the power supply.

**Figure 23. Thermal map at 115 Vac-60 Hz - full load**

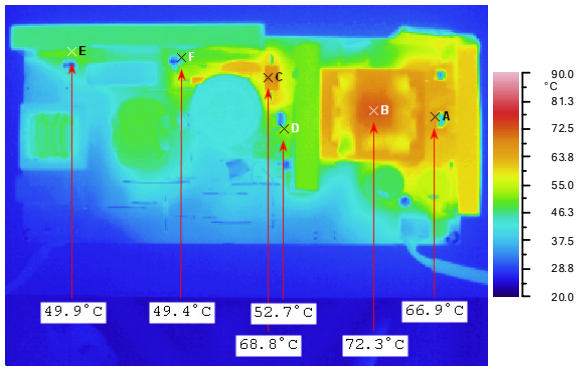



**Figure 24. Thermal map at 230 Vac-50 Hz - full load**

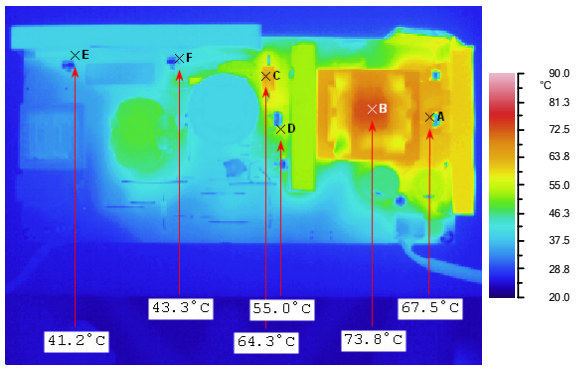



**Table 5. Thermal maps reference points**

| Point | Reference | Description |
|---|---|---|
| A | D6 | Output rectifier |
| B | T1 | Flyback power transformer |
| C | D4A | Flyback transformer clamping transil |
| D | Q5 | Flyback switch |
| E | D2 | Input bridge rectifier |
| F | Q2 | PFC switch |

# 6 Conducted emission pre-compliance test

*Figure 25* and *26* show the average measurement of the conducted noise at full load and nominal mains voltages. The limits shown in the diagrams are from EN55022 Class-B, which is the most popular regulation for domestic equipment and it has more stringent limits compared to those of Class-A, dedicated to IT equipment. As visible in the diagrams, in all test conditions the measures are within the limits.

**Figure 25. CE average measure at 115 Vac and full load**

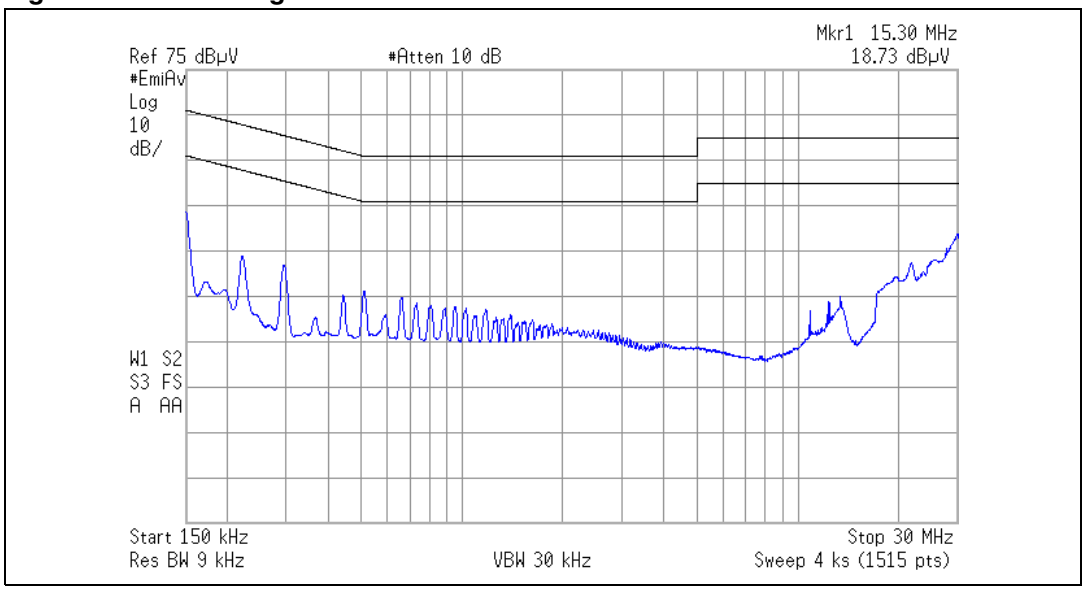
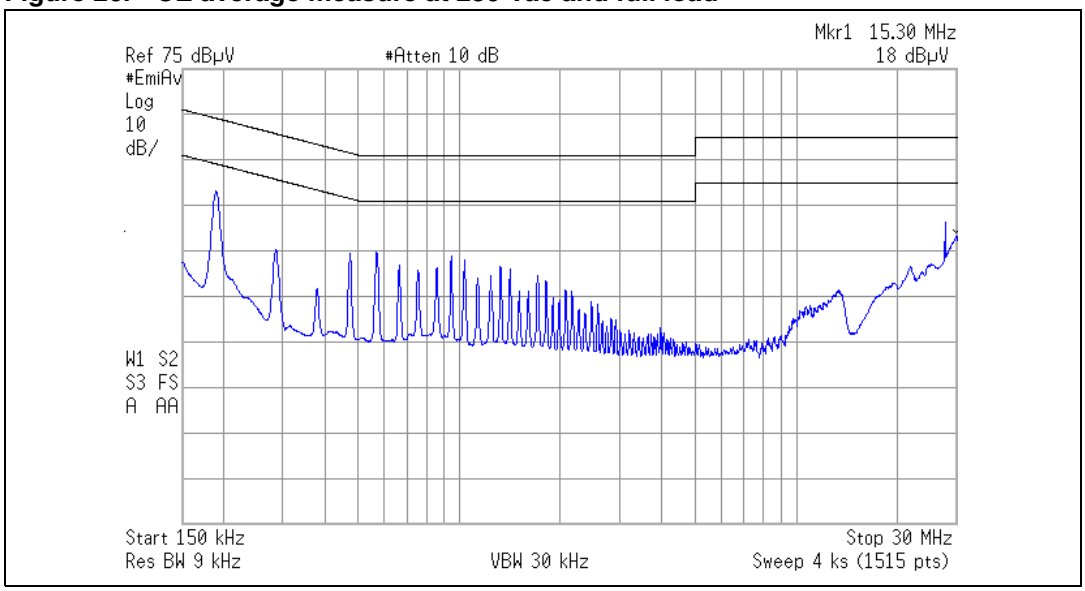



**Figure 26. CE average measure at 230 Vac and full load**



# 7 Bill of material

**Table 6. Bill of material**

| Des. | Part type / part value | Description | Supplier | Case style / package |
|---|---|---|---|---|
| C1 | 2n2F | Y1 - safety cap. DE1E3KX222M | Murata | DWG |
| C2 | 2n2F | Y1 - safety cap. DE1E3KX222M | Murata | DWG |
| C3 | 330nF | X2 - flm cap - R46-I 3470--M1- | Arcotronics | DWG |
| C5 | 470nF - 400V | 400V - flm cap - B32653A4474 | EPCOS | DWG |
| C6 | 100µF - 450V | 450V - aluminium elcap - LLS series - 85°C | Nippon-chemicon | 25X25 mm |
| C7 | 2n2F | Y1 - safety cap. DE1E3KX222M | Murata | DWG |
| C8 | 1nF | 200V cercap - general purpose | AVX | 1206 |
| C9 | 100nF | 50V cercap - general purpose | AVX | 0805 |
| C10 | 1nF | 50V cercap - general purpose | AVX | 1206 |
| C11 | 1nF | 50V cercap - general purpose | AVX | 1206 |
| C12 | 1000µF - 25V | 25V - aluminium elcap - ZL series - 105°C | Rubycon | DWG |
| C13 | 100µF - 25V | 25V - aluminium elcap - YXF series - 105°C | Rubycon | DWG |
| C14 | 220nF | 50V cercap - general purpose | AVX | 1206 |
| C15 | 1µF | 25V cercap - general purpose | AVX | 0805 |
| C16 | 1000uF - 25V | 25V - aluminium elcap - ZL series - 105°C | Rubycon | DWG |
| C17 | 100nF | 50V cercap - general purpose | AVX | 0805 |
| C18 | 220nF | 100V cercap - general purpose | AVX | 1206 |
| C19 | 2n2F | 50V cercap - general purpose | AVX | 1206 |
| C20 | 2n2F | 50V cercap - general purpose | AVX | 1206 |
| C21 | 1uF | 25V cercap - general purpose | AVX | 0805 |
| C22 | 22pF - 2KV | 2KV cap - DEA1X3D220JC1B | Murata | 5mm |
| C23 | 100nF | 50V cercap - general purpose | AVX | 0805 |

**Table 6. Bill of material (continued)**

| Des. | Part type / part value | Description | Supplier | Case style / package |
|---|---|---|---|---|
| C24 | 2n2F | Y1 - safety cap. DE1E3KX222M | Murata | DWG |
| C25 | 220pF | 50V cercap - general purpose | AVX | 0805 |
| C26 | 22nF | 50V cercap - general purpose | AVX | 0805 |
| C30 | 2n2F | 50V cercap - general purpose | AVX | 1206 |
| C31 | 1n8F | 50V cercap - general purpose | AVX | 0805 |
| C32 | 100nF | 50V cercap - general purpose | AVX | 1206 |
| C33 | 100uF - 50V | 50V - aluminium elcap - YXF series - 105°C | Rubycon | DWG |
| C34 | 47nF | 50V cercap - general purpose | AVX | 1206 |
| C35 | 470nF | 50V cercap - general purpose | AVX | 0805 |
| C36 | 100nF | 50V cercap - general purpose | AVX | 0805 |
| C37 | 47pF | 50V cercap - general purpose | AVX | 1206 |
| C38 | 330pF | 50V cercap - general purpose | AVX | 0805 |
| C39 | 100nF | 50V cercap - general purpose | AVX | 1206 |
| C40 | 10nF | 50V cercap - general purpose | AVX | 1206 |
| C41 | 330pF | 50V cercap - general purpose | AVX | 1206 |
| C43 | 2n2F | 50V cercap - general purpose | AVX | 1206 |
| C44 | 1nF | 50V cercap - general purpose | AVX | 0805 |
| C201 | 4n7F | 50V cercap - general purpose | AVX | PTH |
| D1 | 1N4005 | Rectifier - general purpose | Vishay | DO-41 |
| D2 | GBU4J | Single phase bridge rectifier | Vishay | GBU STYLE |
| D3 | STTH2L06 | Ultrafast high voltage rectifier | STMicroelectronics | DO-41 |
| D4A | 1.5KE300A | Transil | STMicroelectronics | DO - 201 |
| D5 | STPS20H100CFP | High voltage power Schottky rectifier | STMicroelectronics | TO - 220FP |
| D6 | S07M | High voltage rectifier | Vishay | SMA |
| D7 | STPS20H100CFP | High voltage power Schottky rectifier | STMicroelectronics | TO - 220FP |

**Table 6. Bill of material (continued)**

| Des. | Part type / part value | Description | Supplier | Case style / package |
|---|---|---|---|---|
| D8 | STTH108A | High voltage ultrafast rectifier | STMicroelectronics | SMA |
| D9 | LL4148 | Fast switching diode | Vishay | MINIMELF |
| D10 | LL4148 | Fast switching diode | Vishay | MINIMELF |
| D11 | STTH102 | Fast switching diode | STMicroelectronics | DO-41 |
| D16 | LL4148 | Fast switching diode | Vishay | MINIMELF |
| D17 | BZV55-B18 | Zener diode | Philips | MINIMELF |
| F1 | Fuse 4A | Fuse T4A - time delay | Wichmann | DWG |
| HS1 | Heat-sink | | | DWG |
| HS2 | Heat-sink | | | DWG |
| HS3 | Heat-sink | | | DWG |
| J1 | MKDS 1,5/ 3-5,08 | PCB term. block, screw conn., pitch 5mm - 3 W. | Phoenix contact | DWG |
| J2 | MKDS 1,5/ 2-5,08 | PCB term. block, screw conn., pitch 5mm - 2 W. | Phoenix contact | DWG |
| L1 | HF2422-203Y1R0-T01 | Input EMI filter | TDK | DWG |
| L2 | SRW25CQ-T05V102 | PFC inductor | TDK | DWG |
| L3 | TSL0709 - 1R5M4R3-PF | 1u5F - radial inductor | TDK | DWG |
| Q2 | STF7NM50 | N-channel power MOSFET | STMicroelectronics | TO-220FP |
| Q3 | BC847C | NPN small signal BJT | ZETEX | SOT-23 |
| Q5 | STF7NM80 | N-channel power MOSFET | STMicroelectronics | TO-220FP |
| Q10 | BC847C | NPN small signal BJT | Zetex | SOT-23 |
| Q11 | BC847C | NPN small signal BJT | Zetex | SOT-23 |
| R1 | 2R5 | NTC resistor - S237 | EPCOS | DWG |
| R3 | 2M2 | SMD standard film res - 1/4W - 1% - 100ppm/°C | Vishay | 1206 |
| R4 | 680K | SMD standard film res - 1/8W - 1% - 100ppm/°C | Vishay | 0805 |
| R5 | 2M2 | SMD standard film res - 1/4W - 1% - 100ppm/°C | Vishay | 1206 |
| R7 | 3M3 | SMD standard film res - 1/4W - 1% - 100ppm/°C | Vishay | 1206 |

**Table 6. Bill of material (continued)**

| Des. | Part type / part value | Description | Supplier | Case style / package |
|---|---|---|---|---|
| R8 | 47K | SMD standard film res - 1/8W - 1% - 100ppm/°C | Vishay | 0805 |
| R10 | 27K | SFR25 axial stand. film res - 0.4W - 1% - 100ppm/°C | Vishay | PTH |
| R11 | 2M2 | SFR25 axial stand. film res - 0.4W - 1% - 100ppm/°C | Vishay | PTH |
| R12 | 3M3 | SMD standard film res - 1/4W - 1% - 100ppm/°C | Vishay | 1206 |
| R13 | 180K | SMD standard film res - 1/4W - 1% - 100ppm/°C | Vishay | 1206 |
| R14 | 3R9 | SMD standard film res - 1/4W - 5% - 250ppm/°C | Vishay | 1206 |
| R17 | 62K | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R18 | 56K | SMD standard film res - 1/4W - 5% - 250ppm/°C | Vishay | 1206 |
| R19 | 9K1 | SMD standard film res - 1/4W - 1% - 100ppm/°C | Vishay | 0805 |
| R21 | 330K | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R22 | R015 | SMD film res 1W - 2512 MSR1 | MEGGIT | 2512 |
| R23 | 27R | SMD standard film res - 1/4W - 5% - 250ppm/°C | Vishay | 1206 |
| R24 | 100K | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R25 | 470R | SFR25 axial stand. film res - 0.4W - 5% - 250ppm/°C | Vishay | PTH |
| R26 | 1Mb | SMD standard film res - 1/8W - 1% - 100ppm/°C | Vishay | 0805 |
| R27 | 0R33 | SFR25 axial stand. film res - 0.4W - 5% - 250ppm/°C | Vishay | PTH |
| R29 | 47K | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R30 | 15K | SMD standard film res - 1/4W - 5% - 250ppm/°C | Vishay | 1206 |
| R31 | 43K | SMD standard film res - 1/4W - 5% - 250ppm/°C | Vishay | 1206 |
| R32 | 15K | SMD standard film res - 1/4W - 5% - 250ppm/°C | Vishay | 1206 |
| R33 | 6K8 | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R34 | 1Mb | SMD standard film res - 1/8W - 1% - 250ppm/°C | Vishay | 0805 |
| R35 | 8R2 | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R36 | 62K | SMD standard film res - 1/4W - 1% - 100ppm/°C | Vishay | 1206 |
| R37 | 10K | SFR25 axial stand. film res - 0.4W - 5% - 250ppm/°C | Vishay | PTH |

**Table 6. Bill of material (continued)**

| Des. | Part type / part value | Description | Supplier | Case style / package |
|---|---|---|---|---|
| R39 | 56K | SMD standard film res - 1/8W - 1% - 100ppm/°C | Vishay | 0805 |
| R42 | 16K | SMD standard film res - 1/4W - 1% - 100ppm/°C | Vishay | 1206 |
| R45 | 2K2 | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R46 | 33R | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R47 | 100K | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R48 | 4K7 | SMD standard film res - 1/8W - 1% - 100ppm/°C | Vishay | 0805 |
| R49 | 24K | SMD standard film res - 1/8W - 1% - 100ppm/°C | Vishay | 0805 |
| R50 | 2K7 | SFR25 axial stand. film res - 0.4W - 5% - 250ppm/°C | Vishay | PTH |
| R51 | 1K0 | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R52 | 0R47 | SFR25 axial stand. film res - 0.4W - 5% - 250ppm/°C | Vishay | PTH |
| R53 | 0R33 | SFR25 axial stand. film res - 0.4W - 5% - 250ppm/°C | Vishay | PTH |
| R54 | 560K | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R55 | 22R | SMD standard film res - 1/4W - 5% - 250ppm/°C | Vishay | 1206 |
| R57 | 1K | SMD standard film res - 1/4W - 5% - 250ppm/°C | Vishay | 1206 |
| R58 | M57703 | Thermistor - B57703M103G | EPCOS | DWG |
| R59 | 12K | SFR25 axial stand. film res - 0.4W - 1% - 100ppm/°C | Vishay | PTH |
| R62 | 4K7 | SMD standard film res - 1/4W - 1% - 100ppm/°C | Vishay | 1206 |
| R63 | 100K | SMD standard film res - 1/4W - 1% - 100ppm/°C | Vishay | 1206 |
| R65 | 22K | SMD standard film res - 1/8W - 1% - 100ppm/°C | Vishay | 0805 |
| R66 | 3R9 | SMD standard film res - 1/4W - 5% - 250ppm/°C | Vishay | 1206 |
| R67 | 12K | SMD standard film res - 1/8W - 1% - 100ppm/°C | Vishay | 0805 |
| R68 | 220K | SMD standard film res - 1/4W - 1% - 100ppm/°C | Vishay | 1206 |
| R69 | 1K0 | SMD standard film res - 1/4W - 1% - 100ppm/°C | Vishay | 1206 |
| R75 | 1K8 | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R76 | 4K7 | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |

**Table 6. Bill of material (continued)**

| Des. | Part type / part value | Description | Supplier | Case style / package |
|---|---|---|---|---|
| R77 | 100K | SMD standard film res - 1/8W - 5% - 250ppm/°C | Vishay | 0805 |
| R78 | 560R | SMD standard film res - 1/4W - 5% - 250ppm/°C | Vishay | 1206 |
| R80 | 1K8 | SMD standard film res - 1/4W - 5% - 250ppm/°C | Vishay | 1206 |
| T1 | SRW32EC-T01H114 | Power transformer | TDK | DWG |
| U1 | L6563S | Transition-mode PFC controller | STMicroelectronics | SO-14 |
| U3 | SFH617A-4 | Optocoupler | Infineon | DIP4-10.16mm |
| U5 | TSM1014AIST | Low consumption CC/CV controller | STMicroelectronics | Mini SO-8 |
| U6 | L6566A | Multi-mode PWM controller | STMicroelectronics | SO-16N |

# 8 PFC coil specifications

## General description and characteristics

- Application type: consumer, home appliances
- Transformer type: open
- Coil former: vertical type, 5+3 pins
- Max. temp. rise: 45 °C
- Max. operating ambient temperature: 60 °C
- Mains insulation: n.a.
- Unit finishing: varnished

## Electrical characteristics

- Converter topology: boost, transition mode
- Core type: CQ25-PC47
- Min. operating frequency: 20 kHz
- Typical operating frequency: 80 kHz
- Primary inductance: 400 µH±10% at 1 kHz-0.25 V [(a)]
- Peak primary current: 3.5 $A_{PK}$
- RMS primary current: 1.2 $A_{RMS}$

## Electrical diagram and winding characteristics

**Figure 27. PFC coil electrical diagram**

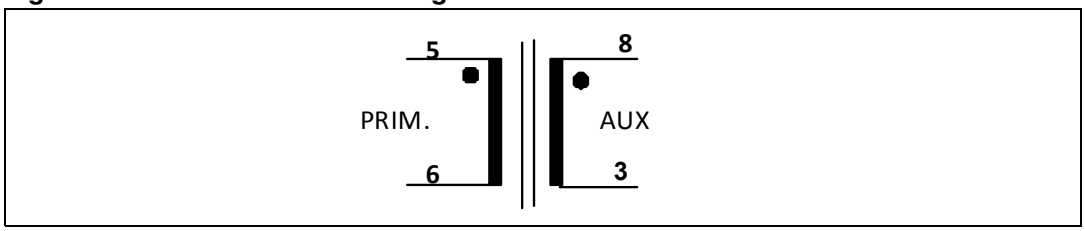



**Table 7. PFC coil winding data**

| Pins | Windings | RMS current | Number of turns | Wire type |
|---|---|---|---|---|
| 8 - 3 | AUX [(1)] | 0.05 $A_{RMS}$ | 5 spaced | ϕ 0.28 mm |
| 5 - 6 | PRIMARY [(2)] | 1.2 $A_{RMS}$ | 50 | Multistrand 10 x ϕ 0.20 mm |

1. Aux winding is wound on coil former before primary winding. To be insulated with a layer of polyester tape.
2. Primary winding external insulation: 2 layers of polyester tape.

a. Measured between pins #5 and #6

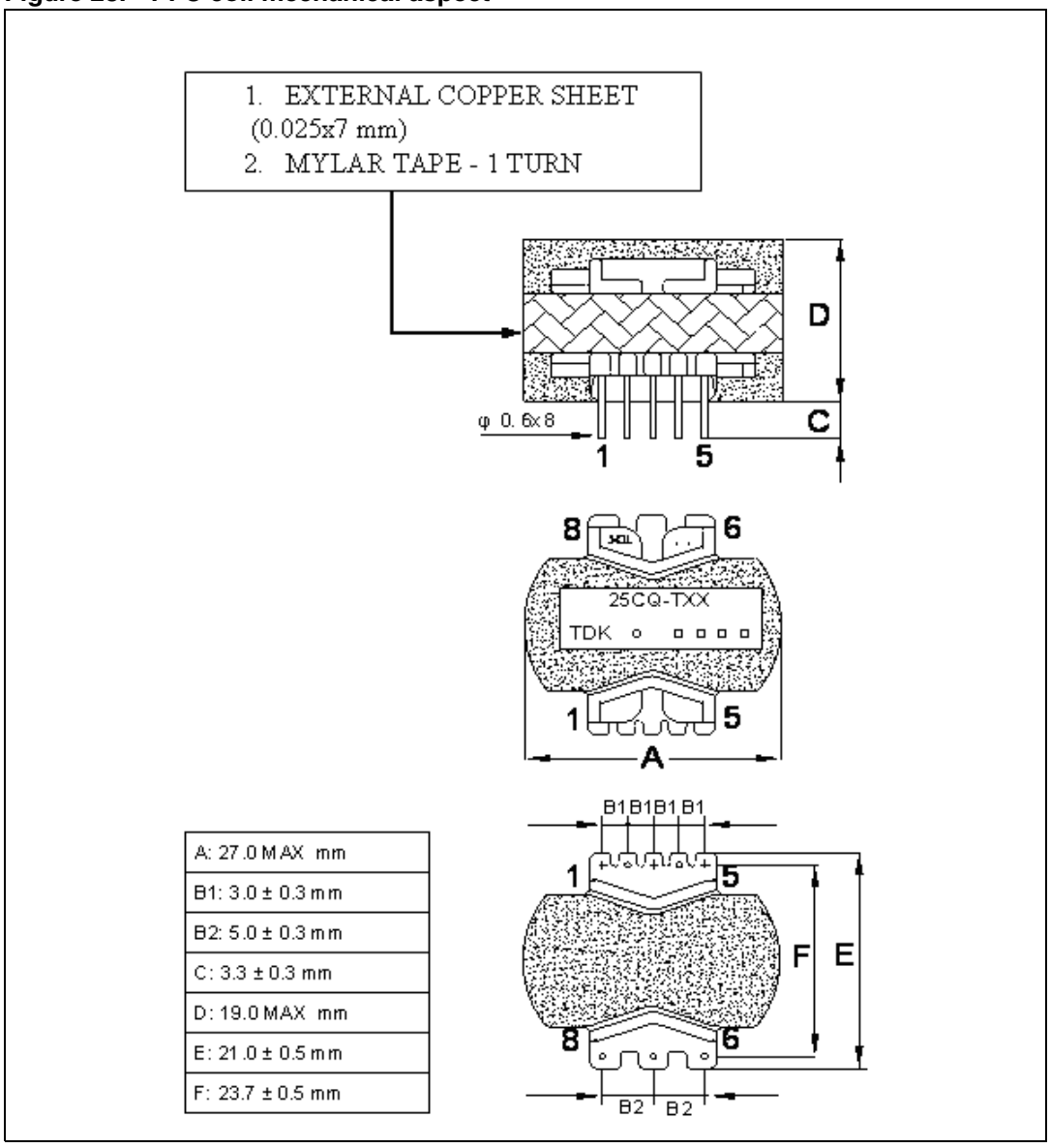
## Mechanical aspect and pin numbering

- Maximum height from PCB: 20 mm
- Coil former type: vertical, 5+3 pins
- Pins #1, 2, 4, 7 are removed
- External copper shield: not insulated, wound around the ferrite core including the coil former. Height is 7 mm. Connected to pin #3 by a solid wire.

## Manufacturer

- TDK electronics europe - germany
- Inductor P/N: 25CQ-T05

**Figure 28. PFC coil mechanical aspect**




| |
|---|
| A: 27.0 MAX mm |
| B1: 3.0 ± 0.3 mm |
| B2: 5.0 ± 0.3 mm |
| C: 3.3 ± 0.3 mm |
| D: 19.0 MAX mm |
| E: 21.0 ± 0.5 mm |
| F: 23.7 ± 0.5 mm |

# 9 Transformer specifications

## General description and characteristics

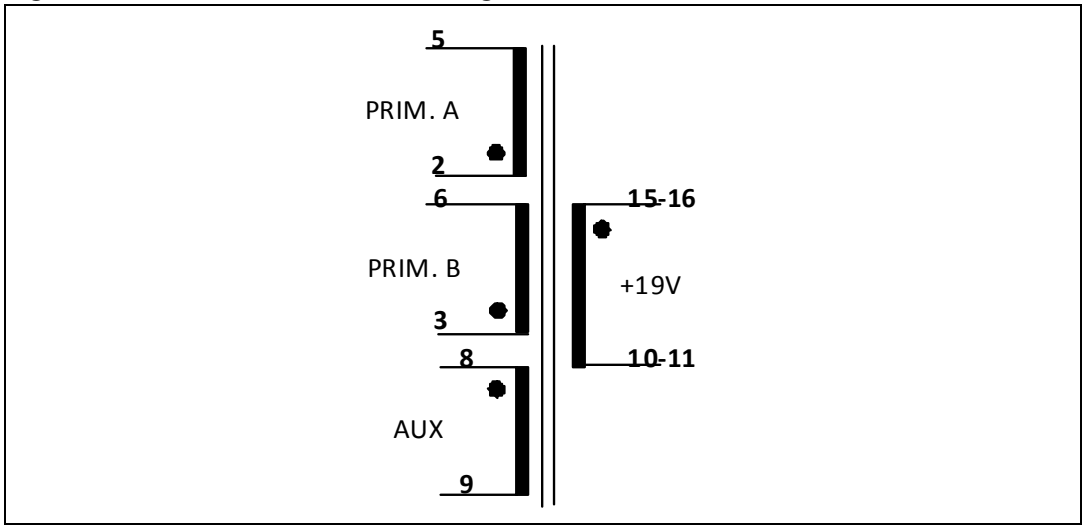
- Application type: consumer, home appliances
- Transformer type: open
- Coil former: horizontal type, 9+9 pins
- Max. temp. rise: 45 °C
- Max. operating ambient temperature: 60 °C
- Mains insulation: according to EN60950
- Unit finishing: varnished

## Electrical characteristics

- Converter topology: flyback, CCM/DCM mode
- Core type: EER34-PC47
- Min. operating frequency: 20 kHz
- Typical operating frequency: 100 kHz
- Primary inductance: 550 µH ± 10% at 1 kHz-0.25 V [(b)]
- Leakage inductance: 17 µH max at 100 kHz-0.25 V [(c)]
- Peak primary current: 2.65 $A_{PK}$
- RMS primary current: 0.78 $A_{RMS}$

## Electrical diagram and winding characteristics

**Figure 29. Transformer electrical diagram**




b. Measured between pins (2, 3)-(5, 6)

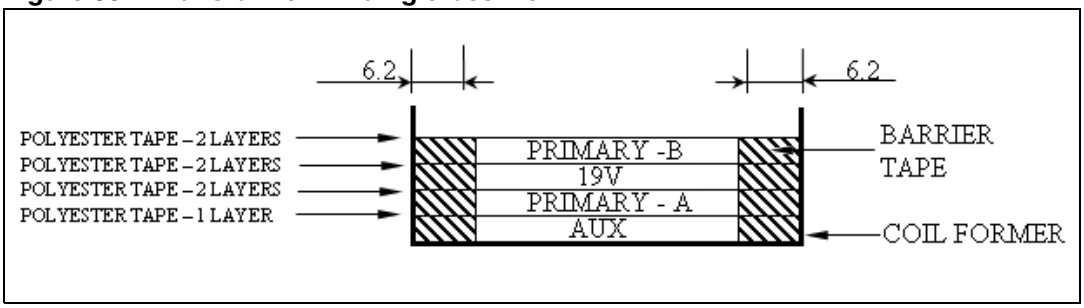
c. Measured between pins (2, 3)-(5, 6) with all secondary windings shorted

**Table 8. Transformer winding data(1)**

| Pins | Winding | RMS current | Number of turns | Number of layers | Wire type |
|---|---|---|---|---|---|
| 5-6 | AUX | 0.05 $A_{RMS}$ | 7 spaced | 1 | G2<br>$\phi$ 0.23 mm |
| 3-1 | Primary - A (2) | 0.39 $A_{RMS}$ | 60 | 2 | G2<br>2 x $\phi$ 0.23 mm |
| 8-10 | 19 V | 5.2 $A_{RMS}$ | 8 | 1 | Multistrand G2<br>4 x $\phi$ 0.64 mm |
| 4-2 | Primary - B | 0.39 $A_{RMS}$ | 60 | 2 | G2<br>2 x $\phi$ 0.23 mm |

1. All terminal wires have to be insulated with tubes
2. Primaries A and B are in parallel

**Figure 30. Transformer winding cross view**



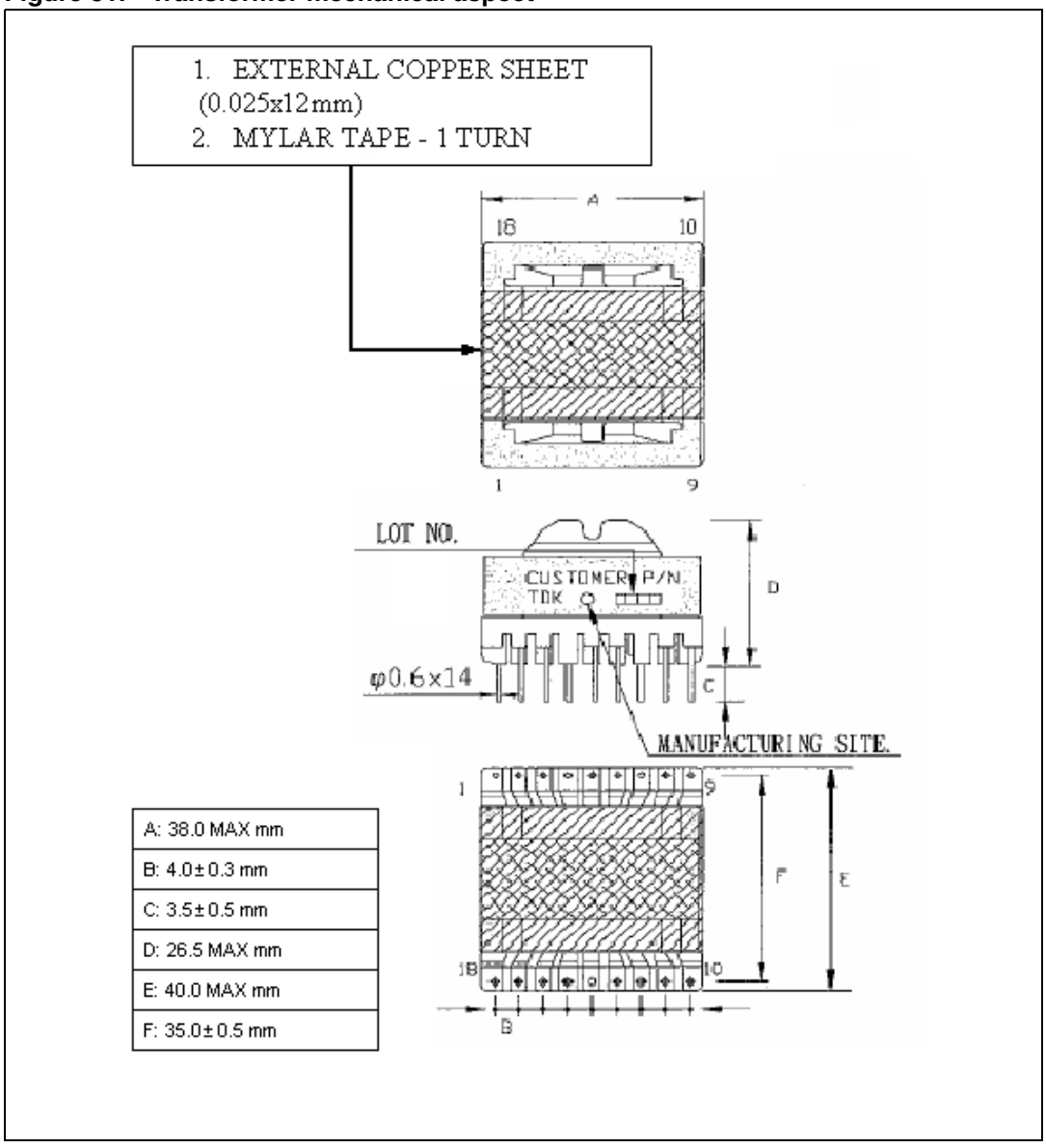
## Mechanical aspect and pin numbering

- Maximum height from PCB: 30 mm
- Coil former type: horizontal, 9+9 pins (pin 2 removed)
- Pin distance: 4 mm
- Row distance: 35 mm
- External copper shield: not insulated, wound around the ferrite core including the coil former. Height is 12 mm.

## Manufacturer

- TDK electronics europe - germany
- Transformer P/N: SRW32EC-T01H114

**Figure 31. Transformer mechanical aspect**



# 10 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 19-May-2009 | 1 | Initial release |
| 25-May-2009 | 2 | Updated *Figure 2* and *Figure 3* |
| 18-Sep-2009 | 3 | Updated *Figure 8* and *Table 6* |
| 29-Nov-2010 | 4 | Updated *Chapter 4* and *Figure 2* |