AN2846
Application note

SCLT3-8 - guidelines for use in industrial automation applications

Introduction

The serial current limited termination device SCLT3-8 provides 8 inputs and supports the data transfer of the input states through a limited opto-transistor count thanks to the digital SPI (serial peripheral interface).

The purpose of this document is to:

- Help designers to use the SCLT3-8 in basic operations and to allow them to use it easily in their own applications by describing the SCLT3-8 behavior in detail (Refer also to the SCLT3-8 device datasheet and to the User guide for the evaluation board STEVAL-IFP000V1.)
- Provide basic schematic diagrams
- Provide information on the thermal behavior of the SCLT3-8 device
- Offer recommendations to achieve robust SCLT3-8 designs to optimize EMI protection in accordance with industry standards (IEC 61000-4-2, 4-4, 4-5 and 4-6)

Contents

1 Application guidelines

1.1 Features of the SCLT3-8

The SCLT is an octal input active termination device designed for 24 V DC high density input modules used in industrial automation. Each channel circuit terminates the connection between a high side proximity sensor and the I/O module.

The advanced features of the SCLT3-8 compared to the basic CLT3-4BT6 device are:

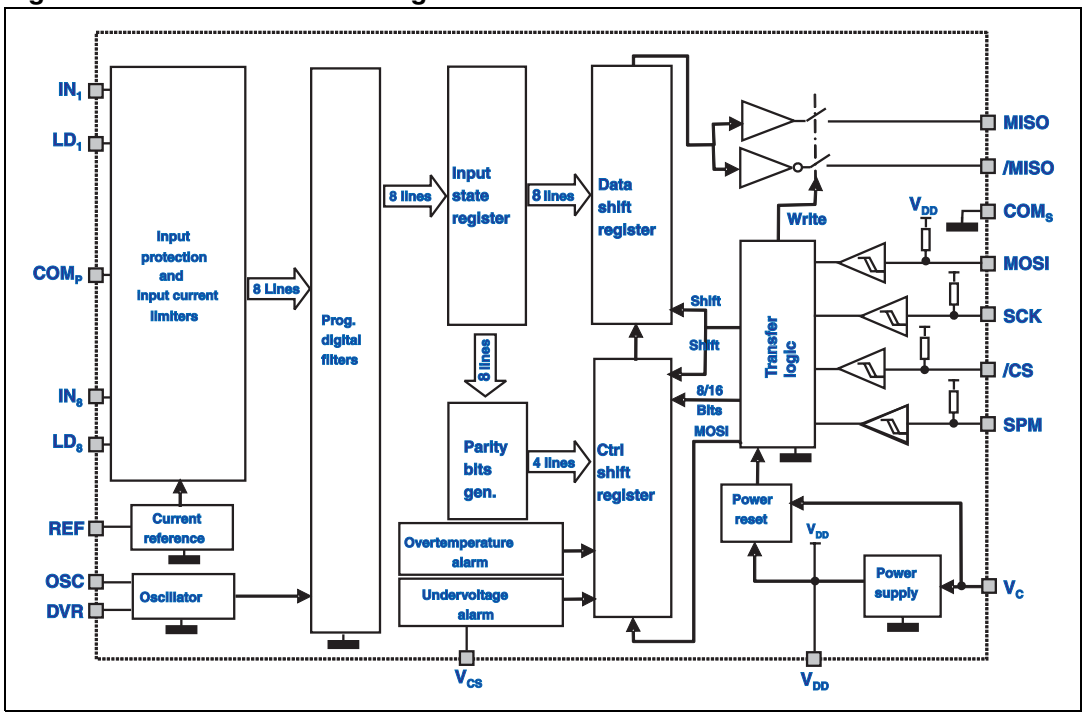
- SPI for digital output count reduction
- Doubling of input terminations: 8 inputs compared to 4
- Input state monitoring by LEDs from the process section
- Undervoltage alarm detection of the power bus
- Power bus loss detection
- 5 V supply source available for external driving circuits like opto-couplers or magnetic isolators
- Overtemperature detection
- Checksum data transmission through SPI for better data transfer integrity

The SCLT3-8 also features an input overvoltage protection. This input protection makes this device robust against electromagnetic interference as defined in IEC 61000-4-x standards: ESD, fast transient bursts, and voltage surges.

It is housed in a very low R_{TH} exposed pad, surface mount, HTSS0P38 package to reduce the circuit board size and the cooling pad.

Figure 1 shows the schematic block diagram for the device.

Figure 1. Schematic block diagram



The SCLT3-8 has been designed to run with SPI protocol $C_{PHA} = 0$ and $C_{POL} = 0$. The frame format is 16 bits or 8 bits long according to SPM pin level. When SPM is grounded, 16 bits are transmitted - 8 input data bits and 8 control bits. When SPM is connected to V_{DD} only the 8 input data bits are transmitted.

Table 1 defines the significance of the16 bits. Bit 15 is the most significant bit. Detailed SPI functionality is described in *Section 1.4*.

Table 1. 16-bit frame definition

Data bits	**Bit15**	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
	IN_8	IN_7	IN_6	IN_5	IN_4	IN_3	IN_2	IN_1
Control Bits	**Bit07**	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
	/UVA	/OTA	PC1	PC2	PC3	PC4	0	1

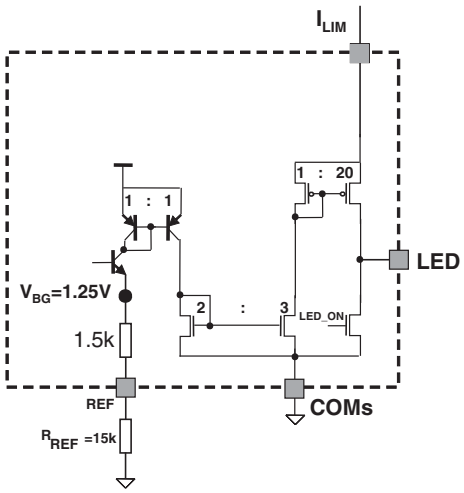
1.2 Current-limited inputs

1.2.1 Maximum input current setting

All internal bias currents sources and particularly the input current limiter are defined by the reference resistor connected to pin REF. A 15 kΩ resistor will assure a typical input limited current of 2.35 mA (see *Figure 2*). The typical limited input current I_{LIM} is given by the formula:

$$I_{LIM} = 30 \cdot \frac{V_{BG}}{(R_{REF} + 1.5\,k)} \text{ with typical } V_{BG} = 1.25\,V$$

Figure 2. Current limiter diagram



The technology used allows a very low current dispersion according to the different channels (less than 10%). The reference voltage V_{BG} is also compensated over the junction temperature range from -25 °C to 150 °C enabling a good stability of the limited current (see *Figure 3*).

Figure 3. Limited current versus junction temperature

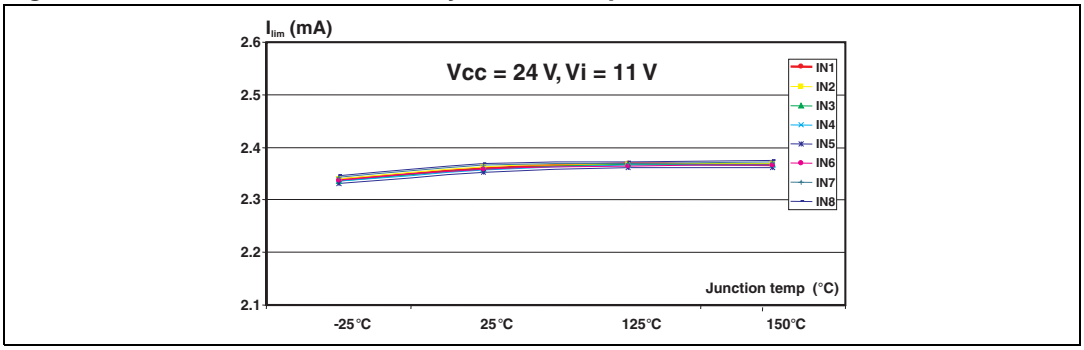
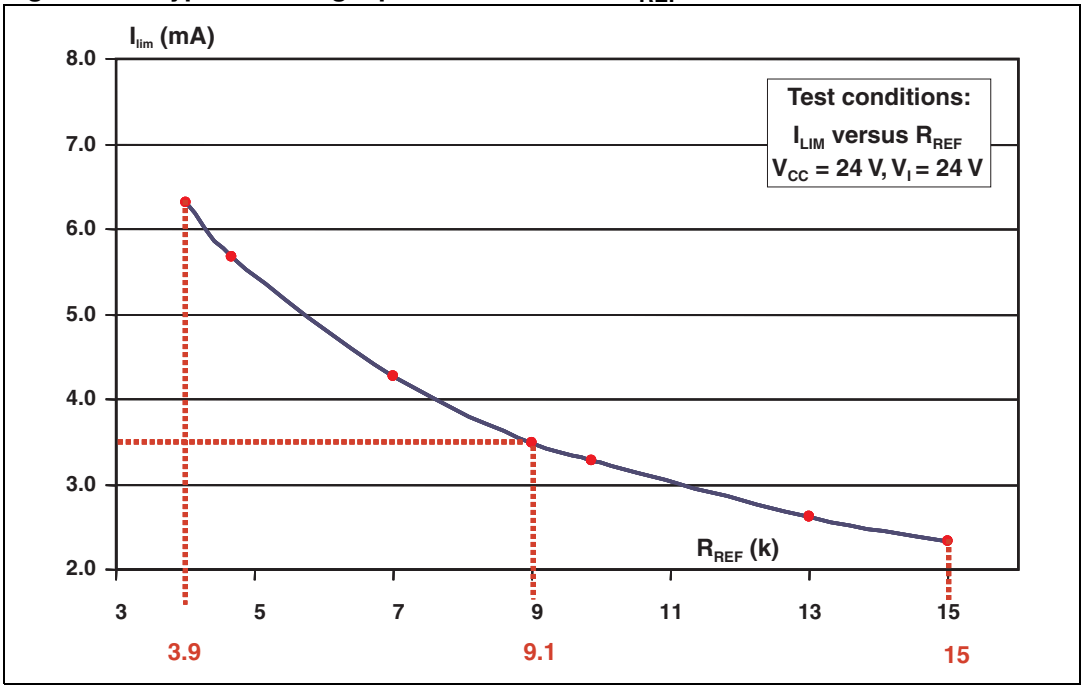


Figure 4 shows the I_{LIM} trend versus R_{REF}, according to the input current setting and therefore the dissipated power, the SCLT3-8 should be cooled with a sufficient copper heat sink area (see *Section 2*)

Figure 4. Typical limiting input current versus R_{REF}



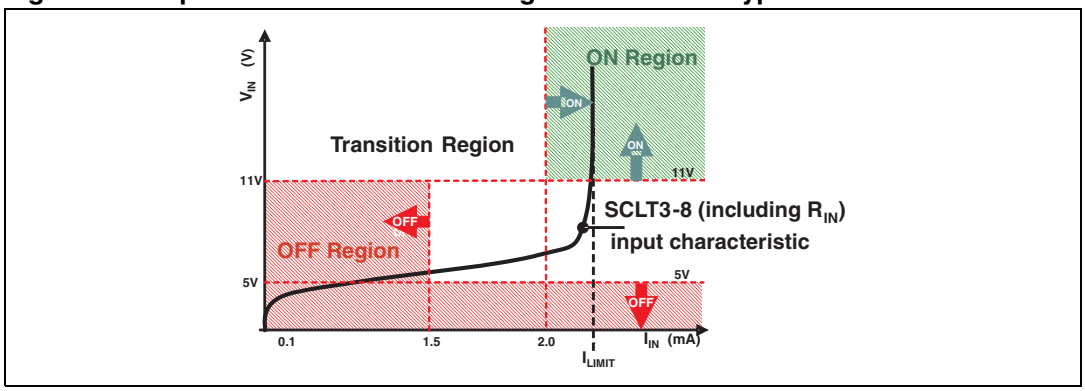
1.2.2 Input characteristics (IEC 61131-2 standard)

According to the IEC 61131-2 standard and referring to type 3, when the input current is less than 1.5 mA the output circuit passes all the input current, keeping the monitoring LED off and transmits a low level state to the input state register.

When the module input voltage V_I, taking into account the 2.2 kΩ input resistor, is higher than 11 V (that is, the SCLT3-8 input voltage V_{IN} is higher than 5 V) the monitoring LED is on and the circuit transmits a high level state to the input state register.

Figure 5 gives the input characteristics and operating regions of type 3, defined in the IEC 61131-2 standard, and the typical SCLT3-8 input characteristic.

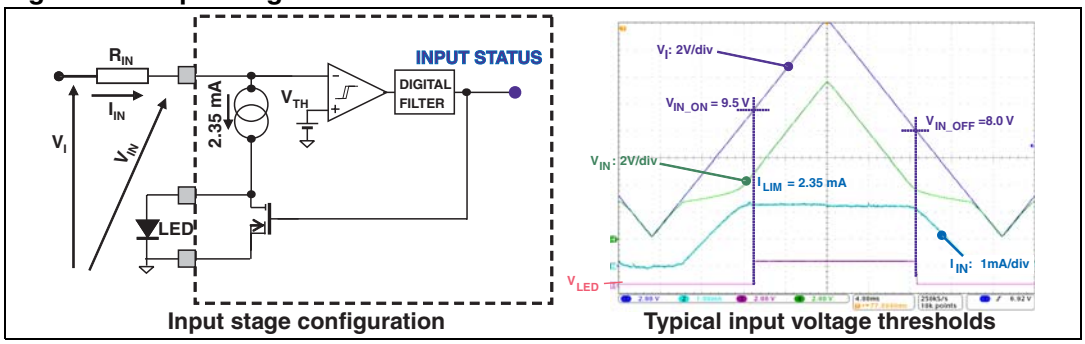
Figure 5. Input characteristic according to IEC 61131-2 type 3



Current limited inputs allow reduced power dissipation into the device as well as reduced power needed by the external supplies. A typical application circuit schematic is shown in *Figure 31* in the application section.

Figure 6 displays the SCLT3-8 input stage configuration and its typical input threshold voltages. Low frequency triangular waveform as the input voltage has been used to better highlight the voltage thresholds. Input current (I_{IN}) and voltage across the LEDs are also displayed in *Figure 6*. The V_{LED} wave shape shows clearly the on-off states of the SCLT3-8.

Figure 6. Input stage



With R_{IN} = 2.2 kΩ, the typical V_{I_ON} and V_{I_OFF} threshold voltages are respectively 9.5 V and 8.5 V, consistent with the 11 V min. and 5 V max specified in the IEC 61131-2 standard. The hysteresis (1 V) improves the input noise immunity.

The module input thresholds are the results of drop voltage across the input resistor R_{IN}, into which flows the input current I_{IN}, and the SCLT3-8 input thresholds V_{TH_ON} and V_{TH_OFF}.

The input current limiter is activated typically when V_{IN} = 3.7 V, before the V_{TH_ON} threshold is reached.

In all cases the following formula can be applied:

$$V_I = R_{IN} \times I_{IN} + V_{IN}$$

When the input current limiter is activated, the formula becomes:

$$V_I = R_{IN} \times I_{ILIM} + V_{IN}$$

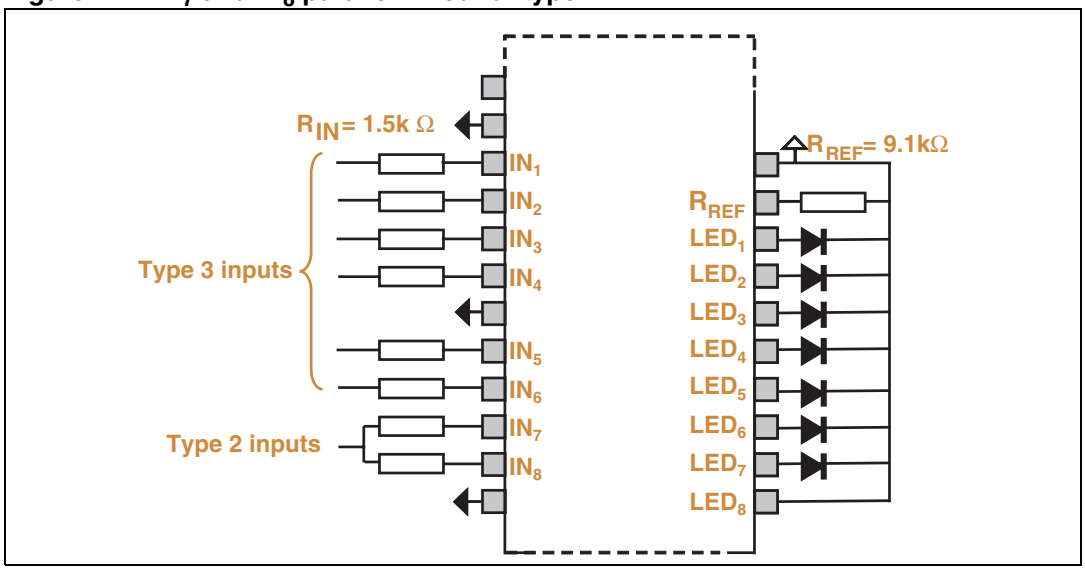
The typical module input threshold voltage can be calculated as follow:

$$V_{IN\_ON} = R_{IN} \times I_{ILIM} + V_{VTH\_ON}$$

The proposed R_{IN} value of 2.2 kΩ has been calculated to meet the IEC 61131-2 threshold requirements. Users can set their own particular application threshold voltages by applying, in the formula given above, the V_{IN} they want to achieve and find the corresponding R_{IN} value. Take note, the higher the R_{IN}, the better will be the immunity against voltage surges.

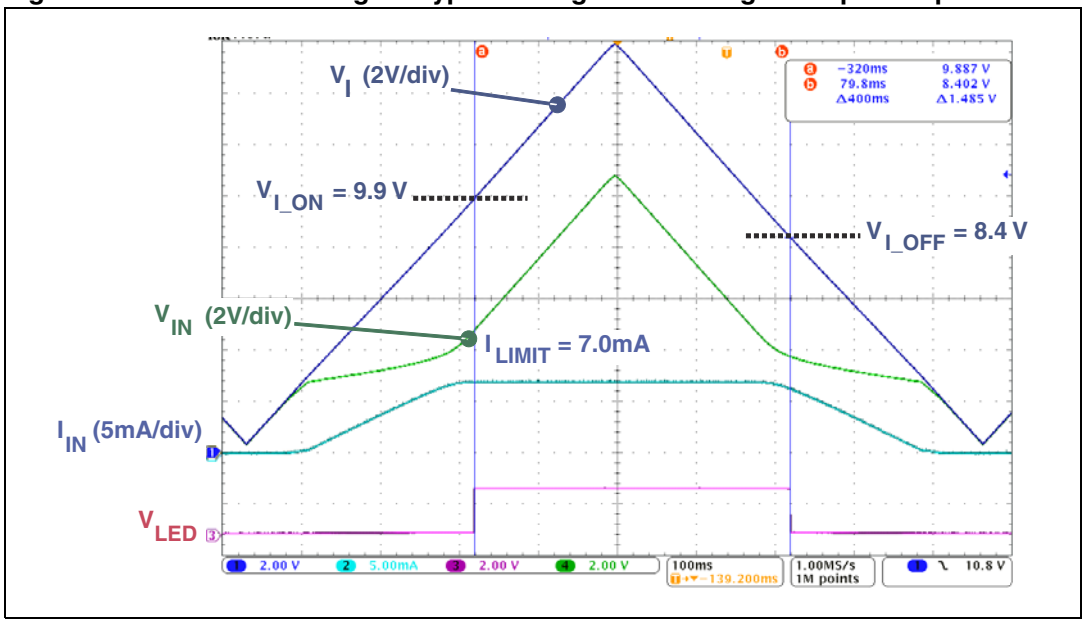
A particular useful application is when an input type 2 is needed. *Figure 7* shows the solution of connecting R_{IN7} and input R_{IN8} = 1.5 kΩ in parallel and tuning the I_{LIM} with R_{REF} = 9.1 kΩ to get 3.5 mA (see *Figure 4*) in each input branch. Of course corresponding bits (B14, B15) will be set together at the right state according to the level applied at the common input. **Unused LED outputs must be grounded to maintain the flow of the current in its corresponding chanel.**

Figure 7. IN_7 and IN_8 parallel wired for type 2



The different threshold voltages and the I_{LIMIT} = 7.0 mA are shown in *Figure 8* below.

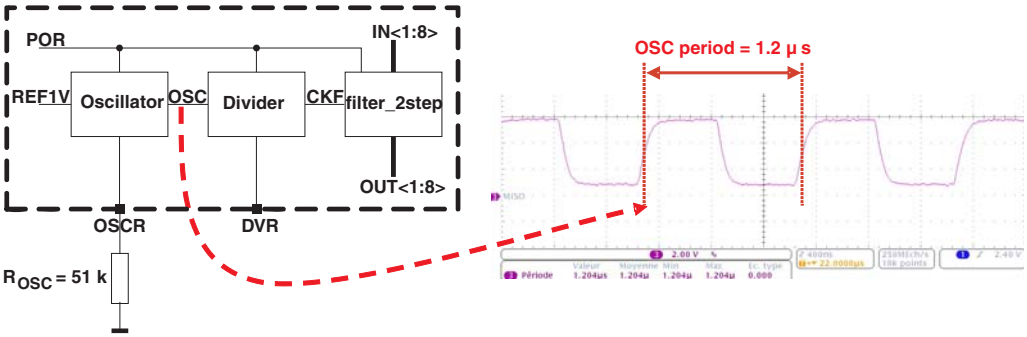
Figure 8. Threshold voltages - type 2 configuration using two inputs in parallel



1.2.3 Digital input filter

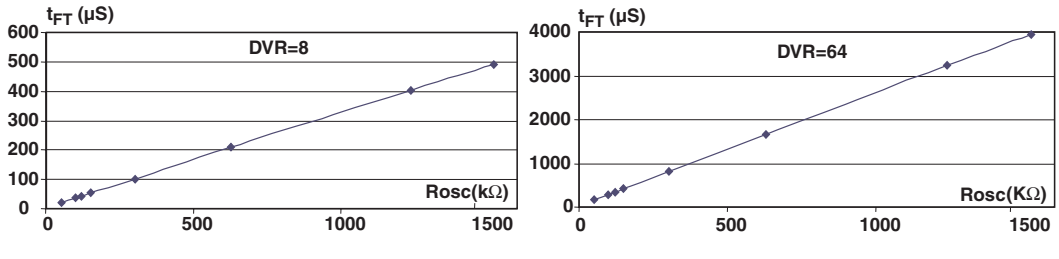
Input parasitic disturbances can be removed by the programmable input digital filter. It is based on an RC oscillator, a divider and a two step filter (see *Figure 9*).

Figure 9. Digital input filter.



The internal capacitor value is typically 10 pF. The oscillator resistor is connected externally on pin R_{OSC}. The clock divider is set at 8 when the pin DVR is connected to GND or at 64 when it is connected to V_{DD}. The two step filter validates the input voltage when it sees at least three rising edges as shown in *Figure 9*. The delay time is between $2 \cdot t_{OSC}$ and $3 \cdot t_{OSC}$. A wide filter time range, t_{FT}, can be set by using the couple R_{OSC} and DVR as shown in below in *Figure 10*.

Figure 10. Minimum t_{FT} versus R_{OSC}



The user can also choose a particular typical filter time, t_{FT}, by calculating the corresponding R_{OSC} value from the formula:

$$R_{OSC} = \frac{t_{FT}}{2} \times \frac{1}{DVR} \times \frac{1}{23.5 \times 10^{-12}}$$

1.2.4 Input signal frequency limitation

The maximum frequency transmitted trough the current limited inputs is limited by 3 factors:

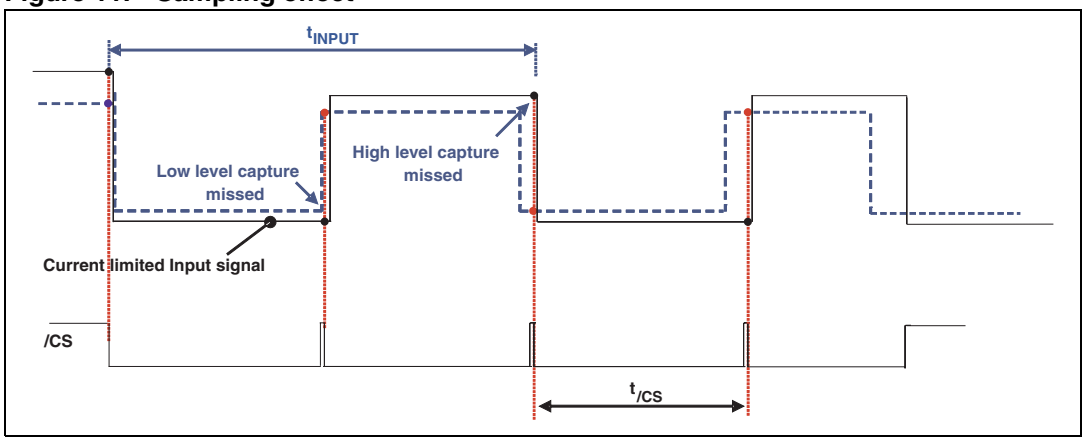
1. The **input digital filter,** which cuts undesirable frequencies. R_{OSC} set to 51 kΩ and DVR connected to GND ensures that the input signal has to be at a stable level for more than 20 µs to be taken into account. This allows a maximum input frequency of 25 kHz. It can be reduced to 130 Hz using the combination of R_{OSC} = 1.5 MΩ and DVR connected to V_{DD}.
2. The **input capacitors C_{IN}** are used to increase the EMI immunity filter of the input signal. R_{IN} = 2.2 kΩ and C_{IN} = 22 nF ensures a 3.2 kHz low pass filter.
3. The **SPI sampling effect** - the input states are taken into account at each /CS fall (see *Section 1.4.4*). This achieves a sampling of inputs at the /CS frequency, as shown in *Figure 11*. The input states will be correctly transmitted if the sampling mode meets the Shannon equation:

$$F_{/CS} = 2 \bullet F_{Input}$$

$$\text{with } F_{/CS} = \frac{1}{t_{/CS}} \text{ : with } t_{/CS} \text{ the } /CS \text{ signal period}$$

$$\text{with } F_{Input} = \text{max input frequency}$$

Figure 11. Sampling effect



As the /CS period is dependant on the frame length, *Table 2* below gives some useful combinations of SCK frequency signal, frame length and current limited input frequency.

Table 2. Input frequency versus SCK and length frame

F_{SCK}	0.1				1.0				2.0				MHz
Frame length	8	16	32	64	8	16	32	64	8	16	32	64	bits
$t_{/CS}$	80	160	320	640	8	16	32	64	4	8	16	32	µs
$F_{current\ limited\ input}$	6.25	3.125	1.56	0.78	62.5	31.25	15.6	7.8	125	62.5	31.25	15.6	kHz

1.2.5 Input state monitoring

The state of each of the 8 monitoring LEDs is an image of the 8 **filtered** input states. All the monitoring LED cathodes have to be connected to ground. In the on state a current of I_{LIM} reduced by 0.15 mA is available for each LED. In case of a LED not being used, the LED output pin must be connected to the ground COM_P to allow the input current to flow back to the ground.

The LEDs must be chosen with a V_F voltage less then 2.7 V (at minimum operating temperature -25 °C).

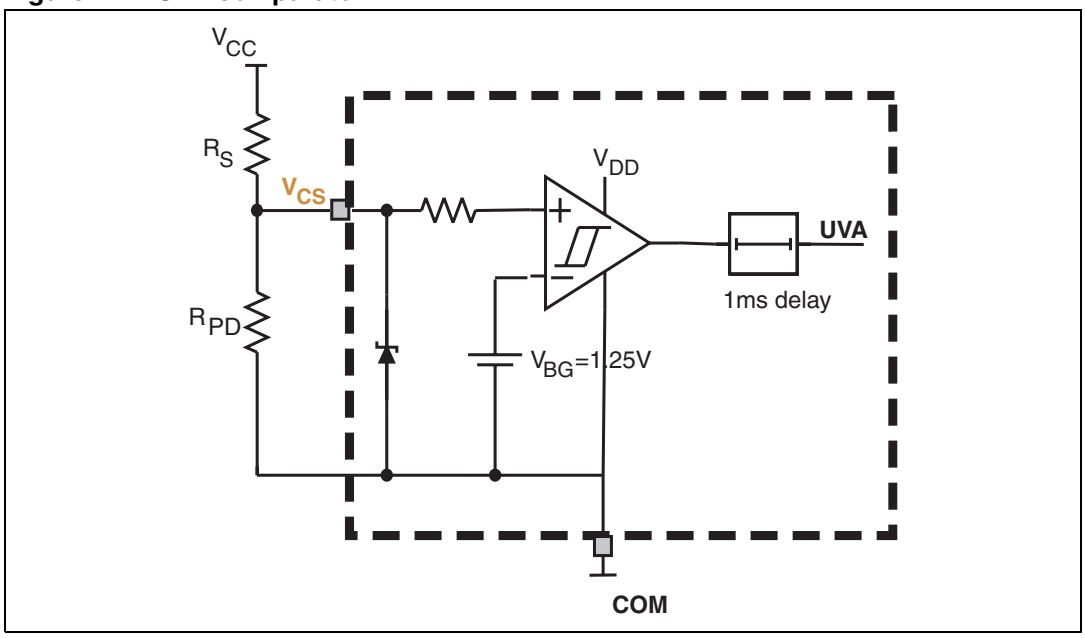
1.3 Monitoring functions and regulator

1.3.1 V_{CC} monitoring

The power bus voltage connected to V_{CC} is sensed by the V_{CS} pin through a resistor bridge. The V_{CS} threshold voltage is typically 1.25 V with a hysteresis of 100 mV. Designers can easily set their own alarm detection voltage by an appropriate resistor bridge (see *Figure 12*) using the formula:

$$V_{CC\_min} = V_{CS}\ (1 + \frac{R_S}{R_{PD}})$$

Figure 12. UVA comparator



For example, the resistor bridge consisting of R_S = 1.5 MΩ and R_{PD} = 120 kΩ produces UVA activation when V_{CC} drops below 17 V. The UVA activation has no effect on SCLT3-8 behavior but the information is transmitted trough the SPI bus by setting bit 7 to low state in the control bits register (see *Figure 13* and *Figure 14*).

To eliminate any short voltage disturbances that could trigger the UVA, a 1 ms delay circuit has been inserted in the output line of the UVA comparator.

Figure 13. V_{CC} = 24 V, UVA bit not activated

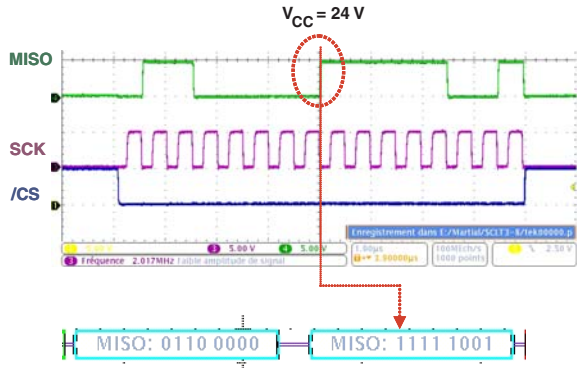
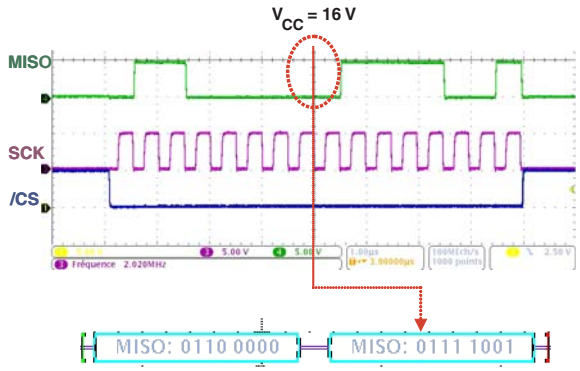


Figure 14. V_{CC} = 16 V, UVA bit activated

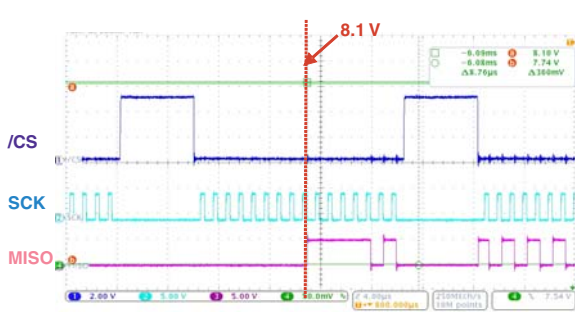


1.3.2 Power loss detection

For a greater voltage drop on V_C, a power supply loss detection has been added. This immediately sets MISO output at low level state when V_C is below 8 V, as shown in *Figure 15* and *Figure 16*. The MCU can then interpret that if all bits are equal to 0, this means that V_C is too low.

Figure 15. Communication stops for V_C < 8 V

Figure 16. Communication resumes for V_C > 8.1 V



1.3.3 Overtemperature detection

When the junction temperature exceeds 150 °C an overtemperature alarm sets the MISO bit 6 at low state in the control bits register. The SCLT3-8 remains operational. The MCU receiving the alarm has to take the corrective actions. The alarm will be reset when the junction temperature falls below 135 °C.

1.3.4 Internal voltage regulator 5 V

The input of this voltage regulator is internally connected to the V_C pin. The voltage regulator supplies the digital part of the SCLT3-8 and therefore it defines the high digital level. It also supplies the sourced current available at pin MISO. It can also supply application needs (such as opto-couplers and micro transformers) through pin V_{DD}. Its total current capability is 9 mA for a 3% voltage drop on V_{DD} (see *Figure 17*).

Figure 17. Regulator output voltage

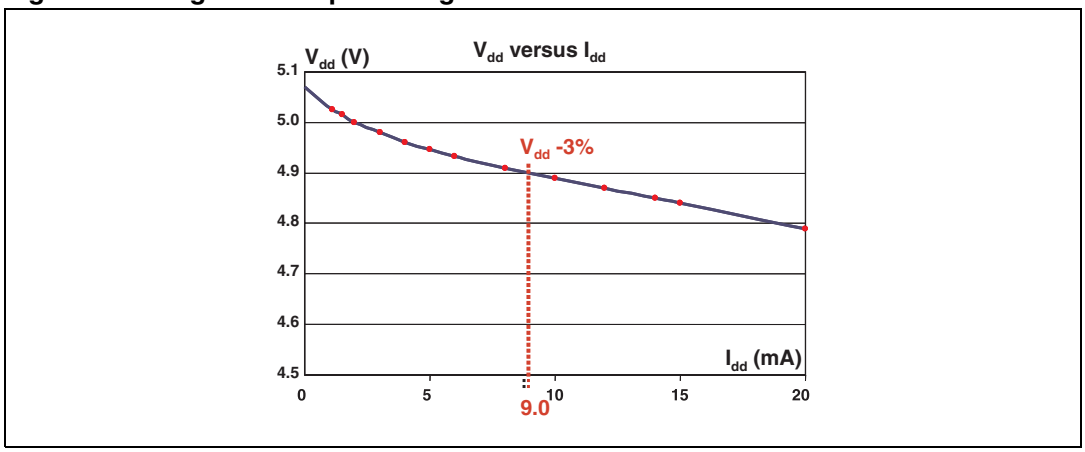


Figure 18 shows the schematic diagram of a solution for applications where greater current is needed. The bypass transistor allows extra current while maintaining a 5 V regulated voltage (see *Figure 19*).

Figure 18. V_{DD} booster schematic

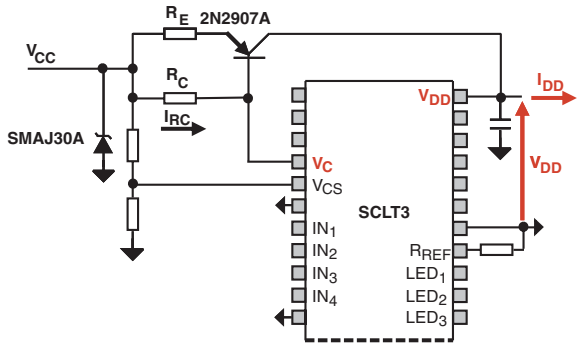
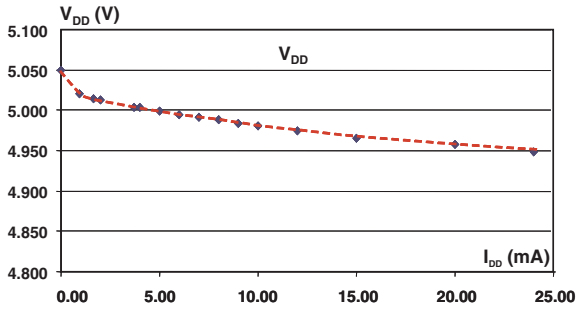


Figure 19. Load regulation with V_{DD} booster



The proposed circuit allows a 25 mA current load capability with a V_{DD} regulation <2%. An additional input protection device, like SMAJ30A, is needed to comply with voltage surges because R_C has to be reduced to limit the voltage drop across it.

The dissipated power in the bypass transistor PZT2N2907A is 550 mW.

Components used:

- PZT2N2907A (SOT223 with 1 cm^2 copper area)
- R_C = 330 Ω (1/8 W), R_E = 51 Ω (1/8 W)

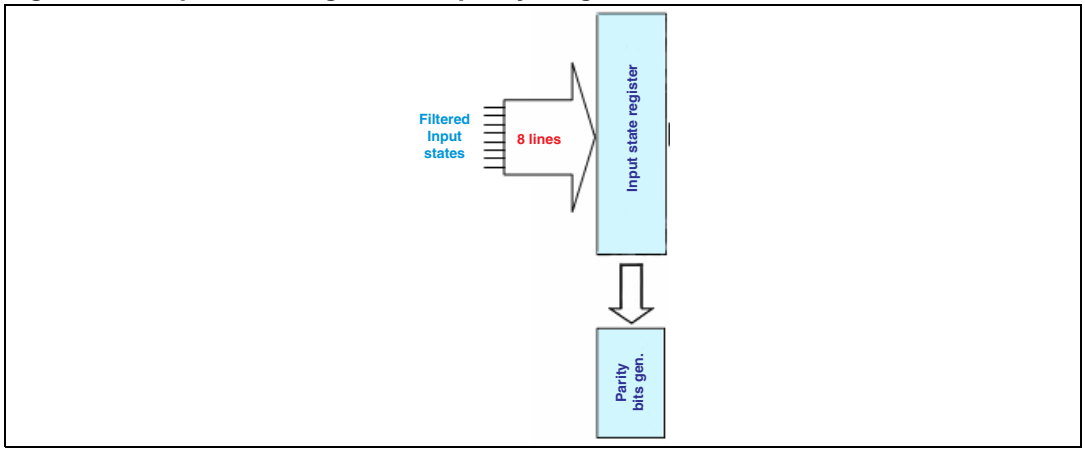
1.4 SPI functional description

Three registers (refer to *Figure 1*) are used to transfer input data and control data to the 16-bit data frame. The data frames are transmitted through four interface signals: /CS, SCK, MOSI, and MISO.

1.4.1 Input state register and parity bit generator

After filtering, the 8 input termination states are stored in an 8-bit input state register. Its content is an image of the filtered input states in real time.

Figure 20. Input state register and parity bit generator.



The SCLT3-8 has been designed to help diagnose incorrect data transmission. The four parity bits generated by the parity bit generator are computed according to the input states register content. They are updated each time the input state register content changes.

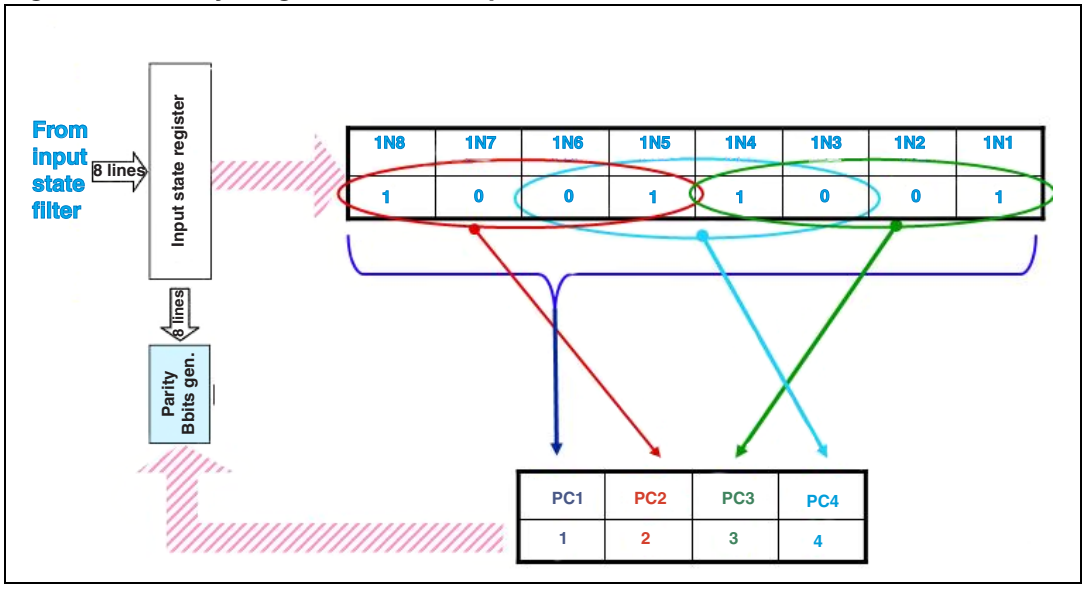
The parity bit 5 of PC1 register controls the 1 to 8 input data states; PC2-bit 4 controls inputs 5 to 8: PC3-bit 3 controls inputs 1 to 4;PC4-bit 2 controls inputs 3 to 6 according to the logic equation:.

$$PC_n = 1 \text{ if } \sum \textbf{INPUTstate} = \text{even, 0 if odd.}$$

See example in *Figure 21*.

The decoding of all the parity bit results will help the microcontroller detect the possible corrupted pair of bits occurring during the transmission.

Figure 21. Parity bit generation example.



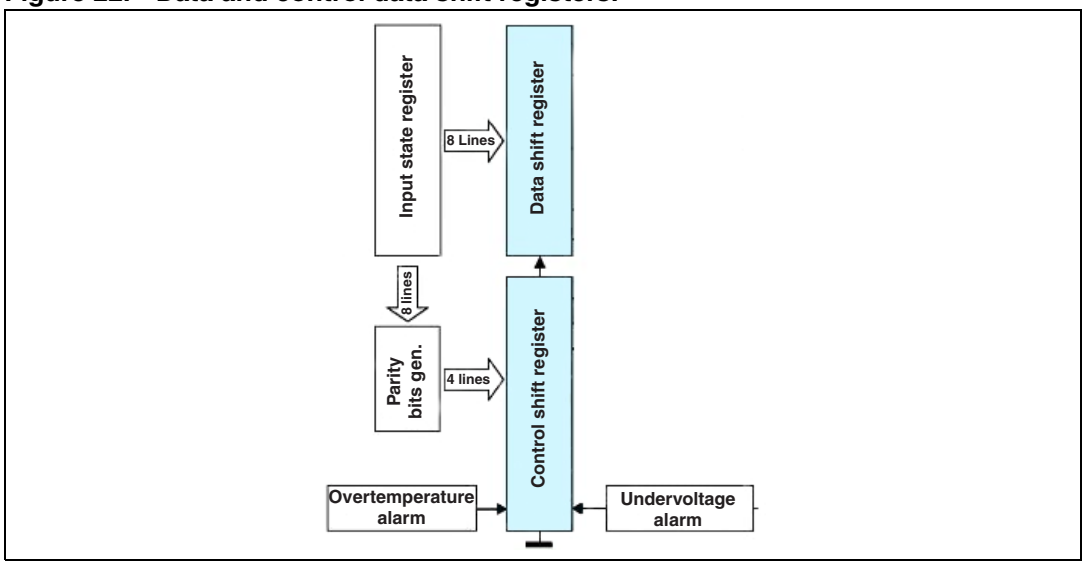
1.4.2 Data shift register and control shift register

Data and control shift registers are each 8 bits long. At each /CS falling edge all the data is frozen and the 8 bits of the input states register are transferred to the data shift register (bits 8 to 15) while the control bits, consisting of four parity bits, overtemperature alarm bit, undervoltage alarm bit and the stop bit, are transferred to the control shift register (bit 0 to 7).

The two last bits (bit 1 and bit 0) are always set respectively to 0 and 1 indicating the end of data frame except in power loss case where all bits are set to 0.

Bit 15 will be the MSB and Bit 0 the LSB.

Figure 22. Data and control data shift registers.



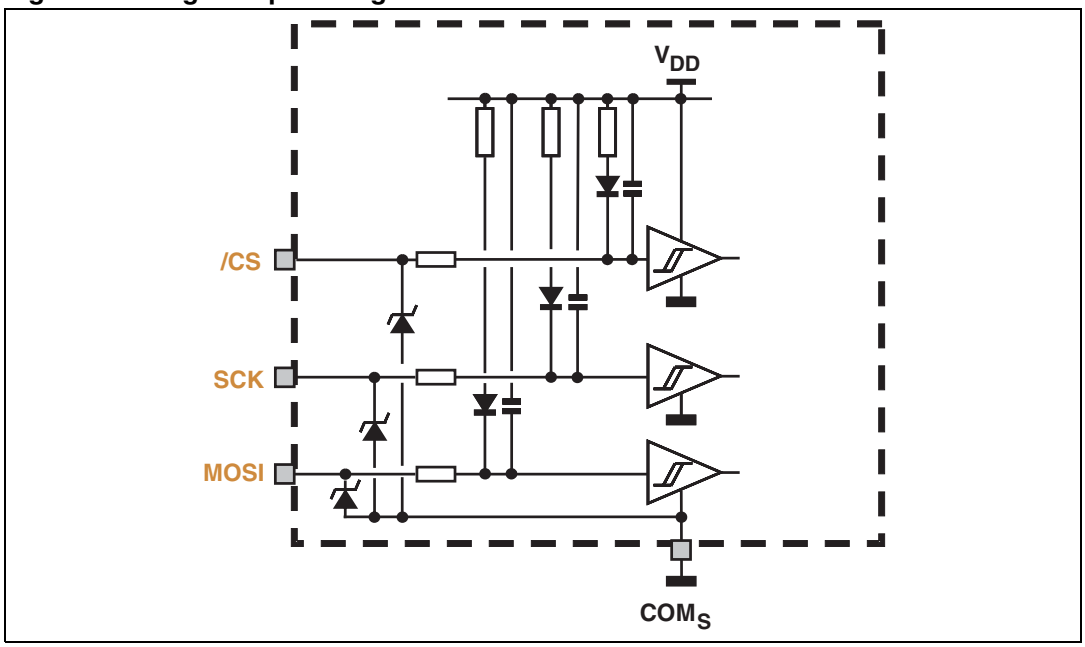
1.4.3 Digital inputs and outputs

These digital pins are involved with the SPI:

- /CS: Chip select input
- SCK: Serial clock input
- MISO: Master-in slave-out output
- /MISO: complementary MISO state
- MOSI: Master-out slave-in input (connected to ground when not used)

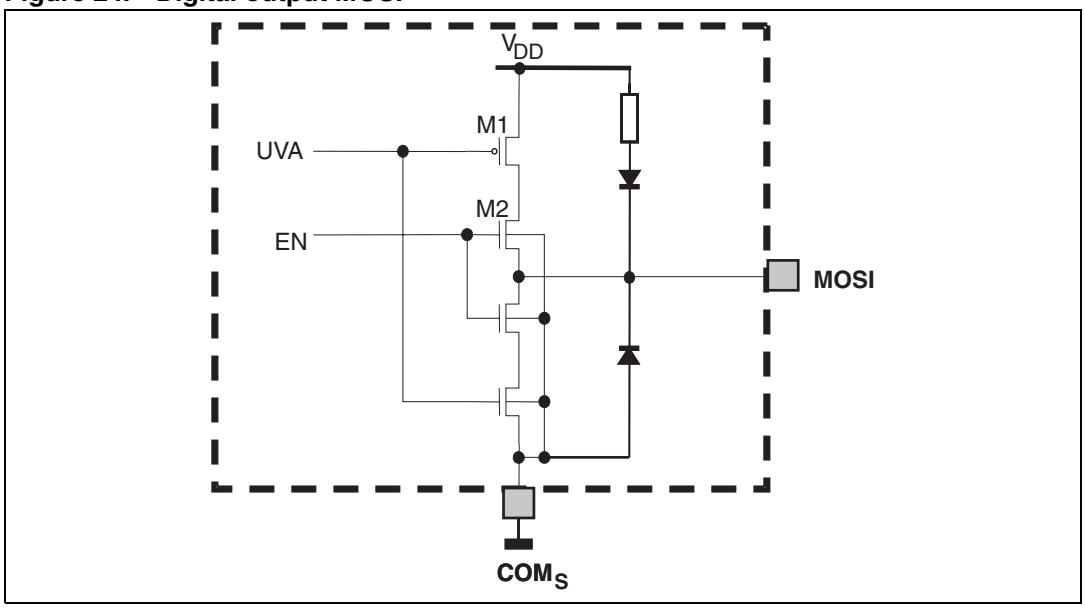
To improve the immunity of the digital inputs against noise, the digital inputs /CS, SCK and MOSI have been designed to use a Schmitt trigger configuration. Each input is connected to V_{DD} through a high impedance pull up resistor to set the input at high level state when no input signal is applied. Protection diodes are inserted with these pull-up resistors to prevent the ESD reaching the V_{DD}. The digital input diagram is given in *Figure 23*.

Figure 23. Digital inputs diagram.



The digital output signal MISO is delivered through a high-Z impedance buffer able to source or sink 3 mA.

Figure 24. Digital output MOSI



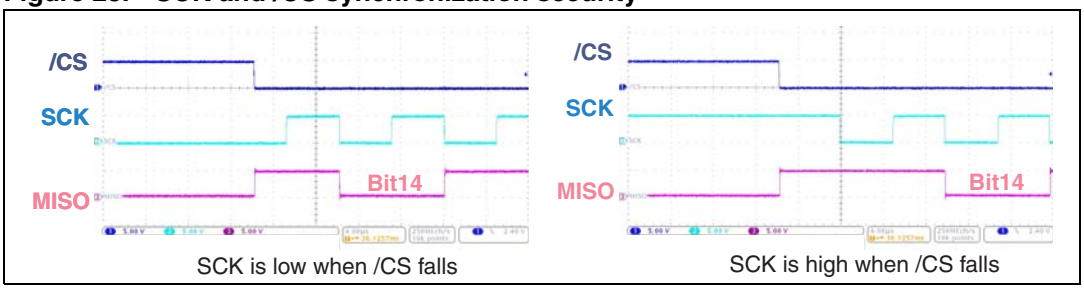
1.4.4 SPI functionality

At the /CS falling edge the following operations are done:

- The input data states, parity and control bits are frozen and stored in the data and control shift registers.
- The MSB (Bit 15) is shifted out first to MISO.

The SCLT3-8 data transfer uses SPI protocol with C_{POL} = 0, C_{PHA} = 0 conditions. This means the SCK signal must be at low level state when the /CS is falling (communication starts). In this case the MSB (bit15) is transferred first from MISO as soon as /CS falls, and all the remaining bits are transferred at each SCK falling edge.

Figure 25. SCK and /CS synchronization security



For more flexibility the SPI protocol has been enhanced and takes into account the case where SCK signal is at high level when /CS falls to low level. In this case, as previously the MSB will be present at MISO pin at the /CS falling edge but the following bit will be available only at the second SCK falling edge.

In both cases the rule is: a rising SCK edge must occur after the falling /CS edge to validate the first SCK falling edge. Otherwise the state change duration of MISO may be too short to correctly trigger the transmission of the MSB (bit 15) (see *Figure 25*).

In normal operation the two last bits are 0 and 1 indicating the end of the transmission.

The data transmission runs as long as the /CS is at low state. As soon as /CS returns to high level, the data transfer is disabled and the MISO output is in high impedance - hi-Z.

When MOSI input is used in daisy chain operation, the inputs are captured at each SCK rising edge and loaded into the shift register. Loaded data has no effect on the SCLT3-8.

Figure 26. 16-bit transmission example

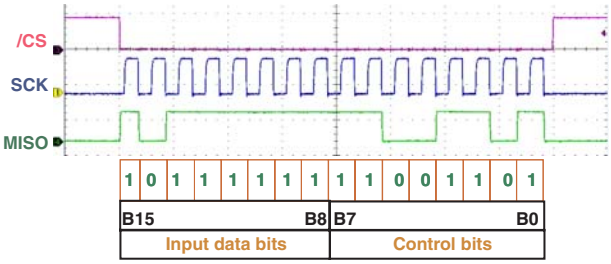


Figure 26 shows a 16-bit transmission example when the application is running in good conditions:

- Application is correctly supplied: /UVA, Bit 7 not activated
- SCLT3-8 junction temperature less than 150 °C: /OTA, bit 6 not activated
- Correct transmission: parity bits in accordance with input states

1.4.5 SPI timing definition

The four SPI signals involved: /CS, SCK, MOSI, MISO are described in *Figure 27*. A fifth /MISO pin output signal is also present.

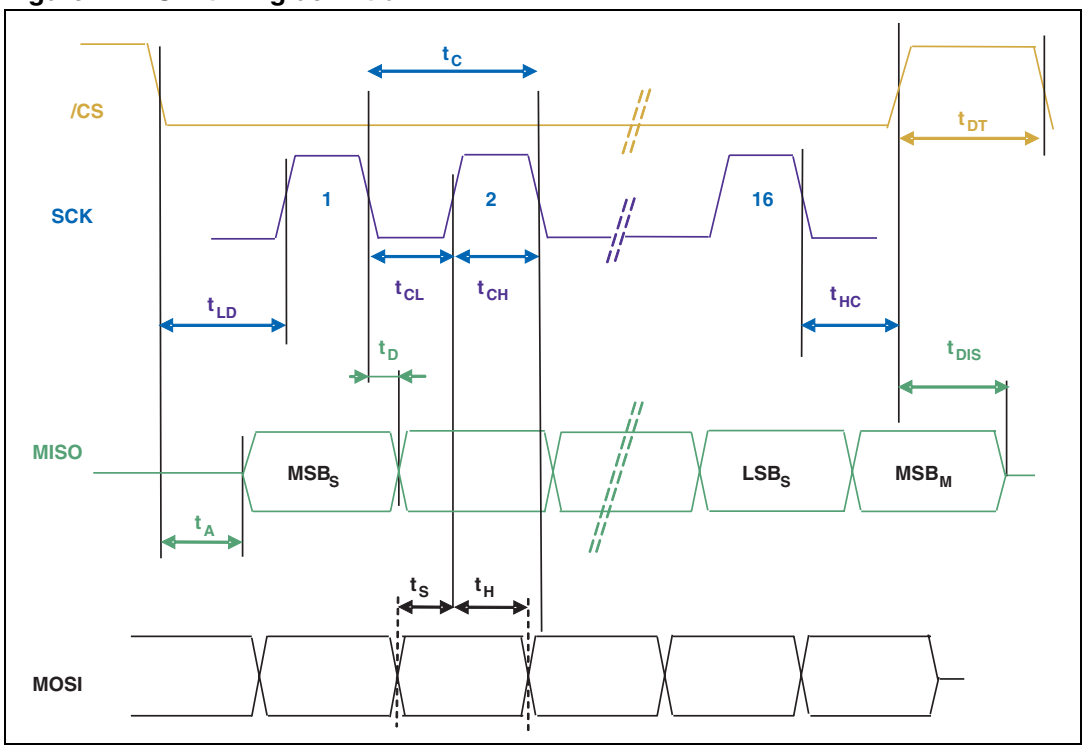
The typical SCK frequency is 1 MHz, but the SCLT3 can run at up to 2 MHz. The other more important timing parameters are:

- t_D: Delay time. This is the delay time of MISO between SCK falling edge and MISO change.
- t_S: Set up time. This is the minimum holding time of MOSI input data for its capture before the SCK rising edge.
- t_H: Holding time. This is the minimum holding time of MOSI input data after the SCK rising edge for its correct capture.

The most important rules to meet to perform a correct data transmission are:

- $t_{CL} > t_D + t_S$
- $t_{CH} > t_H$.

Figure 27. SPI timing definition.



2 Thermal dissipation calculation

2.1 Forward inputs polarity case

In reference to the application schematic defined in *Figure 31*, the dissipated power into the SCLT3-8 P_{SCLT} can be calculated as following:

Consider the worst case where all inputs are connected to 30 V.

$P_{SCLT} = P1 - P2$

where:

P1 is the total power delivered by the supplies

P2 is the total power dissipated by the external components

$P1 = V_{CC} \cdot (I_C + I_{DD} + 8 \cdot I_{LIM})$

External components are: R_{IN}, R_C, LEDs, regulator load

Power dissipated by input resistors = $8 \cdot R_{IN} \cdot I_{LIM}^2$

Power dissipated by supply resistor = $R_C \cdot (I_C + I_{DD})2$

Power dissipated by LEDs = $8 \cdot V_{LED} \cdot I_{LED}$

Power supplied by the V_{DD} linear regulator = $V_{REG} \cdot I_{DD}$

The P_{SCLT} = 560 mW

Assuming:

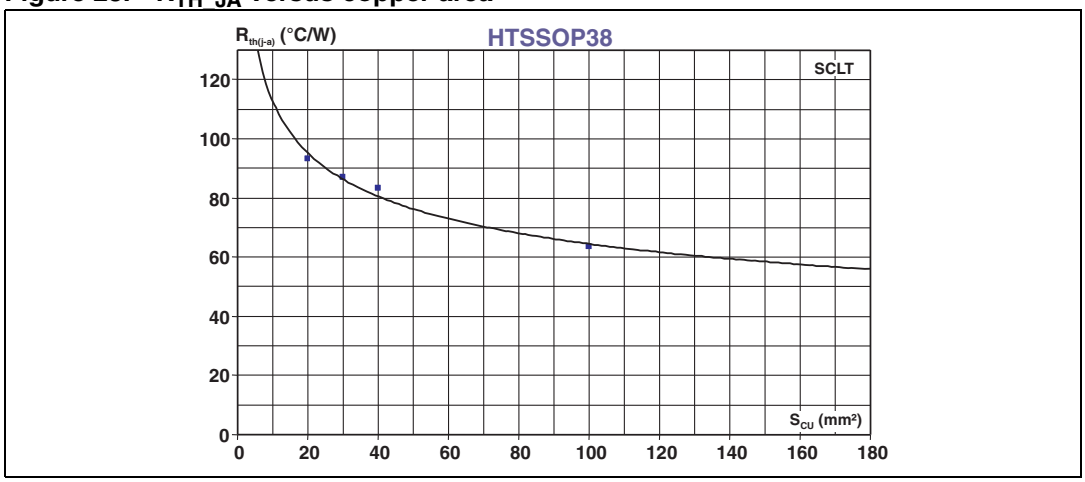
V_{CC} = 30 V, I_{LIM} = 2.35 mA, R_{IN} = 2.2 kΩ, R_C = 1.0 kΩ, V_{LED} = 2 V, V_{DD} = 5 V, I_{DD} = 7MA.

Note: The current flowing through the LED is almost the same as I_{LIMIT}. The difference is about 125 µA used to bias the input circuit device.

With the above mentioned conditions and using copper area of 1cm^2 as heat sink, the SCLT3-8 junction temperature will be around 120 °C with an ambient temperature of 85 °C.

Figure 28 below shows the R_{TH_JA} variations versus the heat sink area on a 35 µm FR4 epoxy single side board.

Figure 28. R_{TH_JA} versus copper area



2.2 Reverse polarity on a single input case

Each input resistor can be connected to a reverse polarity down to -30 V. This case corresponds to a connection mistake or a reverse biasing that is generated by the demagnetization of a monitored inductive solenoid. The involved input can withstand a high reverse current up to 20 mA. The corresponding state transmitted is low level. The other inputs remain operational.

The power dissipated into a reverse polarized input is low, but attention has to be paid to power dissipation into the input resistor which sustains almost all the reverse voltage.

$$P_{dis\_RIN} = \frac{(V_I - 0.7)^2}{R_{IN}}$$

$$P_{dis\_RIN} = 390\ mW \text{ for } V_{IN} = -30\,V \text{ and } R_{IN} = 2.2\ k\Omega$$

2.3 Temperature gradient on the SCLT3 and on the board

Figure 29 shows the case top temperature when SCLT3-8 dissipates 600 mW, which corresponds to maximum supply case with V_{CC} and all module inputs at 32 V. The heat sink is 100 mm^2, and the ambient temperature is 25 °C. In this example the maximum case top temperature reaches 68 °C. The case top temperature is a good indication of the junction temperature, which can be estimated using thermal analysis techniques.

Figure 29. Case top temperature

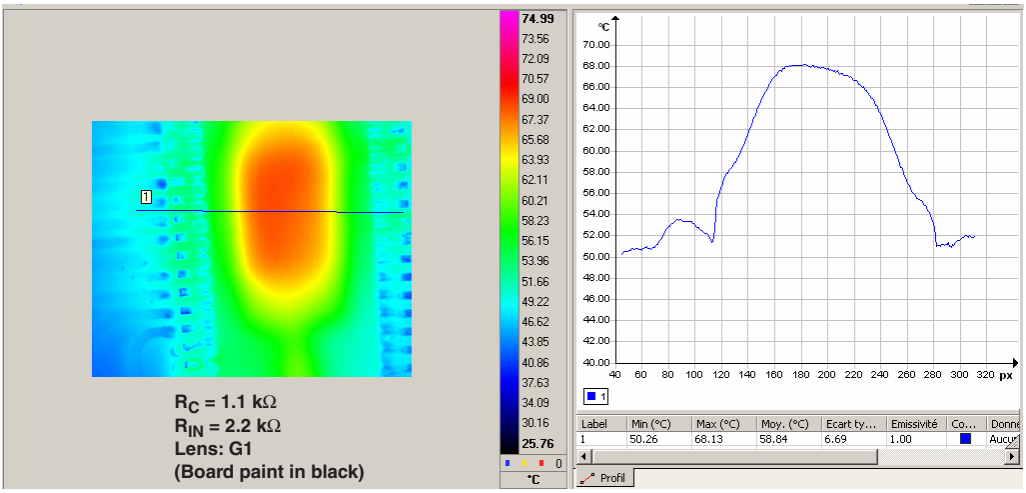
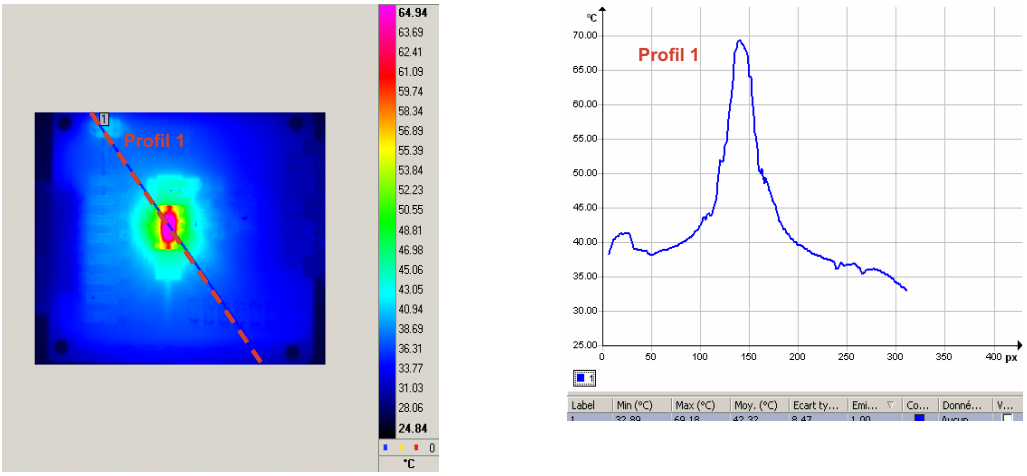


Figure 30 shows the temperature gradient of the SCLT3-8 board with the same supply conditions as above. Almost the totality of the power is concentrated around the SCLT3-8 and its heatsink. No particular temperature hot spot can be detected on the board.

Figure 30. Temperature gradient of the board



3 Application circuit

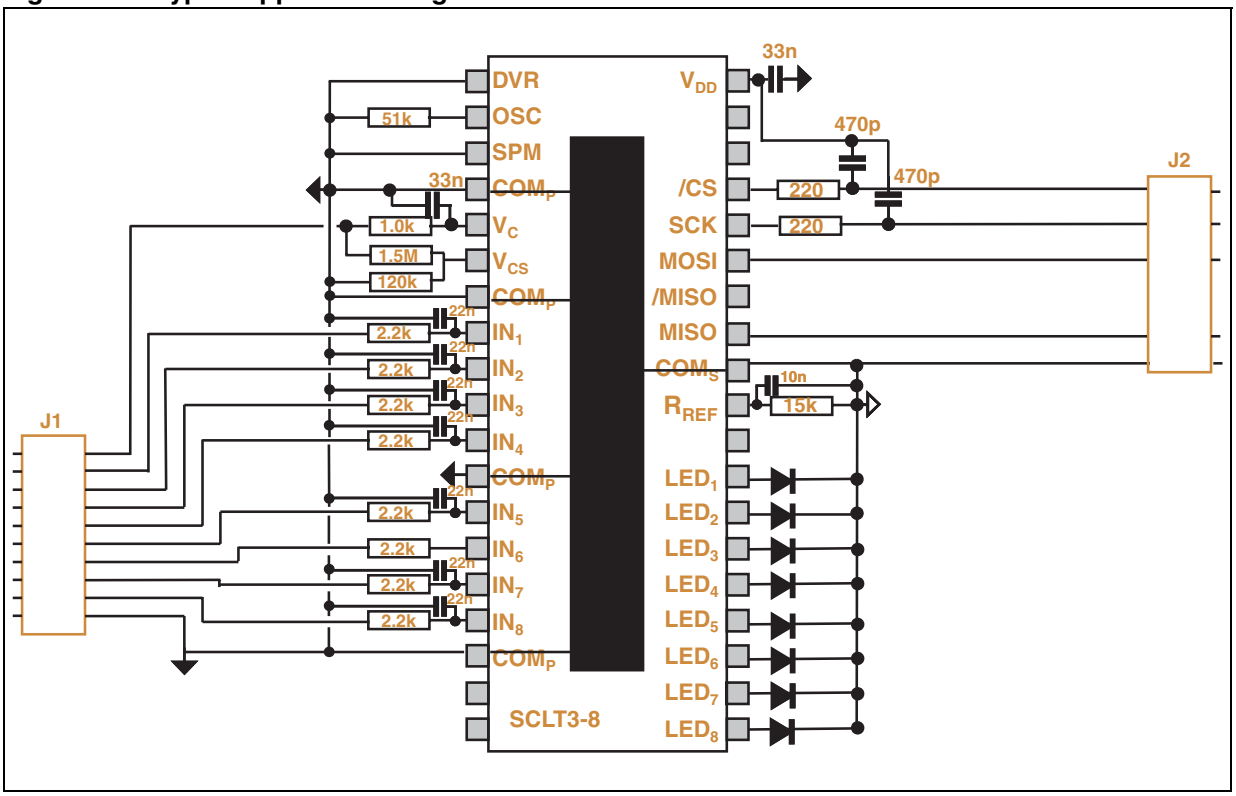
3.1 Basic SCLT3-8 board description

The basic electrical schematic diagram using a single SCLT3-8 fulfills the requirements defined in the IEC 6131-2 standard. It is easy to duplicate this configuration to meet more complex applications using many inputs and several SCLT3-8s.

The major settings are:

- Type 3 configuration
- 16-bit frame (SPM grounded)
- 16 µs digital input filtering (R_{OSC} = 51 kΩ, DVR grounded)

Figure 31. Type 3 application diagram



3.2 Component definitions

The reference resistor R_{REF} tolerance gives the accuracy of the input limiters. 1% accuracy is suggested.

The typical type 3 SCLT3-8 application uses R_{REF} = 15 kΩ and R_{IN} = 2.2 kΩ. Type 2 can be also achieved as shown in *Table 3*.

The input MELF resistors are used to sustain high voltages occurring during surge tests.

Table 3. Type 2 and 3 configurations

	Type 3	Type 2	Unit
R_{REF}	15	3.9	kΩ
R_{IN}	2.2	0.75	kΩ
Typical I_{LIMIT}	2.3	6.5	mA

Using type 2, the power dissipated by the SCLT3-8 reaches 1W with $V_I = V_{CC}$ = 24 V. A copper heat sink area of 1 cm^2 will set T_J at 150 °C with an ambient temperature of 65 °C.

The R_C value has to be chosen with attention. The voltage drop across this resistor is the product of SCLT3-8 supply current and any load current supplied by VDD: regulator output current and sourced MISO current. The resulting voltage V_C must be in any case above the 8 V activation threshold to avoid a spurious power loss detection. 1 kΩ meets this requirement and allows 2 kV of voltage surge.

The 22 nF input capacitors are used to improve the noise immunity of the whole module. Their function is to filter the high frequency electrical noise, and to secure the off state of the module.

Adding a 33 nF capacitor on V_C pin ensures high immunity against electrical noise such as that described in the IEC 61131-2 standard.

R_{OSC} = 51 kΩ and pin DVR grounded set the input digital filter to eliminate pulse widths below 20 µs.

A 33 nF capacitor connected on V_{DD} output ensures a good output of the voltage regulator.

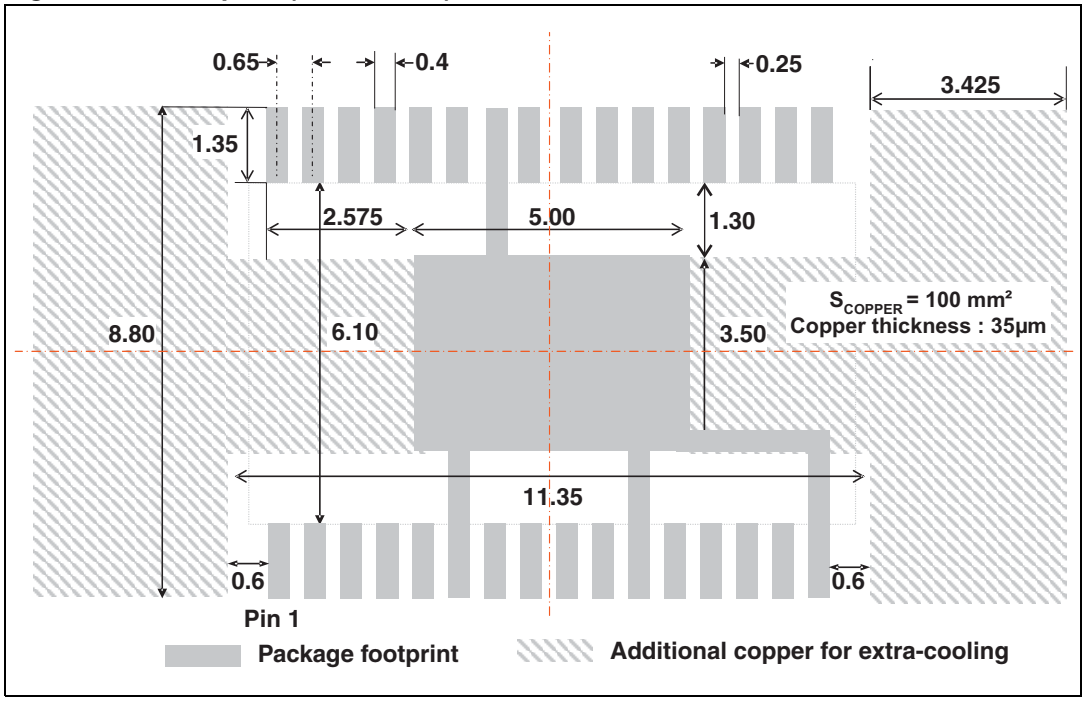
The LEDs must be chosen according to their input diode drop voltage. LED outputs can drive LEDs with forward voltage up to 2.7 V.

Low pass RC filters have been inserted into digital inputs /CS and SCK to improve the immunity against fast transient bursts. R = 220 Ω and C = 470 pF give a good compromise between immunity result and SCLT-3 speed which can run up to 1 MHz.

3.2.1 Footprint

The footprint given in *Figure 32* allows ground connection optimization of COM_P and $COMP_S$. The 1 cm^2 heat sink area defines an R_{TH-JA} of 80 °C/W.

Figure 32. Foot print (not to scale)



4 Isolation management

There are two solutions proposed for galvanic isolation between the SCLT3-8 and the microcontroller.

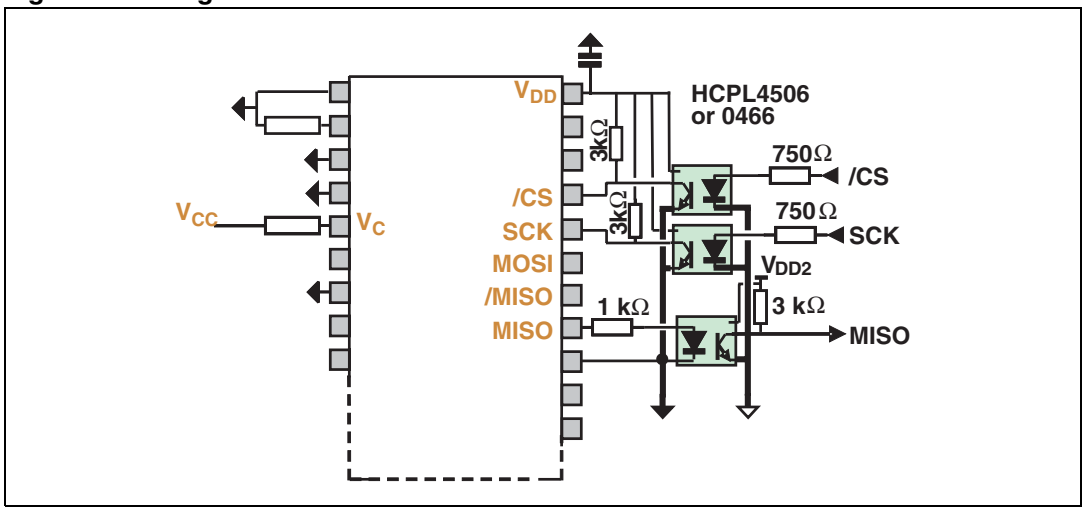
- Opto-coupler isolation
- Magnetic digital isolation

4.1 Opto-coupler isolation

The first solution is given by opto-couplers which must run at a bit rate compatible with the SCK frequency and meet SCLT3-8 requirements in terms of consumption.

HCPL4506 or HCPL0466 can be a solution to drive a single SCLT3-8 for a 1 MHz application.

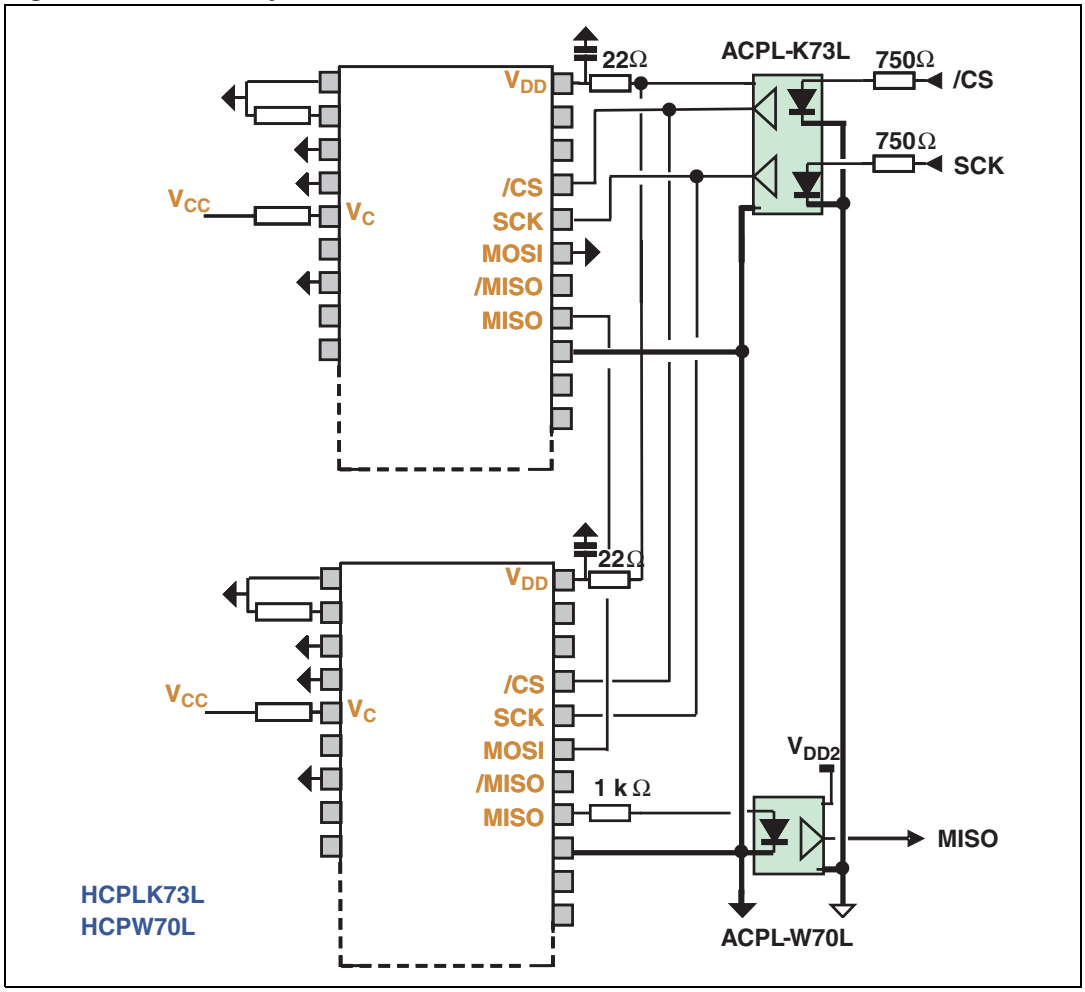
Figure 33. Single SCLT3-8 and HCPL4506 or 0466



If several SCLT3-8s are used, more current is available through V_{DD} pins to supply the opto-couplers. The different outputs V_{DD} can be tied together but, low serial resistors (22 Ω) must be inserted to balance the different regulated output voltages. The load current is shared between the two SCLT3s and allows the voltage drop reduction across each R_C resistor.

Figure 34 shows two SCLT3s in daisy chain configuration using ACPL-K73L (dual) and ACPL-W70L (single).

Figure 34. Two daisy-chained SCLT3-8s and ACPL/K73L/W70L

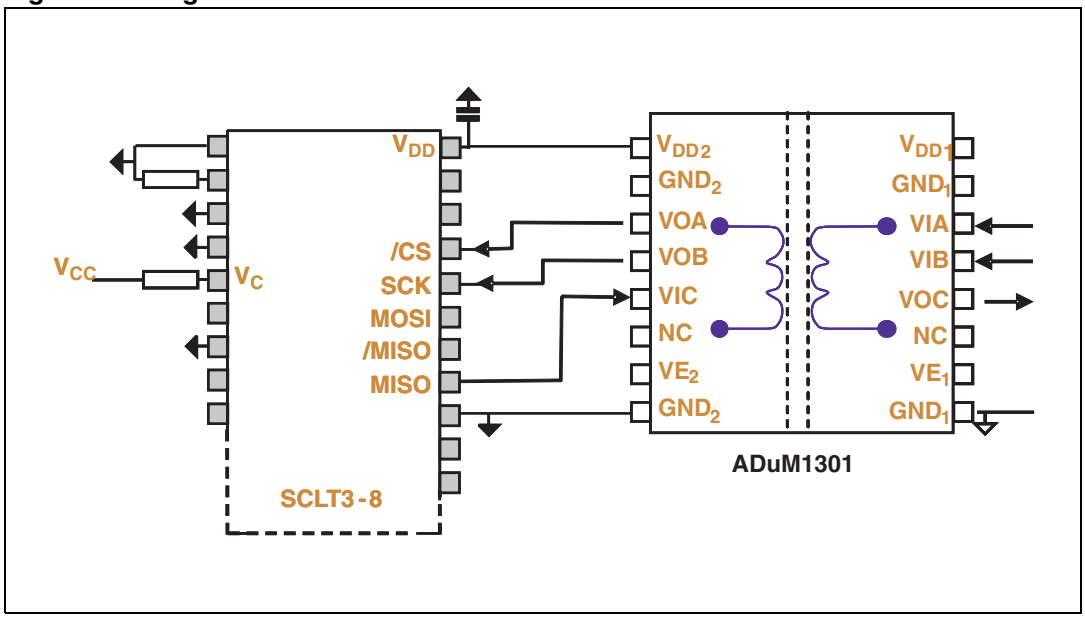


4.2 Magnetic digital isolator

The second solution is given by digital isolators. The triple-channel digital isolator ADUM1301 is convenient for such an SCLT3-8 application. The sending channels V_{IA} and V_{IB} are used for /CS and SCK signals while receiving channel V_{IC} is used for MISO signal.

The V_{DD} pin of SCLT3-8 can easily deliver the typical supply current needed by V_{DD2}, which is around 2.7 mA at 2 MHz as shown in *Figure 35*.

Figure 35. Digital isolator



5 SCLT3-8 link configurations

Parallel and daisy chain configurations can be implemented using SCLT3-8 or other devices compatible with a serial peripheral interface.

In parallel mode the microcontroller selects the SCLT-8 with which it wants to communicate by setting the corresponding /CS to low state as long as the communication lasts. The microcontroller should be able to control as many /CS pins as SCLT-8s it wants to address.

While in daisy chain configuration the microcontroller commands at the same time all the SCLT3-8s connected in series. The data must transit from SCLT3-8 to SCLT3-8 going out from the MISO pin, going in through MOSI pin till reaching the last one connected to the microcontroller. Considering n SCLT3-8s connected in daisy chain, the microcontroller has to read n times 16 bits and the communication time is proportional to n times 16 bits.

Figure 36. Daisy-chain configuration

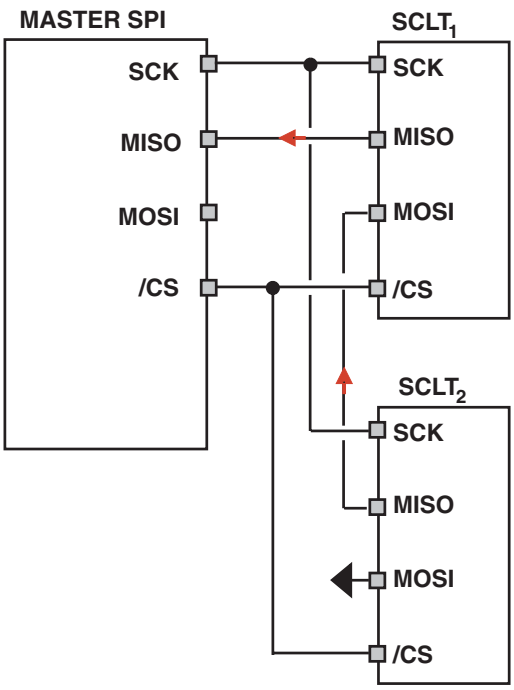
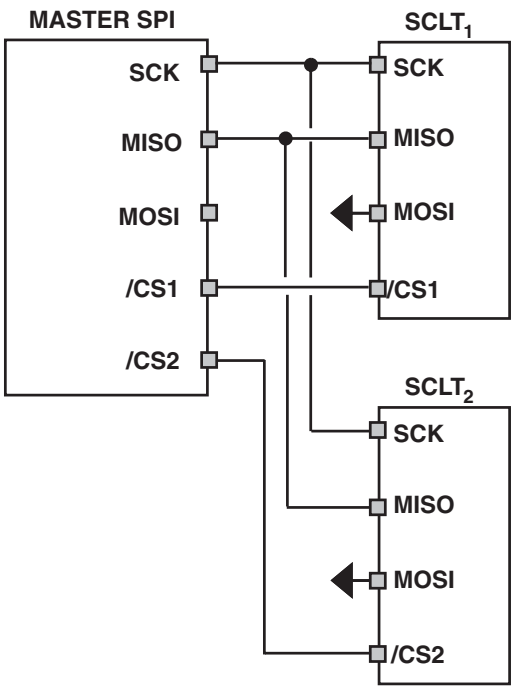


Figure 37. Parallel configuration

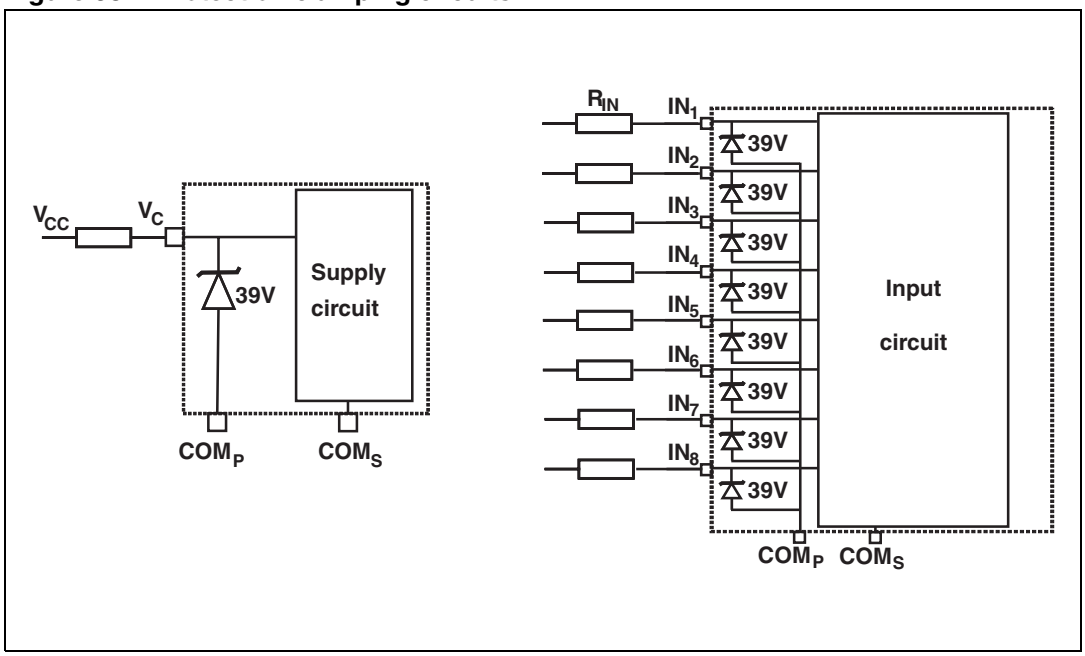


6 Electromagnetic compatibility (EMC) requirements

The SCLT3-8 has been designed to withstand electromagnetic interference as specified in the IEC 61131-2 standard. This international standard gives all the requirements and conditions for tests that must be performed on the programmable logic controllers (PLC) and their associated peripherals. IEC 61000 4-2, 4-4, 4-5 and 4-6 standards define test methods.

The current limited inputs and supply pins of SCLT3-8 are protected against high voltage disturbances by a clamping circuits that are grounded to the common pin COM_P. Combined with serial input resistances R_{IN} or R_C (see *Figure 38*). These clamping circuits are effective against ESD (±8 kV contact), fast transient burt (±2.5 kV), and voltage surge (±1 kV).

Figure 38. Protection clamping circuits



6.1 IEC 61000 4-2

This standard specifies the behavior of the device when subjected to electrostatic discharges. The discharges must be applied to operator accessible parts. This means that these tests have to be performed on each connector pin. The required levels are: air discharge: ±15 kV, contact discharge: ±8 kV.

The system must continue to operate as intended after the discharge. Temporary degradation of the performance is acceptable during the test, but the system must recover by itself after the test (B criterion).

All SCLT3-8 pins are ESD protected.

6.2 IEC 61000 4-4

This standard specifies the behavior of the device when subjected to a fast transient burst. The fast transient burst must be applied on all the input pins of the system. A capacitive clamp-coupling device is used as described in the IEC 61000-4-4 standard. The required sustainable burst voltage level is 2.5 kV. The system must continue to operate as intended. No temporary degradation of the performance is acceptable during the test (A criterion).

New test methodology has been set up to check the frame integrity against fast transient bursts. The need to monitor each bit level leads to using a scope isolated from the test bench through optic fibers. The generation of /CS and SCK input signals are also isolated through the same way as shown in *Figure 39*. Current and voltage level adaptation is done through an optical fiber interface (OFI).

Long frames history can be stored in the monitoring scope for an easier detection of disrupted bits.

The SCLT3-8 immunity has been increased by adding RC filter networks connected on /CS and SCK input pins. But these RC filters act as low pass filters and limit the maxim data transfer speed. For example the filter made of R = 220 Ω, C = 470 pF allows a 1 MHz transmission frequency and ensures device FTB immunity up to 4 kV.

Table 4. Speed - FTB immunity compromise

RC Values	SCK speed	FTB immunity
220 Ω - 220 pF	2 MHz	3 kV
220 Ω – 470 pF	1 MHz	4 kV

The test configuration is shown in *Figure 39*.

Figure 39. Two supplies configuration

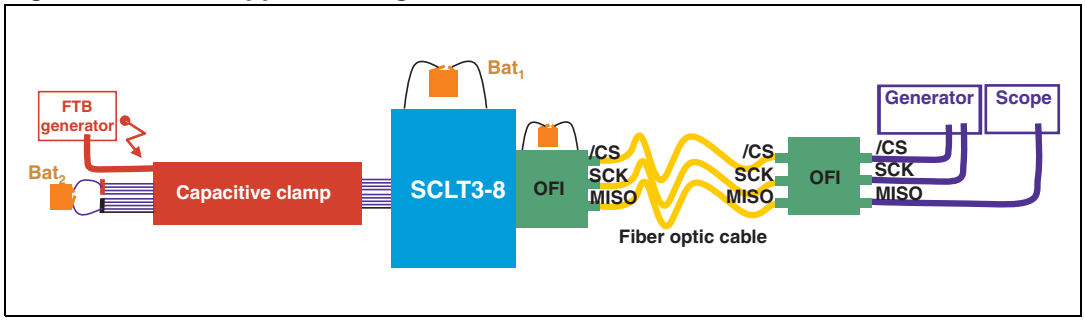


Figure 40 shows the output MISO behavior is not disturbed during fast transient bursts. The FTB signal has been captured through an antenna to observe where the bursts act.

Figure 40. Output MISO behavior during fast transient bursts

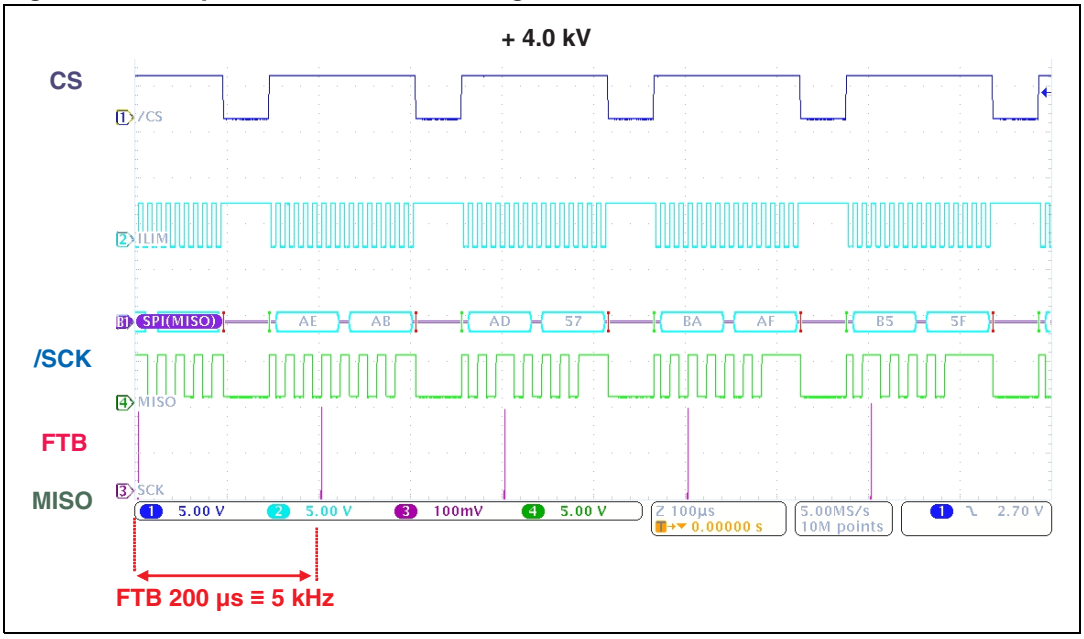
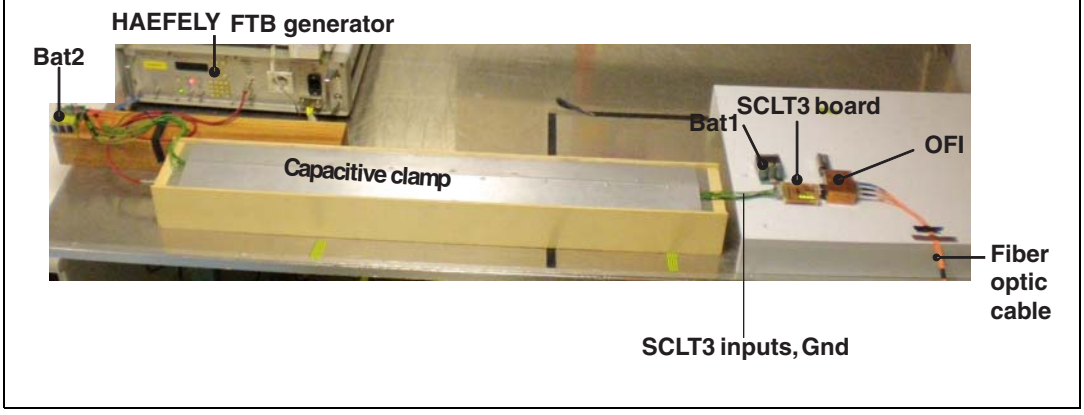


Figure 41. Test bench



6.3 IEC 61000 4-5

This standard specifies the behavior of the device when subjected to voltage surges applied on all input pins of the system. For all analog inputs, the coupling method is a 42 Ω serial resistance and a 0.5 µF capacitor. For the DC power line, the coupling is 2 Ω resistor, and 18 µF capacitor. The required voltage surge levels are:

- 1 kV for the input pins with R_{IN} = 2.2 kΩ,
- 2.5 kV for the pin V_C when R_C = 2.2 kΩ or 1 kV when R_C = 500 Ω.

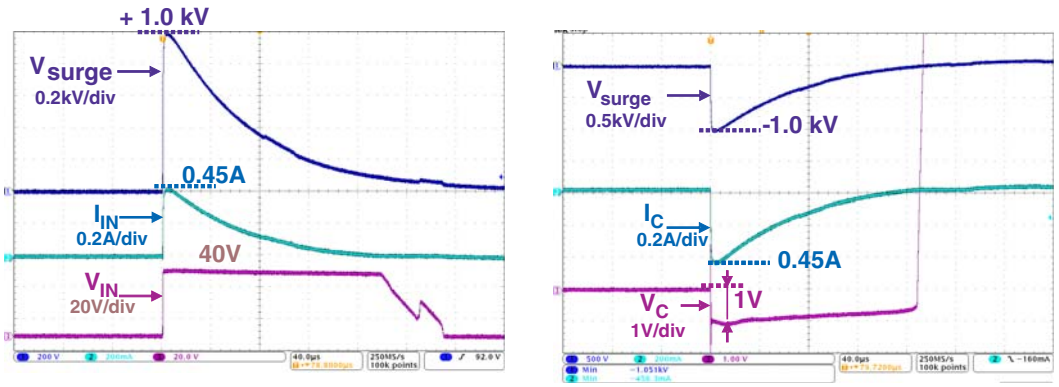
The system must continue to operate as intended. Temporary degradation of the performance is acceptable during the test, but the system must recover by itself after the test (B criterion).

6.3.1 Results on input pins

When a positive surge voltage of 1 kV is applied on the input resistor R_{IN}, the input active clamp protects the SCLT3-8 input and limits the input voltage at 40 V. The input current reaches 0.45 A.

When a negative voltage surge is applied the input diode is biased in forward mode and the current is 0.45 mA (see *Figure 42*)

Figure 42. V_{IN} and I_{IN} behavior

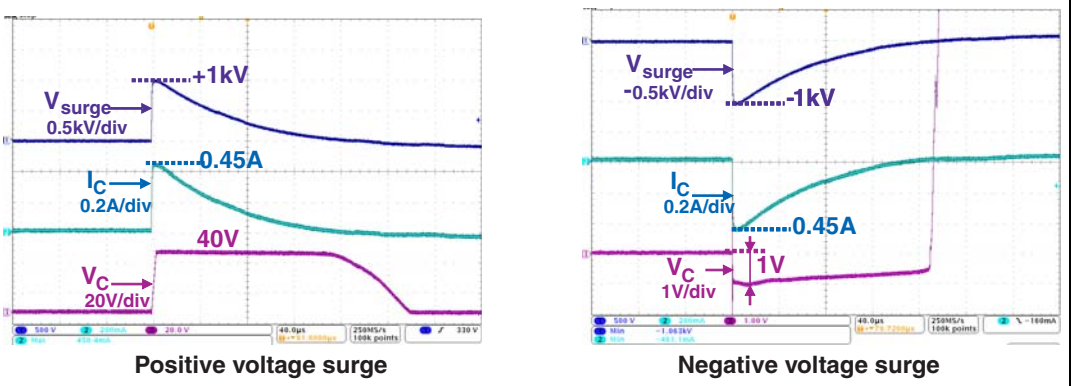


6.3.2 Results on V_C pin

When a positive or negative surge voltage of 1 kV is applied on the supply resistor R_C, the V_C active clamp protects the SCLT3-8 input and limits the input voltage at 40 V. The current reaches 0.45 A.

The wave shapes are similar to the previous ones as shown in *Figure 43*.

Figure 43. V_C behavior with R_C = 2.2 kΩ

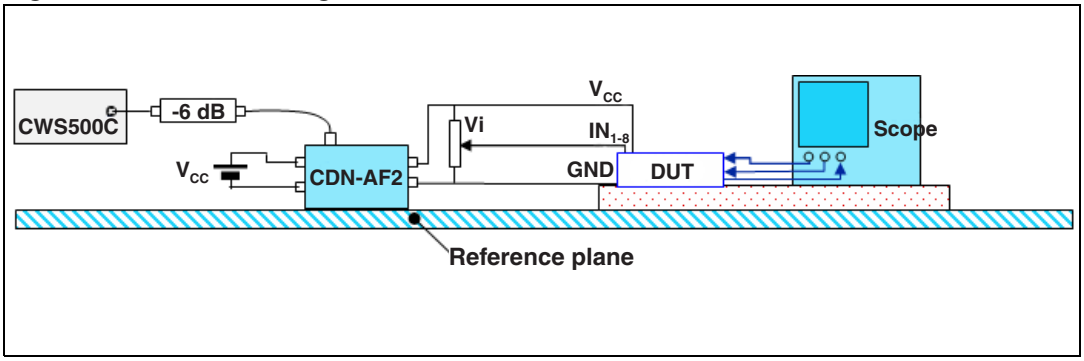


6.4 IEC 61000 4-6

This standard specifies the behavior of the device when subjected to conducted radio frequency interference in the range 150 kHz to 80 MHz. The RF signal, 80% modulated by 1 kHz sinusoidal waveform, is injected at the inputs I_{IN} and V_{CC} through a coupling device network (CDN). The required level defined into IEC 61131-2 is 3 V rms. With these stress conditions, the system must continue to operate with no loss of function (A criterion).

The test configuration used is shown in *Figure 44*.

Figure 44. RF test configuration



SCLT3-8 meets IEC 61000 4-6 and IEC 61311-2 standards requirements. Better immunity can be obtained by decoupling pin SCK with a 470 pF capacitor.

7 Conclusion

This application note illustrates how designers can maximize SCLT3-8 performances in their applications especially in the fields of bus controller interface configurations, thermal behavior and EMI robustness. They will find information that helps them to design new system boards while saving time.

Designed for digital I/O module in factory automation, the SCLT3-8 is a low-loss EMI-proof solution showing high usage flexibility. With the SCLT3-8, designers will be able to develop highly integrated modules interfacing proximity sensors with the following benefits:

- Reduced pin count
- Saved space (only 3 isolation devices for SPI)
- Reduced dissipation
- No need for additional LED supply
- Common SPI availability
- EMI proof

To illustrate its performances and advantages, an evaluation board STEVAL-IFP000V1 using 2 SCLT3-8s configured in daisy chain is available with an optimized layout.

8 Revision history

Table 5. Document revision history

Date	Revision	Changes
22-Feb-2010	1	Initial release.