AN2815
Application note

High-efficiency step-down controller with embedded 2 A LDO regulator

Introduction

The PM6675AS device consists of a single, high-efficiency step-down controller and an independent low dropout (LDO) linear regulator.

The constant on-time (COT) architecture assures fast transient response supporting both electrolytic and ceramic output capacitors. An embedded integrator control loop compensates the DC voltage error due to the output ripple.

Selectable low-consumption mode allows the highest efficiency over a wide range of load conditions. The low-noise mode sets the minimum switching frequency to 33 kHz for audio-sensitive applications. The LDO linear regulator can sink and source up to 2 Apk. Two fixed current limits (±1 A and ±2 A) can be chosen.

An active soft-end is independently performed on both the switching and the linear regulators outputs when disabled.

Figure 1. PM6675AS demonstration board

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Contents

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1 Main features

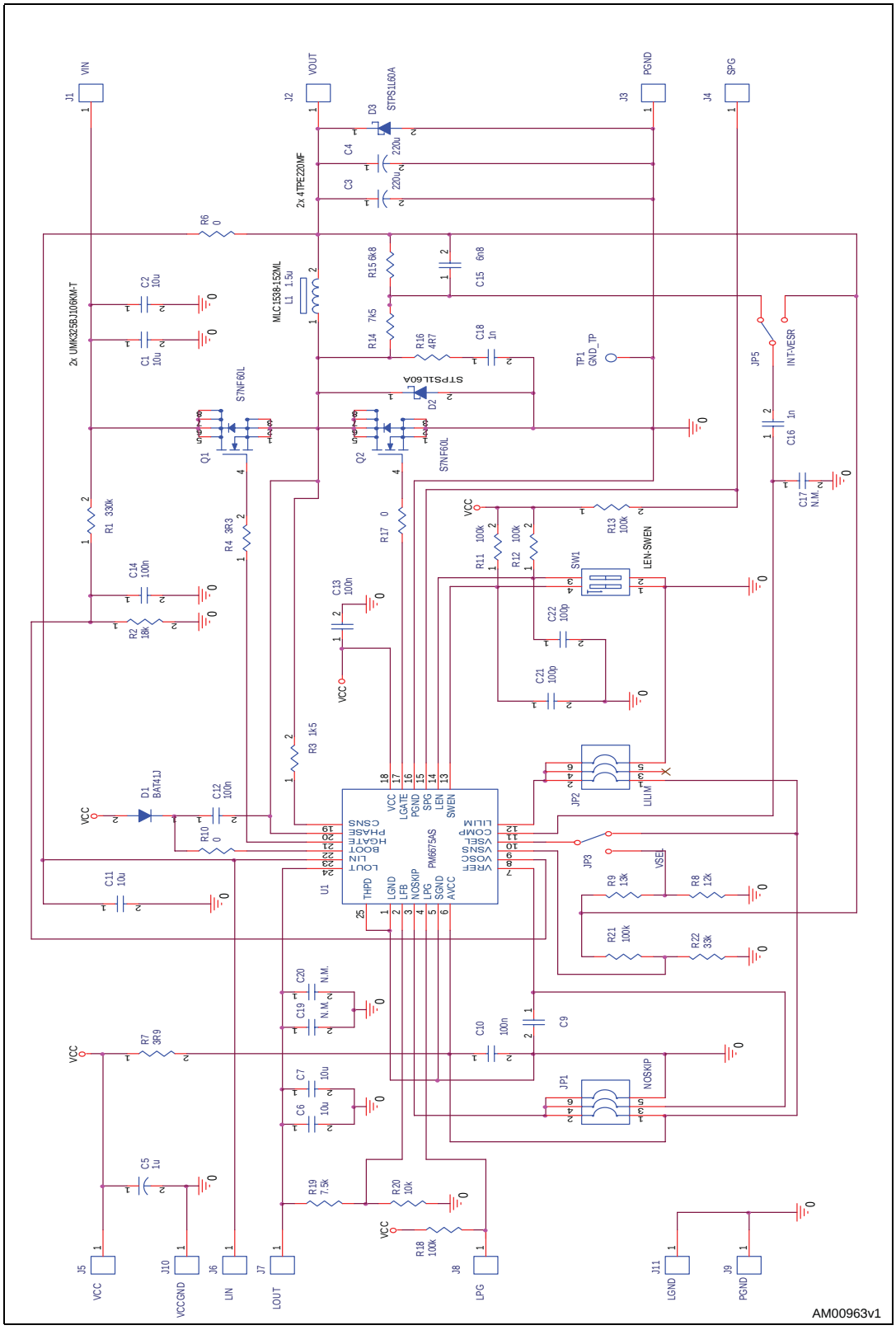
1.1 Switching section

- 4.5 V to 36 V input voltage range
- 0.6 V, ±1% voltage reference
- 1.5 V fixed output voltage
- 0.6 V to 3.3 V adjustable output voltage
- 1.237 V ±1% reference voltage available
- Very fast load transient response constant on-time loop control
- No-R_{SENSE} current sensing using low-side MOSFETs' $R_{DS(on)}$
- Negative current limit
- Latched OVP, UVP and thermal shutdown
- Fixed 3 ms soft-start
- Selectable pulse-skipping at light load
- Selectable non-audible (33 kHz) pulse-skip mode
- All ceramic output capacitor applications supported
- Output voltage ripple compensation
- Output soft-end

1.2 LDO section

- 0.6 V to 3.3 V adjustable output voltage
- Selectable ±1 A or ±2 A current limit
- Dedicated Power Good signal
- Ceramic output capacitors supported
- Output soft-end

Figure 2. PM6675AS demonstration board schematic



2 Bill of material

Table 1. PM6675AS demonstration board bill of material

Qty	Component	Description	Package	Part number	Manufacturer	Value
2	C1, C2	Ceramic, 50 V, X5R, 20%	SMD 1210	UMK325BJ106KM-T	Taiyo Yuden	10 µF
2	C3, C4	POSCAP, 4 V, 15 mΩ, 20%	SMD D Case	4TPE220MF	Sanyo	220 µF
1	C5	Ceramic, 6.3 V, X5R, 10%	SMD 1206		Standard	1 µF
3	C6, C7, C11	Ceramic, 6.3 V, X5R, 10%	SMD 0805	JMK212BJ106KG-T	Taiyo Yuden	10 µF
4	C9, C10, C13, C14	Ceramic, 50 V, X7R, 20%	SMD 0603		Standard	100 n
1	C12	Ceramic, 50 V, X7R, 10%	SMD 0805		Standard	100 n
1	C15	Ceramic, 50 V, X7R, 10%	SMD 0603		Standard	6n8
1	C16	Ceramic, 50 V, X7R, 10%	SMD 0603		Standard	1 n
1	C17	Ceramic, 20%	SMD 0603		Standard	N.M.
1	C18	Ceramic, 50 V, X7R, 10%	SMD 0805		Standard	1 n
2	C19, C20	Ceramic, 6.3 V, X5R, 10%	SMD 0805	JMK212BJ106KG-T	Taiyo Yuden	N.M.
2	C21, C22	Ceramic, 50 V, X7R, 10%	SMD 0603		Standard	100 p
1	R1	Chip resistor, 0.1W, 1%	SMD 0603		Standard	330 kΩ
1	R2	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	18 kΩ
1	R3	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	1.5 kΩ
2	R4, R7	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	3R3
1	R6	Chip resistor, 0.1 W, 1%	SMD 0805		Standard	0
1	R8	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	12 kΩ
1	R9	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	13 kΩ

Table 1. PM6675AS demonstration board bill of material (continued)

Qty	Component	Description	Package	Part number	Manufacturer	Value
3	R10, R17, R21	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	0
4	R11, R12, R13,R18	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	100 kΩ
1	R14	Chip resistor, 0.1 W, 1%	SMD 0805		Standard	15 kΩ
1	R15	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	3k9
1	R16	Chip resistor, 0.1 W, 1%	SMD 0805		Standard	4R7
1	R19	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	7k5
1	R20	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	10 kΩ
1	R22	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	N.M.
1	L1	SMT, 10.6 Arms, 4.36 mΩ	13.8x13.2 mm	MLC1538-152ML	Coilcraft	1.5 µH
2	Q1, Q2	N-Channel, 60 V	SO-8	STS7NF60L	STMicroelectronics	
1	D1	Schottky, 100 V, 0.2 A	SOD-323	BAT41J	STMicroelectronics	
1	D2	Schottky, 60 V, 1 A	DO214-AC	STPS1L60A	STMicroelectronics	
1	D3					N.M.
1	U1	Controller	VFQFPN-24	PM6675AS	STMicroelectronics	
11	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10,J11	Header, single pin				
3	JP1, JP2, JP3	Jumper, 2x3, 100 mils				JP4 N.M.
1	JP5	PCB pads selector				
1	TP6	Test point				
1	SW1	Dip switch 2	DIP-2		Standard	

3 Component assembly and layout

Figure 3. Top side component placement

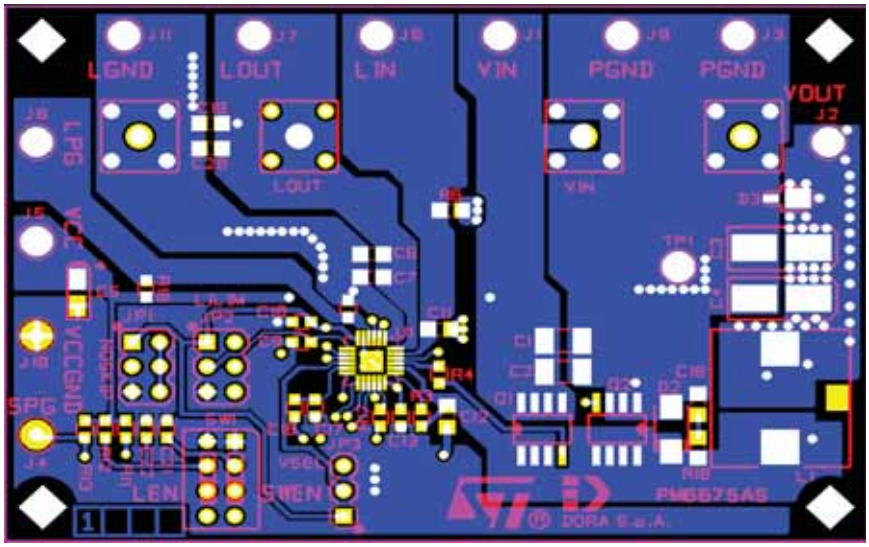


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Figure 4. Top view

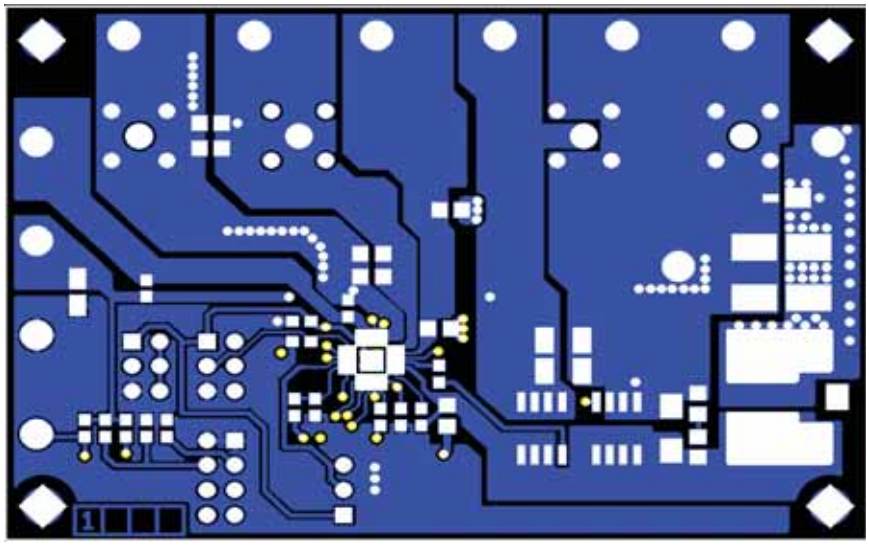

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Figure 5. Layer 2 view

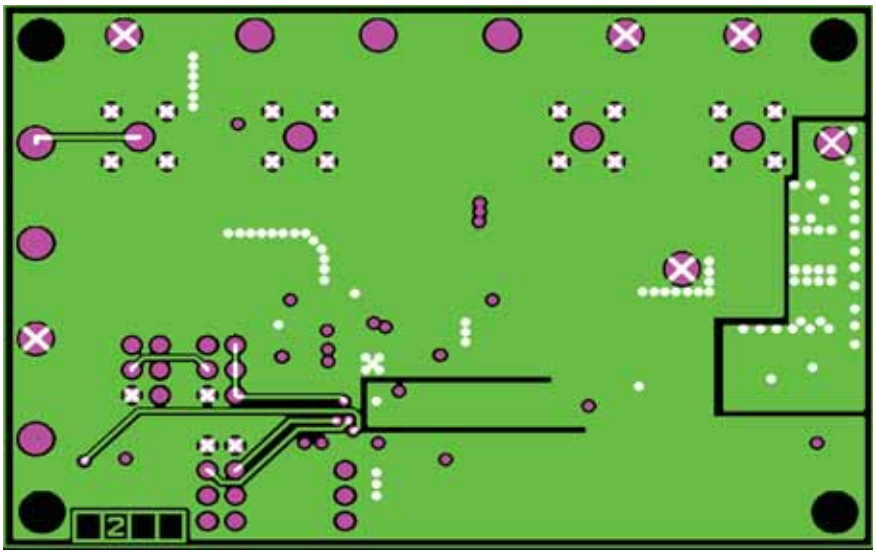

Figure 6. Layer 3 view

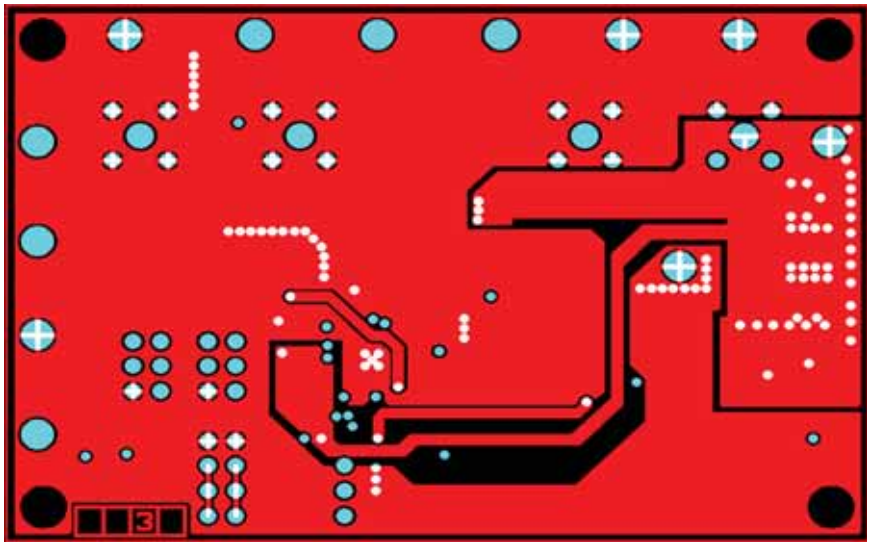

Figure 7. Bottom view

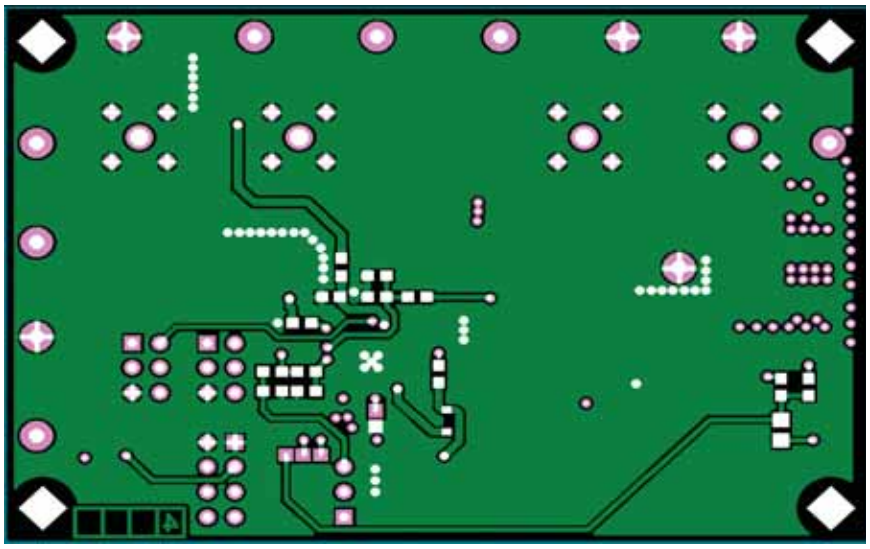

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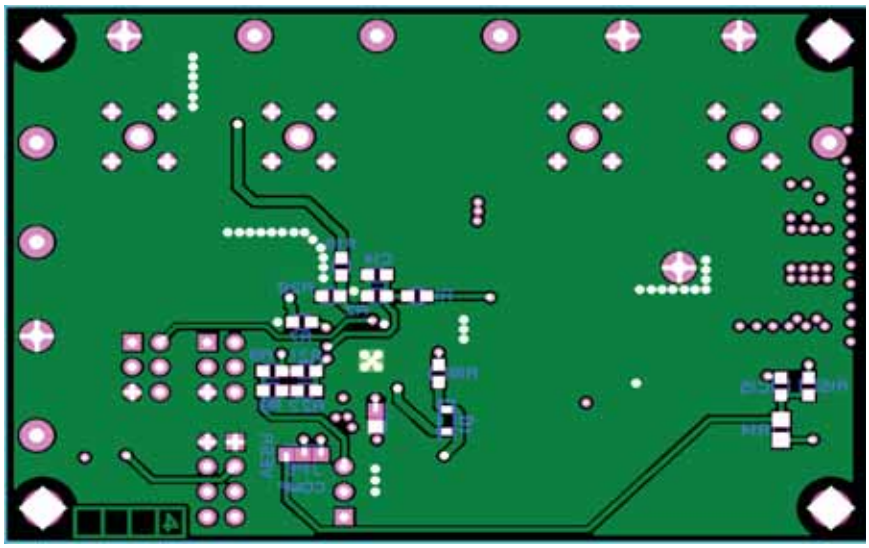
Figure 8. Bottom side component placement



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4 I/O interface

The PM6675AS demonstration board has the following test points as shown in *Table 2*.

Table 2. PM6675AS demonstration kit input and output interface

Test point	Description
VIN	Battery input voltage positive terminal
V_{OUT}	Switching regulator output
PGND	Battery input and VOUT output common return
L_{IN}	LDO linear regulator input
L_{OUT}	LDO linear regulator output
LGND	LDO linear regulator output return
LPG	LDO linear regulator Power Good signal
VCC	+5 V supply, positive terminal
VCCGND	Signal ground and VCC supply return
SPG	V_{OUT} SW regulator Power Good signal
TP1	Connection point between power and signal grounds

5 Recommended equipment

- 4 V to 36 V, 30 W power supply
- Active loads
- Digital mutimeters
- 200 MHz four-trace oscilloscope

6 Configuration

The PM6675AS demonstration board allows the user to choose the desired mode of operation using four jumpers (JP1, JP2, JP3 and JP5) and two resistors. Refer to the following configuration description.

6.1 JP3 fixed or adjustable output voltage (VSEL pin)

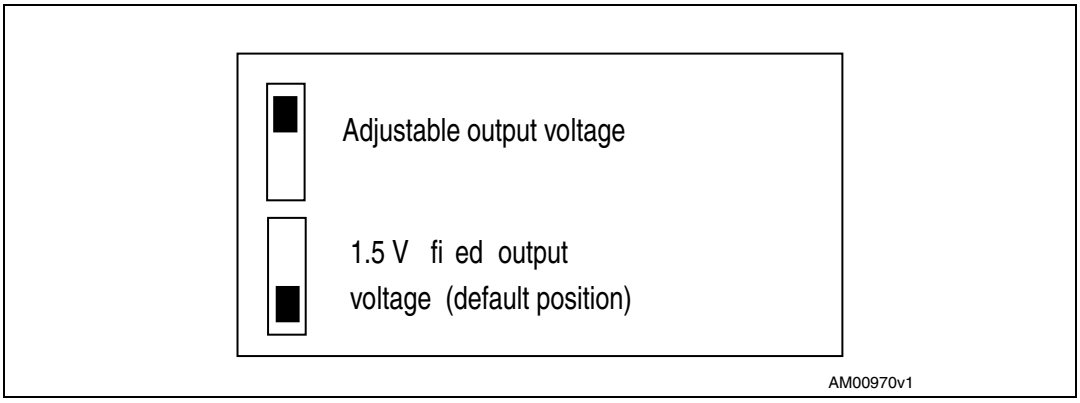
The JP3 jumper is used to choose between fixed output voltage (1.5 V) and a user-defined output voltage in the range 0.6 V to 3.3 V. When connected in the lower position, the fixed 1.5 V output voltage is selected (*Figure 8*).

If JP3 is in the upper position, the output voltage is given by:

Equation 1

$$VOUT_{ADJ} = 0.6 \cdot \frac{R8 + R9}{R8}$$

Figure 9. JP3 (VSEL) setting

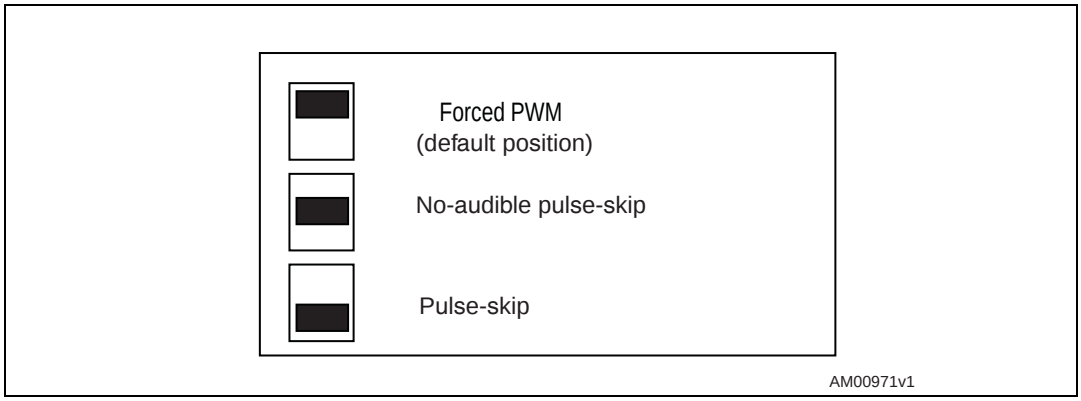


The R8 and R9 resistors are set to 12 kΩ and 13 kΩ respectively (1.25 V output voltage) and can be changed by the user.

6.2 JP1 power-saving mode (NOSKIP pin)

The JP1 jumper allows choosing the mode of operation of the switching section. Three options (forced-PWM, pulse-skip and non-audible pulse-skip) can be selected by changing the JP1 setting as shown in *Figure 9*:

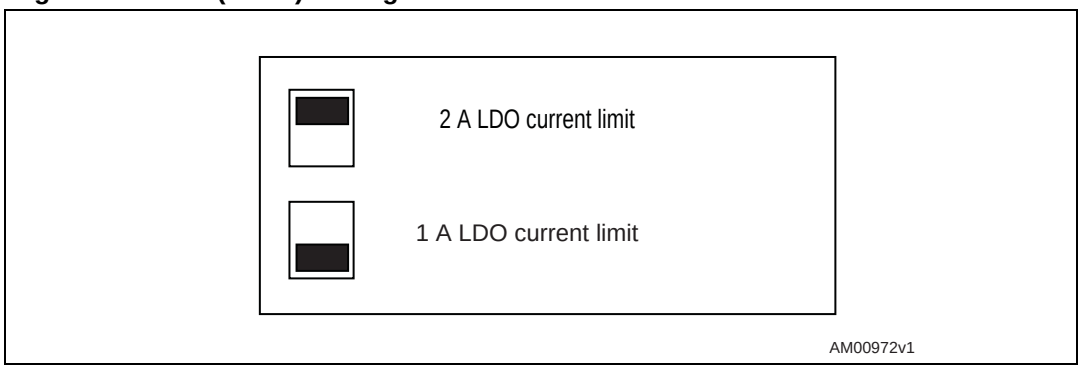
Figure 10. JP1 (NOSKIP) setting



6.3 JP2 LDO current limit (LILIM pin)

The JP2 jumper is used to select the LDO current limit. In the upper position the LDO output current limit is set to 2 A, while in the lower position the current limit is set to 1 A. The middle position is not used.

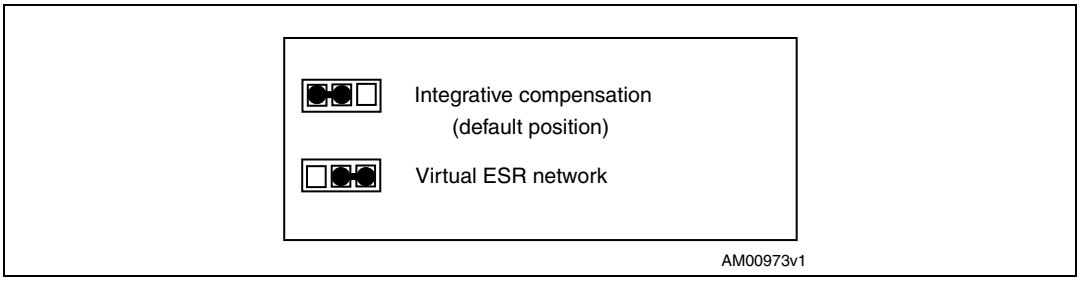
Figure 11. JP2 (LILIM) setting



6.4 JP5 compensation network (COMP pin)

The JP5 jumper is located on the bottom side of the PM6675AS board and allows connecting the integrator input (COMP pin) to the output through a simple capacitor (integrative compensation) or using the "virtual ESR" network for very low ESR output capacitor applications (e.g. all ceramic output cap applications). The integrative compensation is set by default. Refer to the PM6675AS datasheet for details about the all-ceramic output capacitor applications and the virtual ESR design.

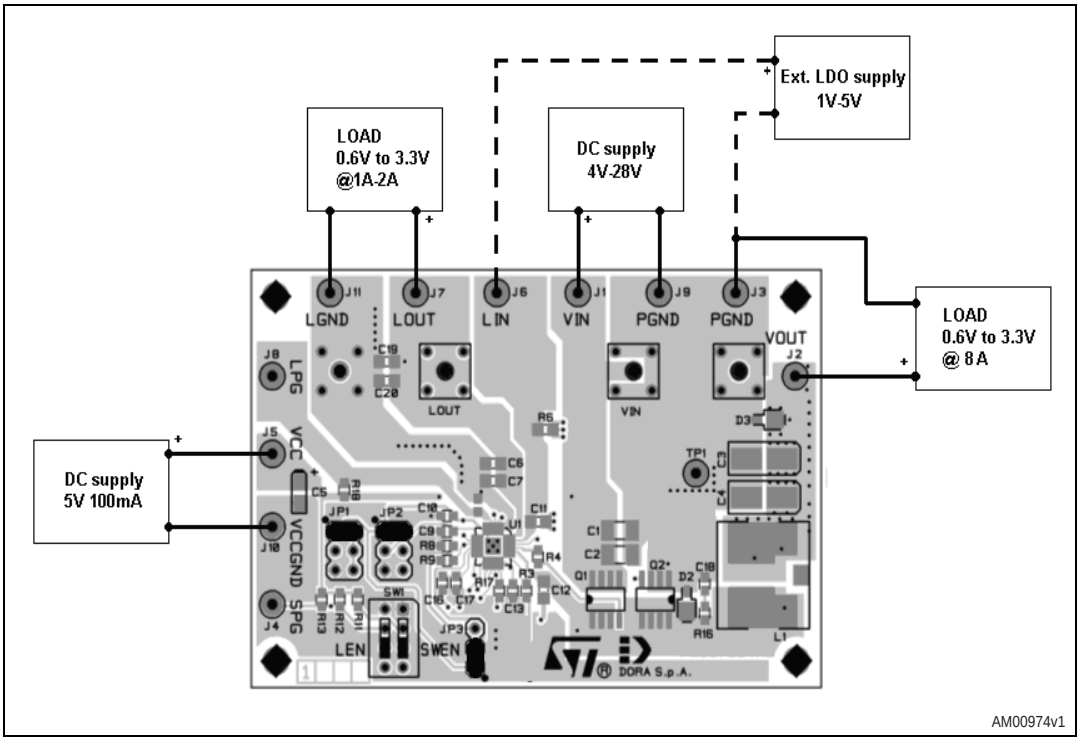
Figure 12. JP5 (COMP) setting



7 Test setup

Figure 12 shows the suggested setup connections between the PM6675AS demonstration board, the loads and the external supply. The LDO input (LIN) is connected to V_{OUT} by default (R6 = 0 Ω).

Figure 13. PM6675AS demonstration board test setup



8 Getting started

The following step-by-step power-up and power-down sequences are provided in order to correctly evaluate the PM6675AS demonstration board performance.

- Power-up sequence
  - Working in an ESD-protected environment is highly recommended. Check all wrist straps and ground mat connections before handling the PM6675AS demonstration board
  - Connect power supplies as shown in the PM6675AS demonstration board test setup (*Figure 12*) and insert the meters in order to perform the desired performance evaluation. Connect the scope-probes as desired
  - Set the JP1 through JP5 jumpers in order to properly configure the PM6675AS board (default position suggested). Set the SWEN-LEN switches to the on position (upper position); Do not change jumper settings when the board is powered
  - Set the V_{CC} supply to 5 V±5% and the current limit to 100 mA
  - Set the V_{IN} supply to a voltage in the range 4.5 V to 36 V. An initial test at 24 V and 2 A current limit is suggested
  - Set all the loads to 0 A
  - Turn-on the V_{IN} supply
  - Turn-on the V_{CC} supply
  - Vary the V_{OUT} load from 0 A to 8 A
  - Vary the L_{OUT} load from 0 A to 2 A to test source capability. If a different LDO input is desired, connect the external rail as dashed in *Figure 12* and remove the R6 resistor. All changes must be done when the board is not powered
  - Vary VIN supply from 4.5 V to 36 V
- Power-down sequence
  - Decrease L_{OUT} loads to 0 A
  - Reduce V_{OUT} load to 0 A
  - Decrease V_{CC} supply from 5 V to 3.8 V in order to test the UVLO
  - Increase V_{CC} supply from 3.8 V to 5 V to restart the device
  - Use the SWEN-LEN switches to test soft-start and soft-end on both outputs
  - Turn-off the V_{OUT} load
  - Turn-off the V_{CC} supply
  - Turn-off the V_{IN} supply

9 PM6675AS demonstration tests

9.1 V_{OUT} and L_{OUT} turn-on (soft-start)

The V_{OUT} soft-start is divided in 4 steps. In each step the current limit is increased by ¼ of the nominal value. This behavior is well understood by loading the rail, as performed in the test. L_{OUT} soft-start is performed at its maximum available current.

Figure 14. V_{OUT} soft-start at 150 mΩ load, pulse-skip mode

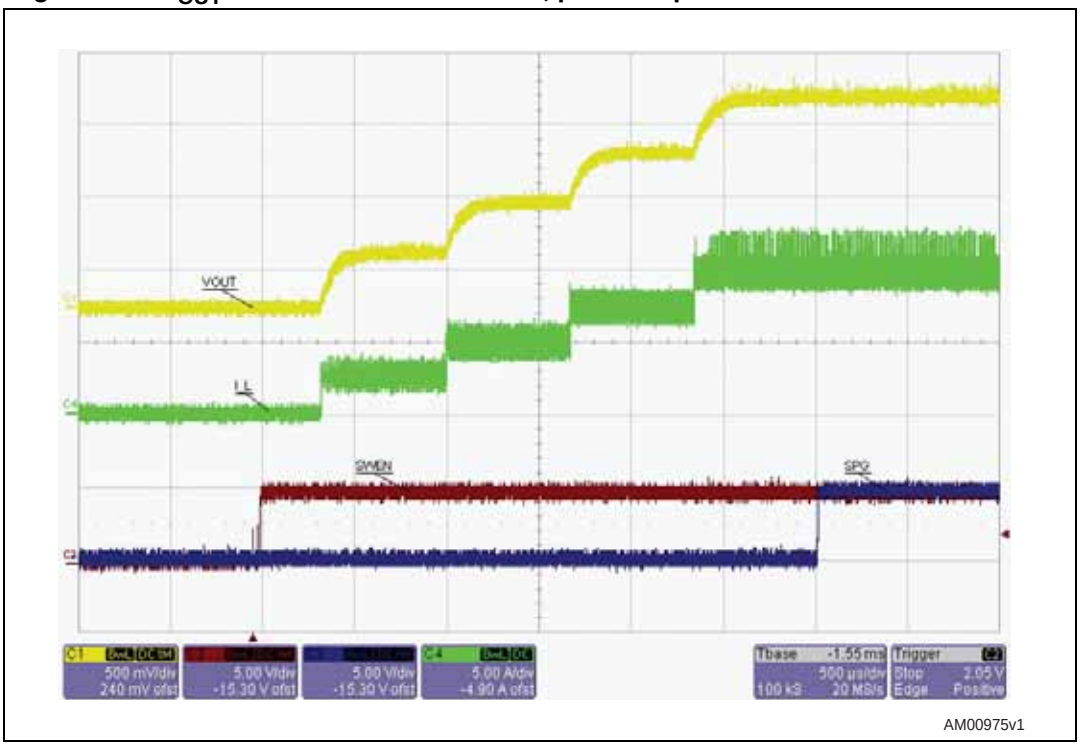
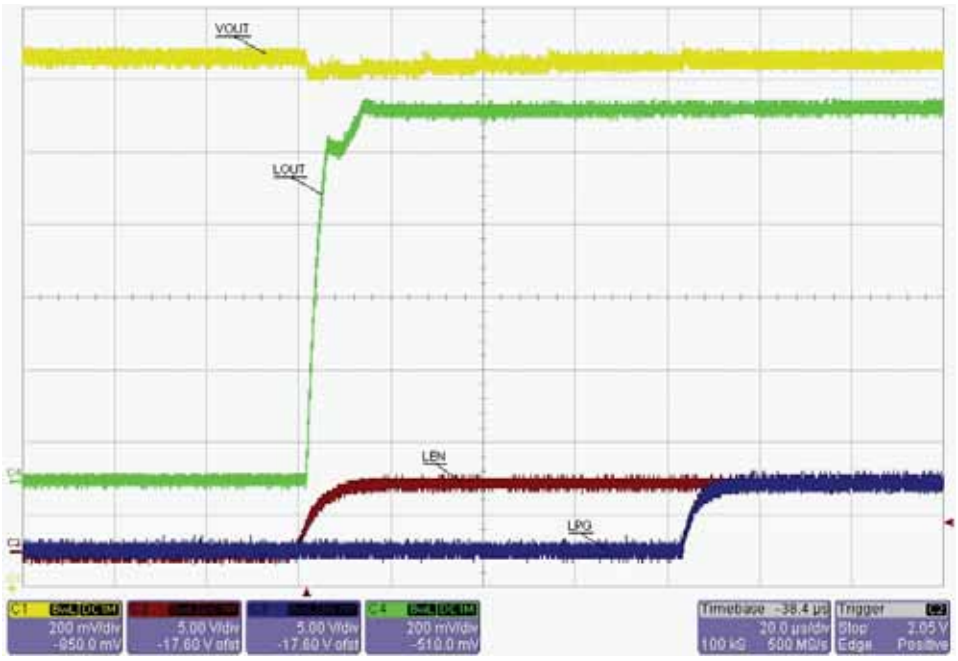


Figure 15. L_{OUT} turn-on, V_{OUT} in pulse-skip mode

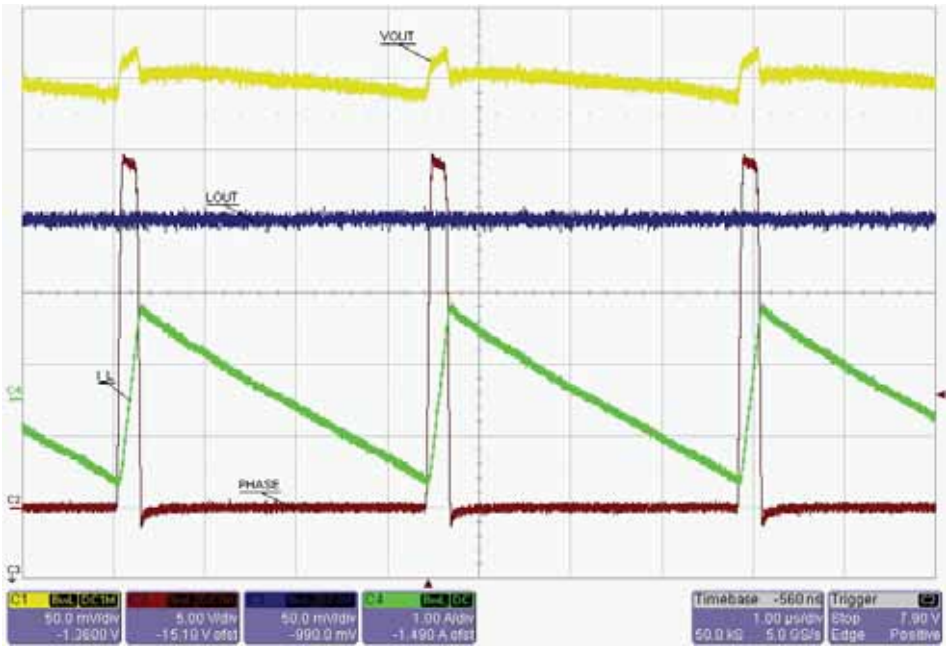


9.2 V_{OUT} working mode

- V_{OUT} forced PWM mode

When the forced PWM working mode is selected (JP1 in the upper position), the inductor current is allowed to become negative and the following waveform can be captured.

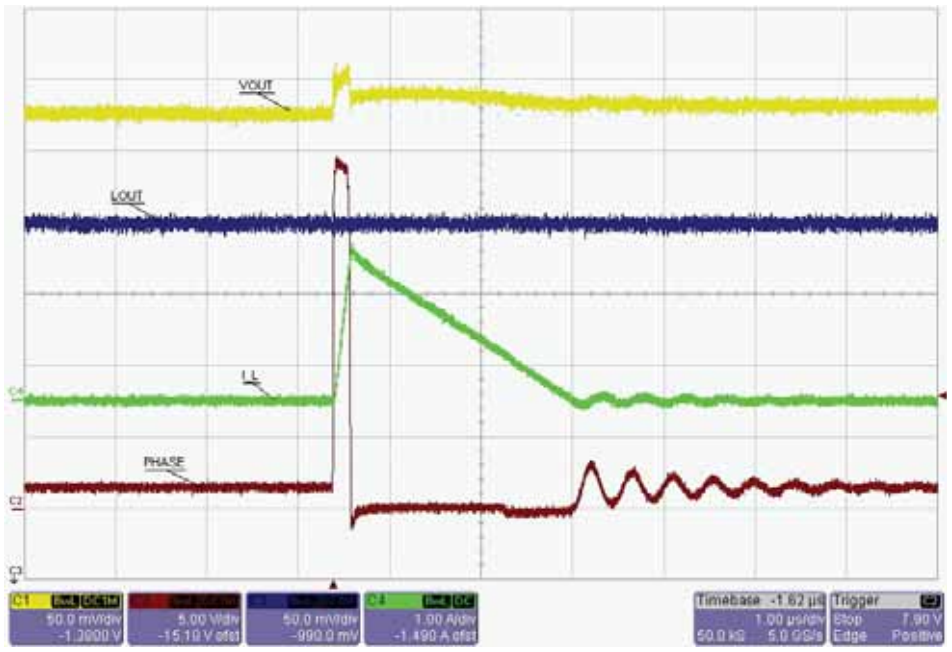
Figure 16. V_{OUT} = 1.5 V, V_{IN} = 24 V, I_{VOUT} = 0 A, forced-PWM mode



- V_{OUT} pulse-skip mode

The default working mode is the pulse-skip algorithm, in which the low-side MOSFET is turned off when the inductor current becomes equal to zero. This behavior allows reaching the maximum efficiency.

Figure 17. V_{OUT} = 1.5 V, V_{IN} = 24 V, I_{VOUT} = 0 A, pulse-skip mode



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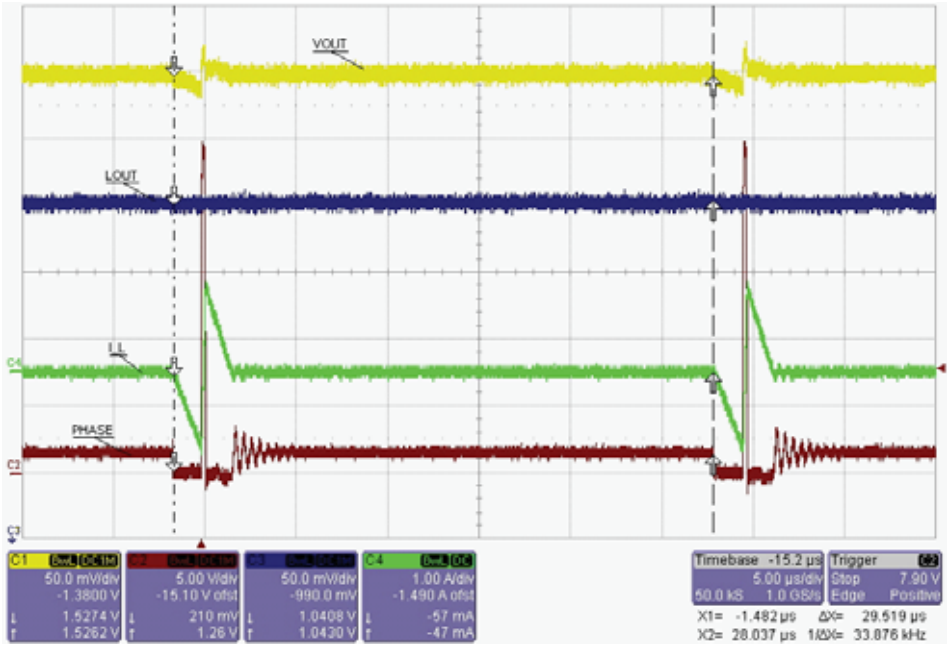
- V_{OUT} non-audible pulse-skip mode

In order to avoid too low switching frequencies, the non-audible pulse-skip mode can be selected (JP1 in the middle). Doing so, the minimum switching frequency allowed is 33 kHz as depicted in *Figure 18*.

Figure 18. V_{OUT} = 1.5 V, V_{IN} = 24 V, no load, non-audible pulse-skip mode (33 kHz)



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9.3 V_{OUT} and L_{OUT} load regulation

Figure 19 and *20* refer to V_{OUT} and L_{OUT} output voltage variations versus load current. The switching section directly supplies the linear LDO.

Figure 19. V_{OUT} load regulation - V_{IN} = 24 V

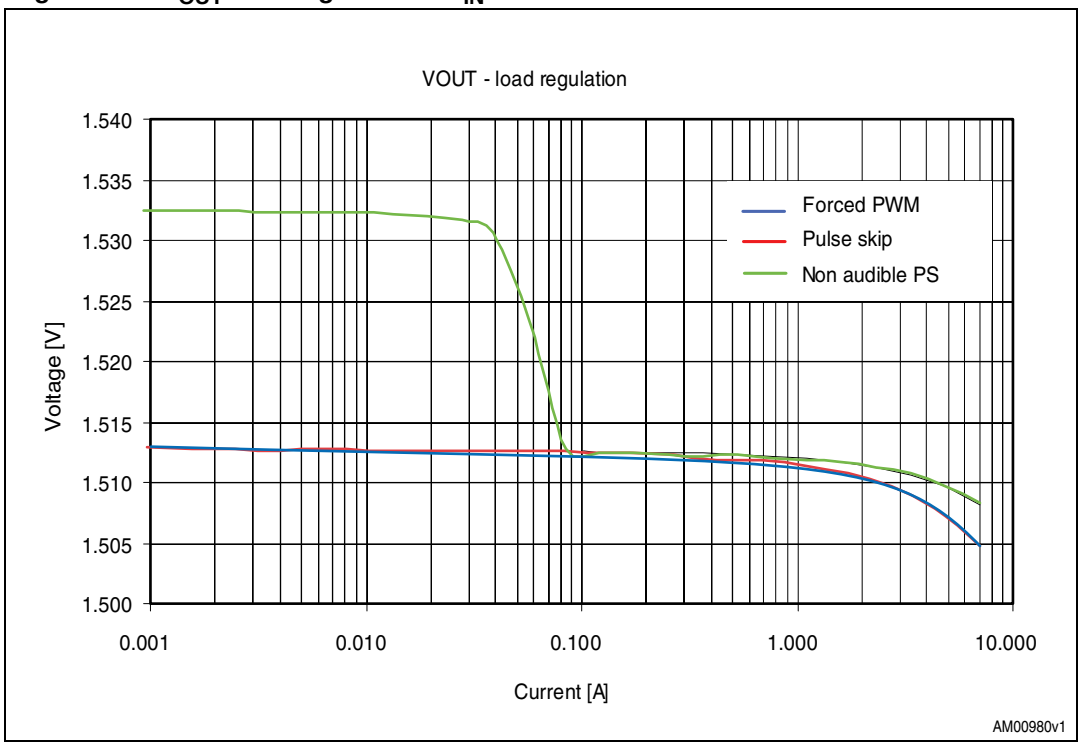
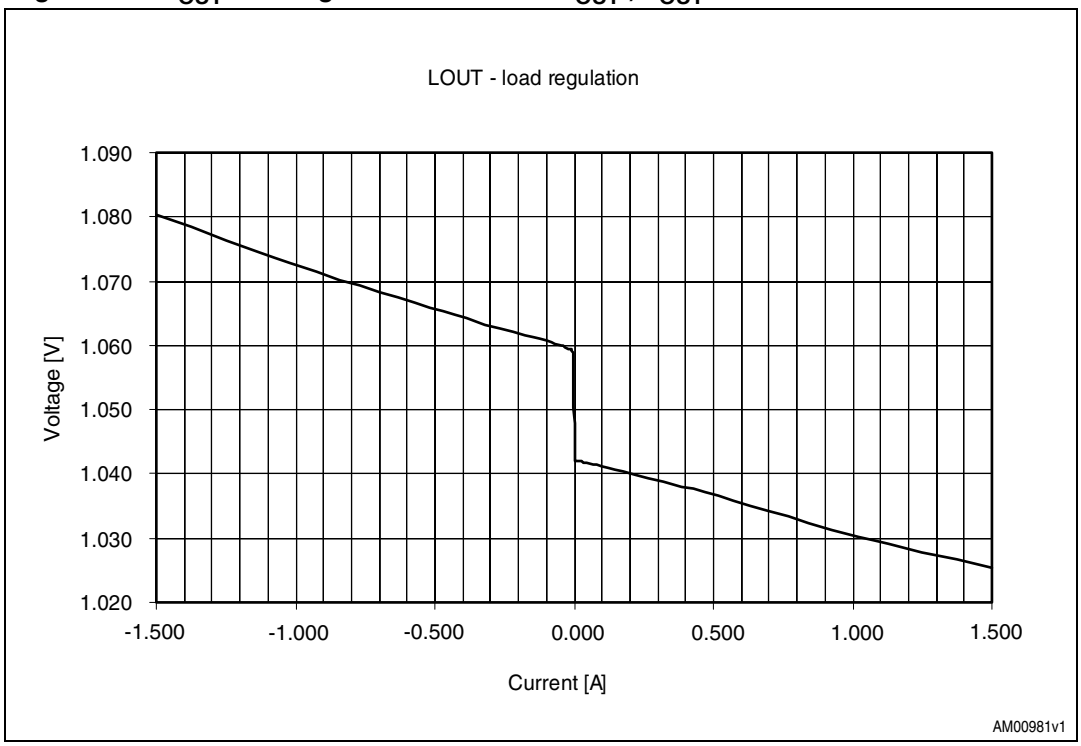


Figure 20. L_{OUT} load regulation - LDOIN = V_{OUT} , V_{OUT} in forced PWM mode



9.4 V_{OUT} and L_{OUT} load transient responses

Transient load responses are evaluated by loading V_{OUT} and L_{OUT} output rails with a current slew rate of 2.5A/µs.

Figure 21. V_{OUT} load transient (V_{IN}=24 V, LOAD=0 A to 7 A at 2.5 A/µs), pulse-skip mode

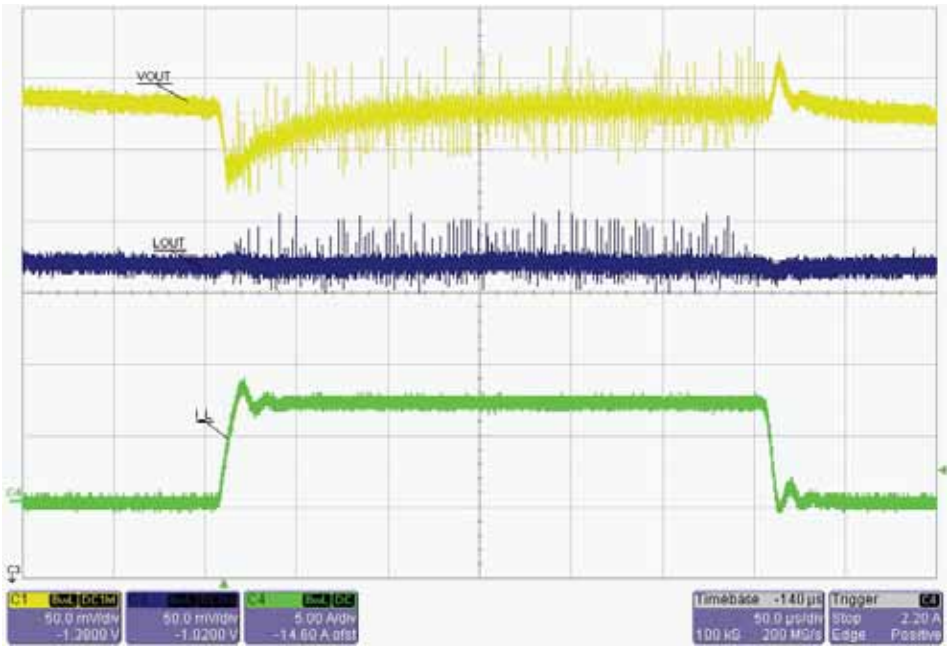
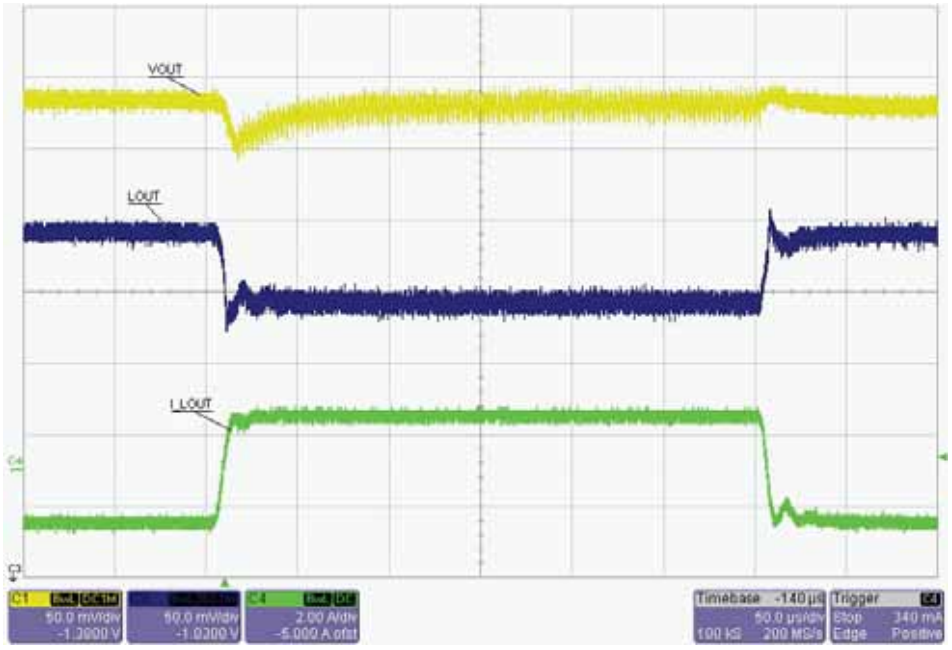


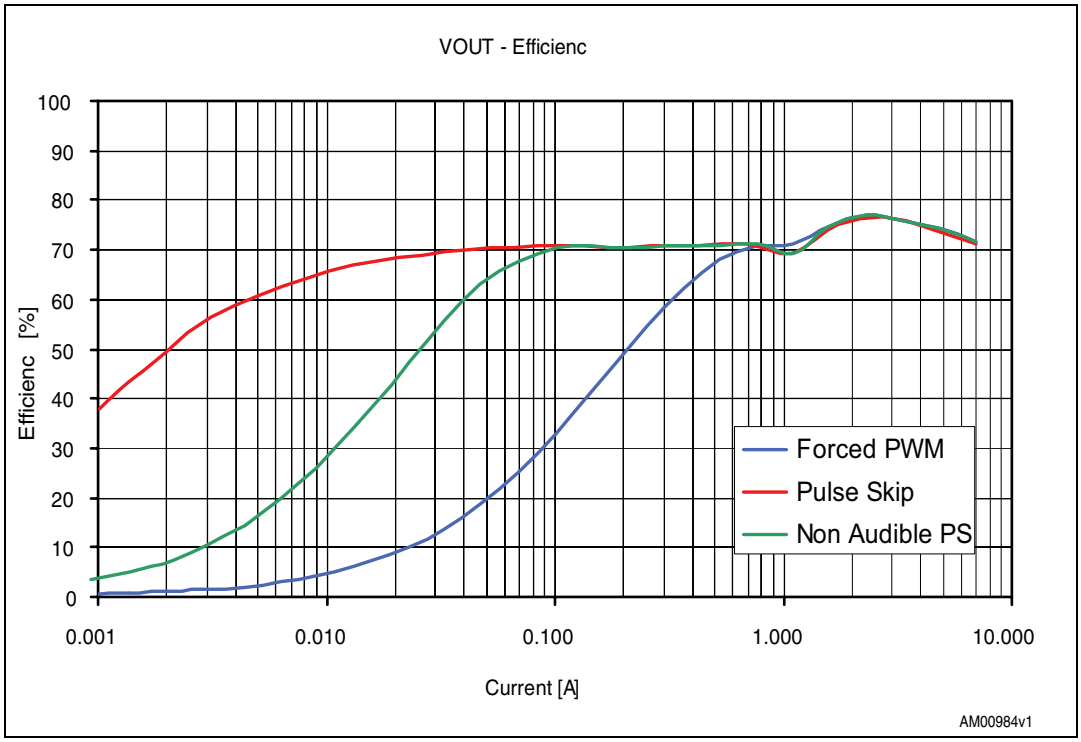
Figure 22. V_{OUT} load transient (V_{IN} = 24 V, LOAD=0 A to 7 A at 2.5 A/µs), pulse-skip mode



9.5 V_{OUT} efficiency

The three working modes lead to different power efficiency. The test setup is V_{IN}=24 V, FSW = 330 kHz, V_{OUT} = 1.5 V. *Figure 23* summarizes the results.

Figure 23. Forced PWM (blue), non-audible pulse-skip (green), pulse-skip (red), efficiency vs. output current



9.6 V_{OUT} gate drivers

The PM6675AS internal MOSFET driver turns on and off the high-side and low-side external MOSFET, avoiding cross-conduction. In the following two pictures the gates signals are shown in two different load conditions: without load (*Figure 24*) and with load (*Figure 25*).

Figure 24. External MOSFET gate signals (V_{IN} = 24 V, LOAD = 0), pulse-skip mode

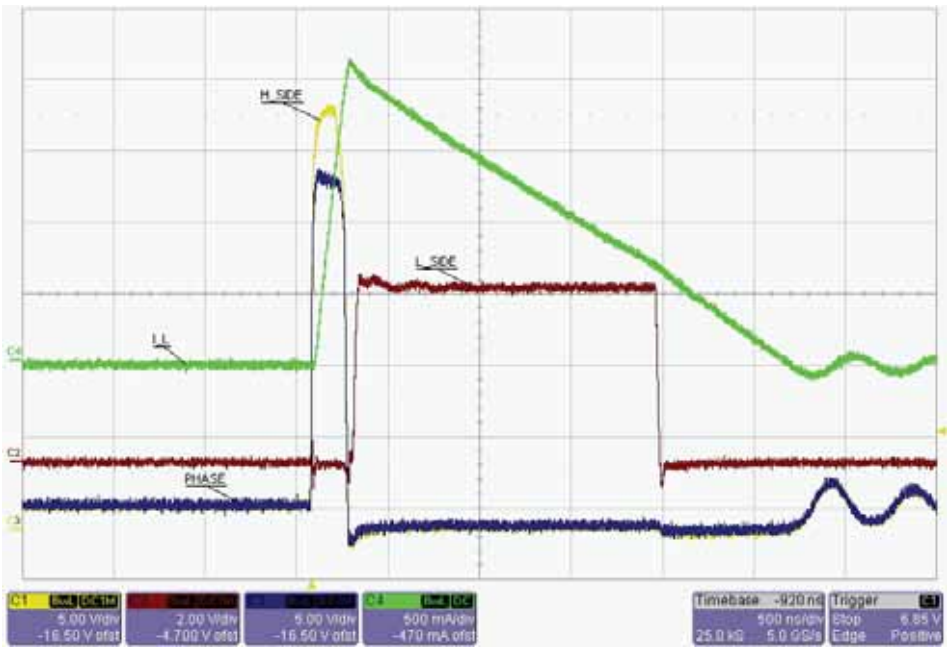
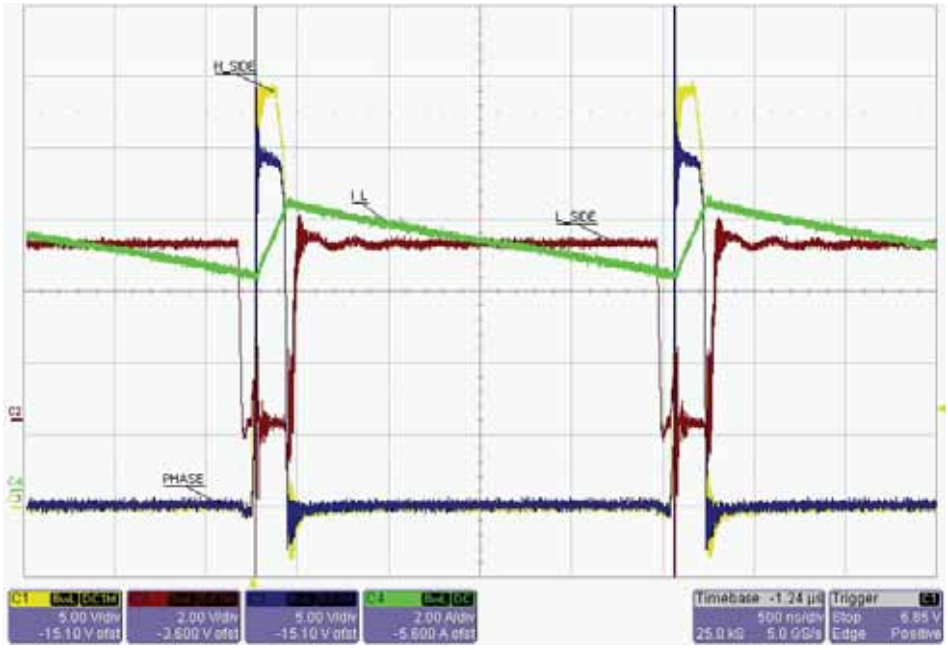


Figure 25. External MOSFET gate signals (V_{IN} = 24 V, LOAD = 7 A), pulse-skip mode

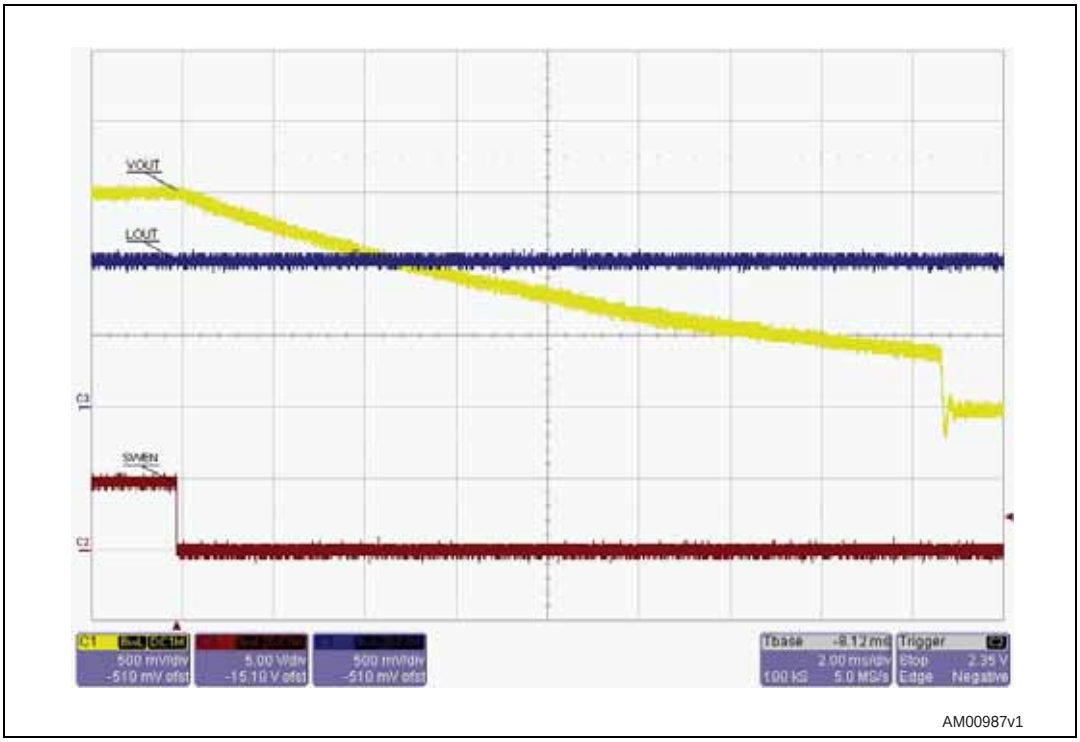


9.7 V_{OUT} and L_{OUT} turn-off (soft-end)

- V_{OUT} soft-end

When the SWEN pin is pulled down, the switching section performs the output capacitor discharge by turning on the discharge MOSFET. The external low-side MOSFET is turned on when the output voltage is lower than about 400 mV.

Figure 26. V_{OUT} and L_{OUT} output voltages, V_{OUT} soft-end, L_{OUT} powered by an auxiliary rail



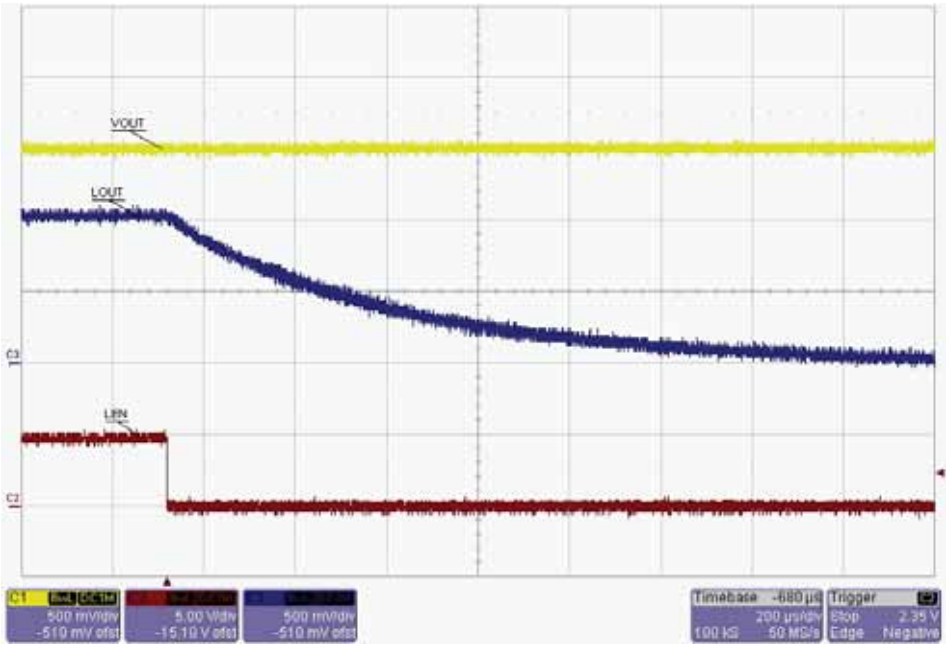
- L_{OUT} soft-end

By pulling down the LEN pin the linear regulator is forced to discharge its output capacitor, by turning on its discharge MOSFET. Doing so, the L_{OUT} rail is turned off in a safe way, avoiding output voltage under ground spikes.

Table 3. Typical discharge MOSFETs $R_{DS(on)}$ resistance

Description	V_{OUT} output	L_{OUT} output
Typical discharge MOSFETs $R_{DS(on)}$	25 Ω	25 Ω

Figure 27. V_{OUT} and L_{OUT} output voltages, L_{OUT} soft-end

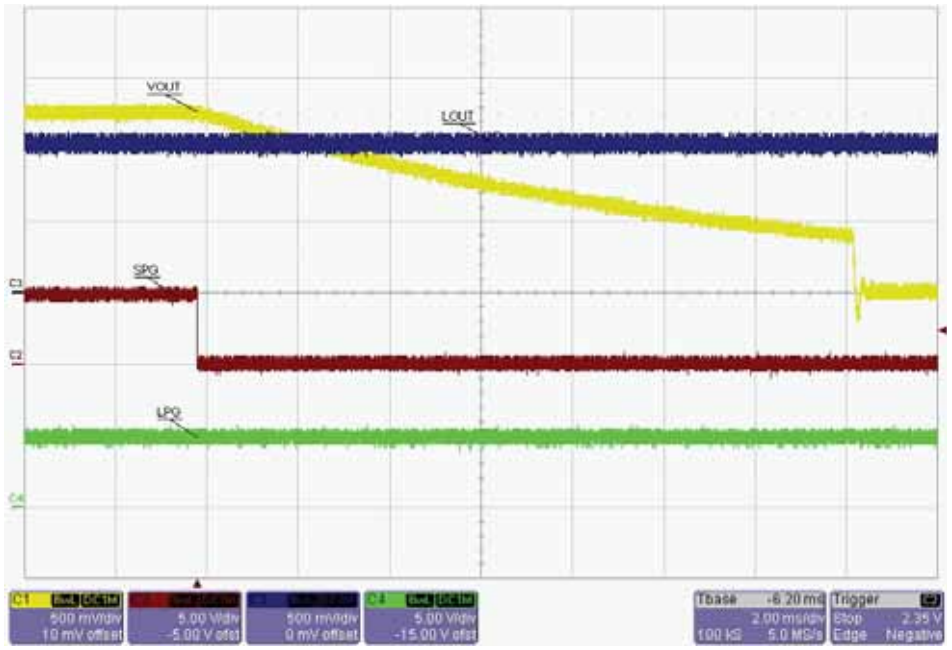


9.8 UV, OV and thermal protections

- Latched UV protection

If the switching section output voltage is lower than the 70% nominal value, the undervoltage state is entered and the discharge MOSFET is turned on (as in the the soft-end state).

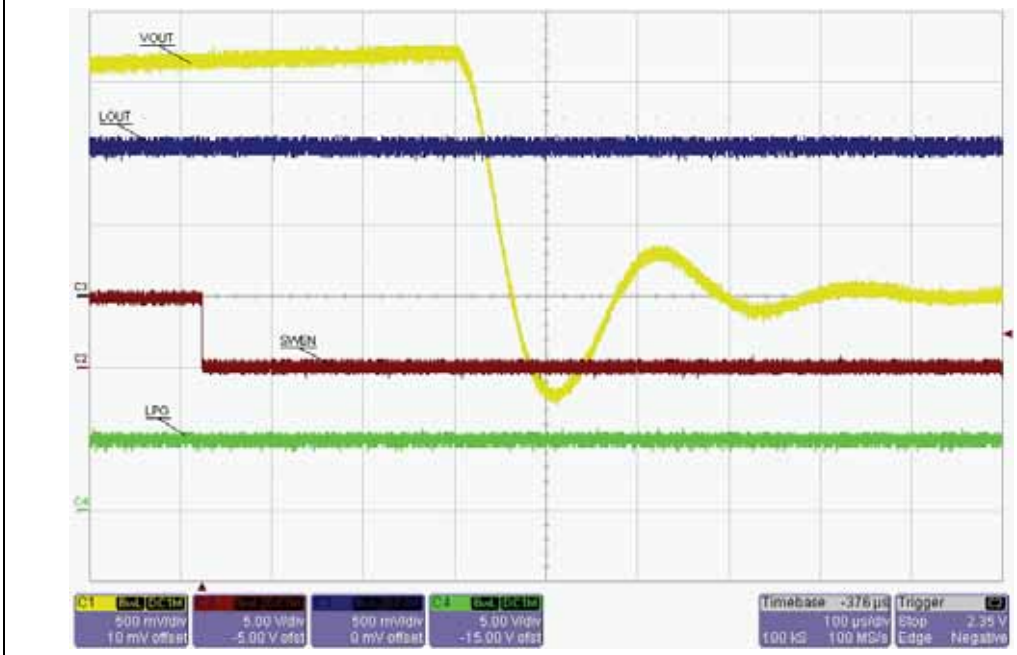
Figure 28. UV protection, pulse-skip mode, L_{OUT} powered by an auxiliary rail



- Latched OV protection

If the switching section output voltage is higher than the 115% nominal value, the overvoltage state is entered and the low-side MOSFET is turned on in order to quickly discharge the output capacitor and avoid load damages.

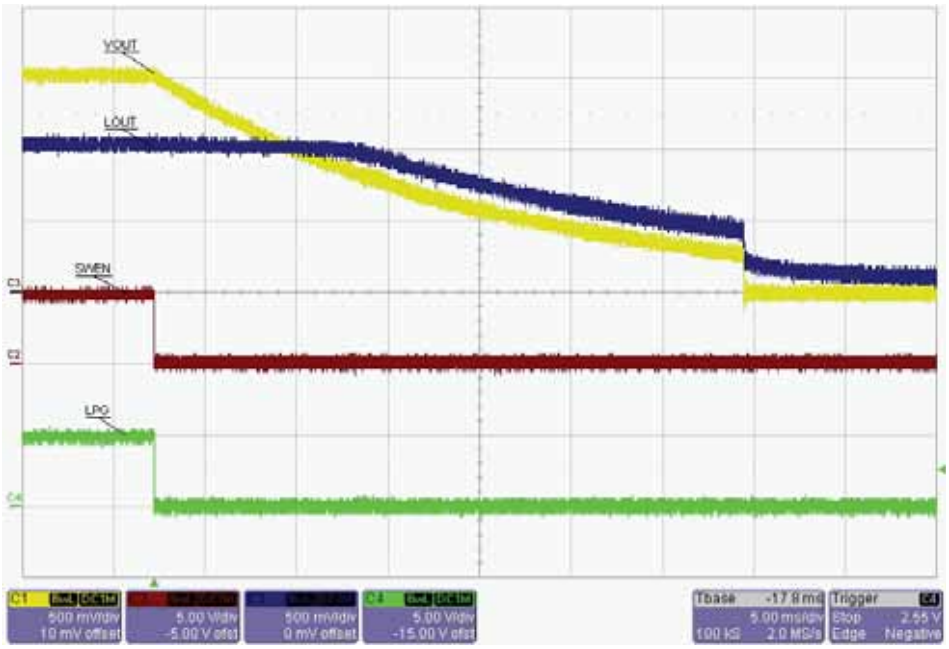
Figure 29. OV protection, pulse-skip mode



- Latched thermal shutdown

If the junction temperature rises above 150 deg the thermal protection circuit turns off the device and discharges the switching section output capacitor by performing the soft-end.

Figure 30. V_{OUT} and L_{OUT} rails, thermal shutdown, pulse-skip mode, L_{OUT} powered by V_{OUT}



9.9 V_{OUT} current limit

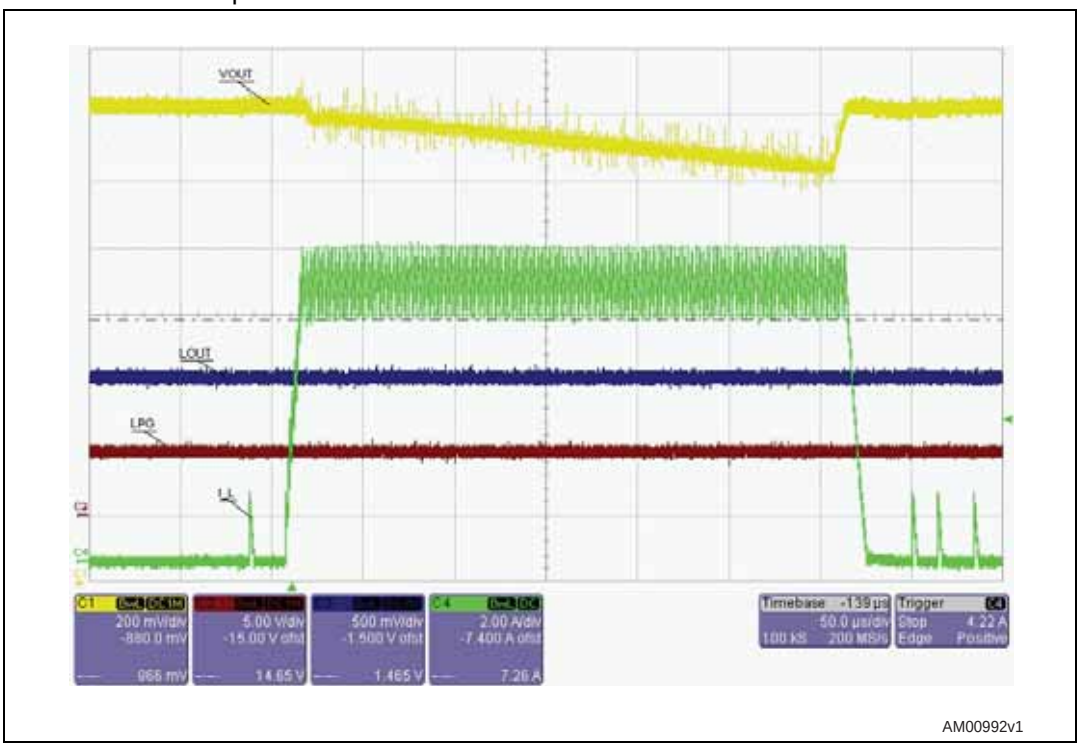
The valley current limit avoids any high-side turn-on if the inductor current is higher than the programmed value. This current limit can be designed with the following equation:

Equation 2

$$I_{CL} = \frac{100\mu A \cdot R_{ILIM}}{R_{LS,DSon}}$$

The current sensing is performed by comparing the voltage drop in the low-side MOSFET, during the TOFF period, with the voltage drop given by an injected current and the current limit resistor.

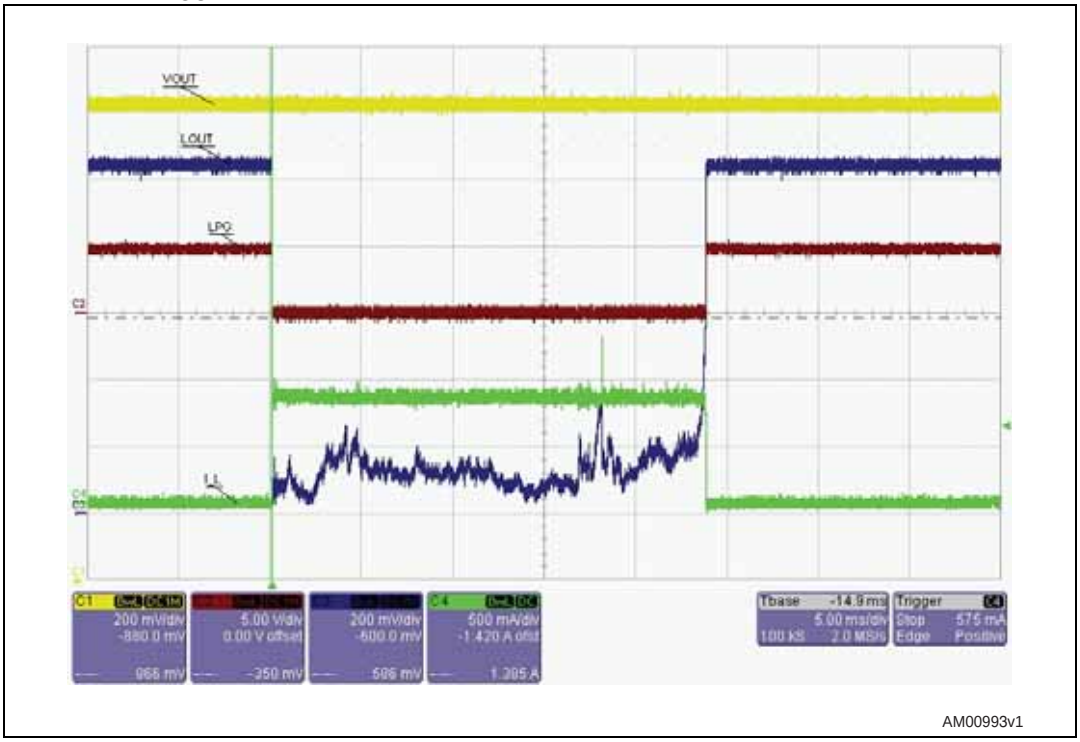
Figure 31. V_{OUT} current limit protection during a load transient (0 A to 9 A at 2.5 A/µs



9.10 L_{OUT} current limit (foldback)

The linear LDO regulator has a foldback protection feature which reduces the current limit to about 1 A when the output voltage is outside the ±10% Power Good window. The current limit is restored to about 2 A when the output voltage re-enters the Power Good window.

Figure 32. L_{OUT} current limit during an output short

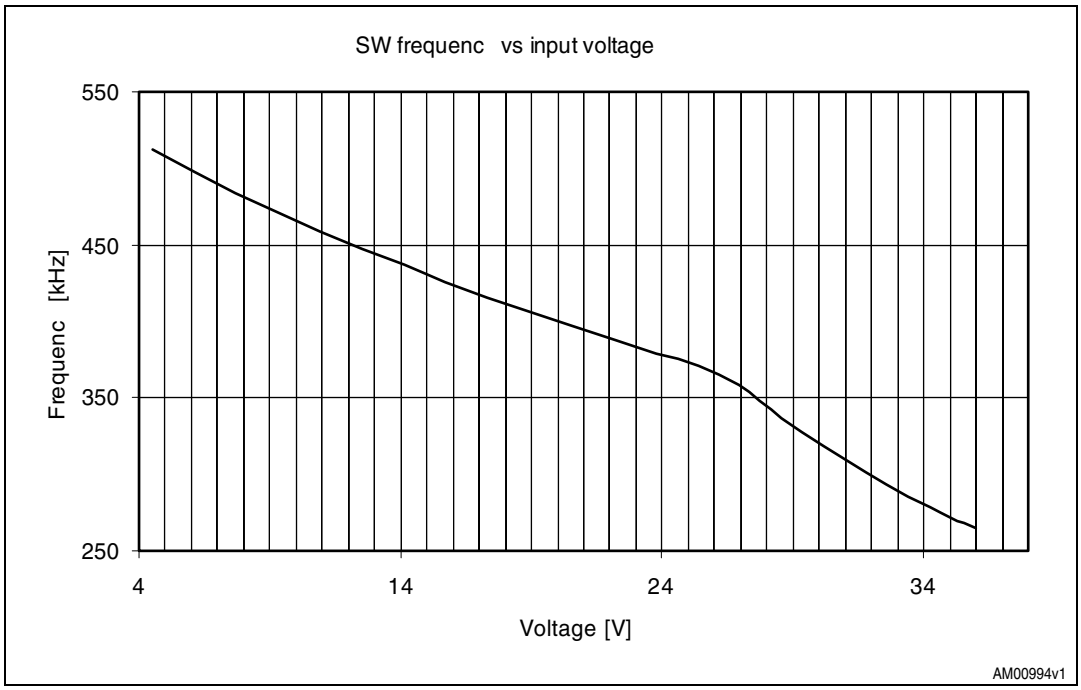


9.11 Switching frequency

- Switching frequency vs. input voltage

The constant on-time controller leads to a quasi-constant switching frequency, slightly following the input voltage.

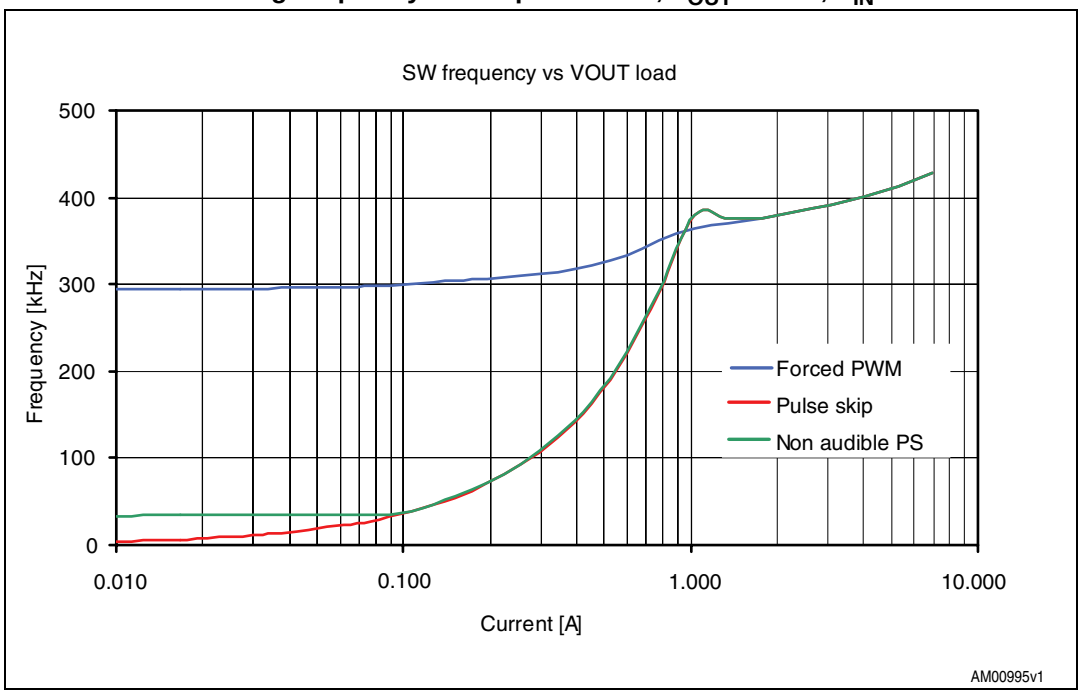
Figure 33. Switching frequency vs. input voltage, V_{OUT} = 1.5 V, I_{VOUT} = 2 A, forced PWM mode



- Switching frequency vs. output current

The switching frequency can decrease to very low values in pulse-skip mode but in non-audible pulse-skip there is a lower limit (about 33kHz). By increasing the load, however, the switching frequency increases a bit, as a consequence of conduction and switching losses.

Figure 34. Forced PWM (blue), non-audible pulse-skip (green) and pulse-skip (red), Switching frequency vs. output current, V_{OUT} = 1.5 V, V_{IN} = 24 V



9.12 Thermal behavior

The IC internal maximum and average temperature can be monitored by an IR camera. For the following measures the test setup is:

- V_{IN} = 24 V
- F_{SW} = 330 kHz
- Pulse-skip mode
- V_{OUT} = 1.5 V at I_{VOUT} = 4 A
- L_{OUT} = 1.05 V, powered by V_{OUT}
- T_{AMB} = 23 °C

By increasing the L_{OUT} current the IC temperature changes as depicted in *Figure 35* through *38*.

Figure 35. I_{LOUT} = 0 A, average IC temperature = 31.0 °C, max internal IC temperature = 33.1 °C

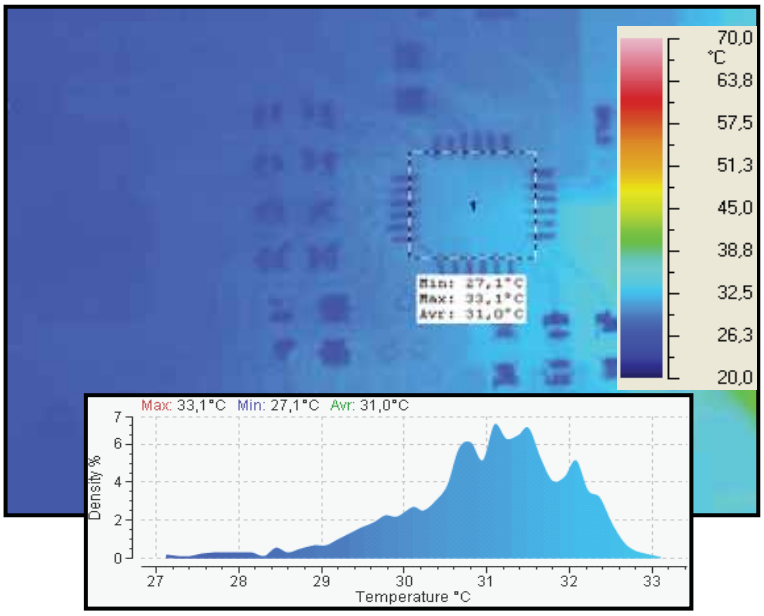


Figure 36. I_{LOUT} = 0.2 A, average IC temperature = 38.2°C, max internal IC temperature = 40.7 °C

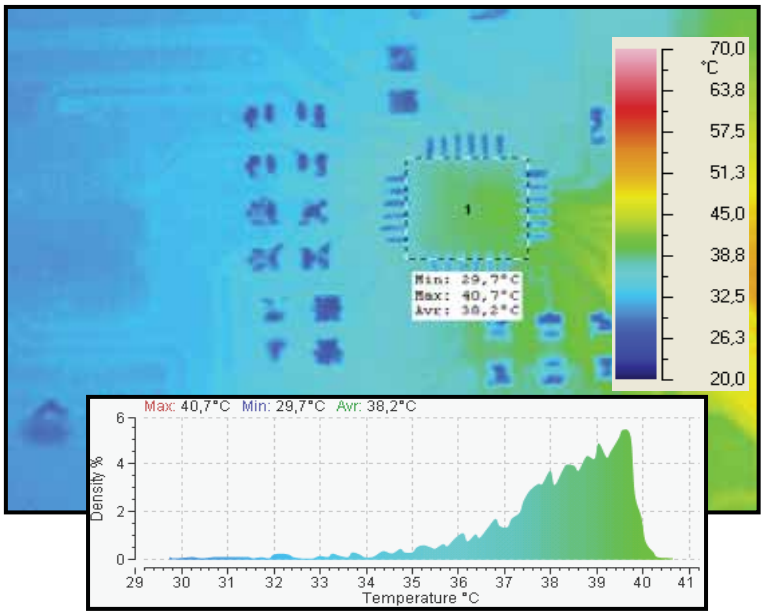


Figure 37. I_{LOUT} = 0.5 A, average IC temperature = 38.2 °C, max internal IC temperature = 41.5 °C

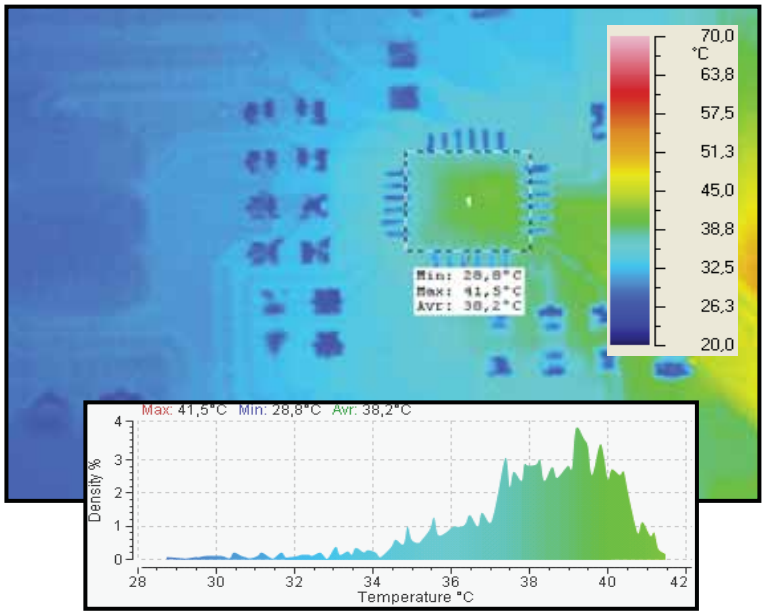
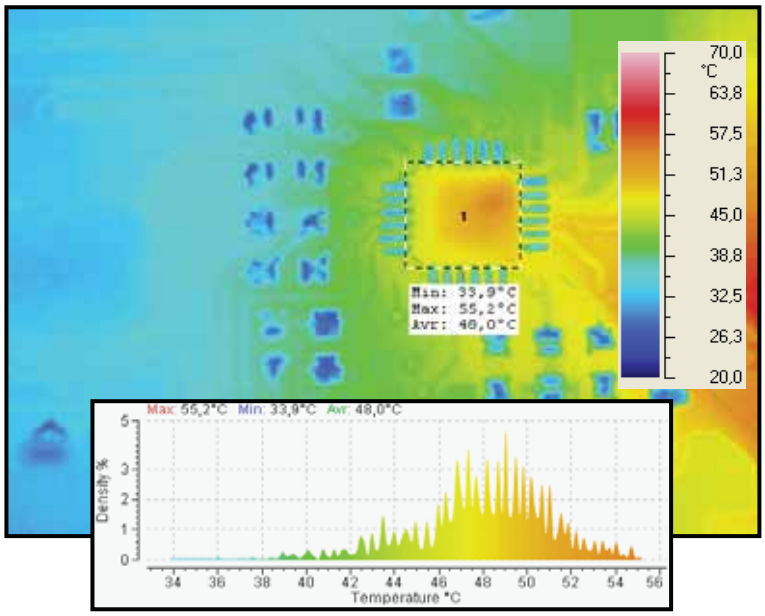


Figure 38. I_{LOUT} = 1.0 A, average IC temperature = 48°C, max internal IC temperature = 55.2 °C



10 Revision history

Table 4. Document revision history

Date	Revision	Changes
20-Aug-2008	1	Initial release