AN2808
Application note

Complete DDR2/3 memory power supply controller

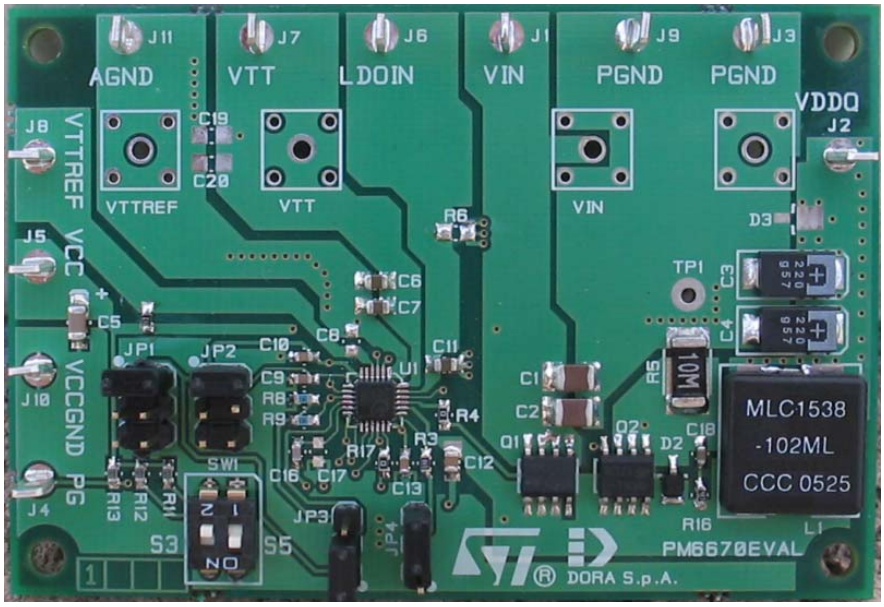
Introduction

The PM6670S device is a complete DDR2/3 power supply regulator for portable applications designed to meet JEDEC specifications. It integrates a constant on-time (COT) buck controller, a 2 Apk sink/source low dropout regulator (LDO) and a 15 mA low noise buffered reference.

The COT architecture ensures a fast transient response supporting both polymeric and ceramic output capacitors. An embedded integrator control loop compensates the DC voltage error caused by the output ripple. The 2 Apk sink/source linear regulator provides the memory termination voltage with a fast load transient response.

The device is fully compliant with system sleep states S3, S4 and S5, setting the LDO output to high-impedance in the suspend-to-RAM state, and performing the tracking discharge of all outputs in the suspend-to-disk state.

Figure 1. PM6670S demonstration board



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1 Main features

1.1 Switching section (VDDQ)

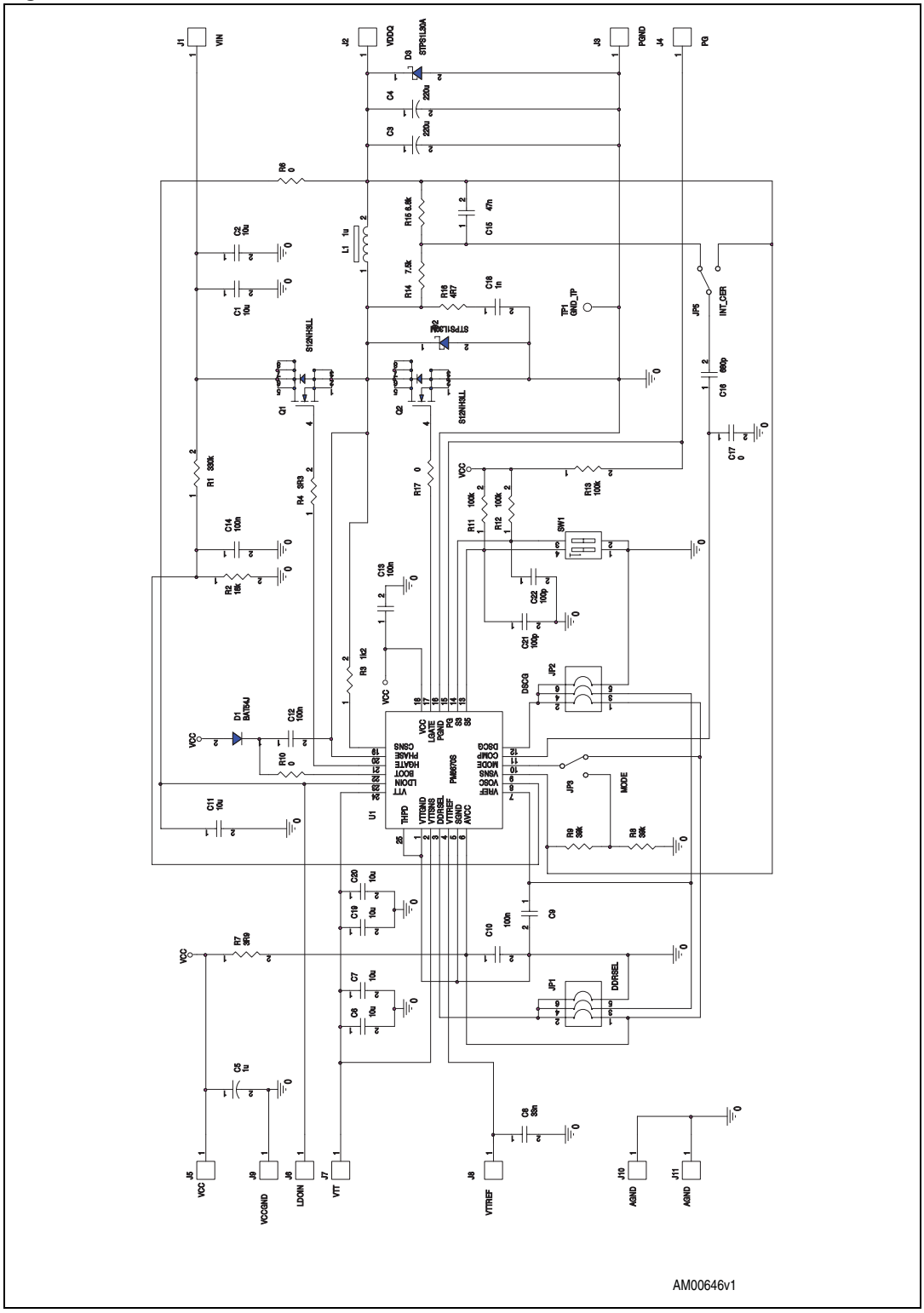
- 4.5 to 28-V input voltage range
- 0.9 V, ±1% voltage reference
- 1.8 V (DDR2) or 1.5 V (DDR3) fixed output voltages
- 0.9 to 2.6 V adjustable output voltage
- 1.237 V ± 1% reference voltage available
- Very fast load transient response constant on-time control loop
- No-RSENSE current sensing using low-side MOSFETs' $R_{DS(on)}$
- Negative current limit
- Latched OVP, UVP and thermal shutdown
- Fixed 3 ms Soft-Start
- Selectable pulse-skipping at light loads
- Selectable non-audible (33 kHz) pulse-skip mode
- All ceramic output capacitor applications supported
- Output voltage ripple compensation

1.2 Reference and termination voltages (VTTREF and VTT)

- 2 A peak LDO with foldback for VTT
- Remote VTT output sensing
- High-Z VTT output in S3
- Ceramic output capacitors supported
- ±15 mA low-noise buffered reference for VTTREF

2 Demonstration kit schematic

Figure 2. Kit schematic



3 Component list

Table 1. BOM list

Qty.	Component	Description	Package	P/n	Manufacturer	Value
2	C1, C2	Ceramic, 50V, X5R, 20%	SMD 1210	UMK325BJ106KM-T	Taiyo Yuden	10 µF
2	C3, C4	POSCAP, 4V, 15mΩ, 20%	SMD 7343 (D)	4TPE220MF	Sanyo	220 µF
1	C5	Ceramic, 6.3V, X5R, 10%	SMD 1206		Standard	1 µF
3	C6, C7, C11	Ceramic, 6.3V, X5R, 10%	SMD 0805	JMK212BJ106KG-T	Taiyo Yuden	10 µF
1	C8	Ceramic, 50V,X7R, 20%	SMD 0603		Standard	33 nF
4	C9, C10, C13, C14	Ceramic, 50V, X7R, 20%	SMD 0603		Standard	100 nF
1	C12	Ceramic, 50V, X7R, 10%	SMD 0805		Standard	100 nF
1	C15	Ceramic, 50V, X7R, 10%	SMD 0603		Standard	6n8
1	C16	Ceramic, 50V, X7R, 10%	SMD 0603		Standard	680 pF
1	C17	Ceramic, 20%	SMD 0603		Standard	N.M.
1	C18	Ceramic, 50V, X7R, 10%	SMD 0603		Standard	1 nF
2	C19, C20	Ceramic, 6.3V, X5R, 10%	SMD 0805	JMK212BJ106KG-T	Taiyo Yuden	N.M.
2	C21, C22	Ceramic, 50V, X7R, 10%	SMD 0603		Standard	100 pF
1	R1	Chip resistor, 0.1W, 1%	SMD 0603		Standard	330 kΩ
1	R2	Chip resistor, 0.1W, 1%	SMD 0603		Standard	18 kΩ
1	R3	Chip resistor, 0.1W, 1%	SMD 0603		Standard	1k2
1	R4	Chip resistor, 0.1W, 1%	SMD 0603		Standard	3R3
1	R6	Chip resistor, 0.1W, 1%	SMD 0805		Standard	0
1	R7	Chip resistor, 0.1W, 1%	SMD 0603		Standard	3R9

Table 1. BOM list (continued)

Qty.	Component	Description	Package	P/n	Manufacturer	Value
1	R8	Chip resistor, 0.1W, 1%	SMD 0603		Standard	39 kΩ
1	R9	Chip resistor, 0.1W, 1%	SMD 0603		Standard	39 kΩ
1	R10	Chip resistor, 0.1W, 1%	SMD 0603		Standard	0
3	R11, R12, R13	Chip resistor, 0.1W, 1%	SMD 0603		Standard	100 kΩ
1	R14	Chip resistor, 0.1W, 1%	SMD 0805		Standard	7k5
1	R15	Chip resistor, 0.1W, 1%	SMD 0603		Standard	6k8
1	R16	Chip resistor, 0.1W, 1%	SMD 0603		Standard	4R7
1	R17	Chip resistor, 0.1W, 1%	SMD 0603		Standard	0
1	L1	SMT, 12.4Arms, 3.46mΩ	15.0x13.2mm	MLC1538-102MX	Coilcraft	1 µH
1	Q1	N-channel, 30V	SO-8	STS12NH3LL	STMicroelectronics	STS12NH3LL
1	Q2	N-channel, 30V	SO-8	STS12NH3LL	STMicroelectronics	STS12NH3LL
1	D1	Schottky, 30V, 0.3A	SOD-323	BAT54J	STMicroelectronics	BAT54J
1	D2	Schottky, 30V, 1A	Stmite (DO216-AA)	STPS1L30M	STMicroelectronics	STPS1L30M
1	D3	Schottky, 30V, 1A	Stmite (DO216-AA)	STPS1L30M	STMicroelectronics	N.M.
1	U1	Controller	VFQFPN-24	PM6670S	STMicroelectronics	PM6670S
11	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10,J11	Header, single pin				
5	JP1, JP2, JP3	Jumper, 2x3, 100mils				
1	JP5	PCB pads selector				
1	TP6	Test point				
1	SW1	Dip switch 2	DIP-2		Standard	

4 Component assembly and layout

Figure 3. Top side component placement

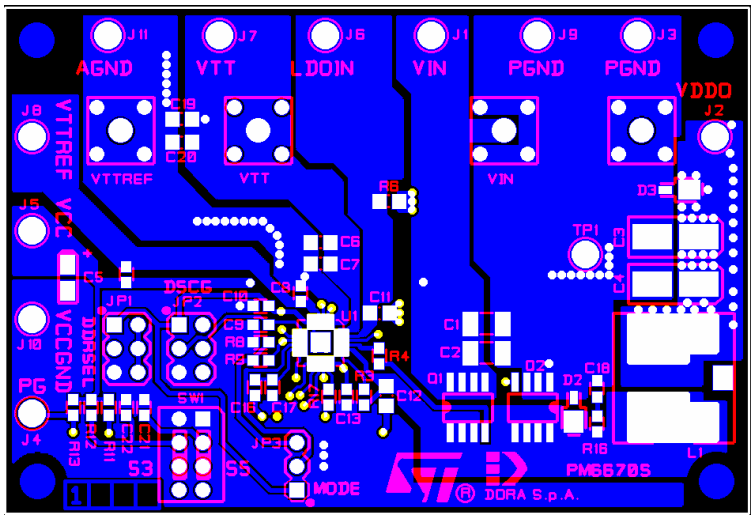


Figure 4. Top side view

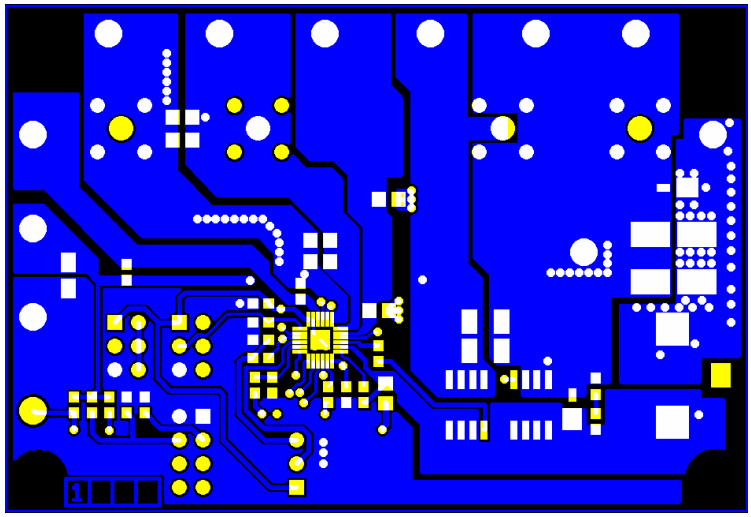


Figure 5. Layer 2 view

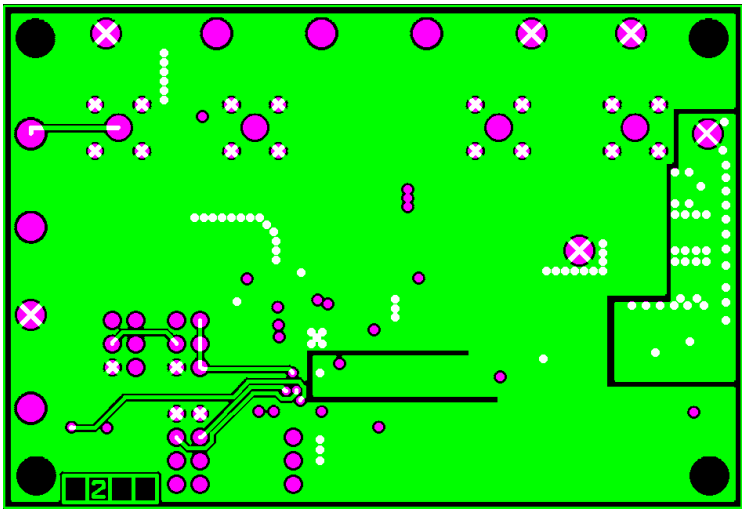


Figure 6. Layer 3 view

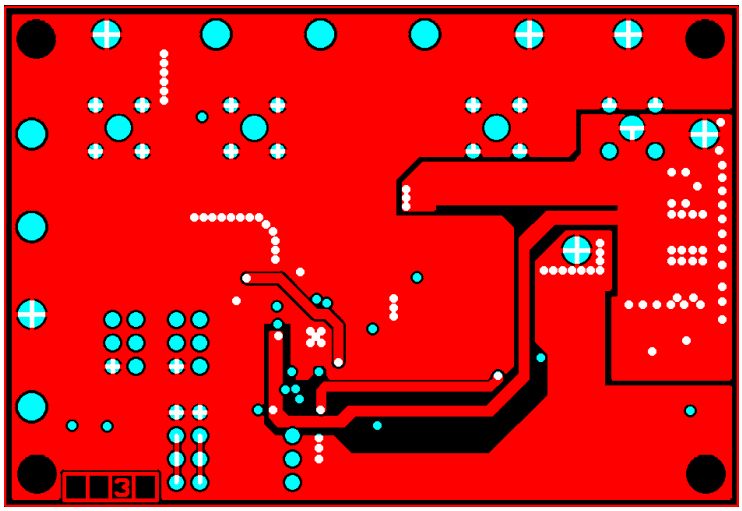


Figure 7. Bottom side view

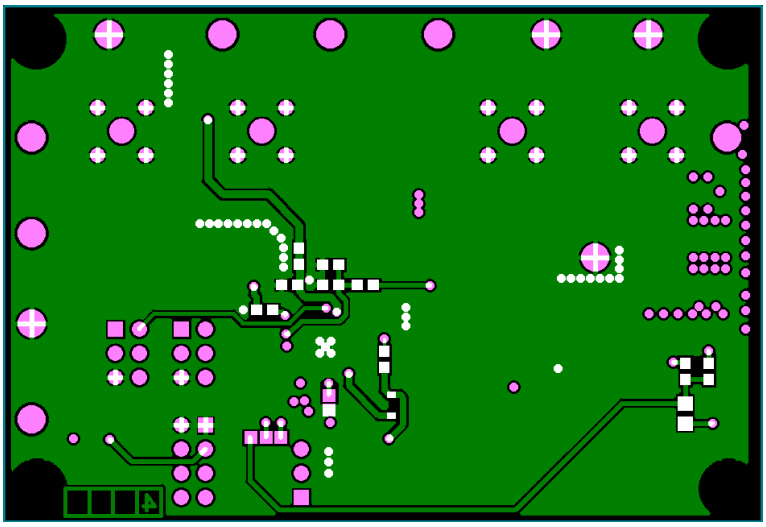
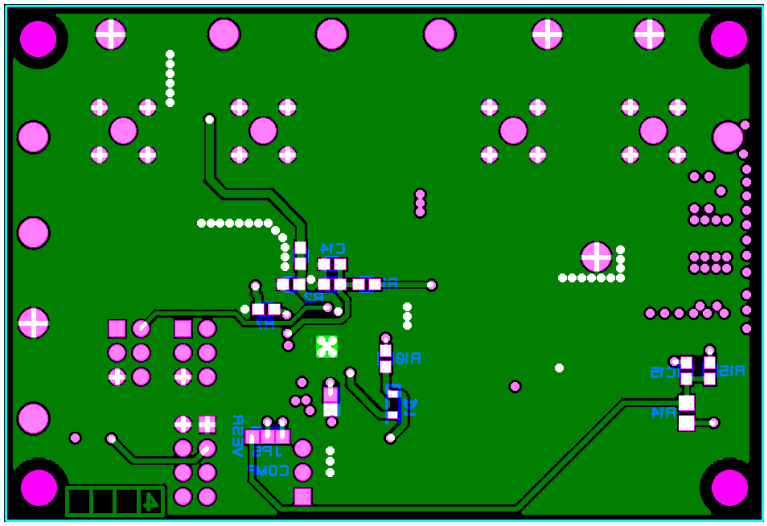


Figure 8. Bottom side component placement



5 I/O interface

The PM6670S demonstration board has the following test points.

Table 2. PM6670S demonstration board input and output interface

Test point	Description
VIN	Battery input voltage positive terminal
PGND	Battery input and VDDQ output common return
VDDQ	VDDQ output
LDOIN	LDO linear regulator input
VTT	VTT output (LDO)
AGND	VTT and VTTREF outputs common return
VTTREF	VTTREF output
VCC	+5 V supply, positive terminal
VCCGND	Signal ground and VCC supply return
PG	VDDQ output Power-Good signal
TP1	Connection point between power and signal grounds

6 Recommended equipment

- 4 to 28-V, 30 W power supply
- Active loads
- Digital mutimeters
- 200 MHz four-trace oscilloscope

7 Configuration

The PM6670S board includes four jumpers (JP1, JP2, JP3 and JP5) and two resistors, which can be configured to select the desired mode of operation.

7.1 JP3 fixed or adjustable output voltage (mode pin)

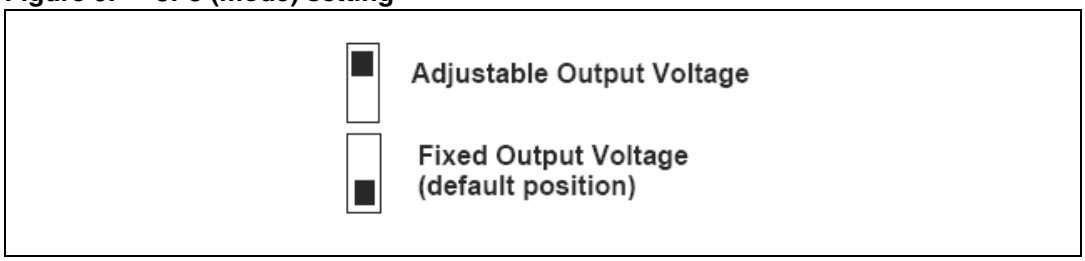
The JP3 jumper is used to choose between a fixed output voltage (1.5 or 1.8 V) and a user-defined output voltage in the range of 0.9 to 2.6 V. When connected in the lower position, the fixed output voltage is selected and the voltage depends on the setting of the DDRSEL pin (*Section 7.2*).

If JP3 is in the upper position, the output voltage is given by:

Equation 1

$$VDDQ_{ADJ} = 0.9 \cdot \frac{R8 + R9}{R8}$$

Figure 9. JP3 (mode) setting



Both the R8 and R9 resistors are set to 39 kΩ (1.8 V by default) and can be changed by the user.

7.2 JP1 DDR2/DDR3 or power-saving mode (DDRSEL pin)

The JP1 jumper provides different options depending on the configuration of JP3. If the fixed output voltage is selected (JP3 in the lower position), the user can choose between 1.8 V (DDR2) or 1.5 V (DDR3), connecting JP1 as shown in *Figure 10*, and the pulse-skip mode is set by default.

When the adjustable output voltage is selected (JP3 in the upper position), the same jumper allows choosing between forced pulse width modulation (PWM), pulse-skip and non-audible pulse-skip modes.

Figure 10. JP1 options when JP3 is in the lower position

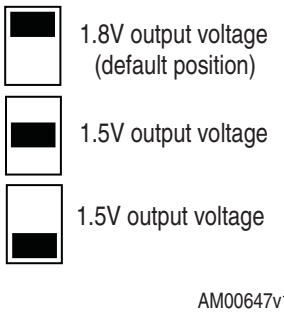
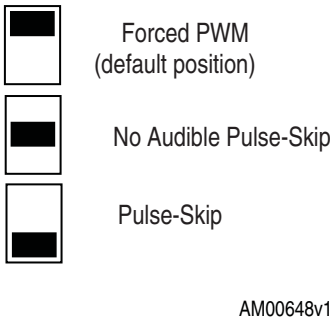


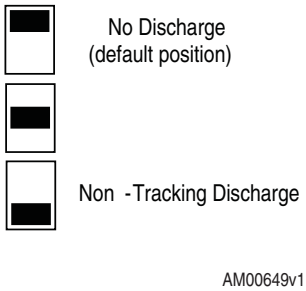
Figure 11. JP1 options when JP3 is in the upper position



7.3 JP2 output discharge (DSCG pin)

The JP2 jumper is used to select the desired output discharge when both the S3 and S5 signals are tied low. In the upper position the outputs are not discharged at all, while in the lower position the outputs are independently discharged using the internal MOSFETs (22 Ω for VDDQ and VTT, 1.5 kΩ for VTTREF). When JP2 is in the central position, the tracking-discharge is programmed. This discharge mode relies on the LDOIN pin being connected to the VDDQ output. See *Section 10.7: VDDQ, VTT and VTTREF turn-off (soft end)*. If an external rail is used to supply the LDO, the tracking discharge cannot be used as the device can be damaged while attempting to sink 1 A from the LDO input.

Figure 12. JP2 (DSCG) setting

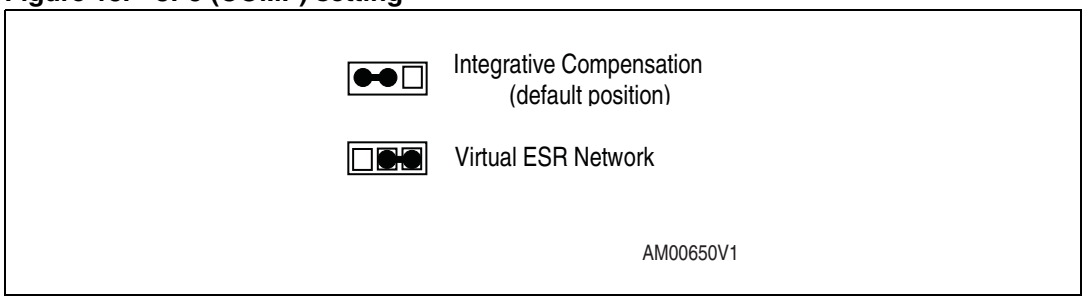


7.4 JP5 compensation network (COMP pin)

The JP5 jumper is located on the bottom side of the PM6670S board and is used to connect the integrator input (COMP pin) to the output through a simple capacitor (integrative compensation) or using the so-called "virtual ESR" network for very low-ESR output capacitor applications (for example, all-ceramic output capacitor applications). The integrative compensation is set by default.

Refer to the PM6670S datasheet for details on all-ceramic output capacitor applications and the virtual-ESR design.

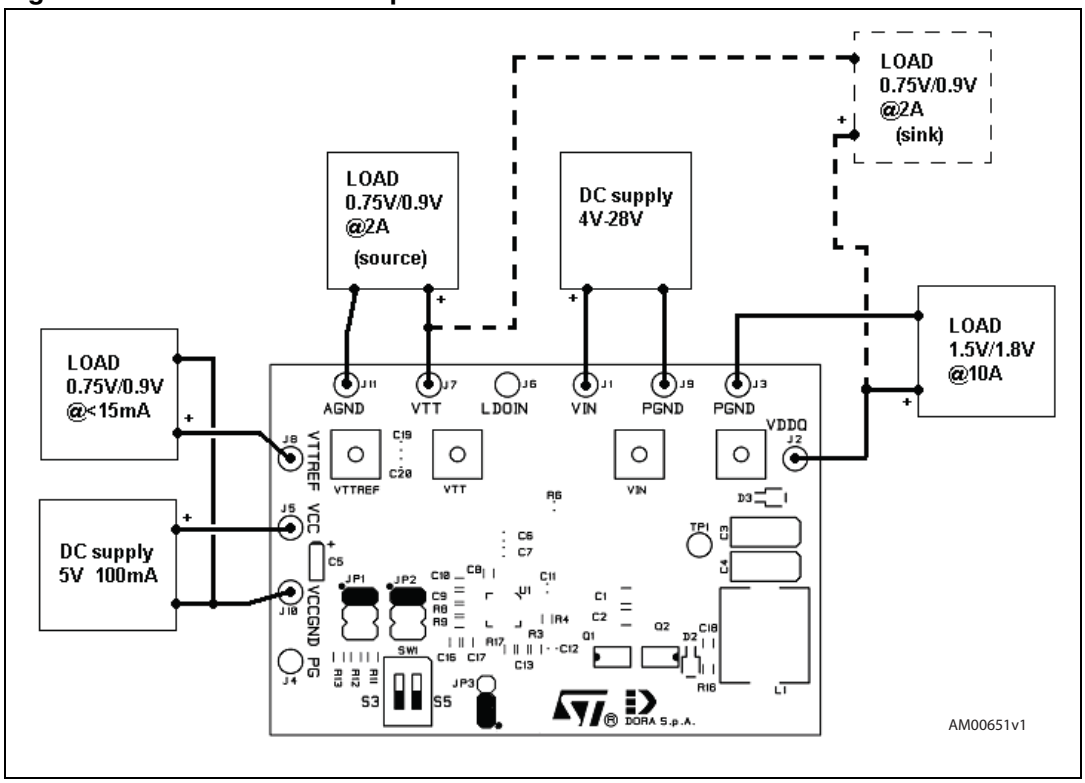
Figure 13. JP5 (COMP) setting



8 Test setup

Figure 14 shows the suggested setup connections between the PM6670S board, the loads and the external supply. The LDO input (LDOIN) is connected to VDDQ by default (R6 = 0 Ω).

Figure 14. PM6670S test setup



9 Getting started

The following step-by-step power-up and power-down sequences are provided in order to correctly evaluate the performance of the PM6670S board.

9.1 Power-up sequence

Working in an ESD-protected environment is highly recommended. Check all wrist straps and mat earth connections before handling the PM6670S board. Connect the power supplies as shown in the PM6670S test setup (*Figure 14*) and insert the meters in order to perform the desired performance evaluation. Connect the scope probes as desired.

1. Set the JP1, JP2, JP3 and JP5 jumpers in order to properly configure the PM6670S board.
2. Set the S3-S5 switches to the ON (upper) position. Do not change the jumper settings when the board is powered.
3. Set the VCC supply to 5 V ± 5% and the current limit to 100 mA.
4. Set the VIN supply to a voltage in the range of 4.5 to 28 V. An initial test at 12 V and 3 A current limit is suggested.
5. Set all the loads to 0 A.
6. Turn on the VIN supply.
7. Turn on the VCC supply.
8. Vary the VDDQ load from 0 A to 10 A.
9. Vary the VTT load from 0 A to 2 A to test the source capability. To test the sink capability use the dashed VTT load shown in *Figure 14*.
10. Vary the VTTREF load to test the source capability.
11. Vary the VIN supply from 4.5 to 28 V.

9.2 Power-down sequence

1. Decrease the VTTREF and VTT loads to 0 A.
2. Reduce the VDDQ load to 5 A.
3. Decrease the VCC supply from 5 to 3.8 V in order to test the UVLO.
4. Increase the VCC supply from 3.8 to 5 V to restart the device.
5. Use the S3-S5 switches to enter/exit the S0-S3-S5 states.
6. Turn off the VDDQ load.
7. Turn off the VCC supply.
8. Turn off the VIN supply.

10 PM6670S evaluation tests

10.1 Turning on VDDQ, VTT and VTTREF (soft-start)

The VDDQ soft-start is divided into four steps. In each step, the current limit is increased by ¼ of the nominal value, as shown in *Figure 15*. VTT and VTTREF soft-starts are performed at their maximum available current.

Figure 15. VDDQ soft-start at 150 mΩ load, pulse-skip mode

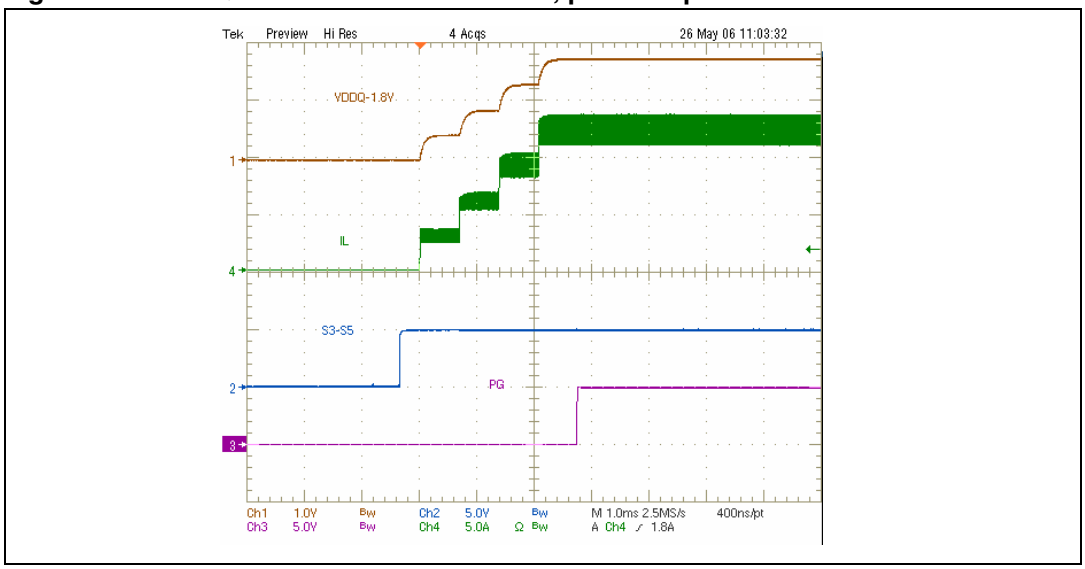


Figure 16. VDDQ turn-on (S5), pulse-skip mode

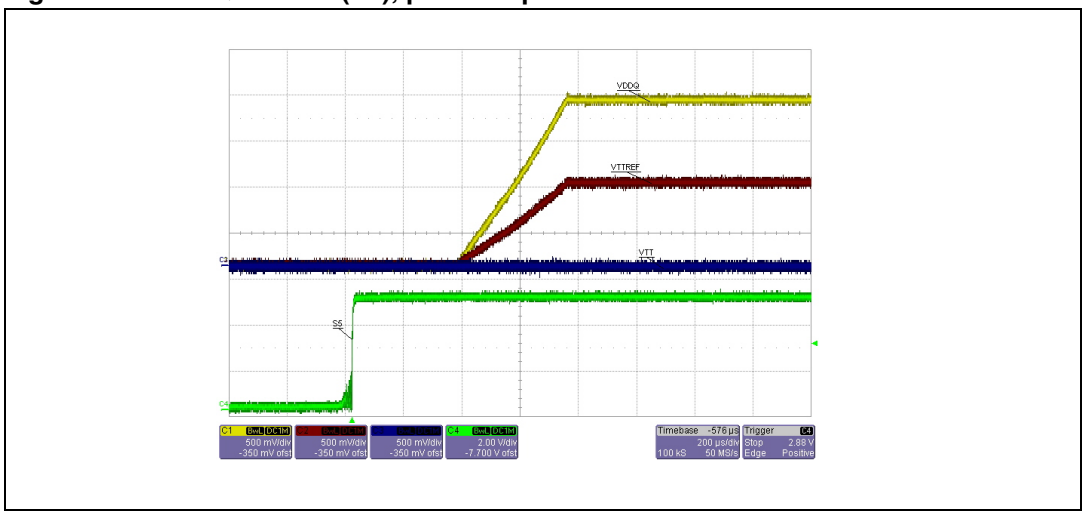
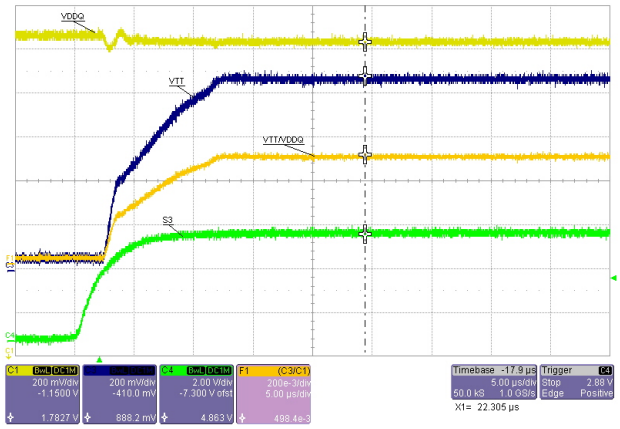


Figure 17. VTT turn-on (S0), pulse-skip mode

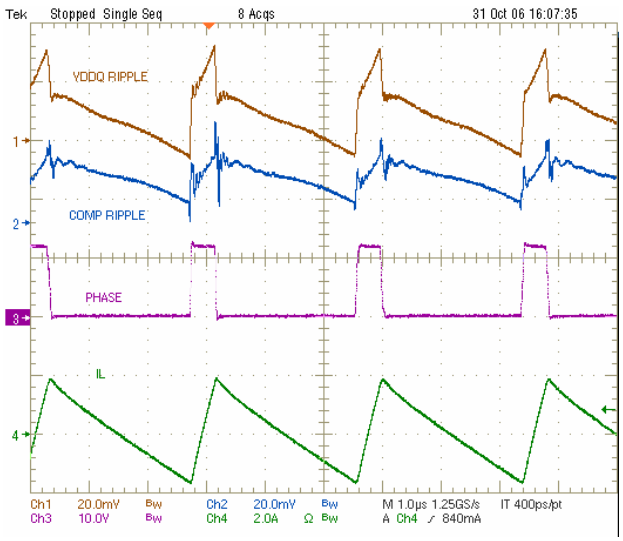


10.2 VDDQ working mode

10.2.1 VDDQ forced pulse width mode

When the forced PWM working mode is selected (JP3 and JP1 in the upper position) the inductor current is allowed to become negative and the following waveform can be captured.

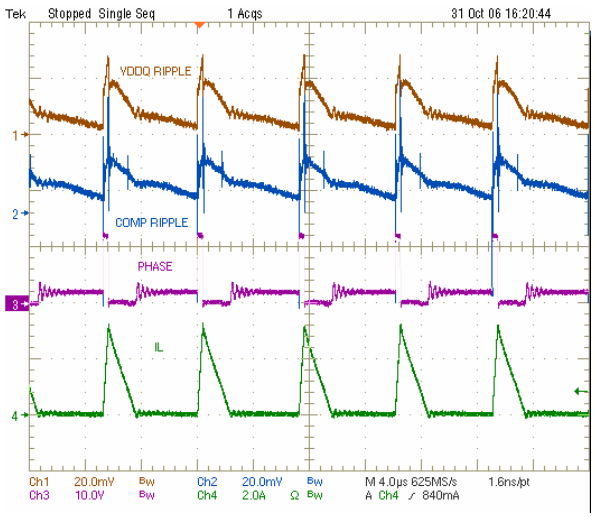
Figure 18. VDDQ = 1.8 V, VIN = 12 V, IVDDQ = 0 A, forced PWM mode



10.2.2 VDDQ pulse-skip mode

The default working mode is the pulse-skip mode, in which the low-side MOSFET is turned off when the inductor current becomes equal to zero. This configuration guarantees maximum efficiency.

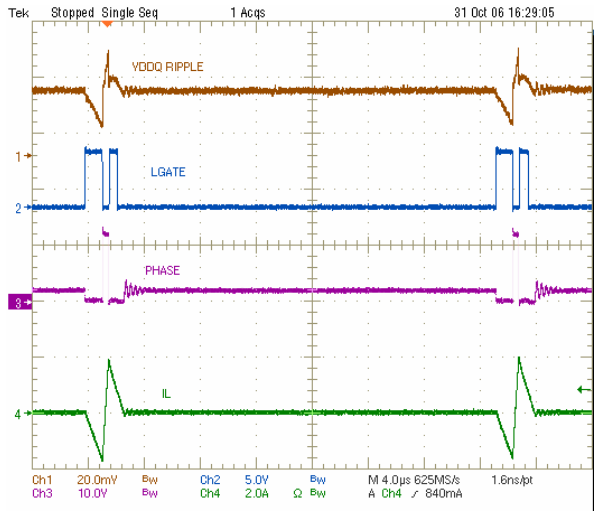
Figure 19. VDDQ = 1.8 V, VIN = 12 V, IVDDQ = 0.5 A, pulse-skip mode



10.2.3 VDDQ non-audible pulse-skip mode

To avoid a too low switching frequency, the non-audible pulse-skip mode can be selected (JP3 in the upper position and JP1 in the middle). The minimum switching frequency allowed is 33 kHz, as shown in *Figure 20*.

Figure 20. VDDQ = 1.8 V, VIN = 12 V, no load, no-audible pulse-skip mode (33 kHz)



10.3 VDDQ, VTT and VTTREF load regulation

The following figures show the VDDQ, VTT and VTTREF output voltages against the load currents. The switching section works in pulse-skip mode and directly feeds VTT LDO.

Figure 21. VDDQ load regulation, VIN = 12 V, pulse-skip mode

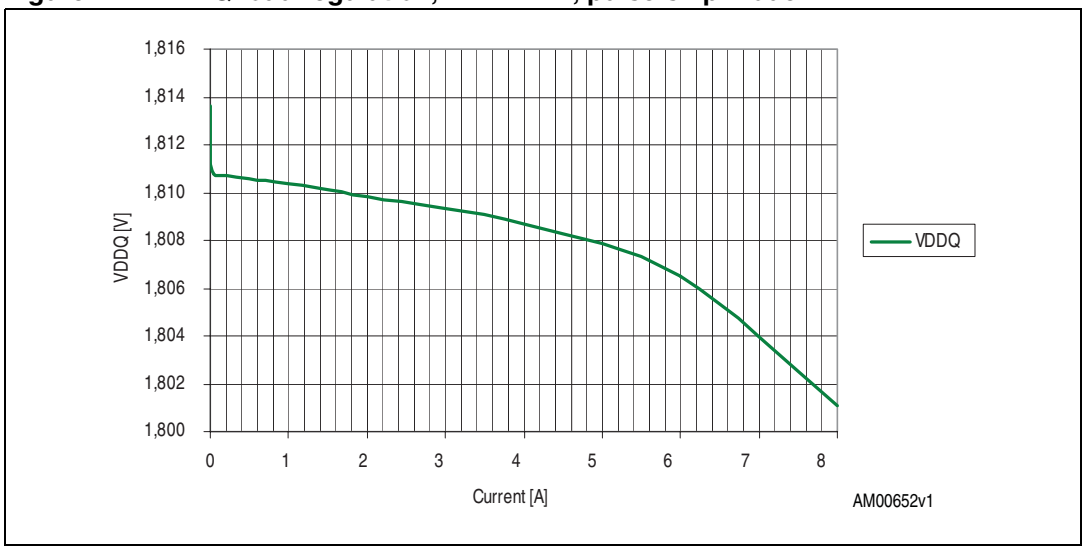


Figure 22. VTT load regulation, LDOIN = VDDQ

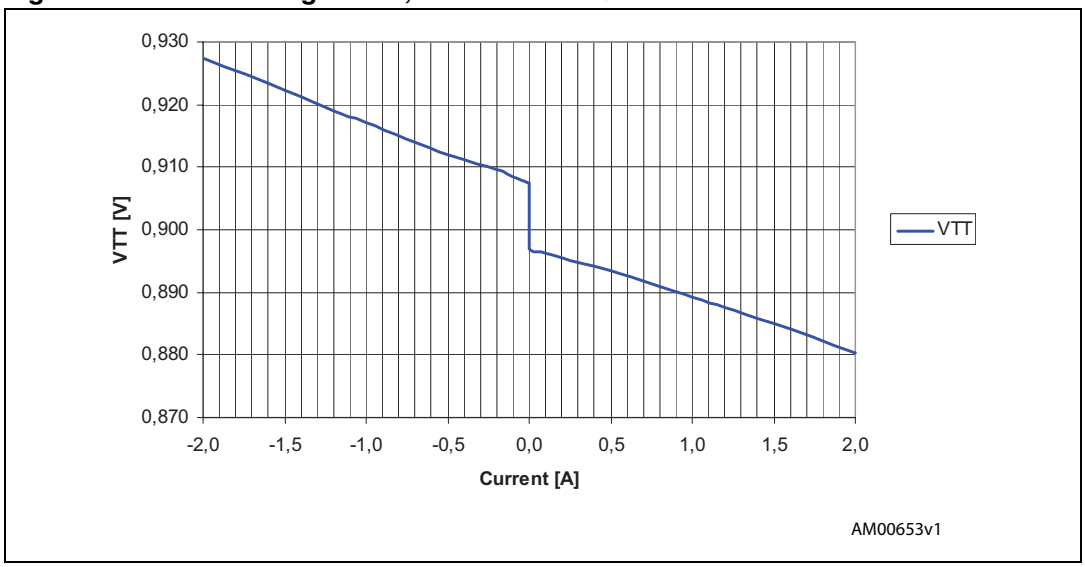
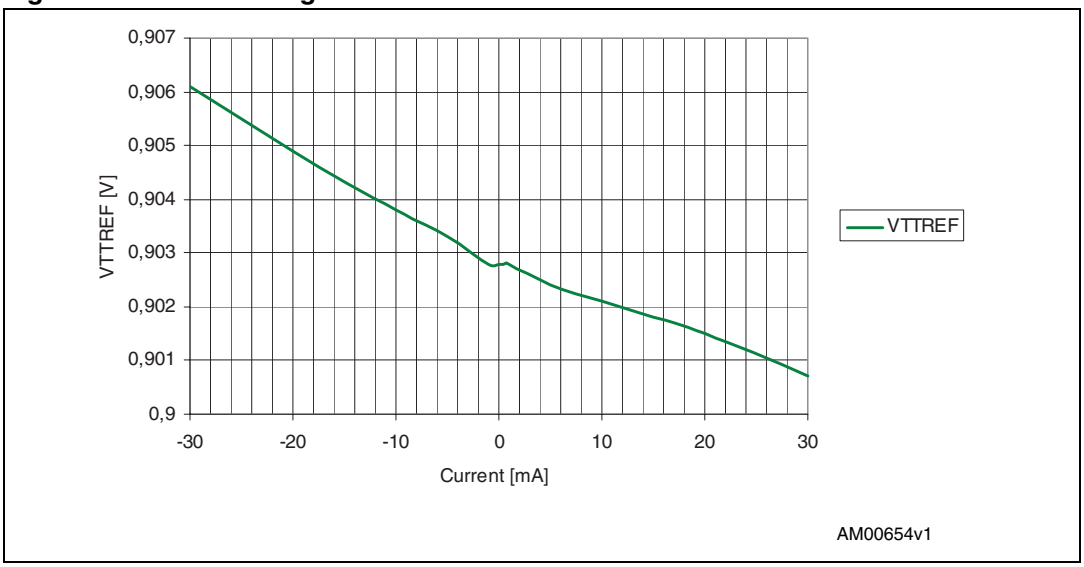


Figure 23. VTT load regulation



10.4 VDDQ and VTT load transient responses

Transient load responses are evaluated by loading the VDDQ and VTT output rails with a current slew rate of 2.5 A/µs.

Figure 24. VDDQ load transient (VIN = 12 V, LOAD = 0 A -> 8 A at 2.5 A/µs), pulse-skip mode

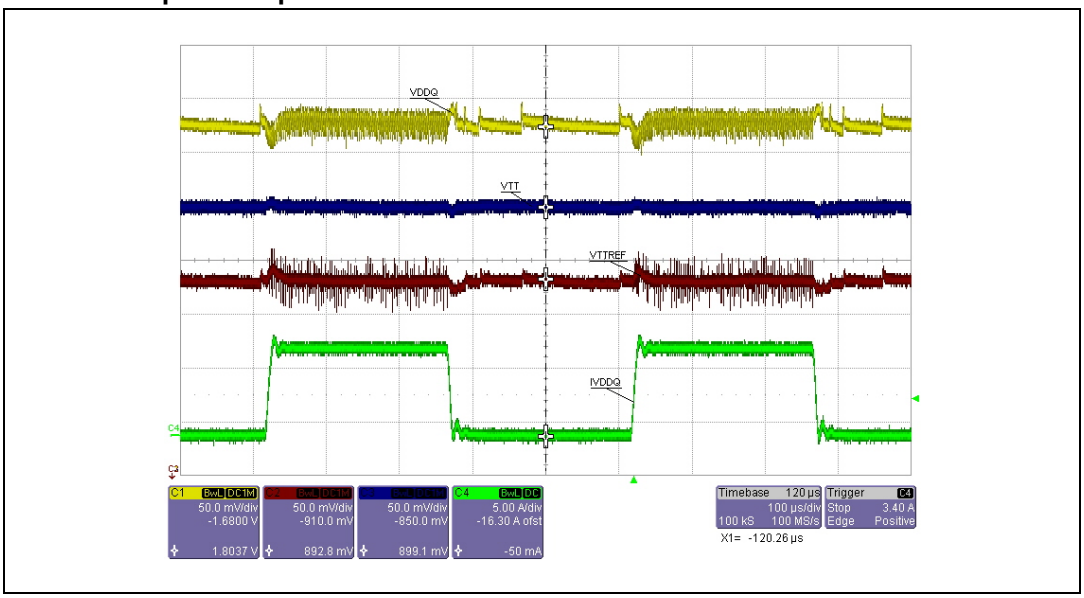
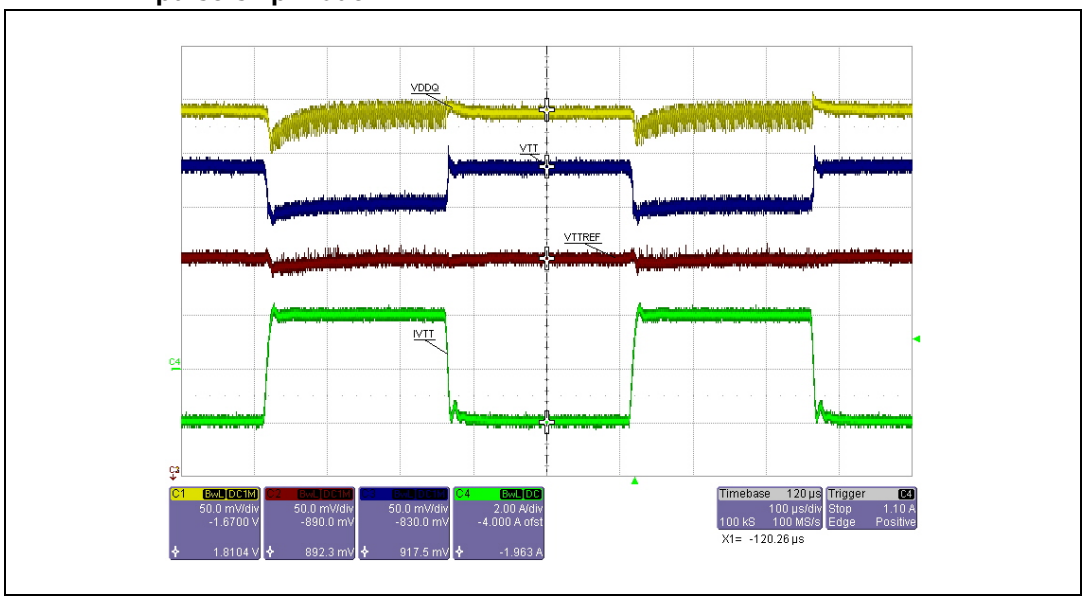


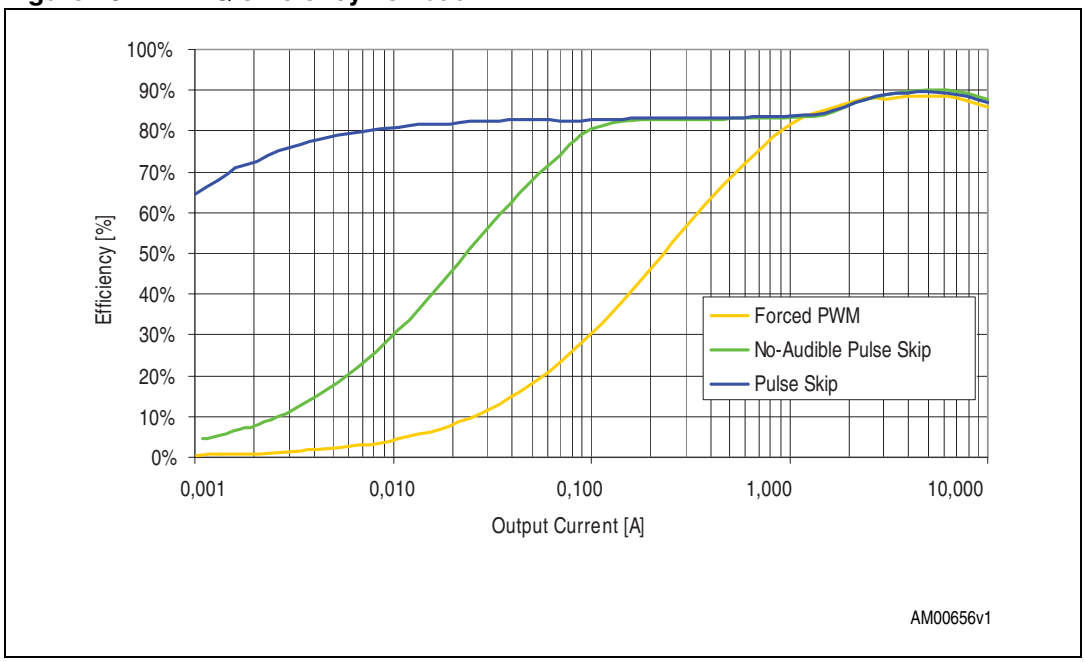
Figure 25. VTT load transient (VIN = 12 V, LOAD = -2 A -> 2 A at 2.5 A/µs), pulse-skip mode



10.5 VDDQ efficiency

The three working modes lead to different power efficiencies. The test should be setup so that VIN = 12 V, FSW = 400 kHz and VDDQ = 1.8 V. The following chart sums up the results.

Figure 26. VDDQ efficiency vs. load[(a)]



a. Forced PWM (yellow), no-audible pulse-skip (green), pulse-skip (blue).

10.6 VDDQ gate drivers

The PM6670S internal MOSFET driver turns on and off the high-side and low-side external MOSFET, avoiding cross-conduction. In *Figure 27* and *Figure 28*, the gate signals are depicted in two different load conditions: without load and with load.

Figure 27. External MOSFET gate signal (VIN = 12 V, load = 0 A), pulse-skip mode

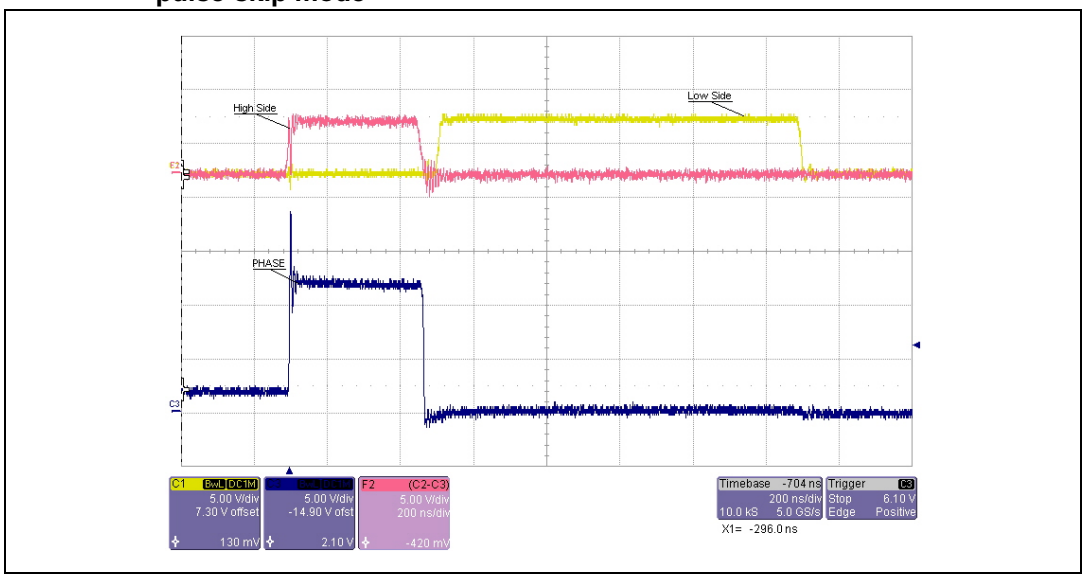
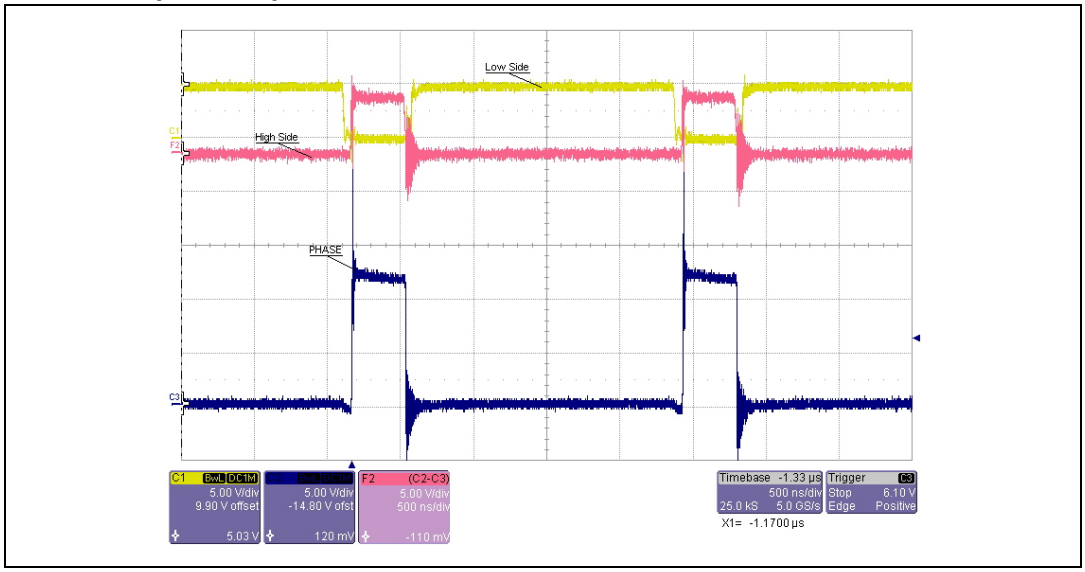


Figure 28. External MOSFET gate signal (VIN = 12 V, load = 8 A), pulse-skip mode

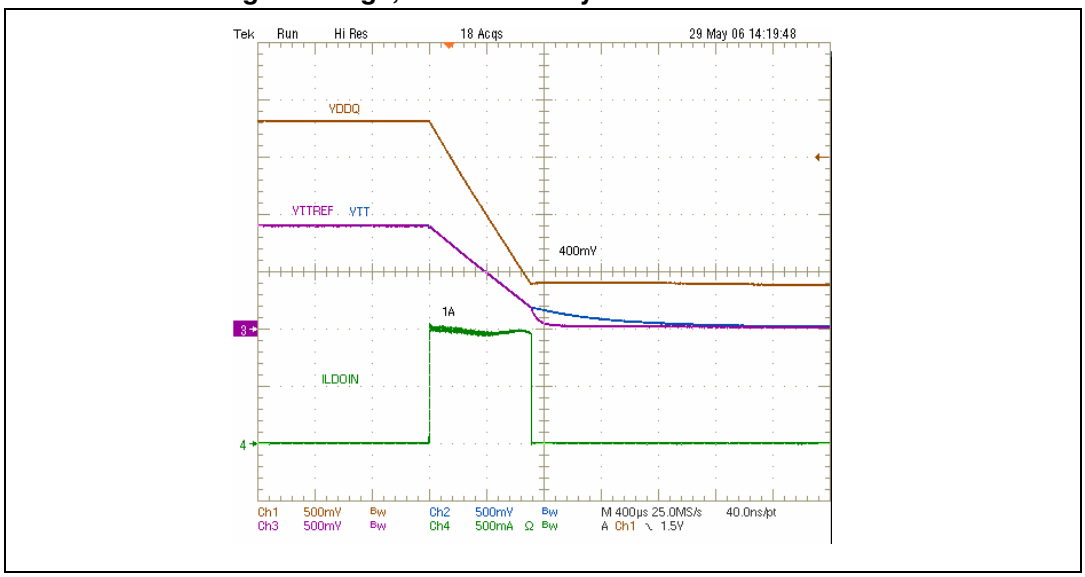


10.7 VDDQ, VTT and VTTREF turn-off (soft end)

10.7.1 Tracking discharge

The JP2 jumper, if placed in the middle, allows the output tracking to be discharged. When S3 and S5 are pulled down, VTT discharges VDDQ by sinking 1 A and, at the same time, tracks the VDDQ half. When VDDQ reaches approximately 400 mV, the output discharge MOSFETs are all closed and each rail is finally discharged.

Figure 29. VDDQ, VTTREF, VTT output voltages and LDO input current, tracking discharge, no load on any rail



10.7.2 Non-tracking discharge

When the non-tracking discharge is programmed (JP2 in the lower position) and S3-S5 are both tied to GND, each output rail is discharged through its discharge MOSFET, as depicted in *Figure 30*.

Figure 30. VDDQ, VTTREF, VTT – no-tracking discharge, no load on any output

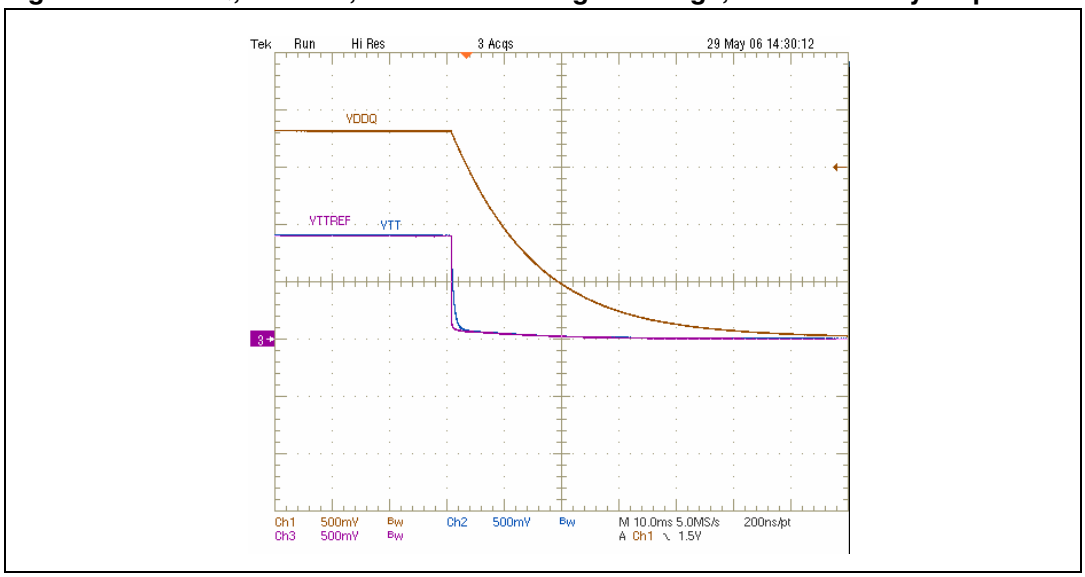


Table 3. Measured discharge resistance in soft-discharge mode

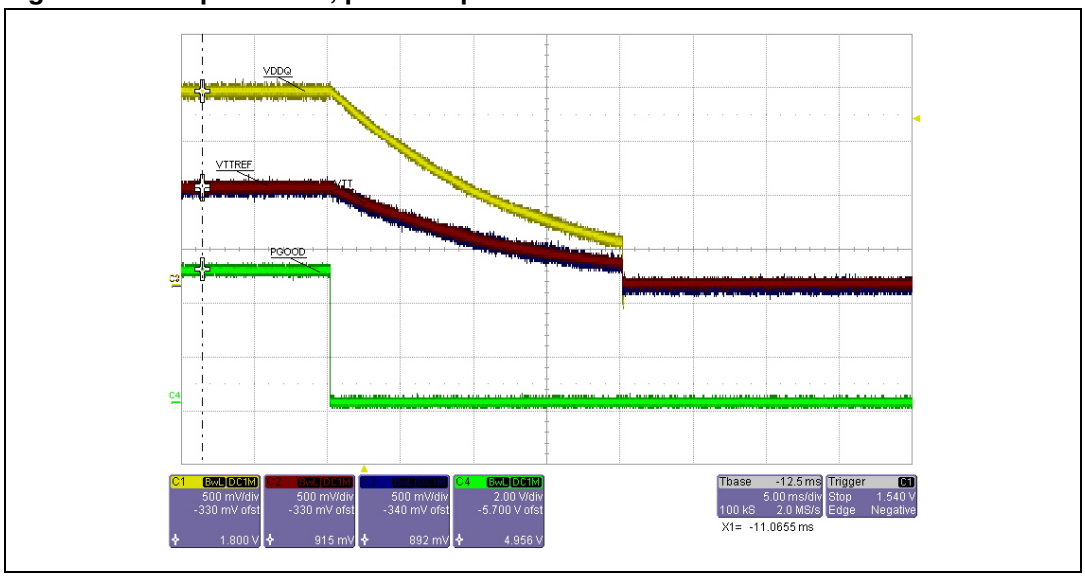
	VDDQ output	VTTREF output	VTT output
Measured N.T.D. discharge MOSFET's $R_{DS(on)}$	25Ω	1.5kΩ	23Ω

10.8 UV, OV and thermal protections

10.8.1 Latched UV protection

If the output voltage is lower than the 70% nominal value, the under-voltage state is entered and the discharge MOSFETs are turned on (as in the non-tracking soft end).

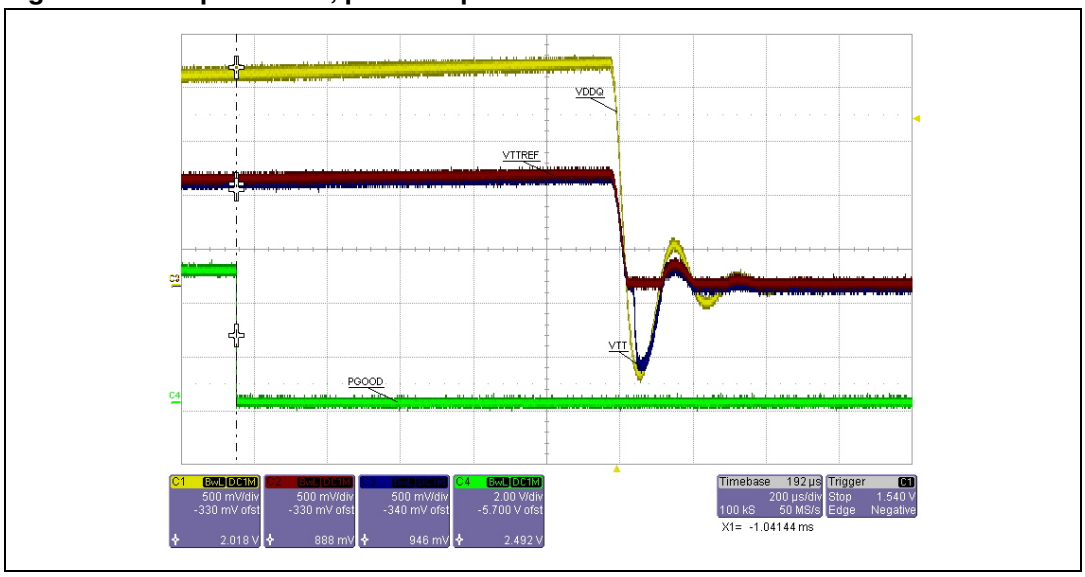
Figure 31. UV protection, pulse-skip mode



10.8.2 Latched OV protection

If the output voltage is higher than the 115% nominal value, the over-voltage state is entered and the low-side MOSFET is turned on. VTT and VTTREF are discharged through their discharge MOSFETs.

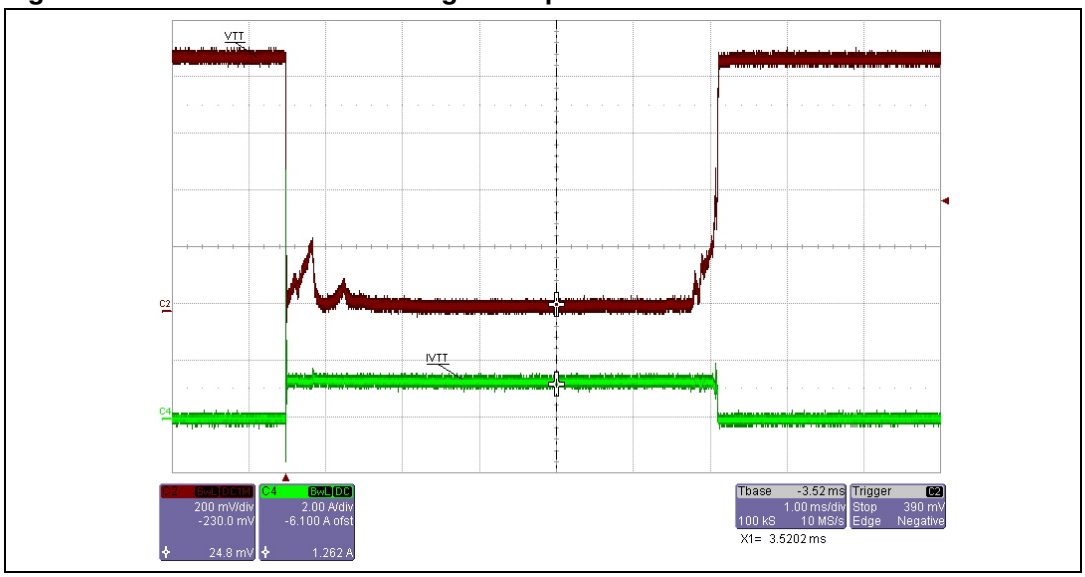
Figure 32. OV protection, pulse-skip mode



10.9 VTT current limit (foldback)

VTT LDO has a foldback protection feature which reduces the current limit to 1 A when the VTT output voltage is outside the ±10% optimum power window. The current limit is restored to 2 A when the output voltage re-enters the optimum power window.

Figure 33. VTT current limit during an output short

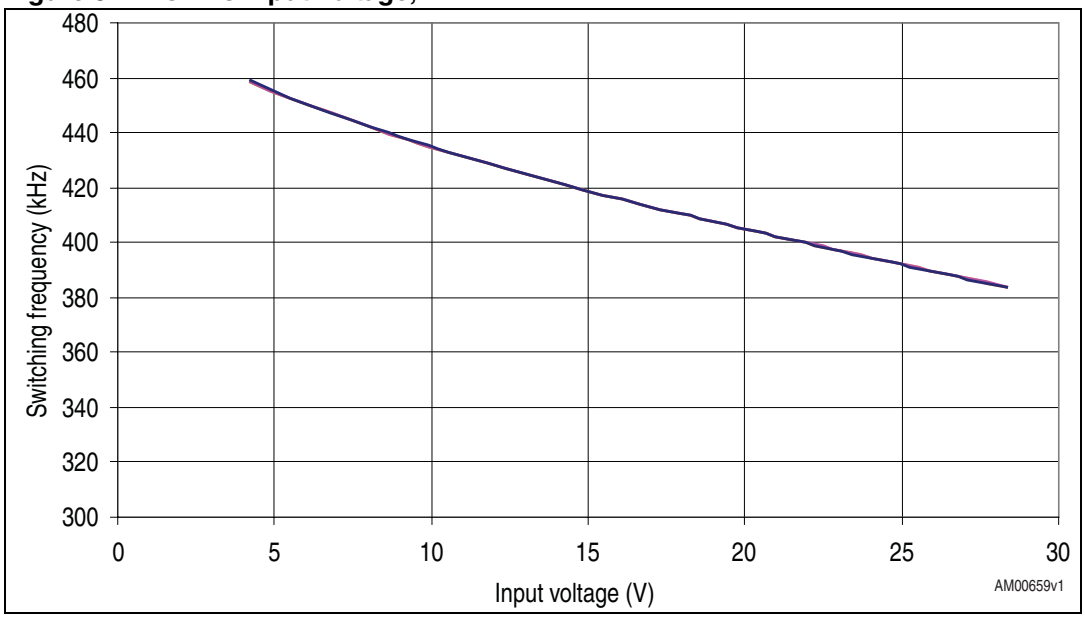


10.10 Switching frequency

10.10.1 Switching frequency vs input voltage

The constant on-time controller leads to a quasi-constant switching frequency, that more or less follows the input voltage.

Figure 34. fsw vs input voltage, DDR2[(b)]

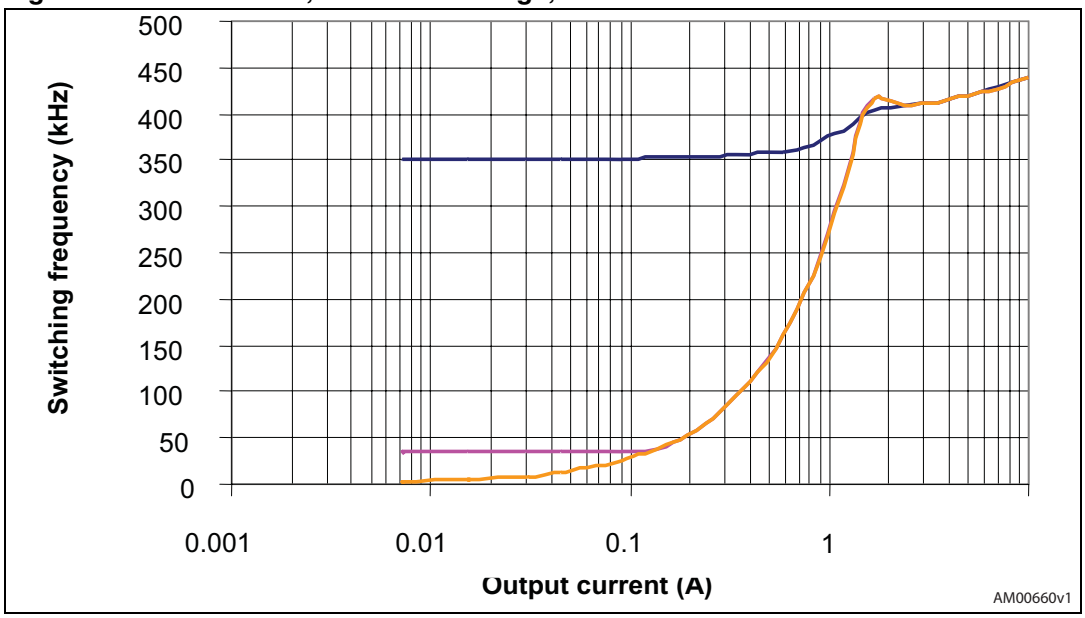


b. Forced PWM (blue), no-audible pulse-skip (purple) and pulse-skip (yellow). Switching frequency vs input voltage, VDDQ = 1.8 V, IVDDQ = 7 A.

10.10.2 Switching frequency vs output current

The switching frequency can decrease to very low values in pulse-skip mode, whereas in non-audible pulse-skip there is a lower limit (about 33 kHz). With increasing loads, however, the switching frequency increases slightly as a consequence of conduction and switching losses.

Figure 35. fsw vs iload, Vin = 12 V voltage, DDR2[c]



10.11 Thermal behavior

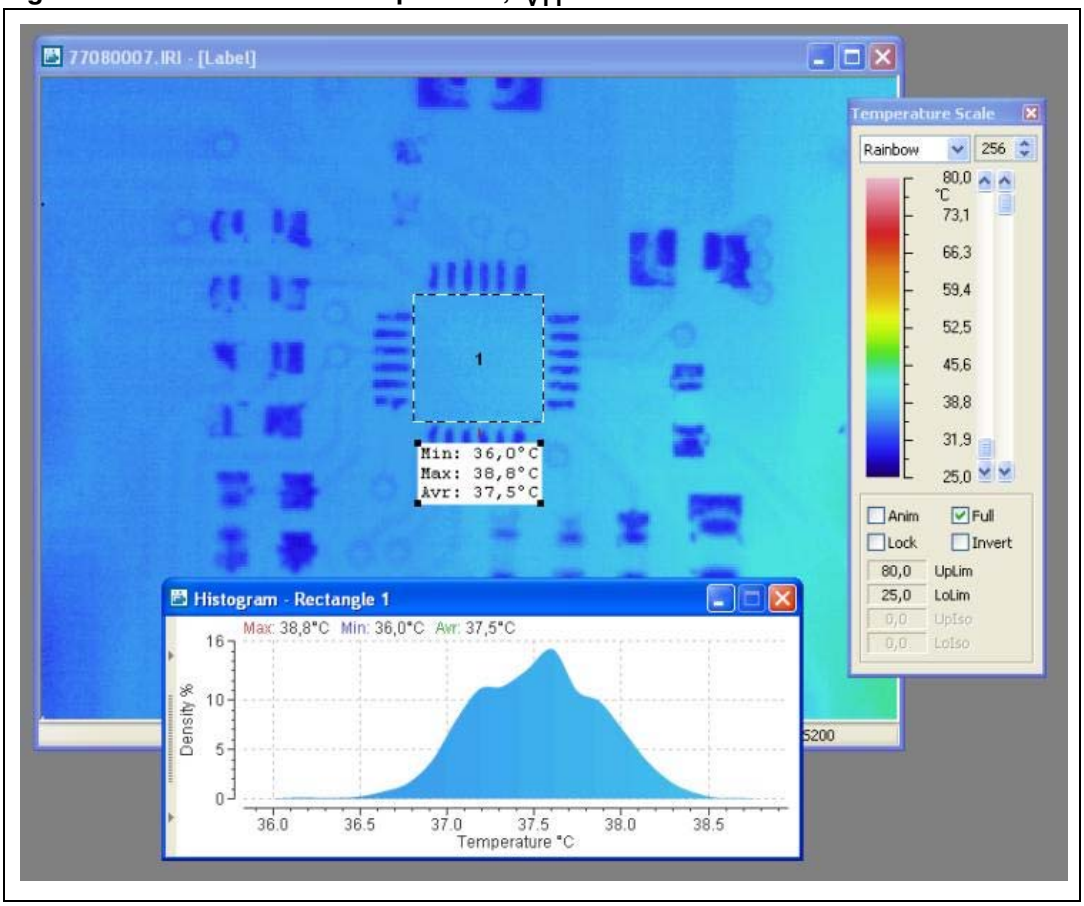
The IC's internal maximum and average temperature can be monitored by an IR camera. For the following measures the test setup is:

- V_{IN} =12 V
- F_{SW} = 360 kHz
- Pulse skip mode
- I_{VDDQ} = 8 A
- VTT rail powered by VDDQ
- T_{AMB} = 26° C

When the VTT current is increased, the IC temperature changes as shown in the following charts.

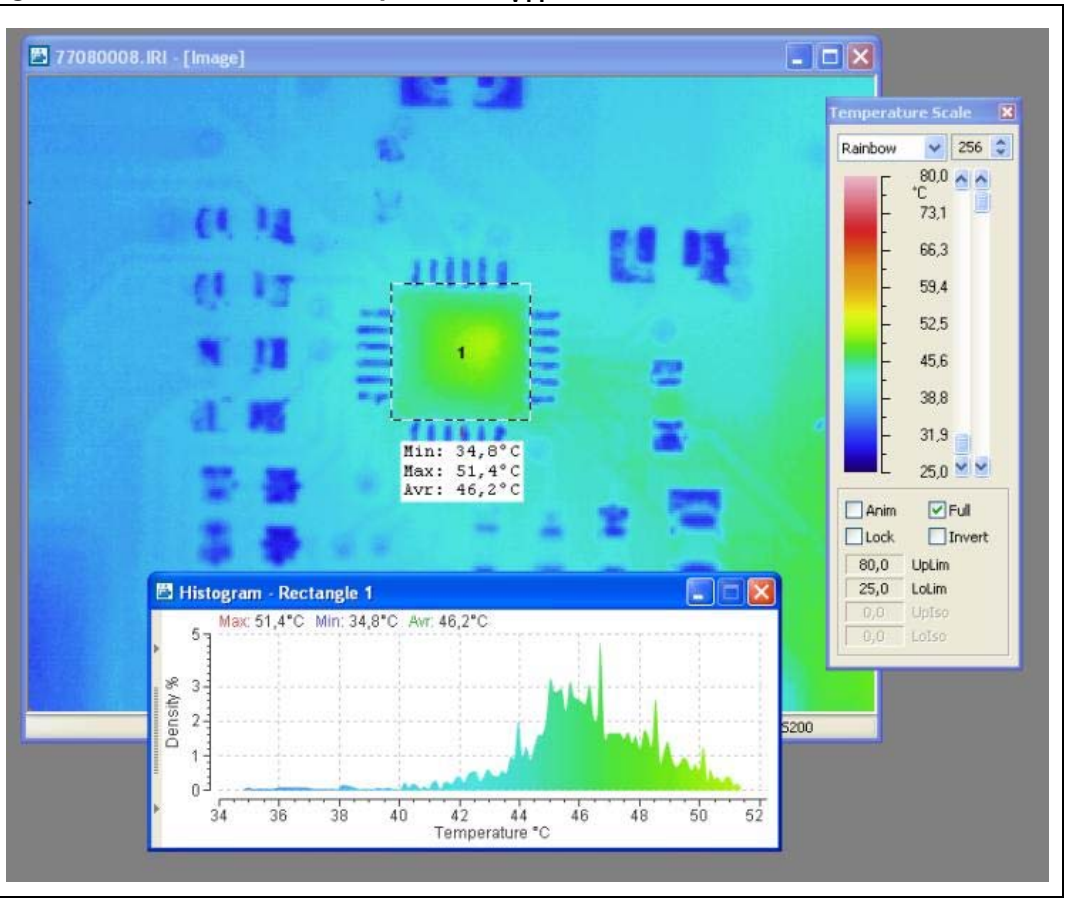
c. Forced PWM (blue), no-audible pulse-skip (purple) and pulse-skip (yellow). Switching frequency vs output current, VDDQ = 1.8 V, no load.

Figure 36. VTT current vs temperature, I_{VTT} = 0 A[(d)]



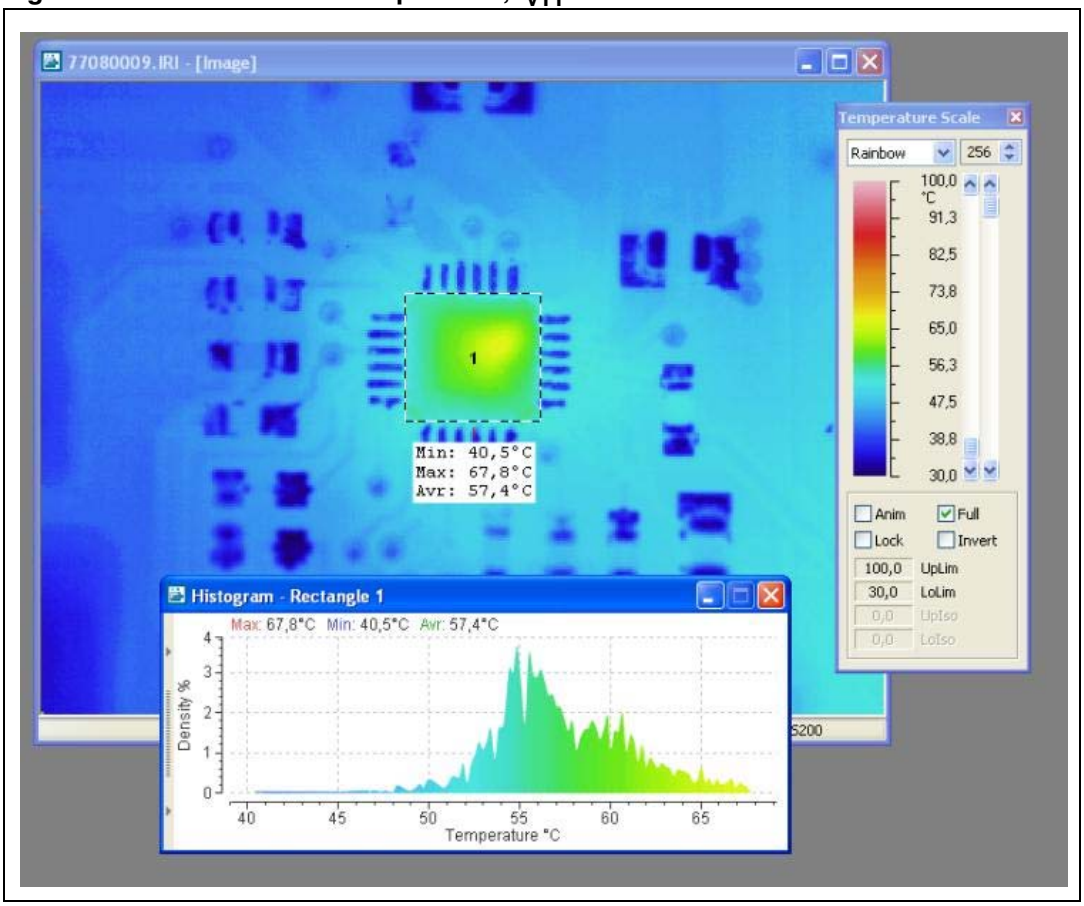
d. Average IC temperature = 37.5° C. Maximum internal IC temperature = 38.8° C.

Figure 37. VTT current vs temperature, I_{VTT} = 0.5 A[e]



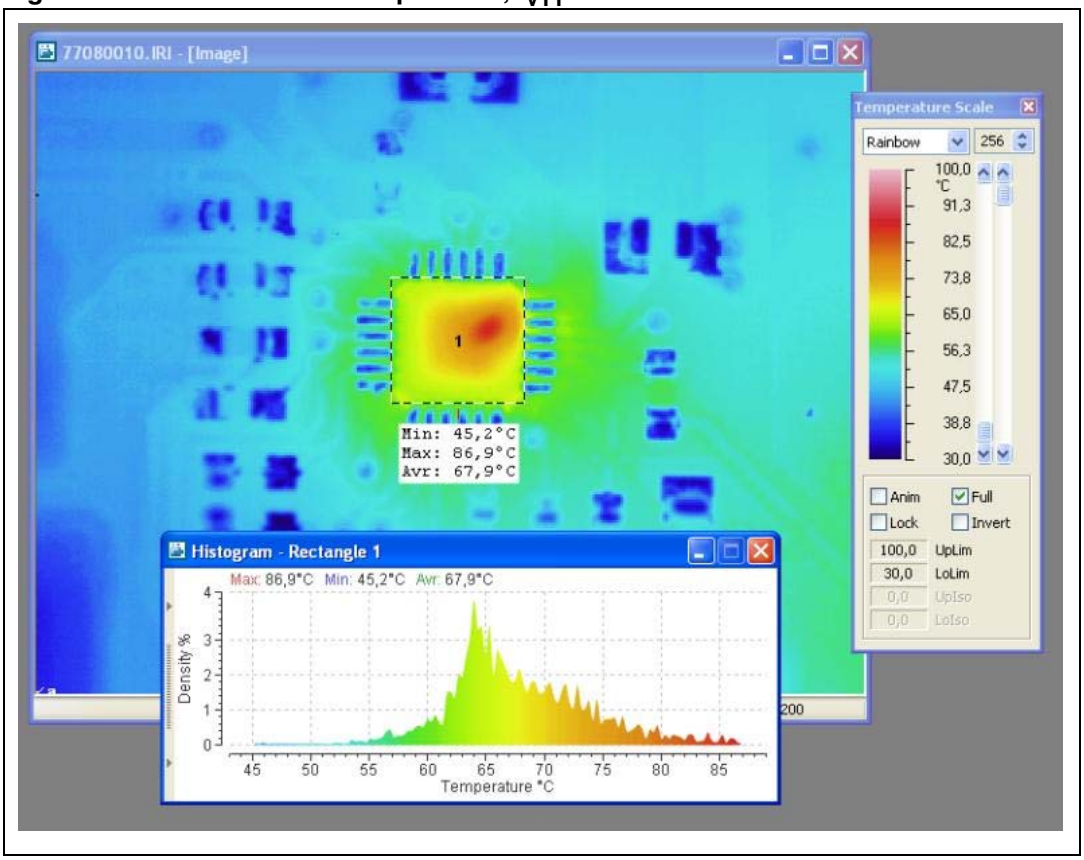
e. Average IC temperature = 46.2° C. Maximum internal IC temperature = 51.4° C.

Figure 38. VTT current vs temperature, I_{VTT} = 1 A[f]



f. Average IC temperature = 57.4° C. Maximum internal IC temperature = 67.8° C.

Figure 39. VTT current vs temperature, I_{VTT} = 1.5 A(g)



10.12 DDR memories (VDDQ = 2.5 V) characterization

The PM6670S is also suitable for DDR memories with a VDDQ rail equal to 2.5 V. The VTT linear regulator is always tracking VTTREF, a buffered replica of the VDDQ half, so the termination rail is equal to 1.25 V as required by the DDR JEDEC standards (JESD79 and JESD8-9 specifications).

The following graphs show each rail load regulation.

g. Average IC temperature = 67.9° C. Maximum internal IC temperature = 86.9° C.

Figure 40. VDDQ load regulation, Vin = 12 V and switching frequency 400 kHz

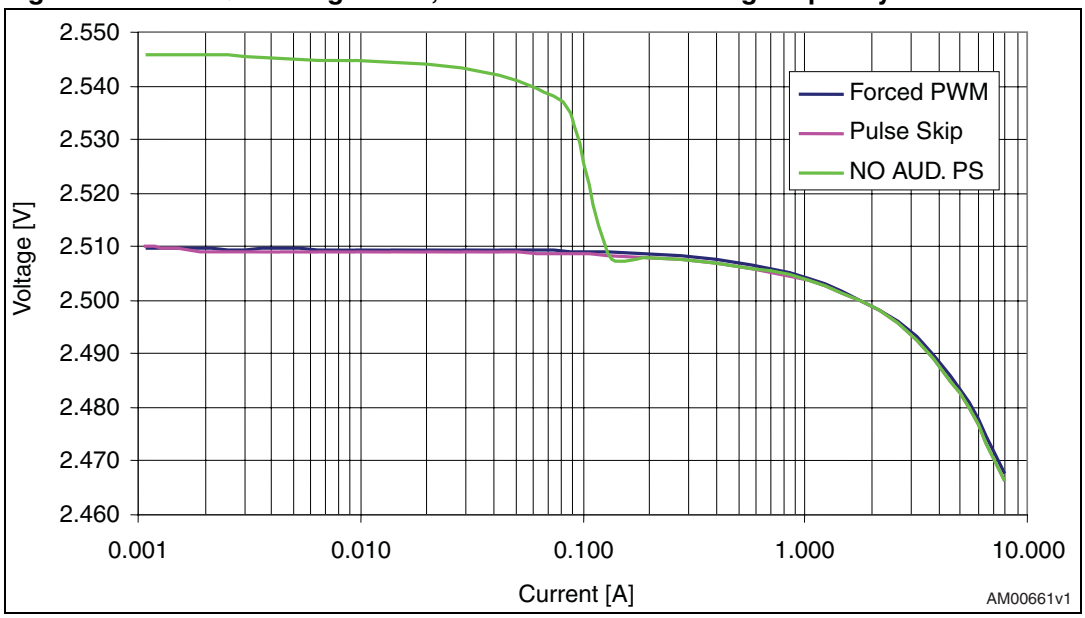


Figure 41. VDDQ load regulation, Vin = 5 V and switching frequency 400 kHz

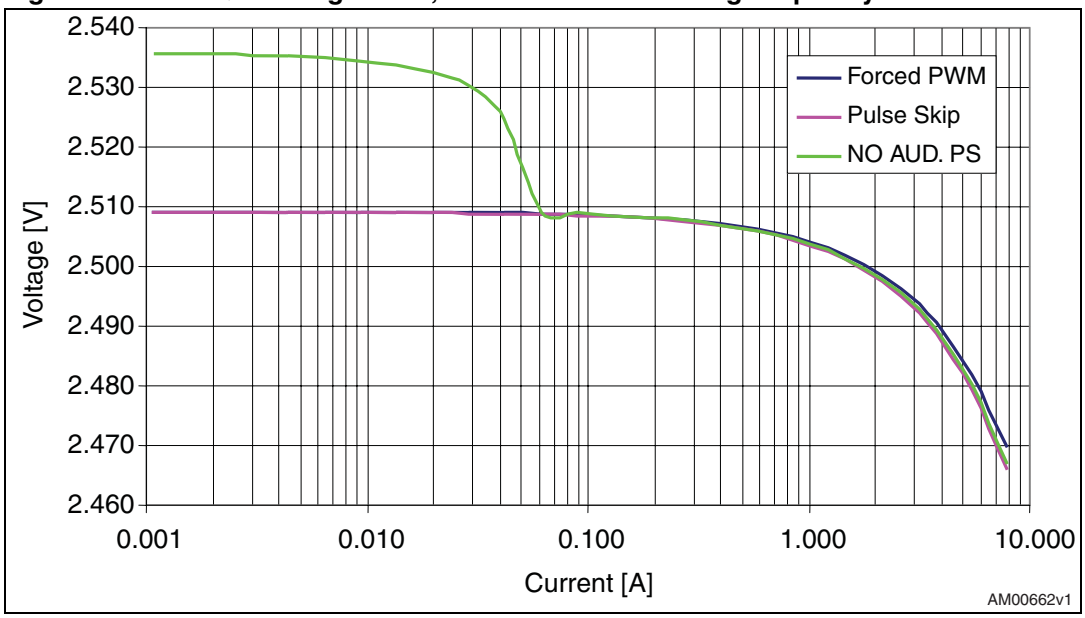


Figure 42. VTT load regulation (h)

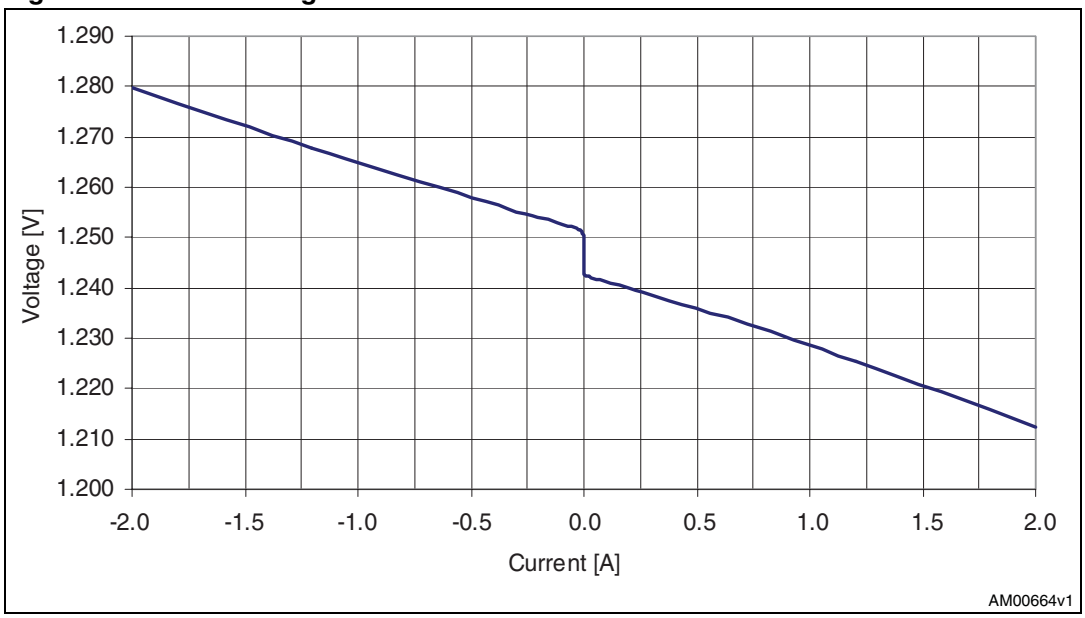
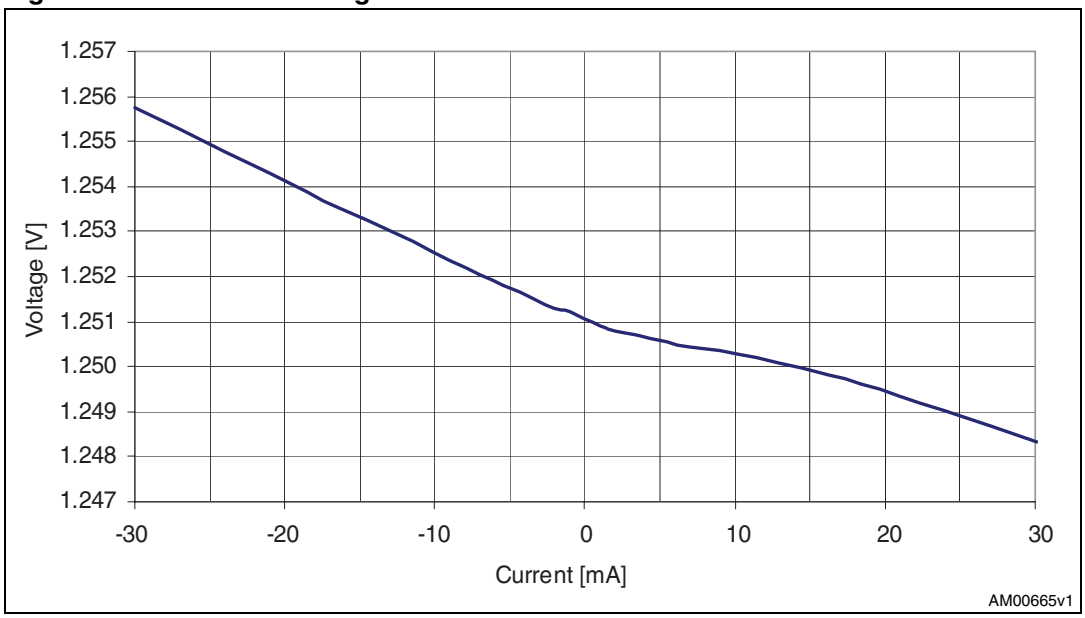


Figure 43. VTTREF load regulation (h)



The efficiency of the switching section is still very high, as shown by the following graphs in which the VDDQ efficiency is computed against the load, with 12 and 5 V input voltages.

All of the three working modes (forced PWM, pulse skip and non-audible pulse skip) have been tested.

h. LDOIN = VDDQ, input voltage 5 V, switching frequency 400 kHz, forced PWM mode.

Figure 44. Efficiency vs load – VDDQ = 2.5 V, Vin = 12 V

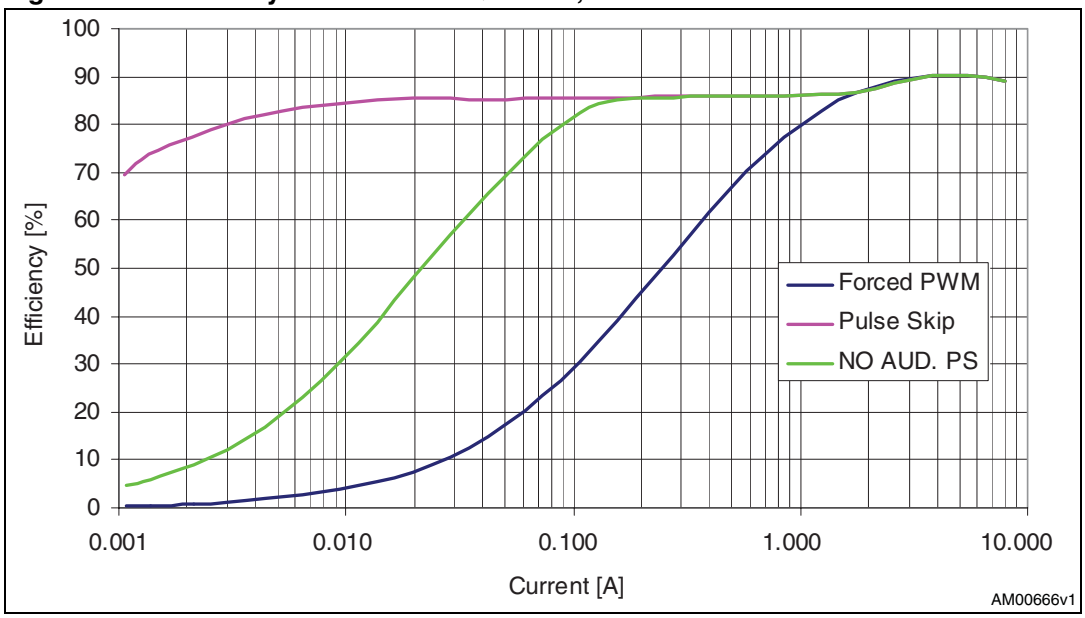
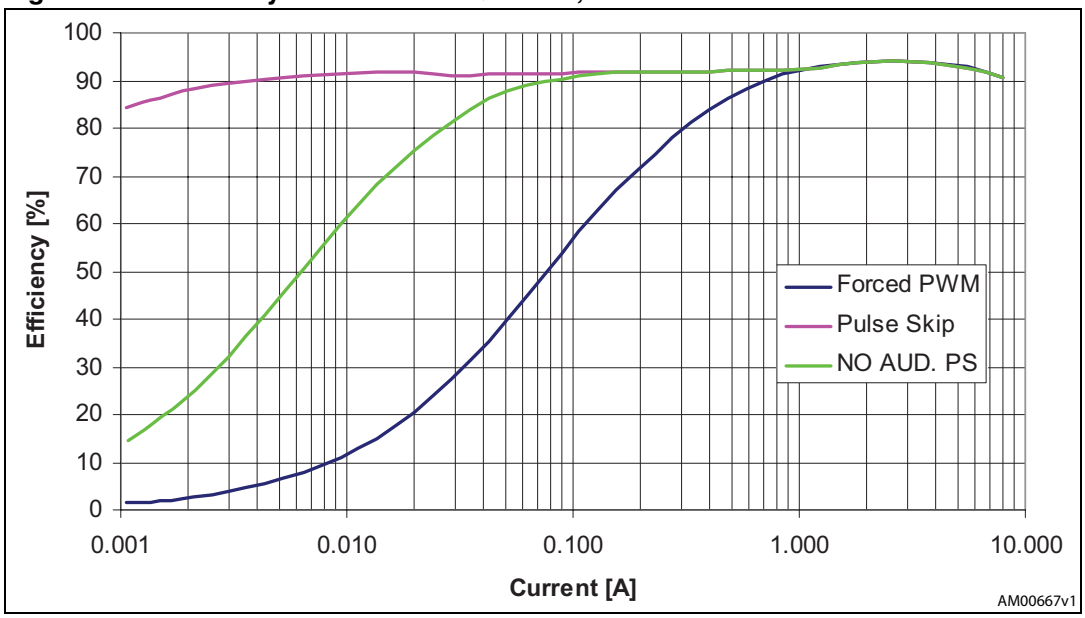


Figure 45. Efficiency vs load – VDDQ = 2.5 V, Vin = 5 V



When the input voltage is equal to 5 V the VDDQ rail efficiency is higher than 90%, with a load greater than 4 mA. This can also be achieved with a very low load when the pulse skip or non-audible pulse skip working mode is selected. The following two graphs show how the switching frequency can change with the load: by decreasing the switching frequency the regulator can greatly increase the efficiency.

Figure 46. SW efficiency vs load – VDDQ = 2.5 V, Vin = 12 V

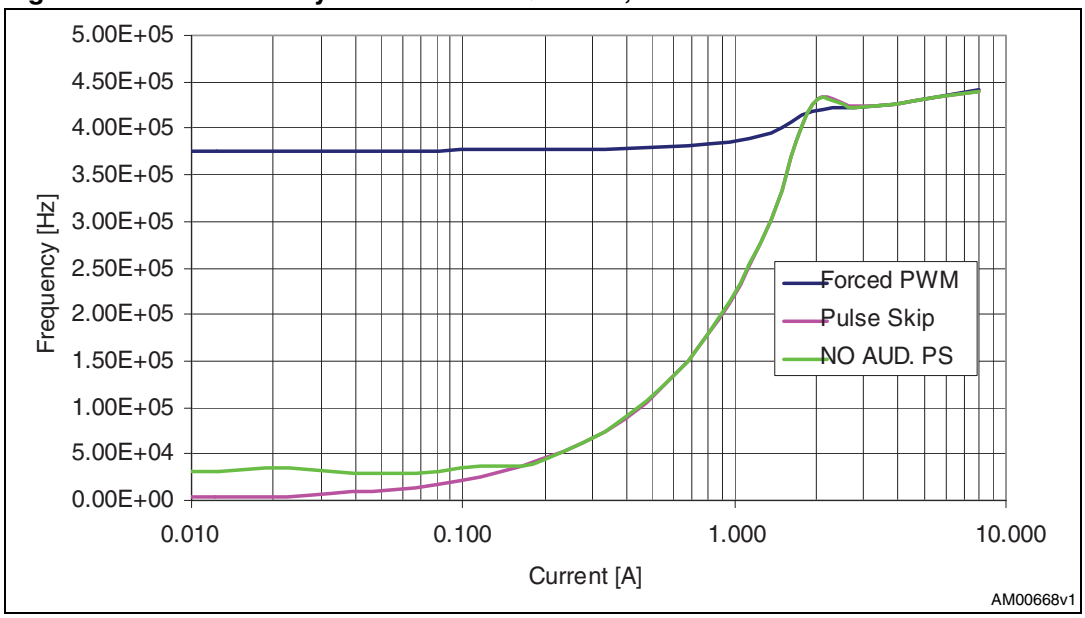
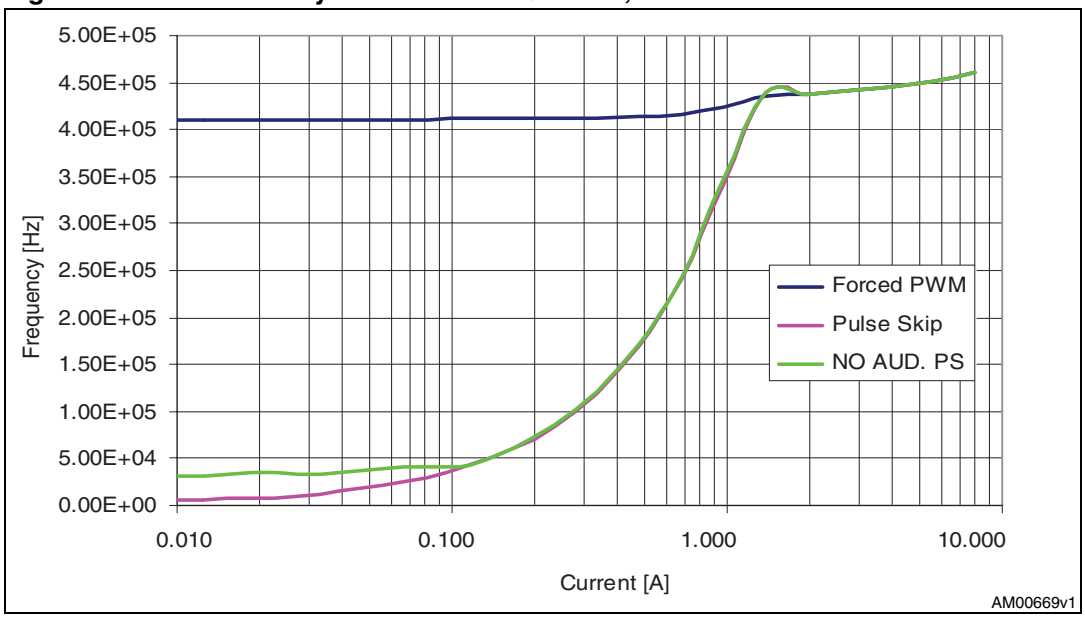


Figure 47. SW efficiency vs load – VDDQ = 2.5 V, Vin = 5 V



The dynamic behavior of the PM6670S can be seen in the following figures, which show the VDDQ and VTT load transient response with 5 V input voltage.

Figure 48. VDDQ load transient response[i]

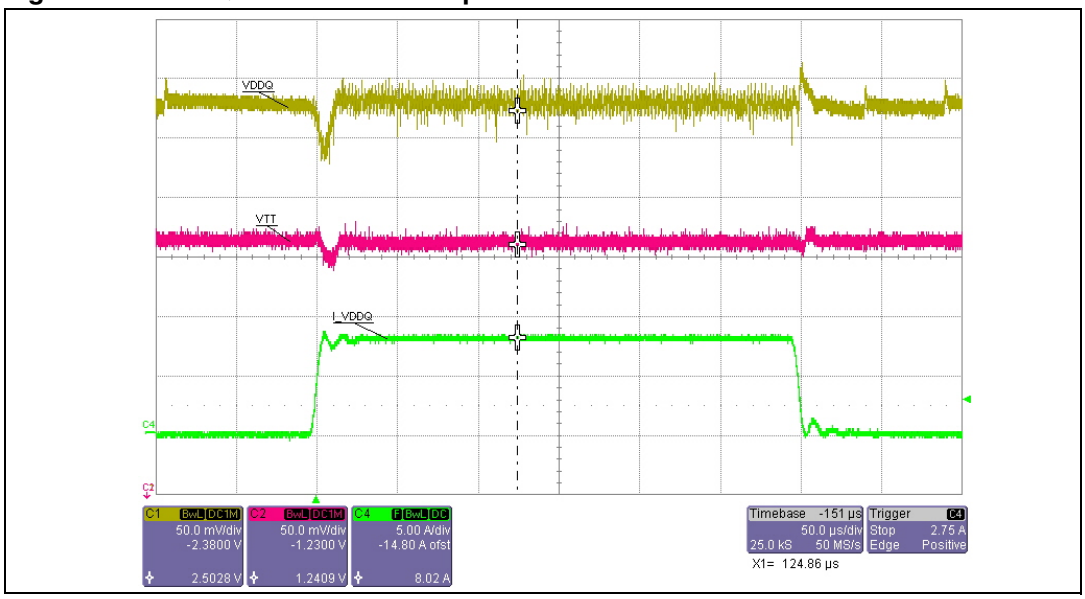
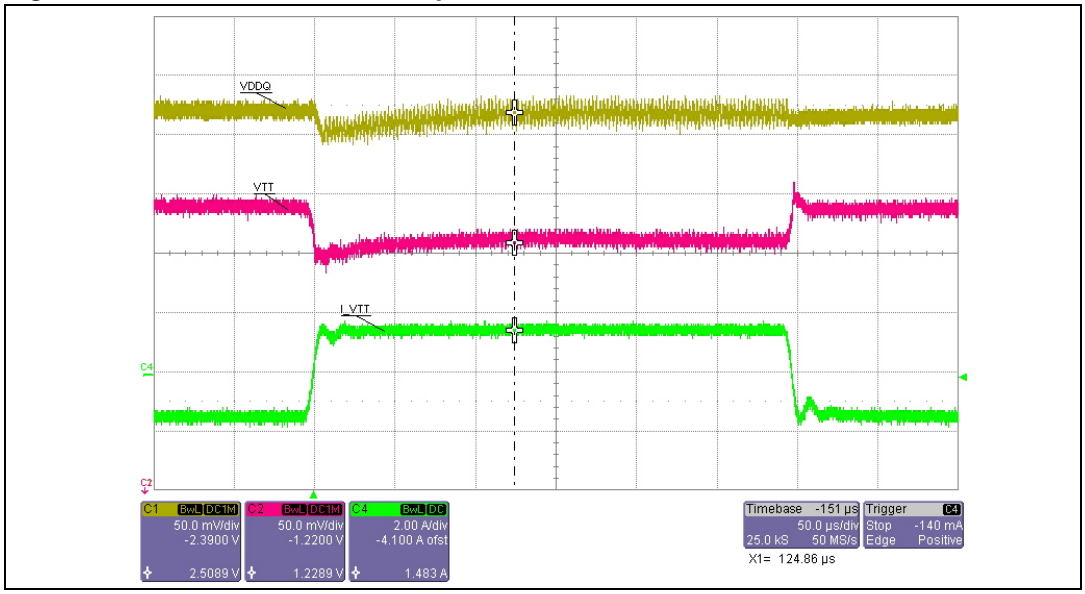


Figure 49. VTT load transient response[j]



i. The load changes from 0 to 8 A at 2.5 A/µs, input voltage 5 V, switching frequency 400 kHz, pulse skip mode.

j. The load changes from -1.5 to 1.5 A at 2.5 A/µs, input voltage 5 V, switching frequency 400 kHz, LDOIN = VDDQ pulse skip mode.

Revision history

Table 4. Document revision history

Date	Revision	Changes
14-Nov-2008	1	Initial release