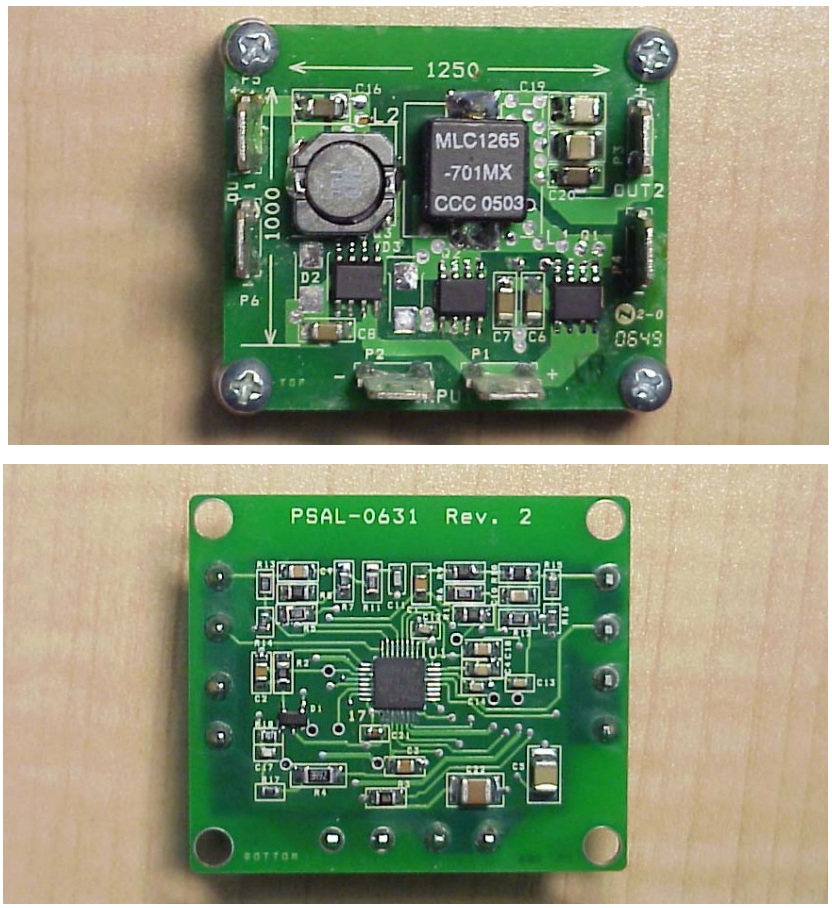
AN2683
Application note

Compact dual output point of load converter based on the PM6680 step-down controller

Introduction

This application note demonstrates the performance of the PM6680 dual step-down controller by implementing a two output point of load converter in a small printed circuit board footprint. Utilizing constant on-time architecture and featuring a no-audio skip mode of operation, a common bus voltage that ranges between 10 to 16 V_{DC} is converted to 1.0 V_{DC} at 10.5 amps and 1.8 V_{DC} at 2.5 amps for a total output power level of 15 watts. The unique no-audio skip feature significantly improves efficiency at light load. Using surface mount components on both the top and bottom of the circuit board and featuring ceramic output capacitors, the area needed for the converter measures only 1.0 by 1.25 inches (25.4 by 37.75 mm). The method for component value dimensioning is described along with the schematic and construction details. Typical efficiencies and functional test data are also presented.

Figure 1. PM6680 - top and bottom view



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1 Main characteristics

1.1 Input voltage range

Table 1. Input voltage range 10 - 16 V_{DC}

Output	Nominal voltage V_{DC}	Max. current amp	Regulation %(1)
1	1.8	2.5	0.44
2	1.0	10.5	2.6

1. Regulation over entire line and load range

1.2 Output ripple voltage

- Output 1: 45 mV p-p at maximum output current
- Output 2: 30 mV p-p at maximum output current

1.3 Switching frequency

- Output 1: 1 - 300 kHz
- Output 2: 2 - 400 kHz

1.4 Output overload/short circuit

- Output 1: nominal trip level 3.37 A (135%)
- Output 2: nominal trip level 13.65 A (130%)

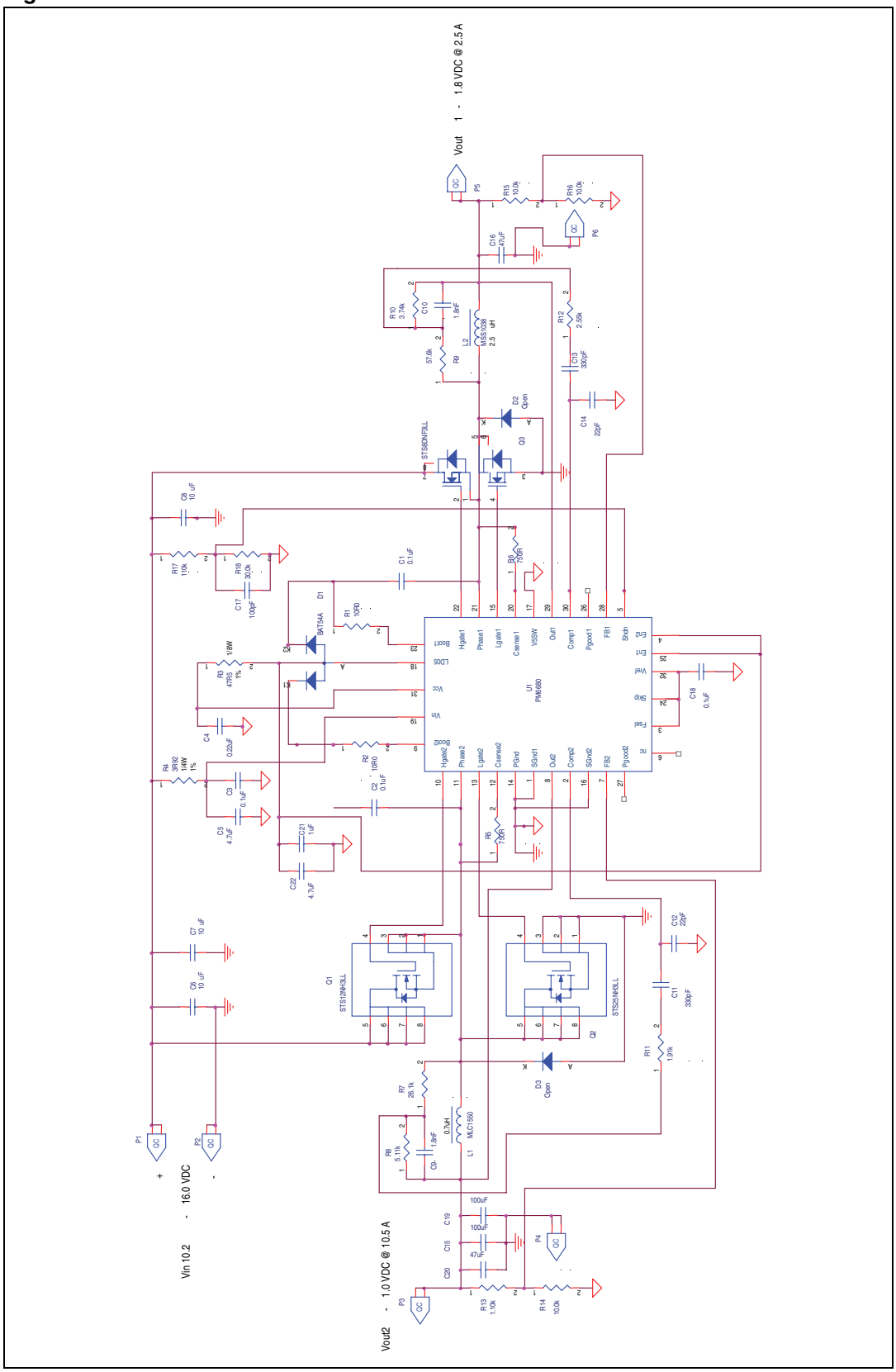
Protection is latched. Power must be cycled to reset.

2 Circuit description

The PM6680 contains all the control circuitry needed to implement two independent step-down synchronous buck regulators using the constant on-time method. The constant on-time method, an improved variant of hysteretic control, provides superior transient response to changes of input voltage and load levels. One of the big advantages of this control method is that it can provide this quick response without the use of an error amplifier which in turn eliminates the need for frequency compensation.

As shown in the photographs (*Figure 1*) all the parts used are surface mount type including the inductors. The circuit board is a multiple layer type consisting of six layers. The top two layers are power routing, the middle two are ground layers split as power and signal, and the bottom two are signal routing layers. In this design, in order to have a low inductor value for the higher current 10.5 A output side, the PM6680 runs in its intermediate range with output one running at 300 kHz and output two running at 400 kHz. So as a consequence the 2.5 A output will run at 300 kHz. With the switching frequencies established the dimensions of the other components can be defined.

Figure 2. Circuit board schematic



As a starting point for the value of the inductors we look at the full load current (I_{fl}) for each output and let the inductor ripple (I_r) current equal 20 to 30 percent of it. For this design a value of 30 percent is used.

$I_r = I_{fl} * 0.3$

for

- Output 1: $I_r = 0.75$ A
- Output 2: $I_r = 3.15$ A

Then the values of the inductors are calculated using the formula:

Equation 1:

$$L = \frac{V_{in} - V_{out}}{f_{sw} \cdot I_r} \cdot \frac{V_{out}}{V_{in}}$$

where V_{in} is the nominal input voltage, V_{out} the output voltage and f_{sw} the switching frequency.

So for input 1:

Equation 2

$$L = \frac{12 - 1.8}{300kHz \cdot 0.75} \cdot \frac{1.8}{12} = 6.8\mu H$$

and for output 2:

Equation 3

$$L = \frac{12 - 1}{400kHz \cdot 3.15} \cdot \frac{12}{1} = 0.7\mu H$$

The output filter capacitors are roughly approximated so that the change in output voltage (ΔV_{out}) during a positive load transient (load is reduced) is minimized. For this design an output voltage change of two to three percent of the total output voltage is considered acceptable. The formula used is:

Equation 4

$$C > \frac{L \cdot (I_{fl})^2}{2 \cdot (V_{in} - V_{out}) \cdot \Lambda V_{out}}$$

For output 1 a ΔV_{out} of 2.5% of 1.8 V_{DC} or 45 mV is used, thus:

Equation 5

$$46.2\mu F > \frac{6.8\mu H \cdot (2.5)^2}{2 \cdot (12 - 1.8) \cdot 0.045}$$

This is a nonstandard value so a 47 µF is used.

For output 2 a ΔV_{out} of 2% of 1.0 V_{DC} or 20 mV is used:

Equation 6

$$175\mu F > \frac{0.7\mu H \cdot (10.5)^2}{2 \cdot (12 - 1.0) \cdot 0.020}$$

As the formula indicates the capacitor value should be greater than that calculated. Even though the board area is small, this section allows the use of ceramic capacitors that are comprised of two 100 µF and one 47 µF all in parallel and which still fit in the required footprint.

With these values of capacitors the ripple voltage can be checked. This is dominated by the equivalent series resistance (ESR) of the capacitors. The ESR must be equal or less than the value calculated by:

Equation 7:

$$ESR \leq \frac{V_r}{I_r}$$

where V_r is the output ripple voltage and I_r is the inductor ripple current. The ESR for the capacitors is given in their datasheets at the frequency they are used at as shown in the graphs. The value is basically the same at both 300 and 400 kHz. For the 47 µF the ESR is 2 mΩ and for the 100 µF it is 1.5 mΩ With these values we can calculate the ripple voltage V_r by:

Equation 8:

$$V_r = I_r \cdot ESR$$

for output 1:

Equation 9

$$0.75A \cdot 2m\Omega = 1.5mV$$

for output 2:

Equation 10

$$3.15A \cdot 545\mu\Omega = 1.9mV$$

These values conform to the specification. They are higher in a practical circuit because of parasitic inductance and loop resistance. Good circuit board layout techniques are essential. Additionally, because of the constant on-time control, the system regulates the output voltage by the valley value of the ripple voltage. A minimum amount of ripple voltage of 30 mV should be on the comp pin to accomplish this. Since the calculated ripple voltage is much lower than this, an additional circuit called the virtual ESR network is incorporated to provide the additional voltage. Before addressing this design, the current limit resistor values will be established. In this design the $R_{DS(on)}$ of the lower MOSFETS is used to implement the current limit. For output 1 with its relatively low output current the MOSFET chosen was the STS8DNF3LL with a nominal $R_{DS(on)}$ of 18 mΩ This particular part is a dual, that is two MOSFETs are contained in the same SO-8 package realizing further circuit board space savings. The current limit is a valley type that operates during the conduction of the low side MOSFET. A 100 µA internal current generator connected to the C_{sense} pin along with a resistor establishes a voltage to which the voltage generated by the $R_{DS(on)}$ is compared. If the $R_{DS(on)}$ voltage is greater, then the voltage at the C_{sense} pin the generation of a new conduction cycle is inhibited. The value of Rc_{sense} is determined by:

Equation 11:

$$Rc_{sense} = \frac{R_{DS(on)} \cdot I_{valley}}{100\mu A}$$

The 18 mΩ value for $R_{DS(on)}$ is a nominal 25 °C number. As current is switched through the device and the ambient is raised, the $R_{DS(on)}$ increases. An increase of approximately 140% is used. Targeting the maximum output current (I_{outmax}) at 3.375 A and having a I_r of 0.750 A the valley current value is:

Equation 12

$$I_{valley} = I_{out(max)} - \frac{I_r}{2}$$

then:

Equation 13

$$3.375A - \frac{0.750}{2} = 3.0A$$

R_{csense} is then:

Equation 14

$$\frac{25m\Omega \cdot 3.0A}{100\mu A} = 750\Omega$$

For output 2 the current levels are substantially higher than output 1 and two discrete MOSFETS must be used. With a nominal input voltage of 12 volts and a one volt output the low side MOSFET is conducting over 90 percent of the time. This means that the $R_{DS(on)}$ of the low side MOSFET must be as low as possible. For this design the STS25NH3LL MOSFET with a nominal 3.2 mΩ on resistance is used. Because of the high current and duty cycle an $R_{DS(on)}$ multiplier of 200% for the R_{csense} calculation is used. Again targeting the output 2 maximum current at 13.65 A the valley current is:

Equation 15

$$13.65A - \frac{3.15A}{2} = 12.075A$$

R_{csense} for output 2 then is:

Equation 16

$$\frac{6.4m\Omega \cdot 12.75A}{100\mu A} = 773\Omega$$

With the maximum output currents established attention can be redirected at designing the virtual ESR network. As mentioned earlier, the ripple voltage should be greater than 30 mV and range between 30 to 50 mV. To derive the necessary minimum value of the virtual ESR (VESR) to produce the ripple voltage the following formula is used:

Equation 17

$$VESR_{(min)} = \left(\frac{0.05V}{I_r}\right) - ESR_{cout}$$

for output 1:

Equation 18

$$\left(\frac{0.05V}{0.75A}\right) - 2m\Omega = 64.6m\Omega$$

for output 2:

Equation 19

$$\left(\frac{0.05V}{3.15A}\right) - 0.545m\Omega = 15.3m\Omega$$

The total ESR (ESR_{tot}) is the sum of the virtual ESR (VESR) and the ESR (ESR_{cout}) of the output capacitor.

for output 1:

Equation 20

$$64.6m\Omega + 2m\Omega = 66.6m\Omega$$

for output 2:

Equation 21

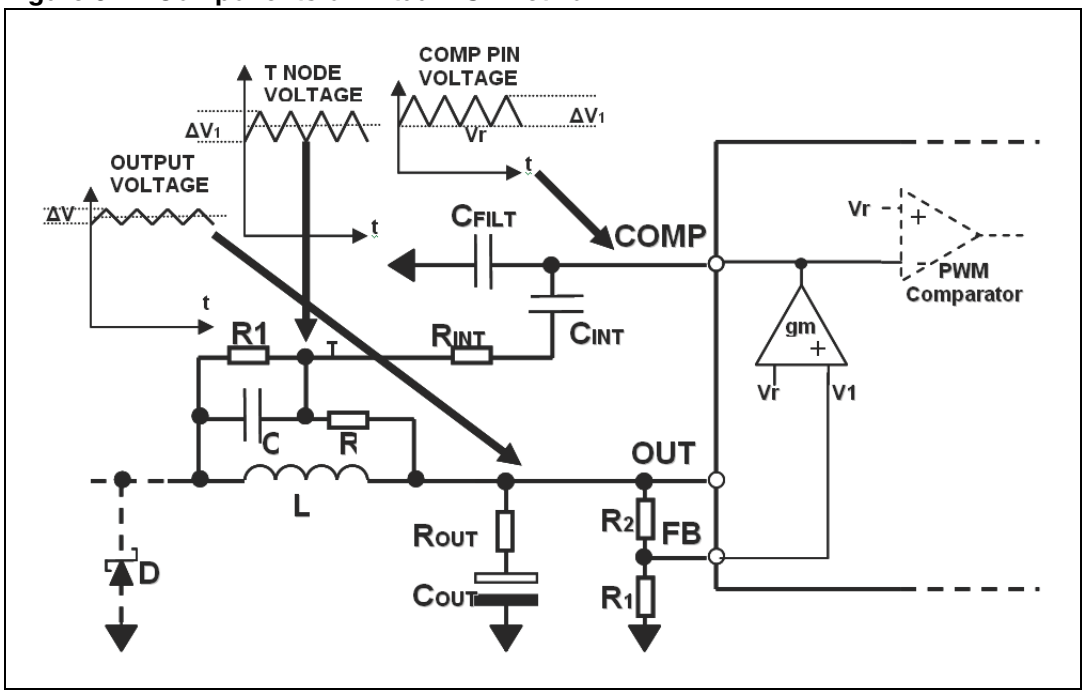
$$15.3m\Omega + 0.545m\Omega = 15.8m\Omega$$

The first component to be dimensioned in the virtual ESR network is C_{int} as shown in *Figure 3* below. Before this can be done the corner frequency (f_z) of the output capacitor must be determined by:

Equation 22

$$f_Z = \frac{1}{2\pi C_{out} ESR_{tot}}$$

Figure 3. Components of virtual ESR network



for output 1:

Equation 23

$$\frac{1}{2\pi \cdot 47\mu F \cdot 67m\Omega} = 50.56kHz$$

for output 2:

Equation 24

$$\frac{1}{2\pi \cdot 247\mu F \cdot 15.54m\Omega} = 41.46kHz$$

With f_z established the stability of the system needs to be verified. The system is stable if the switching frequency (f_{sw}) is greater than 4 times the corner frequency (f_z) of C_{out}; $f_{sw} > f_z \times 4$.

for output 1:

Equation 25

$$50.56kHz \cdot 4 = 202.2kHz$$

Equation 26

$$202.2kHz < 300kHz \qquad OK$$

for output 2:

Equation 27

$$41.46kHz \cdot 4 = 165.8kHz$$

Equation 28

$$165.8kHz < 400kHz \qquad OK$$

The value of C_{int} is actually computed three different ways. The maximum value that results from the computations is the value that should be used. In the formulas for calculating C_{int} the following constants are used: gm = 50 µs (the transconductance of the integrator amplifier); k = 4; V_r = 0.9 V (internal reference voltage).

Equation 29

$$C_{int} > \frac{gm}{2\pi\left(\frac{fsw}{k} - f_z\right)} \cdot \frac{V_r}{V_{out}} \quad \text{or} \quad \frac{gm}{2\pi \cdot f_z} \cdot \frac{V_r}{V_{out}} \quad \text{or} \quad \frac{6\mu A \cdot C_{out}}{\frac{I_{out(max)}}{4} + \frac{I_r}{2}}$$

for output 1:

Equation 30

$$\frac{50\mu s}{2\pi \cdot \left(\frac{300kHz}{4} - 50.56kHz\right)} \cdot \frac{0.9V}{1.8V} = 162.8pF$$

or

Equation 31

$$\frac{50\mu s}{2\pi \cdot 50.56kHz} \cdot \frac{0.9V}{1.8V} = 78.7pF$$

or

Equation 32

$$\frac{6\mu A \cdot 47\mu F}{\frac{3.375A}{4} + \frac{0.75A}{2}} = 231.3pF$$

for output 2

Equation 33

$$\frac{50\mu s}{2\pi \cdot \left(\frac{400kHz}{4} - 41.46kHz\right)} \cdot \frac{0.9V}{1.0V} = 122.4pF$$

or

Equation 34

$$\frac{50\mu s}{2\pi \cdot 41.46kHz} \cdot \frac{0.9V}{1.0V} = 172.8pF$$

or

Equation 35

$$\frac{6\mu A \cdot 247\mu F}{\frac{13.65A}{4} + \frac{3.15A}{2}} = 297.1pF$$

Standard values must be used. In both cases a value rounded up to 330 pF will be used for C_{int}. The next part of the network to be calculated is the capacitor C_{filt}. The formula for this part is straightforward which is:

Equation 36

$$C_{filt} = \frac{C_{int} \cdot (1-q)}{q}$$

Where q is an attenuation factor equal to 0.95.

Since C_{int} is the same for both outputs C_{filt} is the same for both outputs:

Equation 37

$$\frac{330pF \cdot (1-0.95)}{0.95} = 17.3pF$$

A standard value of 22 pF is used. Building on the previous calculations the value of R_{int} is the next part to be established. The formula for R_{int} is given below:

Equation 38

$$R_{int} = \frac{1}{2\pi \cdot 10 \cdot fsw \cdot \frac{C_{int} \cdot C_{filt}}{C_{int} + C_{filt}}}$$

for output 1:

Equation 39

$$R_{int} = \frac{1}{2\pi \cdot 10 \cdot 300kHz \cdot \frac{330pF \cdot 22pF}{330pF + 22pF}} = 2570\Omega$$

using standard value 2.55 kΩ

for output 2:

Equation 40

$$R_{int} = \frac{1}{2\pi \cdot 10 \cdot 400kHz \cdot \frac{330pF \cdot 22pF}{330pF + 22pF}} = 1929\Omega$$

using standard value 1.91 kΩ

Then, the value of the C of the virtual ESR network is calculated. It is simply:

Equation 41

$$C = C_{int} \cdot 5$$

Since C_{int} is the same for both outputs:

Equation 42

$$C = 330pF \cdot 5 = 1650pF$$

Use standard value 1.8 nF.

Next, the R value of the network is established. This is determined by the formula:

Equation 43

$$R = \frac{L}{ESR_{tot} \cdot C}$$

for output 1:

Equation 44

$$\frac{6.8\mu H}{65m\Omega \cdot 1.8nF} = 58.12K\Omega$$

for output 2:

Equation 45

$$\frac{0.7\mu H}{15m\Omega \cdot 1.8nF} = 25.92K\Omega$$

The standard value of 57.6 KΩ can be used for output 1 and 26.1 KΩ for output 2. Finally the last component of the virtual ESR network R1 is computed with the formula:

Equation 46

$$R1 = \frac{R \cdot \left(\frac{1}{C\pi f_z}\right)}{R - \frac{1}{C\pi f_z}}$$

for output 1:

Equation 47

$$\frac{57.6K\Omega \cdot \left(\frac{1}{1.8nF\pi 50.56kHz}\right)}{57.6K\Omega - \frac{1}{1.8nF\pi 50.56kHz}} = 3723\Omega$$

for output 2:

Equation 48

$$\frac{26.1K\Omega \cdot \left(\frac{1}{1.8nF\pi 41.46kHz}\right)}{26.1K\Omega - \frac{1}{1.8nF\pi 41.46kHz}} = 5098\Omega$$

The standard value of 3.74 KΩ can be used for output 1 and 5.11 KΩ for output 2. With the design of the virtual ESR complete the only other output components to be determined are the resistor dividers that connect to the feedback pins FB1 and FB2. With an internal reference voltage (V_r) of 0.9 volts the determination of the values is straightforward by:

Equation 49

$$R2 = \frac{V_{out} - V_r}{\frac{V_r}{R1}}$$

where R1 is the resistor connecting the feedback pin to ground (resistors R14 and R16 in the schematic) and R2 is the resistor connecting the output to the feedback pin (resistors R13 and R15 in the schematic). The value for R1 is chosen as 10.0 KΩ for both outputs. The value for R2 is then:

for output 1:

Equation 50

$$R2 = \frac{1.8V - 0.9V}{\frac{0.9V}{10K\Omega}} = 10K\Omega$$

for output 2:

Equation 51

$$R2 = \frac{1.0V - 0.9V}{\frac{0.9V}{10K\Omega}} = 1.11K\Omega$$

Use standard values 10.0 KΩ ohm for R15 and 1.10 KΩ ohm for R13. With the output component values determined it is important not to overlook the dimensioning of input components critical to proper operation. These are the input capacitors that provide the high frequency input currents needed by the converters. Locate these capacitors as close as possible to the drain of the upper MOSFET and also make sure to minimize the inductance to the other power components on the power ground plane. The ripple current (I_r) ratings should meet or exceed the value as computed below:

Equation 52

$$I_r = \sqrt{D_1 \cdot I_{out1}^2 \cdot (1 - D_1) + D_2 \cdot I_{out2}^2 \cdot (1 - D_2)}$$

where D is the duty cycle of the converter and is given by:

Equation 53

$$D = \frac{V_{out}}{V_{in}}$$

and I_{out} is the maximum output current of the converter.

For output 1 D1 is:

Equation 54

$$\frac{1.8V}{12V} = 0.15$$

For output 2 D2 is:

Equation 55

$$\frac{1.0V}{12V} = 0.083$$

So then we have:

Equation 56

$$I_r = \sqrt{0.15 \cdot 3.375^2 \cdot (1 - 0.15) + 0.083 \cdot 13.65^2 \cdot (1 - 0.083)} = 3.95A$$

3 Construction

With the components dimensioned the construction of the circuit board can be considered. With this type of high frequency converter separate power and signal grounds are a must. Additionally, the small board area necessitated component placement on both sides and the use of additional layers for routing the signal interconnects and providing lower conductor resistance in the heavy current paths. In *Figure 4*. below the top layer component placement is shown. The top layer components are comprised of the power handling ones such as the MOSFETS and inductors. Along with the power component placement is *Figure 5* that shows the top copper power traces. The first inner layer shown in *Figure 6* is a layer that has redundant power traces to lower resistance in the high current paths. The power ground and signal ground layers are shown in *Figure 7* and *8* respectively. Care must be taken that they connect at only one point close to pin 14 of the PM6680. The component placement for the bottom layer is shown in *Figure 9*, these are the parts that do the signal conditioning and connect to the PM6680 controller. Of special note on the bottom layer copper shown in *Figure 10*, is the square copper island under U1 (the PM6680). This island connects to the thermal sink contact that is on the bottom of the package. A requirement for proper operation is that this pad be connected to signal ground. As shown in *Figure 11*, which is the fourth inner layer used for additional signal routing, a matrix of nine vias are used to make the connection to the signal ground layer. The board uses 1-ounce copper on all layers. While not necessary for the signal traces, keeping the copper weight even on all the layers reduces the chances of the board warping during the manufacturing process.

Figure 4. Top layer component placement

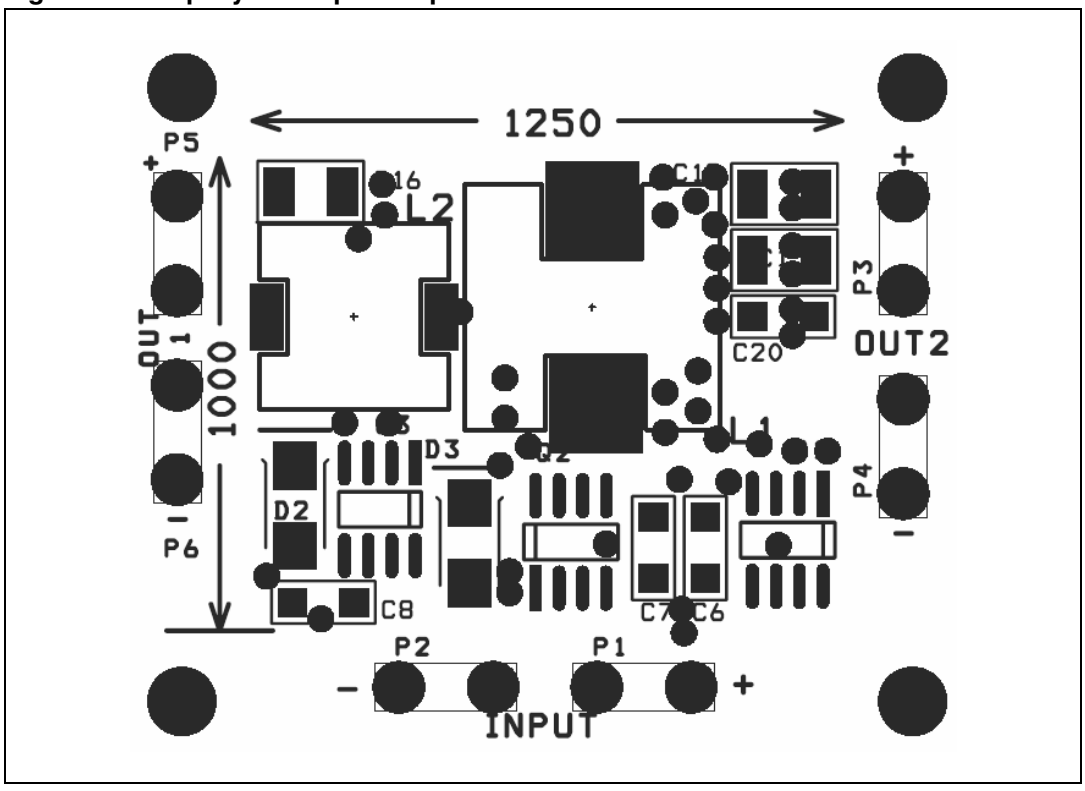


Figure 5. Top layer copper

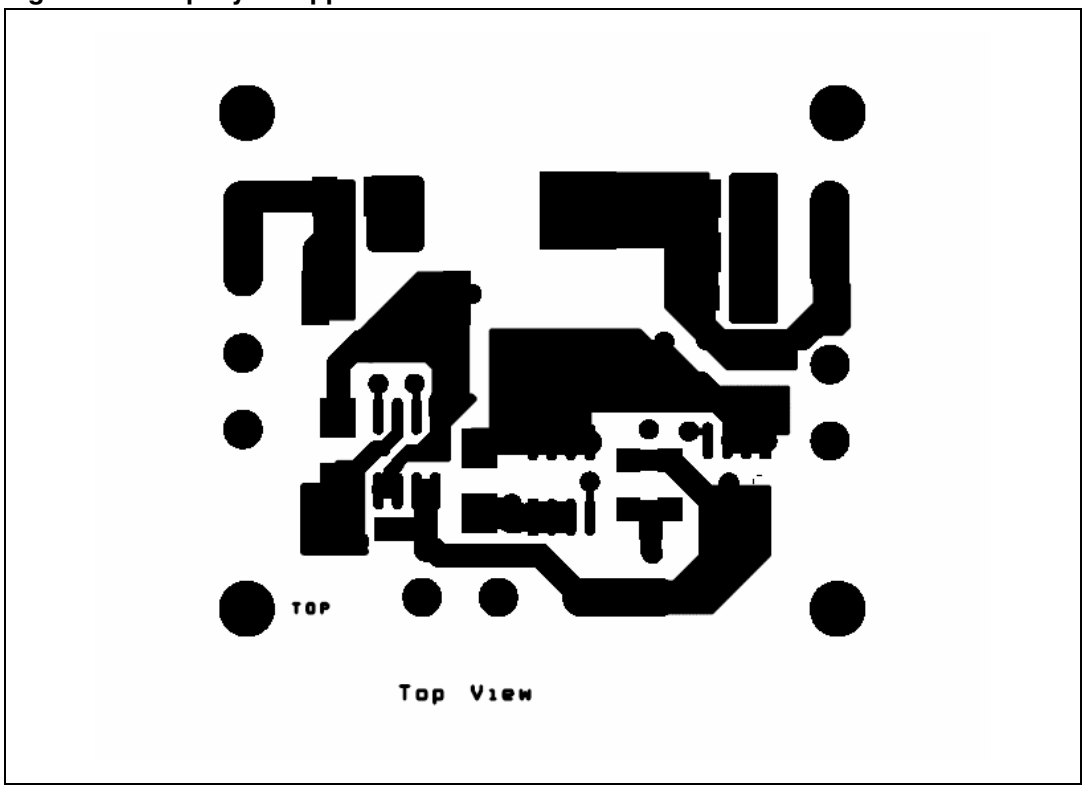


Figure 6. Inner layer 1 showing additional power traces

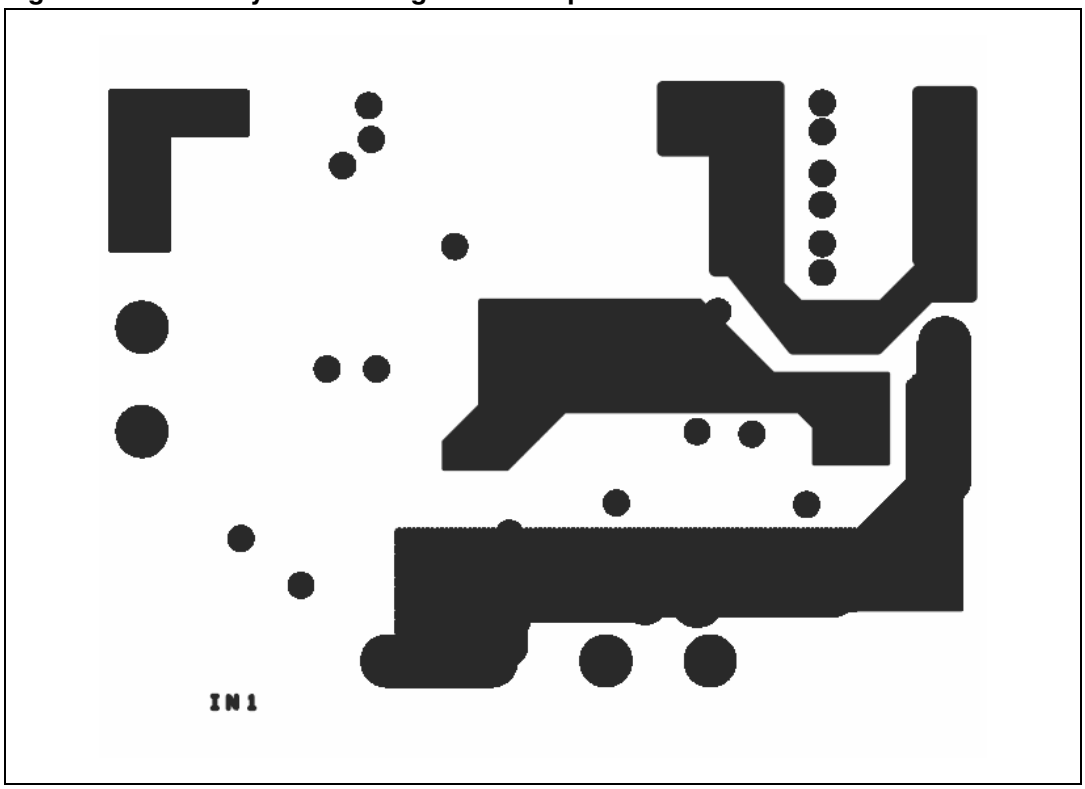


Figure 7. Power ground layer (inner layer 2)

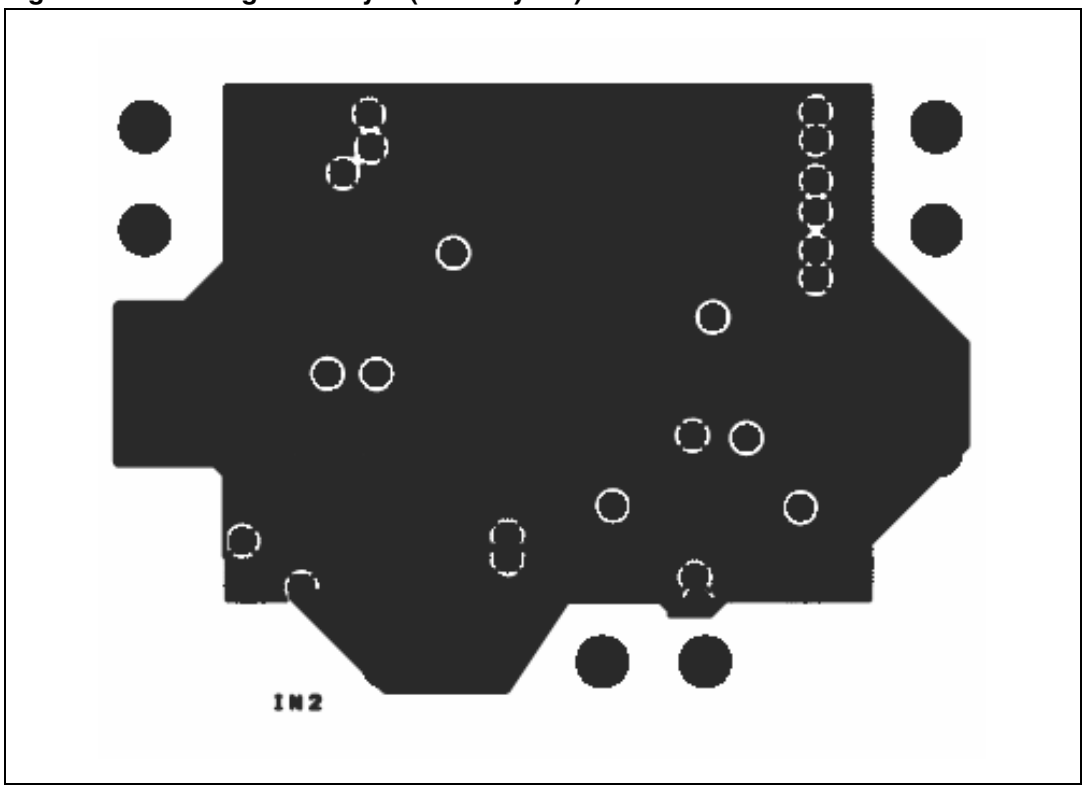


Figure 8. Signal ground layer (inner layer 3)

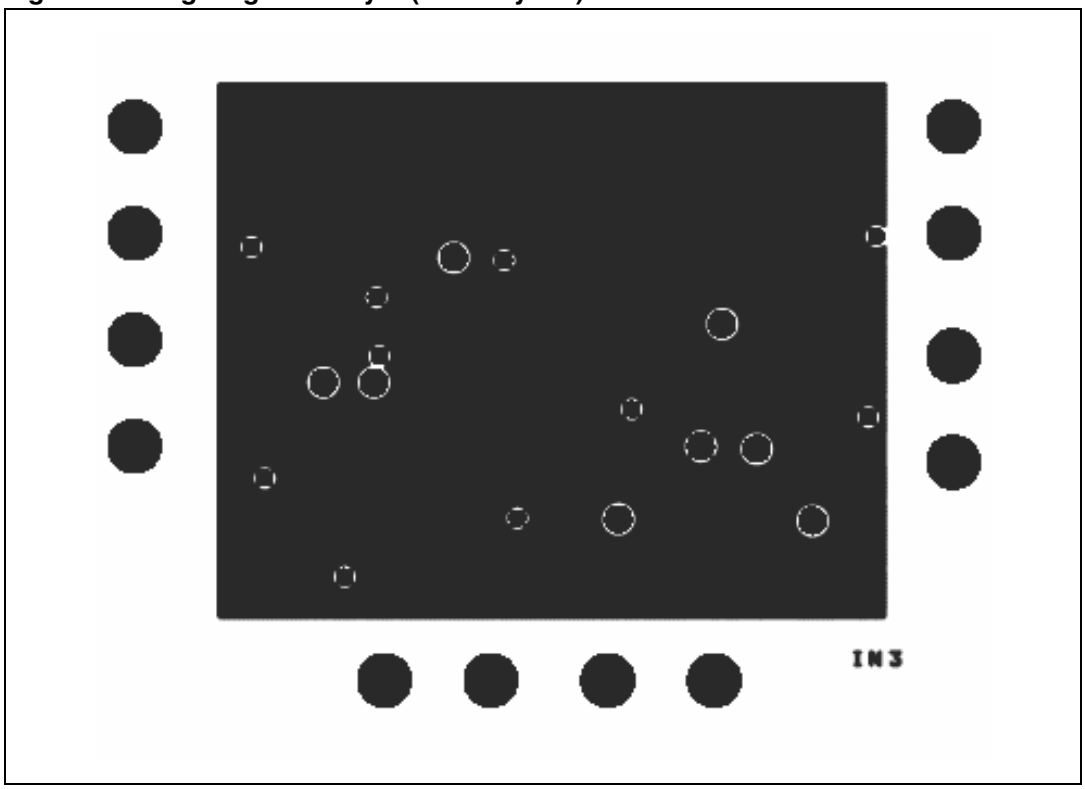


Figure 9. Bottom layer components placement (mirrored)

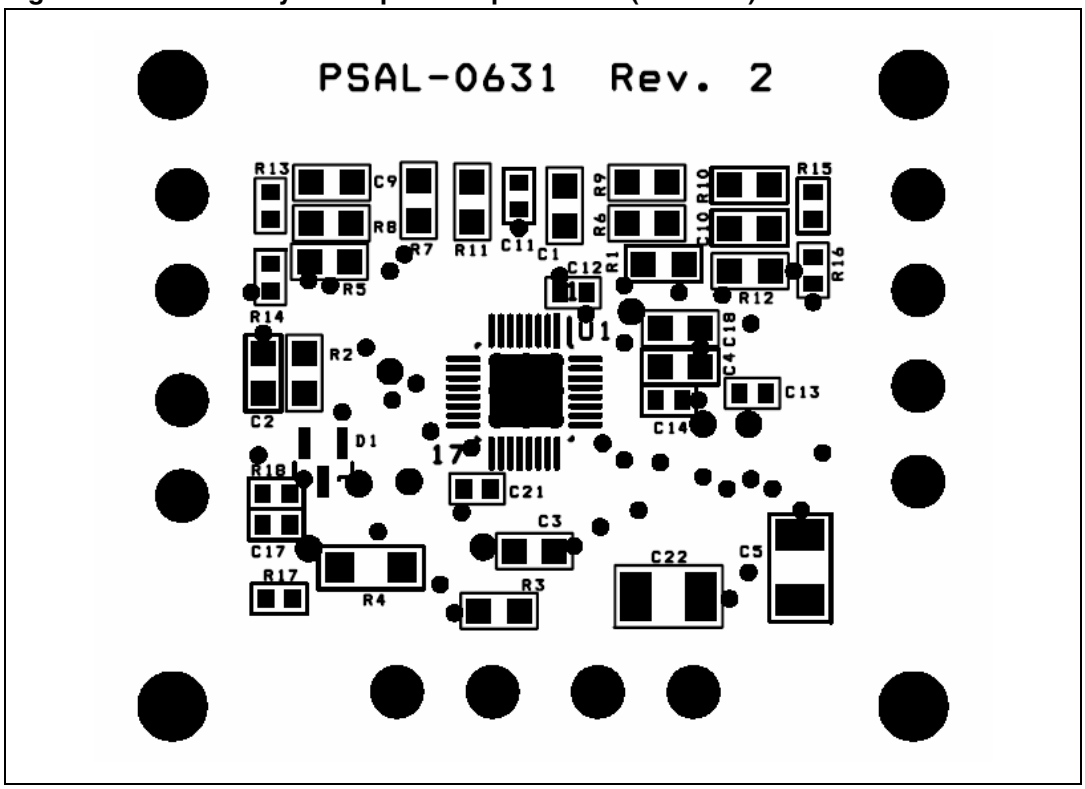


Figure 10. Bottom layer copper (mirrored)

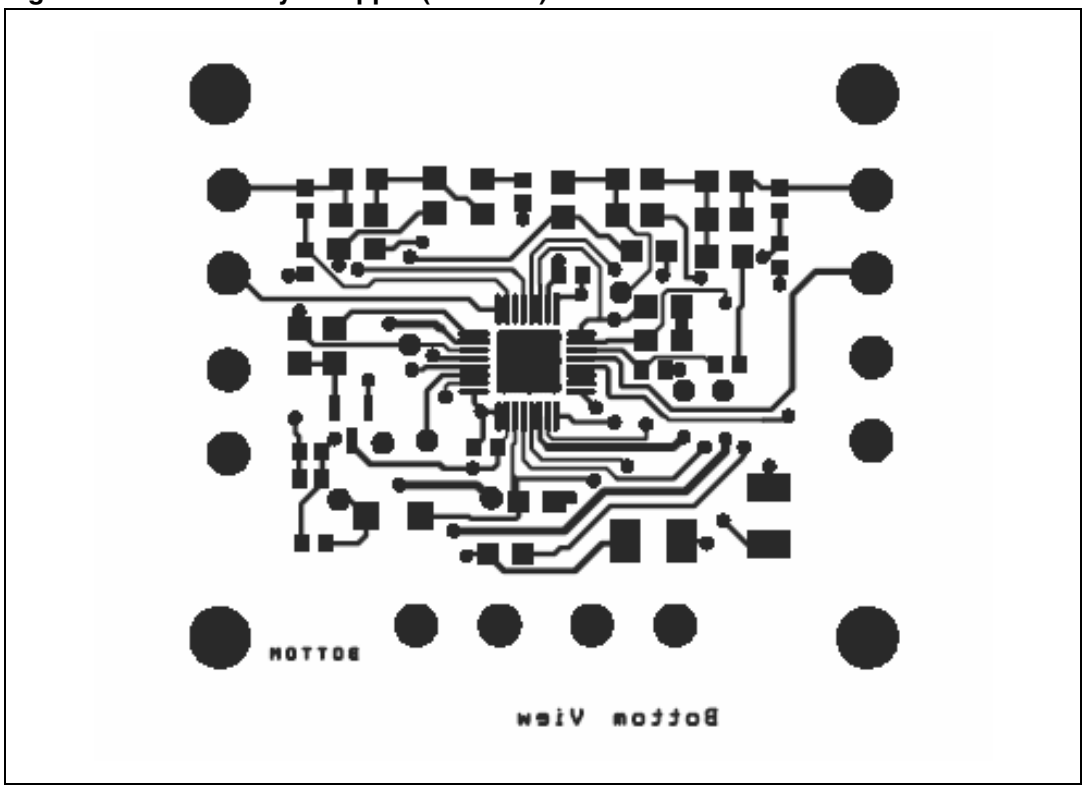
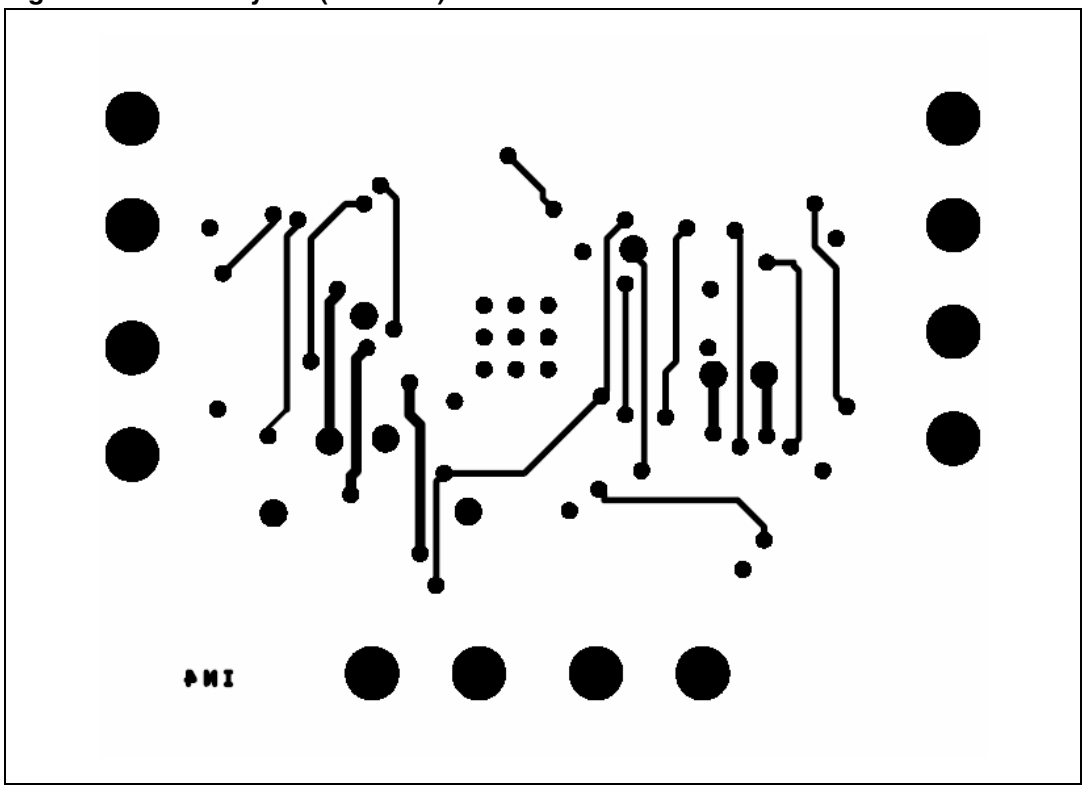


Figure 11. Inner layer 4 (mirrored)



4 Functional testing

Using the component values calculated the demonstration board's efficiency was evaluated. Each converter was tested individually with the idle converter disabled by grounding its enable pin so that the power consumed by the idle converter's MOSFET driver section would not be included in the input power calculation. The efficiency of each section was measured in two different modes of operation, normal PWM and no-audible skip mode. In all cases the input voltage was set to 12.0 V_{DC}.

Figure 12. Efficiency vs. load current in PWM mode (1.0 V)

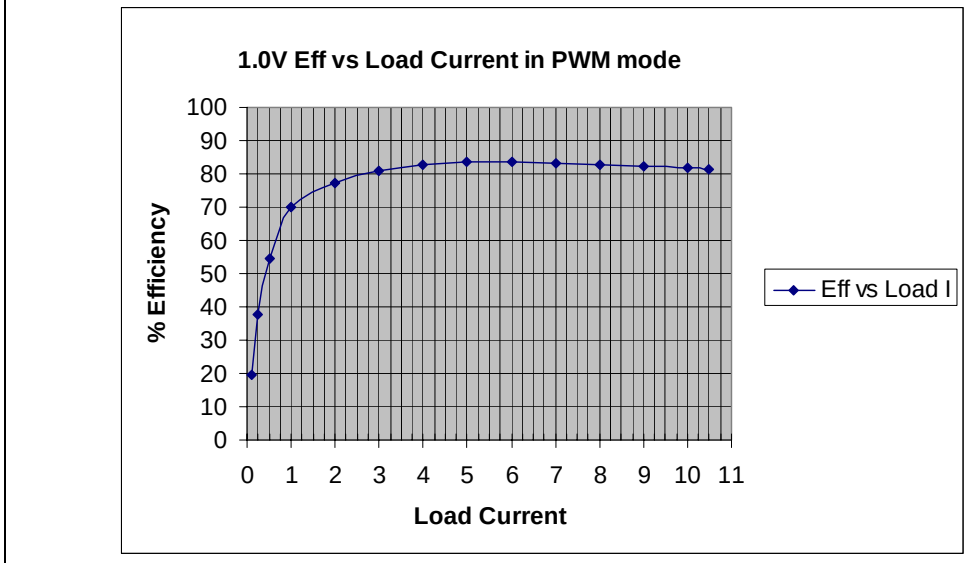
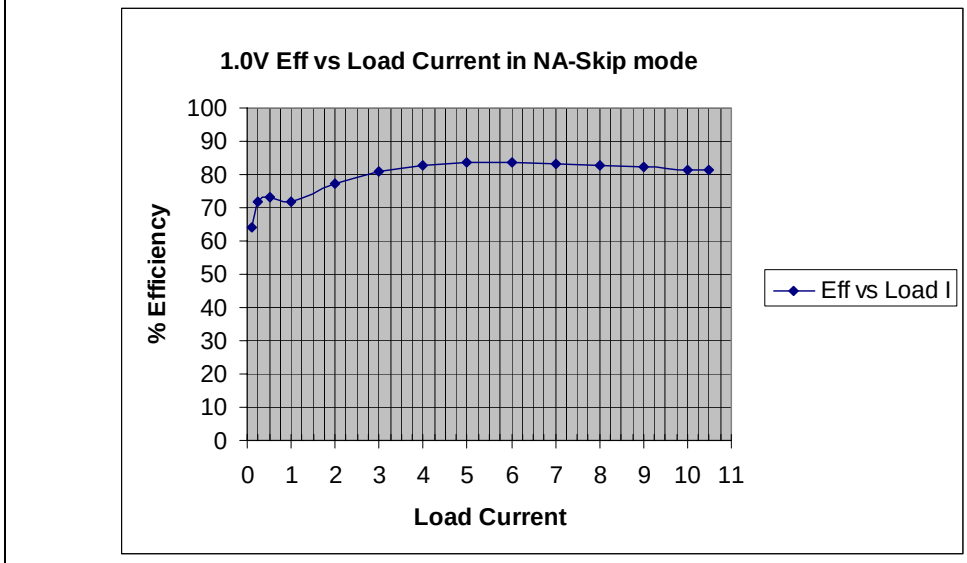


Figure 13. Efficiency vs. load current in NA-skip mode (1.0 V)



As can be seen at significant load current the efficiency for the 1.0 V output averages in the lower eighty percent area. Additionally, the graph for no-audible skip mode shows the advantage of running in this mode. By using the current zero-crossing detector the condition of negative current that occurs at light load is sensed. The control circuit then keeps the average current equal to the load current by skipping cycles. The result is higher efficiency at light load. As the load is increased and the inductor current does not go to zero, normal PWM operation is resumed.

Figure 14. Efficiency vs. load current in PWM mode (1.8 V)

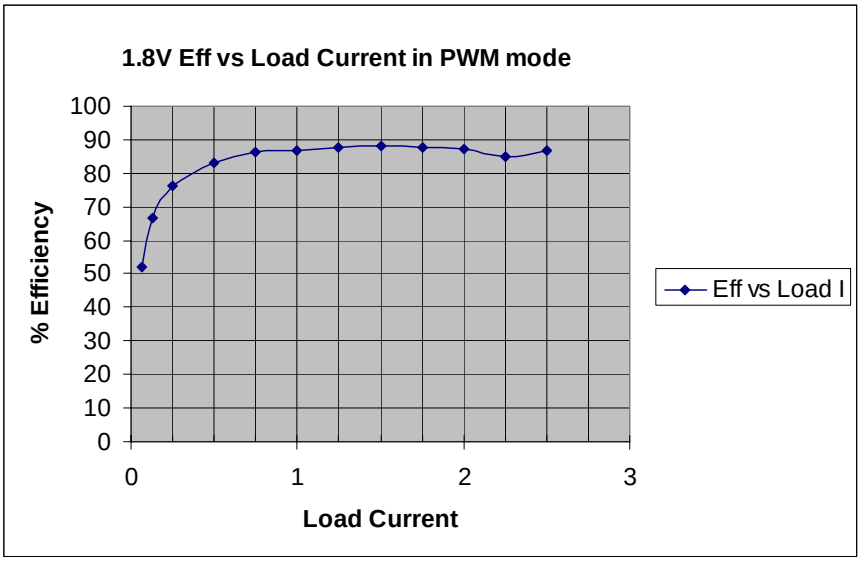
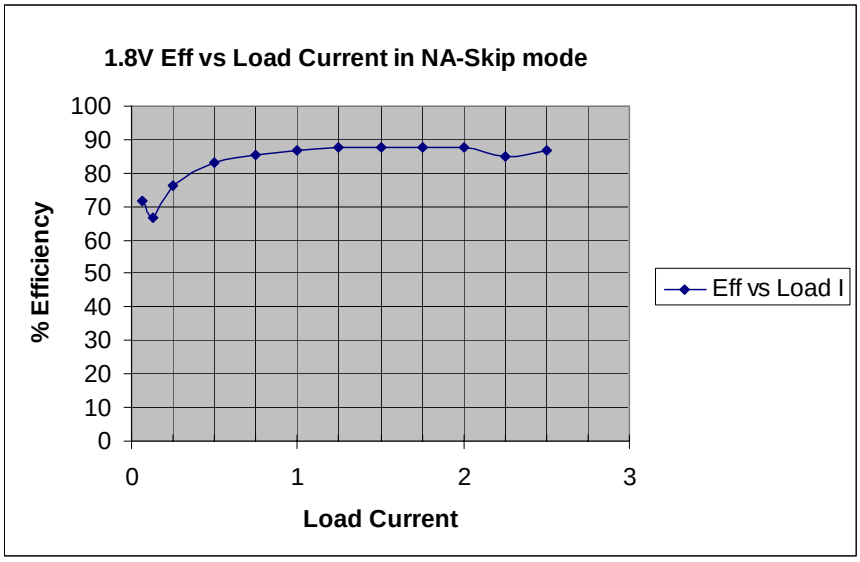


Figure 15. Efficiency vs. load current in NA-skip mode (1.8 V)



The graphs in *Figure 14* and *15* show that the 1.8 V output has better efficiency than the 1.0 V output, in the high eighties at high current levels. Along with the efficiency measurements further functional testing was conducted as outlined in the following sections.

4.1 Input/output voltage

The input voltage was swept from 10.2 to 16 V_{DC} at the load levels indicated. The output voltage was recorded at each level and did not vary more than 1 mV over the entire input range. Input/output voltage at different load levels.

Table 2. 1.0 V_{DC} output

Load current	Output voltage
50 mA	0.998 V_{DC}
7.5 A	1.019 V_{DC}
10.5 A	1.027 V_{DC}

Table 3. 1.8 V_{DC} output

Load current	Output voltage
50 mA	1.792 V_{DC}
1.8 A	1.794 V_{DC}
2.5 A	1.794 V_{DC}

4.2 Ripple/noise voltage

The maximum peak to peak ripple voltage was measured at the load level indicated.

Table 4. 1.0 V_{DC} output

Load current	Ripple voltage p-p
10.5 A	25 mV

Table 5. 1.8 V_{DC} output

Load current	Ripple voltage p-p
2.5 A	20 mV

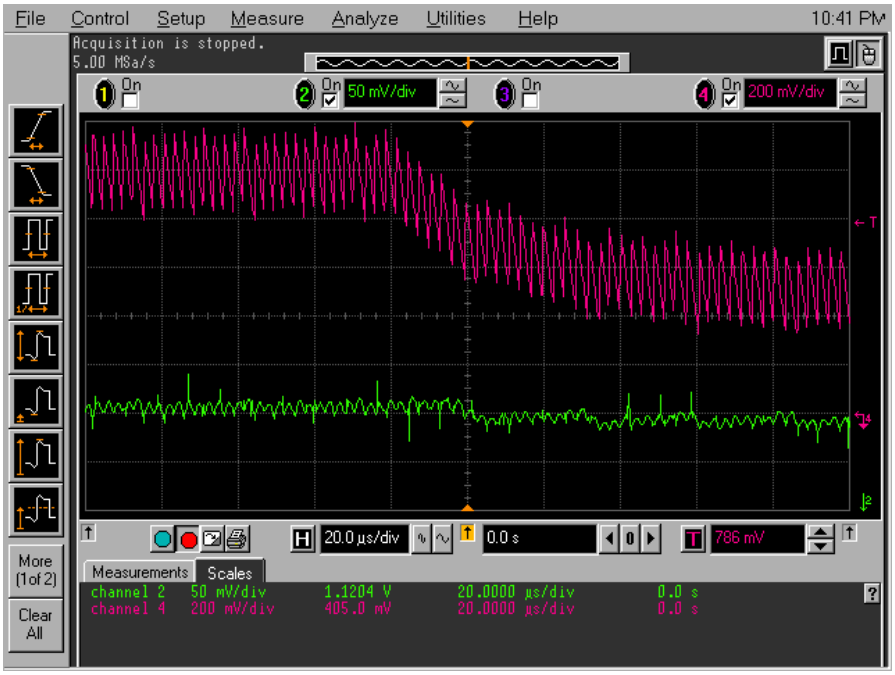
4.3 Load transient overshoot

The output load levels were varied in a stepwise fashion at the percentage and load levels indicated. The maximum change in output voltage was recorded in the following oscilloscope photographs.

Table 6. 1.0 V_{DC} output

Percent load change	Current level change (A)
100 to 50%	5.25 to 10.5
50 to 100%	5.25 to 10.5
20 to 80%	2.0 to 8.5

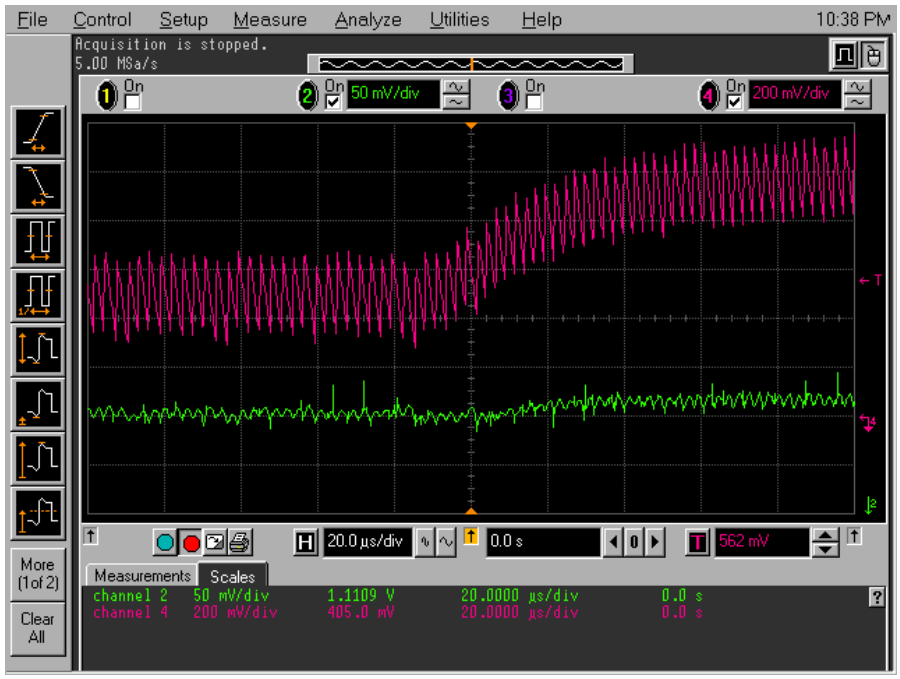
Figure 16. V_{DC} output - 100% to 50% load change (20µs/div)



where:

- Top trace - L1 current 2 A/division
- Bottom trace - output voltage 50 mV/division

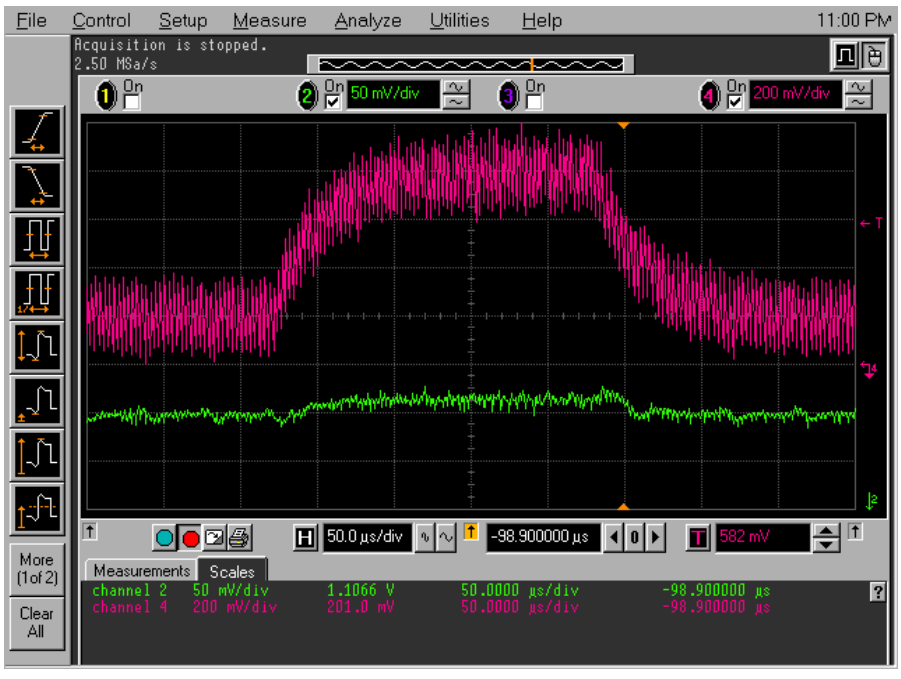
Figure 17. V_{DC} output - 50% to 100% load change (20µs/div)



where:

- Top trace - L1 current 2 A/division
- Bottom trace - output voltage 50 mV/division

Figure 18. V_{DC} output - 20% to 80% step load change (50µs/div)



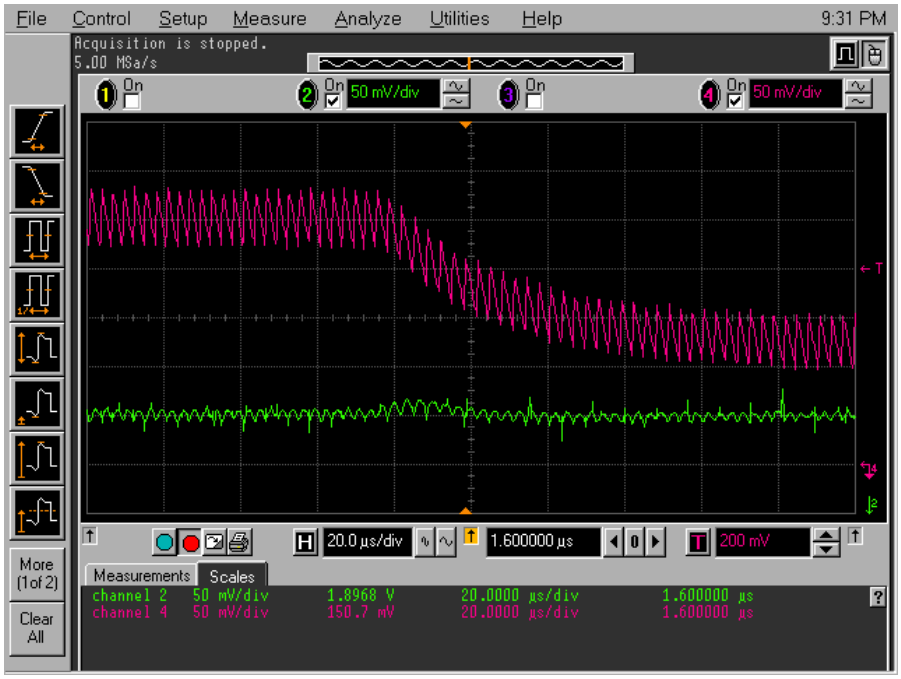
where:

- Top trace - L1 current 2 A/division
- Bottom trace - output voltage 50 mV/division

Table 7. 1.8 V_{DC} output

Percent load change	Current level change (A)
100 to 50%	2.5 to 1.25
50 to 100%	1.25 to 2.5
20 to 80%	0.5 to 2

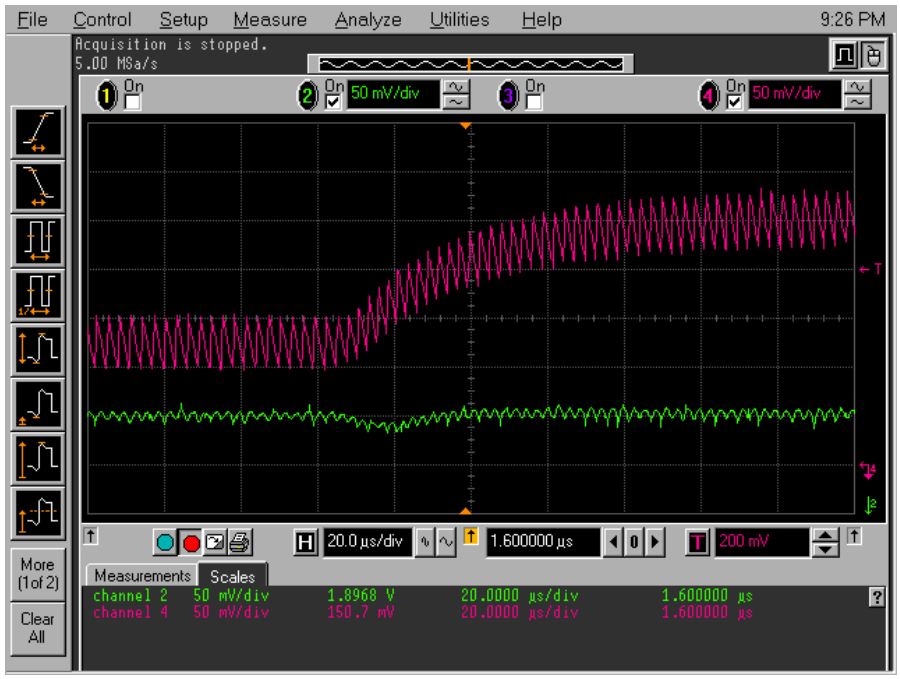
Figure 19. V_{DC} output - 100% to 50% load change (20µs/div)



where:

- Top trace - L1 current 0.5 A/division
- Bottom trace - output voltage 50 mV/division

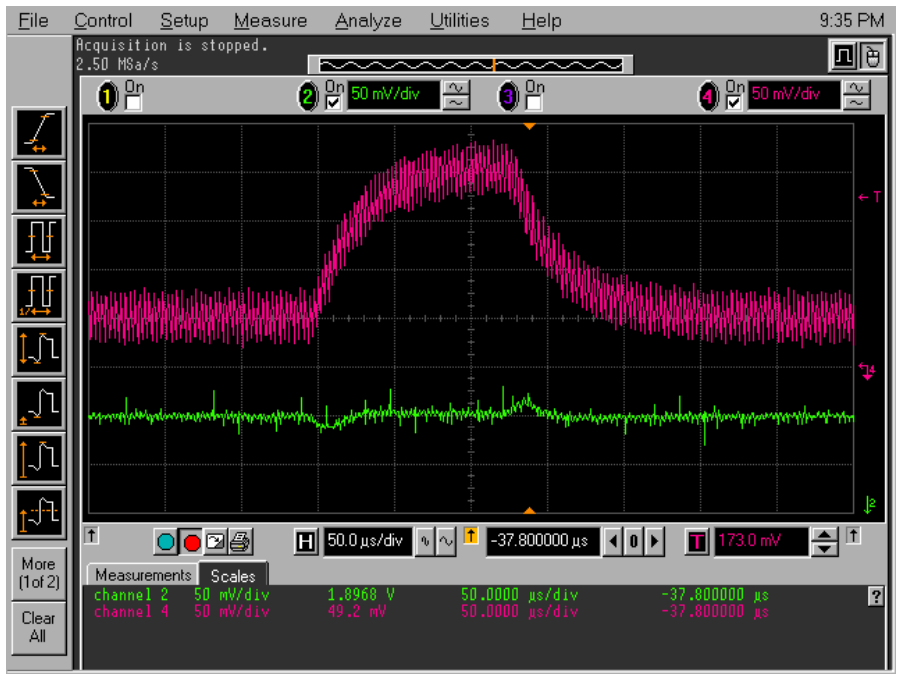
Figure 20. V_{DC} output - 50% to 100% load change (20µs/div)



where:

- Top trace - L1 current 0.5 A/division
- Bottom trace - output voltage 50 mV/division

Figure 21. V_{DC} output - 20% to 80% step load change (50µs/div)



where:

- Top trace - L1 current 0.5 A/division
- Bottom trace - output voltage 50 mV/division

4.4 Output current limit

Each output was loaded to its maximum rated load level. The load was increased in 10% increments of the maximum rated load until the overcurrent limiting functioned. The level was recorded.

Table 8. 1.0 V_{DC} output

Percent of maximum load (A)
130% (13.65)

Table 9. 1.8 V_{DC} output

Percent of maximum load (A)
130% (3.25)

After the overcurrent limit functioned, the load level was adjusted back the maximum rated level and the input power was shut off and reapplied. The outputs resumed to normal operation.

4.5 Output short circuit

Each output in turn was loaded to its maximum rated load level. A short was then applied to the output at which time the overcurrent protection functioned. The opposite output remained running. The short was then removed and the output remained latched off. The input power was removed and then reapplied. The output resumed normal function. With input power removed, each output in turn was shorted. Then input power was applied. The shorted output's current limiting function operated while the non-shorted output ran normally. The short was then removed and the input power was recycled. The output resumed normal function.

4.6 Input under voltage lockout

With each output loaded to its nominal load level the input voltage was slowly increased from 0 to 6 V_{DC} and the output voltages were recorded. The input voltage was then slowly increased from 6 to 8 V_{DC} and the output voltages were recorded. The voltage at which the device turns on is adjusted by the voltage divider consisting of R17 and R18 connected to the SHDN pin(5). The typical turn-on threshold is 1.35 V_{DC} and the device typically shuts down with 0.85 V_{DC} on the pin.

Table 10. 1.0 V_{DC} output

Voltage at V_{in} 6 V_{DC}	Voltage at V_{in} 8 V_{DC}
0.0	1.017

Table 11. 1.8 V_{DC} output

Voltage at V_{in} 6 V_{DC}	Voltage at V_{in} 8 V_{DC}
0.0	1.795

5 Bill of material

Table 12. Part list

Part reference	Value / type	PCB footprint	Manufacturer	P/N
C1	0.1 µF 50 V X5R	SM_0805	Any	
C2	0.1 µF 50 V X5R	SM_0805	Any	
C3	0.1 µF 50 V X5R	SM_0805	Any	
C4	0.22 µF 25 V X5R	SM_0805	Any	
C5	4.7 µF 25 V X5R	SM_1210	Any	
C6	10 µF 25 V X5R	SM_1206	Any	
C7	10 µF 25 V X5R	SM_1206	Any	
C8	10 µF 25 V X5R	SM_1206	Any	
C9	1.8 nF 50 V X5R	SM_0805	Any	
C10	1.8 nF 50 V X5R	SM_0805	Any	
C11	330 pF 50 V NPO	SM_0603	Any	
C12	22 pF 50 V NPO	SM_0603	Any	
C13	330 pF 50 V NPO	SM_0603	Any	
C14	22 pF 50 V NPO	SM_0603	Any	
C15	100 µF 6.3 V X5R	SM_1210	TDK or equivalent	C3225X5ROJ107K
C16	47 µF 6.3 V X5R	SM_1206	TDK or equivalent	C3216X5ROJ476K
C17	100 pF 50 V NPO	SM_0603	Any	
C18	0.1 µF 50 V X5R	SM_0805	Any	
C19	100 µF 6.3 V X5R	SM_1210	TDK or equivalent	C3225X5ROJ107K
C20	47 µF 6.3 V X5R	SM_1206	TDK or equivalent	C3216X5ROJ476K
C21	4.7 µF 25 V X5R	SM_1210	Any	
C22	1 µF 16 V X5R	SM_0603	Any	
D1	BAT54A dual Schottky	SOT-23	STMicroelectronics	BAT54A
D2	Open	DO-214AC		
D3	Open	DO-214AC		
L1	0.7 µH 17 A	Custom	Coilcraft	MLC1265-701MLB
L2	7.0 µH 4.35 A	Custom	Coilcraft	MSS1038-702NLB
Q1	STS12NH3LL MOSFET	SO-8	STMicroelectronics	STS12NH3LL
Q2	STS25NH3LL MOSFET	SO-8	STMicroelectronics	STS25NH3LL

Table 12. Part list (continued)

Part reference	Value / type	PCB footprint	Manufacturer	P/N
Q3	STS8DNF3LL dual MOSFET	SO-8	STMicroelectronics	STS8DNF3LL
R1	10R0 1%	SM_0805	Any	
R2	10R0 1%	SM_0805	Any	
R3	47R5 1%	SM_0805	Any	
R4	3R92 1%	SM_1206	Any	
R5	750R 1%	SM_0805	Any	
R6	750R 1%	SM_0805	Any	
R7	21.6k 1%	SM_0805	Any	
R8	5.11k 1%	SM_0805	Any	
R9	57.6k 1%	SM_0805	Any	
R10	3.74k 1%	SM_0805	Any	
R11	1.91k 1%	SM_0805	Any	
R12	2.55k 1%	SM_0805	Any	
R13	1.10k 1%	SM_0603	Any	
R14	10.0k 1%	SM_0603	Any	
R15	10.0k 1%	SM_0603	Any	
R16	10.0k 1%	SM_0603	Any	
R17	110k 1%	SM_0603	Any	
R18	30.0k 1%	SM_0603	Any	
U1	PM6680 Dual Dc-Dc Controller	VFQFPN-32 5x5	STMicroelectronics	PM6680

6 Revision history

Table 13. Document revision history

Date	Revision	Changes
15-Apr-2008	1	Initial release.