AN2556
Application note

Porting an application from the ST10F269Zx to the ST10F273Z4

Introduction

The ST10F273Z4 is a derivative of the STMicroelectronics ST10 family of 16-bit single-chip CMOS microcontrollers and is functionally upwardly compatible with the ST10F269Zx.

The goal of this document is to highlight the differences between the ST10F269Zx and the ST10F273Z4 devices. It is intended for hardware or software designers who are adapting an existing application based on the ST10F269Zx to the ST10F273Z4.

This document first presents the modified functionalities of the ST10F273Z4, and then presents the new functionalities before looking at the modified and the new registers. In each section of the document, differences with the ST10F269Zx that may have an impact are stressed and some advice is given on how best to handle these differences and impacts.

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1 Modified features

1.1 Pinout

1.1.1 Pinout modification summary

Table 1 below summarizes the modifications made in the pinout.

Table 1. Pinout modifications table

Pin No.	ST10F269Zx		ST10F273Z4	
	Name	Function	Name	Function
17	DC2	Internal voltage regulator decoupling. Connect to nearest V_{SS} via a 330nF capacitor.	V_{DD}	5V power supply pin
56	DC1	Internal voltage regulator decoupling. Connect to nearest V_{SS} via a 330nF capacitor.	V_{18}	Internal voltage regulator decoupling. Connect to nearest V_{SS} via a 10 - 100nF capacitor.
99	$\overline{EA}$	Selects code execution out of internal Flash or external memory according to level during reset	$\overline{EA}$-V_{STBY}	Selects code execution out of internal Flash or external memory according to level during reset. Power supply input for standby mode.
143	V_{SS}	Ground pin	XTAL3	Input to the 32 kHz oscillator amplifier circuit. If not used should be tied to ground to avoid consumption. In addition, bit OFF32 in RTCCON register should be set.
144	V_{DD}	5V power supply pin	XTAL4	Output of the 32 kHz oscillator amplifier circuit. If not used should be left open to avoid spurious consumption.

1.1.2 Pin 17

In the ST10F269Zx, a decoupling capacitor of 330nF minimum has to be connected between pin 17 (named DC2) and the nearest V_{SS} pin.

This is no longer the case in the ST10F273Z4 device where pin 17 is a V_{DD} pin.

Hardware impacts

PCB must be adapted.

Software impacts

None.

1.1.3 Pin 56

In the ST10F269Zx, a decoupling capacitor of 330nF minimum has to be connected between pin 56 (named DC1) and the nearest V_{SS} pin.

In the ST10F273Z4, pin 56 is named V_{18} and a capacitor with a value between 10nF minimum and 100nF maximum must be connected between it and the nearest V_{SS} pin.

Hardware impacts

The capacitor value may need to be changed. As the value is much lower, the footprint of the capacitor might be smaller and thus a modification of the PCB may be needed.

Software impacts

None.

1.1.4 Pin 99

In the ST10F269Zx, pin 99 is named $\overline{EA}$ and when it is reset it is used to select the start from internal Flash or external memory.

Pin 99 now has an additional function in the ST10F273Z4 which is to provide the 5V power supply to the device in standby mode (new power saving mode). It is therefore named $\overline{EA}$-V_{STBY}.

Hardware impacts

Modification depends on the previous use of the ST10F269Zx and on the use or non-use of Standby mode.

For an application that does not use Standby mode, no change is required on the PCB. If the new application uses the Standby mode, the $\overline{EA}$-V_{STBY} pin must be separated from the common 5V and have a specific supply path.

Software impacts

None.

1.1.5 Pins 143 and 144

These pins are a V_{SS}-V_{DD} pair in the ST10F269Zx. In the ST10F273Z4, they are now used as an XTAL3-XTAL4 pair for connection to an optional 32 kHz crystal to clock the Real Time Clock during Power-Down.

Hardware impacts

The PCB must be redesigned.

In case the optional 32 kHz is not used:

- XTAL3 must be linked to Ground as was previously the case for ST10F269Zx.
- XTAL4 can be left open or it may be connected to Ground via a capacitor to reduce the potential effect of RF noise which could be propagated inside the device if it is left floating.

Software impacts

If the optional 32 kHz is not used, but the RTC is used, bit OFF32 of the RTCCON register should be set. Prior to setting the OFF32 bit in RTCCON register, the RTC must be enabled by setting RTCEN, bit 4 of XPERCON, and XPEN, bit 2 of SYSCON.

1.2 XRAM

The XRAM of the ST10F269Zx and ST10F273Z4 devices is not the same size. Each configuration is detailed below.

The ST10F269Zx has 10 Kbytes of extension RAM whereas the ST10F273Z4 has 34 Kbytes.

The XRAM of the ST10F269Zx is divided into two ranges, namely, XRAM1 with 2 Kbytes and XRAM2 with 8 Kbytes:

- The **XRAM1** address range is 00'E000h - 00'E7FFh if enabled.
- The **XRAM2** address range is 00'C000h - 00'DFFFh if enabled.

The XRAM of the ST10F273Z4 is divided into two ranges, namely, XRAM1 with 2 Kbytes (compatible with the ST10F269Zx) and XRAM2 with 32 Kbytes (which has a user reprogrammable address range):

- The **XRAM1** address range is 00'E000h - 00'E7FFh if enabled (XPEN set - bit 2 of SYSCON register - **AND** XRAM1EN set - bit 2 of XPERCON register).
- The **XRAM2** address range is 0F'0000h - 0F'7FFFh, by default (compatible with ST10F273Z4 superset) if enabled (XPEN set - bit 2 of SYSCON register - **AND** XRAM2EN set - bit 3 of XPERCON register).

1.2.1 Hardware impacts

None.

1.2.2 Software impacts

There is no change when enabling the XRAM blocks: The XPERCON register is still used to enable them via the XRAM1EN and XRAM2EN bits and the XPEN bit of SYSCON.

In the ST10 F273Z4 the memory mapping of the application is impacted by the difference in XRAM size and by the location of XRAM2 in segment 15. In the ST10F269Zx the whole XRAM is in page 3 of segment 0.

Variables and PEC transfers

For architectural reasons, the PEC destination and source pointers must be in segment 0. Therefore all RAM variables and arrays that will be PEC addressed must be located within either the DPRAM (00'F600h - 00'FDFFh) or the XRAM1 (00'E000h - 00'E7FFh).

About Toolchain memory model

A change in the Toolchain configuration is needed to take into account the new location of XRAM2. In the ST10F269Zx, all the XRAM is in page 3 which is then automatically addressed using DPP3 that points to page 3 (in order to access the DPRAM and the SFR/ESFR). In the ST10F273Z4, it is necessary to dedicate a DPP to access some of the XRAM2.

Example in case of Small Memory Model with Tasking toolchain:

The Small Memory Model allows a total code size from 16 Mbytes up to 64 Kbytes of fast accessible 'normal user data' in three different memory configurations with the possibility to access more data, if more than 64 Kbytes of data is needed.

The three memory configurations possible for this 64K of 'normal user data' are:

- Default

  Four DPP registers are assumed to contain their system startup value (0-3), providing one linear data area of 64 Kbytes in the first segment (00'0000h - 00'FFFFh).

- Linear Address

  DPP3 contains page number 3, allowing access to SYSTEM (extended) SFR registers and a bit-addressable memory. DPP0 - DPP2 provides a linear data area of 48 Kbytes anywhere in the memory.

- Paged

  DPP3 contains page number 3, allowing access to SYSTEM (extended) SFR registers and a bit-addressable memory. DPP0, DPP1 and DPP2 contain a page number of a data area of 16 Kbytes anywhere in the memory.

The Default configuration can no longer be used. The other configurations offer the following possibilities:

- Using Linear Address configuration, nearly all the XRAM2 block is covered with DPPs but then access to constants must be made via EXTP instructions.
- Paged configuration allows the user to assign up to two DPPs to XRAM2 and one DPP for constants.

1.3 Flash EEPROM

Table 2. Flash memories key characteristics

Characteristic	ST10F269Zx	ST10F273Z4
Flash size	256 Kbytes	512 Kbytes
Flash organization	7 blocks	10 blocks
Programming voltage	5 volts	5 volts
Programming method	Write/Erase Controller	Write/Erase Controller
Program/Erase cycles	100000	100000

Table 3: Flash memories mapping on page 9 shows the differences between the ST10F273Z4 and the ST10F269Zx.

1.3.1 Hardware impacts

None.

1.3.2 Software impacts

Mapping of the applications is impacted because in the ST10F273Z4 the first 32 Kbytes of Flash are divided into four sectors of 8 Kbytes each, whereas the ST10F269Zx has only three sectors.

Moreover, the Flash Write/Erase controller is different and therefore the programming routines must be updated.

When the XPEN bit of the SYSCON register and the XRAM2EN bit of XPERCON register are set, access to the address range 09'0000h - 0D'FFFFh is not redirected to the external memory. The linker-locator configuration of the toolchain should be checked in order to prevent use of this memory range.

Note: This range can be redirected to the external memory by changing the value of the register XADRS3. Refer to Section 4.1: XADRS3 register for more details.

Table 3. Flash memories mapping

Segment number	ST10F269Zx Flash mapping		ST10F273Z4 Flash mapping	
14	0E'0000 - 0E'FFFF	External memory	0E'0000 - 0E'FFFF	Flash registers
13	05'0000 - 0D'FFFF		09'0000 - 0D'FFFF	Reserved
12				
11				
10				
9				
8			08'0000 - 08'FFFF	IBank 1, Block 1: 64 Kbytes
7			07'0000 - 07'FFFF	IBank 1, Block 0: 64 Kbytes
6			06'0000 - 06'FFFF	IBank 0, Block 9: 64 Kbytes
5			05'0000 - 05'FFFF	IBank 0, Block 8: 64 Kbytes
4	04'0000 - 04'FFFF	Block 6: 64 Kbytes	04'0000 - 04'FFFF	IBank 0, Block 7: 64 Kbytes
3	03'0000 - 03'FFFF	Block 5: 64 Kbytes	03'0000 - 03'FFFF	IBank 0, Block 6: 64 Kbytes
2	02'0000 - 02'FFFF	Block 4: 64 Kbytes	02'0000 - 02'FFFF	IBank 0, Block 5: 64 Kbytes
1	01'8000 - 01'FFFF	Block 3: 32 Kbytes	01'8000 - 01'FFFF	IBank 0, Block 4: 32 Kbytes
	01'0000 - 01'7FFF	External memory	01'0000 - 01'7FFF	External memory
0	00'8000 - 00'FFFF	External memory Internal RAM	00'8000 -00'FFFF	External memory Internal RAM
	00'6000 - 00'7FFF	Block 2: 8 Kbytes	00'6000 - 00'7FFF	IBank 0, Block 3: 8 Kbytes
	00'4000 - 00'5FFF	Block 1: 8 Kbytes	00'4000 - 00'5FFF	IBank 0, Block 2: 8 Kbytes
	00'0000 - 00'3FFF	Block 0: 16 Kbytes	00'2000 - 00'3FFF	IBank 0, Block 1: 8 Kbytes
			00'0000 - 00'1FFF	IBank 0, Block 0: 8 Kbytes

1.4 A/D converter

The Analog Digital converter has been redesigned in the ST10F273Z4. The ST10F273Z4 still provides an Analog/Digital converter with 10-bit resolution and a sample & hold circuit on-chip.

1.4.1 Hardware/software impacts: conversion timing control

The A/D Converter is not fully compatible with the ST10F269Zx (timing and programming model). In the ST10F269Zx, the sample time (for loading the capacitors) and the conversion time is programmable and can be adjusted to the external circuitry. The total conversion time is compatible with the formula used for the ST10F269Zx, but the meaning of the field bits ADCTC and ADSTC are no longer compatible

Table 4. ST10F273Z4 conversion timing table

ADCTC	ADSTC	Sample	Comparison	Extra	Total conversion
00	00	TCL * 120	TCL * 240	TCL * 28	TCL * 388
00	01	TCL * 140	TCL * 280	TCL * 16	TCL * 436
00	10	TCL * 200	TCL * 280	TCL * 52	TCL * 532
00	11	TCL * 400	TCL * 280	TCL * 44	TCL * 724
11	00	TCL * 240	TCL * 120	TCL * 52	TCL * 772
11	01	TCL * 280	TCL * 560	TCL * 28	TCL * 868
11	10	TCL * 400	TCL * 560	TCL * 100	TCL * 1060
11	11	TCL * 800	TCL * 560	TCL * 52	TCL * 1444
10	00	TCL * 480	TCL * 960	TCL * 100	TCL * 1540
10	01	TCL * 560	TCL * 1120	TCL * 52	TCL * 1732
10	10	TCL * 800	TCL * 1120	TCL * 196	TCL * 2116
10	11	TCL * 1600	TCL * 1120	TCL * 164	TCL * 2884

The user should take care of the sample time parameter: This is the time where the capacitances of the converter are loaded via the respective analog input pin. *Table 5: ST10F273Z4 vs. ST10F269Zx sample time comparison table* shows the differences in sample time.

Table 5. ST10F273Z4 vs. ST10F269Zx sample time comparison table

ADCTC	ADSTC	ST10F269Zx sample time	ST10F273Z4 sample time	Ratio F273Z4_time / F269_time	ADCTC
00	00	TCL * 48	TCL * 120	2.5	00
00	01	TCL * 96	TCL * 140	1.46	00
00	10	TCL * 192	TCL * 200	1.04	00
00	11	TCL * 384	TCL * 400	1.04	00
11	00	TCL * 96	TCL * 240	2.5	11
11	01	TCL * 192	TCL * 280	1.46	11
11	10	TCL * 384	TCL * 400	1.04	11
11	11	TCL * 768	TCL * 800	1.04	11
10	00	TCL * 192	TCL * 480	2.08	10
10	01	TCL * 384	TCL * 560	1.46	10

Table 5. ST10F273Z4 vs. ST10F269Zx sample time comparison table (continued)

ADCTC	ADSTC	ST10F269Zx sample time	ST10F273Z4 sample time	Ratio F273Z4_time / F269_time	ADCTC
10	10	TCL * 768	TCL * 800	1.04	10
10	11	TCL * 1536	TCL * 1600	1.04	10

In the default configuration, the sample time of the ST10F273Z4 is 2.5 times longer compared to the ST10F269Zx. This has an impact on the frequency of the input signal that can be applied to the ST10F273Z4.

1.4.2 Hardware impacts: electrical characteristics

Table 6: ADC differences lists the differences in the DC characteristics of the two devices.

Table 6. ADC differences

Parameter	Symbol	Limit values for ST10F269Zx		Limit values for ST10F273Z4		Unit
		Min	Max	Min	Max	
Analog reference voltage	V_{AREF} (1)	4.0	V_{DD} + 0.1	4.5	V_{DD}	V
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V_{AGND}	V_{AREF}	V
ADC input capacitance	C_{AIN}				C_{P1} + C_{P2} +C_S	pF
Port5, not sampling		-	10	-	7	
Port5, sampling		-	15	-	10.5	
Port1, not sampling		-	N.A.	-	9	
Port1, sampling		-	N.A.	-	12.5	
Sample time	t_S	48TCL	1536TCL	1µs 120TCL	1600TCL	
Conversion time	t_C	388TCL	2884TCL	388TCL	2884TCL	
Total unadjusted error	TUE					LSB
Port5		-2.0	+2.0	-2.0	+2.0	
Port1 - no overload		-	-	-5.0	+5.0	
Port1 - overload		-	-	-7.0	+7.0	
Internal resistance of analog source	R_{ASRC}		t_S[ns]/150 - 0.25			kΩ
Analog switch resistance	R_{SW}	N.A.	N.A.			Ω
	Port5			-	600	
	Port1			-	1000	
	R_{AD}			-	1300	

Table 6. ADC differences (continued)

Parameter	Symbol	Limit values for ST10F269Zx		Limit values for ST10F273Z4		Unit
		Min	Max	Min	Max	
Reference supply current	I_{AREF}					µA
Running mode		-	500	-	500	
Power-down mode		-	1	-	1	
Differential nonlinearity	DNL	-0.5	+0.5	1	1	LSB
Integral nonlinearity	INL	-1.5	+1.5	-1.5	1.5	LSB
Offset error	OFS	-1.0	+1.0	-1.5	1.5	LSB

1. The V_{AREF} pin is also used as the supply pin of the ADC module. As there is a higher current sink on this pin on the ST10F273Z4 with regard to the ST10F269Zx, avoid using a resistor (for example, because of an RC filter). This creates an offset in the reference.

1.4.3 Software impacts

Self-calibration and ADC initialization routine

An automatic self-calibration adjusts the ADC module to process parameter variations at each reset event. After reset, the busy flag (read-only) ADBSY is set because the self-calibration is ongoing. The duration of self-calibration depends on the CPU clock: It takes up to 40.629 ± 1 clock pulse. The user should poll this bit to know when the self-calibration is done and then initialize the ADC module.

Such self-calibration is seen in the ST10F273Z4 as a conversion and thus the ADCIR bit is set. The software should perform a dummy read of the ADDAT register and clear the ADCIR and ADCEIR flag before configuring the ADC module and starting the first conversion.

ADCON (FFA0h / A0h) **SFR** **Reset value: 0000h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCTC		ADSTC		ADC RQ	ADC IN	AD WR	AD BSY	AD ST	AD OFF	ADM		ADCH			
RW		RW		RW	RW	RW	RO	RW	RW	RW		RW			

Table 7. ADCON register: ADOFF bit

Bit	Function	CommentS
ADOFF	**ADC disable** 0: Analog circuitry of A/D converter is turned on. 1: Analog circuitry of A/D converter is turned off.	New bit valid only for the ST10F273Z4. Reserved for the ST10F269Zx.

Bit 6 of the ADCON register was reserved in previous ST10 devices. It now has the function of enabling or disabling the ADC. By default this bit is cleared and the ST10F273Z4 is compatible with ST10F269Zx. Therefore, there is no impact on the software, provided it is not written to this bit.

Port1 additional channels

A new multiplexer selects between up to 16 + 8 analog input channels (alternate functions of Port 5 and Port1). The selection of Port1 or Port5 as inputs of ADC is made via the ADCMUX bit and bit 0 of XMISC register. By default the multiplexer selects Port5, so there is no impact on the software with regard to ST10F269Zx implementation. Note that XMISCEN and bit 10 of the XPERCON register must be set in order to have access to the XMISC register.

XMISC (EB46h) **XREG** **Reset value: --00h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												VREG OFF	CAN CK2	CAN PAR	ADC MUX
-												RW	RW	RW	RW

Table 8. XMISC register: ADCMUX bit

Bit	Function
ADCMUX	**ADC Multiplexer** 0: Default configuration, analog inputs on ports P5.y can be converted. 1: Analog inputs on port P1.z can be converted, only 8 channels can be managed.

1.5 Real time clock

The RTC module can be clocked by two different sources: The main oscillator (pins XTAL1 and XTAL2) or the 32 kHz low power oscillator (pins XTAL3 and XTAL4). Selection of the clocking can be made via an additional bit in the RTCCON register.

1.5.1 Hardware impacts

Check the usage of pins XTAL3 and XTAL4 (143 and 144 respectively).

1.5.2 Software impacts

The address range of the RTC registers have been modified from 00'EC00h - 00'ECFFh on the ST10F269Zx to 00'EE00h - 00'EEFFh on ST10F273Z4. This relocation has no impact if the software uses register names defined by the toolchain and if the CPU selection is changed to ST10F273Z4. If the software was using the address of the RTC register directly, it must be modified according to new mapping.

In the ST10F269Zx, both byte and word accesses were allowed for the RTC module. In the ST10F273Z4, only word accesses are possible.

Check that the code is not creating byte accesses to the RTC module.

In addition, new bits(OFF32, OSC) have been added into the RTCCON register. There is no impact if the code was not writing to the upper part of the RTCCON register which was reserved.

The handling of the RTCAIR and RTCSIR flags (bit 2 and 0 of RTCCON register respectively) is also changed:

In the ST10F273Z4 these flags are cleared by writing them to 1.

In the ST10F269Zx these flags are cleared by writing them to 0.

As these flags must be cleared by software when entering the corresponding interrupt service routine, a change in the application code is needed.

Example for RTCSIR flag

Replace the ST10F269Zx code:

```
RTCCON &= 0xFFFE;// Clear RTCSIR flag
```

by the following code for ST10F273Z4:

```
RTCCON |= 0x0001;// Write 1 into RTCSIR flag to clear it
```

ST10F269Zx: RTCCON (F1C4h/E2h) **ESFR** **Reset value: --00h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RTC OFF	Reserved			RTC AEN	RTC AIR	RTC SEN	RTC SIR
-								RW	-			RW	RW	RW	RW

ST10F273Z4: RTCCON (F1C4h/E2h) **ESFR** **Reset value: 0000h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						OFF 32	OSC	RTC OFF	Reserved			RTC AEN	RTC AIR	RTC SEN	RTC SIR
-						RW	RO	RW	-			RW	RW	RW	RW

Table 9. RTCCON register bits

Bit	Function	Reset value
RTCSIR	**RTC Second Interrupt Request flag (every basic clock unit)** 0: The bit is reset less than a Basic Clock unit ago. 1: Interrupt is triggered.	0
RTCSEN	**RTC Second interrupt Enable** 0: RTC_SecIT is disabled. 1: RTC_SecIT is enabled, it is generated every basic clock unit.	0
RTCAIR	**RTC Alarm Interrupt Request flag (when the alarm is triggered)** 0: The bit is reset less than a Basic Clock unit ago. 1: Interrupt is triggered.	0
RTCAEN	**RTC Alarm Interrupt Enable** 0: RTC_alarmIT is disabled. 1: RTC_alarmIT is enabled.	0
RTCOFF	**RTC Switch Off bit** 0: Clock oscillator and RTC run during Power Down mode. 1: Clock oscillator is switched off during Power Down mode; RTC dividers and counters are stopped and registers can be written.	0

Table 9. RTCCON register bits

Bit	Function	Reset value
OSC	**Oscillator Selection flag** 0: The clock oscillator used by the RTC is the main oscillator. 1: The clock oscillator used by the RTC is the low power 32 kHz oscillator.	0
OFF32	**32 kHz Oscillator Switch Off bit** 0: The 32 kHz oscillator is enabled. The RTC is clocked with 32 kHz if there is a valid signal. 1: The 32 kHz oscillator is disabled. The RTC is clocked by the main oscillator.	0

1.6 CAN modules

ST10F269Zx has two CAN modules of the B-CAN type.

ST10F273Z4 has two CAN modules of the C-CAN type. These modules are functionally compatible with the modules of the ST10F269Zx.

The C-CAN cells provide additional Message Objects and new functionalities like Time Triggered Protocol capability. The main difference is that the Message Objects are no longer directly accessed as memory but are available through a Message Interface. This changes the programming model of the modules.

1.6.1 Hardware impacts

None.

1.6.2 Software impacts

Rewrite the CAN drivers.

1.7 Ports input control

In ST10F269Zx, the Port Input Control register PICON is used to select between TTL and CMOS-like input thresholds. The CMOS-like input thresholds are defined above the TTL levels and feature a hysteresis of 250mV to prevent the inputs from toggling while the respective input signal levels are near the thresholds. This feature is available for all pins of Port 2, Port 3, Port4, Port 7 and Port 8.

In ST10F273Z4, Port 6 has been added. In addition the default hysteresis is now 500mV for TTL levels and 800mV for CMOS levels.

ST10F269Zx: PICON (F1C4h/E2h) **ESFR** **Reset value: --00h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								P8 LIN	P7 LIN	Res	P4 LIN	P3 HIN	P3 LIN	P2 HIN	P2 LIN
-								RW	RW	-	RW	RW	RW	RW	RW

ST10F273Z4: PICON (F1C4h/E2h) ESFR Reset value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								P8 LIN	P7 LIN	P6 LIN	P4 LIN	P3 HIN	P3 LIN	P2 HIN	P2 LIN
-								RW	RW	RW	RW	RW	RW	RW	RW

Table 10. PICON register bits

Bit	Function	Reset value
PxLIN	**Port x Low Byte Input Level Selection** 0: Pins Px.7-0 switch on standard TTL input levels. 1: Pins Px.7-0 switch on CMOS input levels.	0
PxHIN	**Port x High Byte Input Level Selection** 0: Pins Px.15-8 switch on standard TTL input levels. 1: Pins Px.15-8 switch on CMOS input levels.	0

1.7.1 Hardware impacts

None.

1.7.2 Software impacts

None, if the software is not written to PICON bit 5 (P6LIN).

1.8 Ports output control

In ST10F269Zx the Port Output Control register, POCONx, allows selection of the port output driver characteristics of a port. The aim of these selections is to adapt the output drivers to the application's requirements, and eventually to improve the EMI behavior of the device. Two characteristics may be selected:

- **Edge characteristic** defines the rise/fall time for the respective output, that is, the transition time. Slow edge reduces the peak currents that are sunk/sourced when changing the voltage level of an external capacitive load.
- **Driver characteristic** defines either the general driving capability of the respective driver, or if the driver strength is reduced after the target output level has been reached or not. Reducing the driver strength increases the output's internal resistance, which attenuates noise that is imported via the output line.

This feature is not available for ST10F273Z4.

1.8.1 Hardware impacts

Some modifications might be needed depending on the use of this functionality.

1.8.2 Software impacts

Parts related to the initialization of the POCONx registers should be suppressed.

1.9 PLL and on-chip main oscillator

Compared to the ST10F269Zx, several modifications have been introduced:

- PLL multiplication factors have been adapted in order to match the new frequency range.
- On-chip main oscillator input frequency range has been reshaped, reducing it to 4 to12 MHz. This allows a power consumption reduction when the Real Time Clock is running in Power Down mode using as a reference the on-chip main oscillator clock.
- When the PLL is used, the CPU frequency range is 16 to 64 MHz.

Figure 1.: ST10F273Z4 clock generation diagram gives a simplified overview of the CPU clock generation. Values will be set for each stage depending on the multiplication factor selected via Port0 at reset. The CPU clock is in fact generated mainly from a VCO with the following characteristics:

- Input range: 1 to 3.5 MHz, which explains the Prescaler that divides the XTAL frequency
- Output range: 64 to 128 MHz which is then divided through Divider1 to generate the CPU clock

Figure 1. ST10F273Z4 clock generation diagram

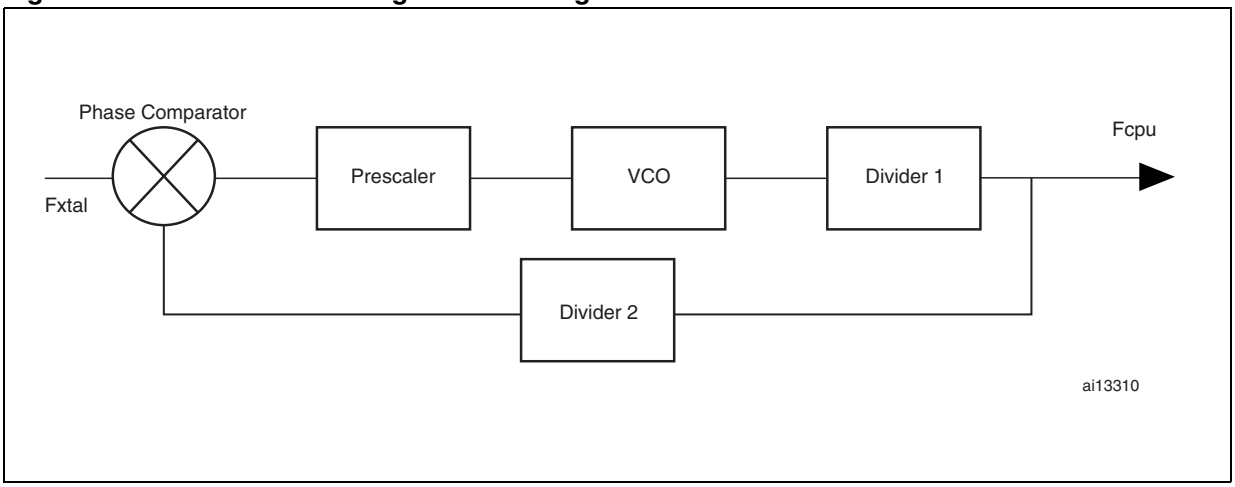


Table 11.: ST10F269Zx vs. ST10F273Z4 PLL ratio lists the new PLL multiplications factors and the corresponding frequency ranges for the ST10F273Z4.

Table 11. ST10F269Zx vs. ST10F273Z4 PLL ratio(1)

P0.15-13 (P0H.7-5)			PLL multiplication factor		ST10F273Z4 oscillator	
			ST10F269Zx	ST10F273Z4	Input range (MHz)	CPU clock range (MHz)
1	1	1	* 4	* 4	4 to 8	16 to 32
1	1	0	* 3	* 3	5.34 to 10.66	16.02 to 32
1	0	1	* 2	* 8	4 to 8	32 to 64
1	0	0	* 5	* 5	6.4 to 12	32 to 60
0	1	1	* 1	* 1	1 to 64	10 to 64

Table 11. ST10F269Zx vs. ST10F273Z4 PLL ratio(1) (continued)

P0.15-13 (P0H.7-5)			PLL multiplication factor		ST10F273Z4 oscillator	
			ST10F269Zx	ST10F273Z4	Input range (MHz)	CPU clock range (MHz)
0	1	0	* 1.5	* 10	4 to 6.4	40 to 64
0	0	1	* 0.5	* 0.5	4 to 12	2 to 6
0	0	0	* 2.5	* 16	4	64

1. All configurations need a crystal (or ceramic resonator) to generate the CPU clock through the internal oscillator amplifier, except the Direct Drive mode (oscillator amplifier disabled, so no crystal or resonator can be used). Vice versa, the clock can be forced through an external clock source only in Direct Drive mode.

1.9.1 Hardware impacts

The Port0 configuration may be changed with regard to the new PLL factor.

The component on XTAL1 & XTAL2 (Crystal and capacitors, or resonator) must be changed for the following reasons:

- The input frequency range is now reduced.
- It is no longer possible to use a crystal or a ceramic resonator in Direct Drive mode.
- It is no longer possible to use a PLL factor with a frequency generator.
- The electrical characteristics of the main oscillator have changed (transconductance)

1.9.2 Software impacts

None.

2 New features

2.1 Additional XPeripherals

Some peripherals have been added to ST10F273Z4. They are mapped on the XBus and are linked to additional alternate functions of some ports.

The additional XPeripherals include the following:

- A second SSC (SSC of ST10F269Zx becomes SSC0, while the new one is referred to as XSSC or SSC1). Note that some restrictions and functional differences due to the XBus peculiarities are present between the classic SSC and the new XSSC.
- A second ASC (ASC0 of ST10F269Zx remains ASC0, while the new one is referred to as XASC or ASC1). Note that some restrictions and functional differences due to the XBus peculiarities are present between the classic ASC and the new XASC.
- An I2C interface is added (see X-I2C or I2C interface).

In addition to the above XPeripherals, ST10F273Z4 also features a second PWM (PWM of the ST10F269Zx becomes PWM0, while the new one is referred to as XPWM or PWM1). Note that some restrictions and functional differences due to the XBus peculiarities are present between the classic PWM and the new XPWM.

2.1.1 Hardware impacts

None if the additional XPeripherals are not used.

2.1.2 Software impacts

None, if the additional Peripherals are not used. As they are XPeripherals, they can be enabled/disabled via the XPERCON and SYSCON registers. By default, the setting of XPERCON and SYSCON is compatible with ST10F269Zx.

2.2 Programmable divider on CLKOUT

A specific register mapped on the X-Bus allows the user to choose the division factor on the CLKOUT signal (P3.15).

XCLKOUTDIV (E902h) **XBUS** **Reset value: --00h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DIV							
-								RW							

Table 12. XCLKOUTDIV register: DIV bit

Bit	Function
DIV	$f_{clkout} = f_{CPU}/(DIV + 1)$

2.2.1 Hardware impacts

None.

2.2.2 Software impacts

None, if only CLKOUT is needed.

When the CLKOUT function is enabled by setting the CLKEN bit of register SYSCON, CPU clock output is on P3.15 by default.

To access the XCLKOUTDIV register and thus program the clock prescaling factor, the XMISCEN bit of XPERCON and XPEN of the SYSCON registers must be set.

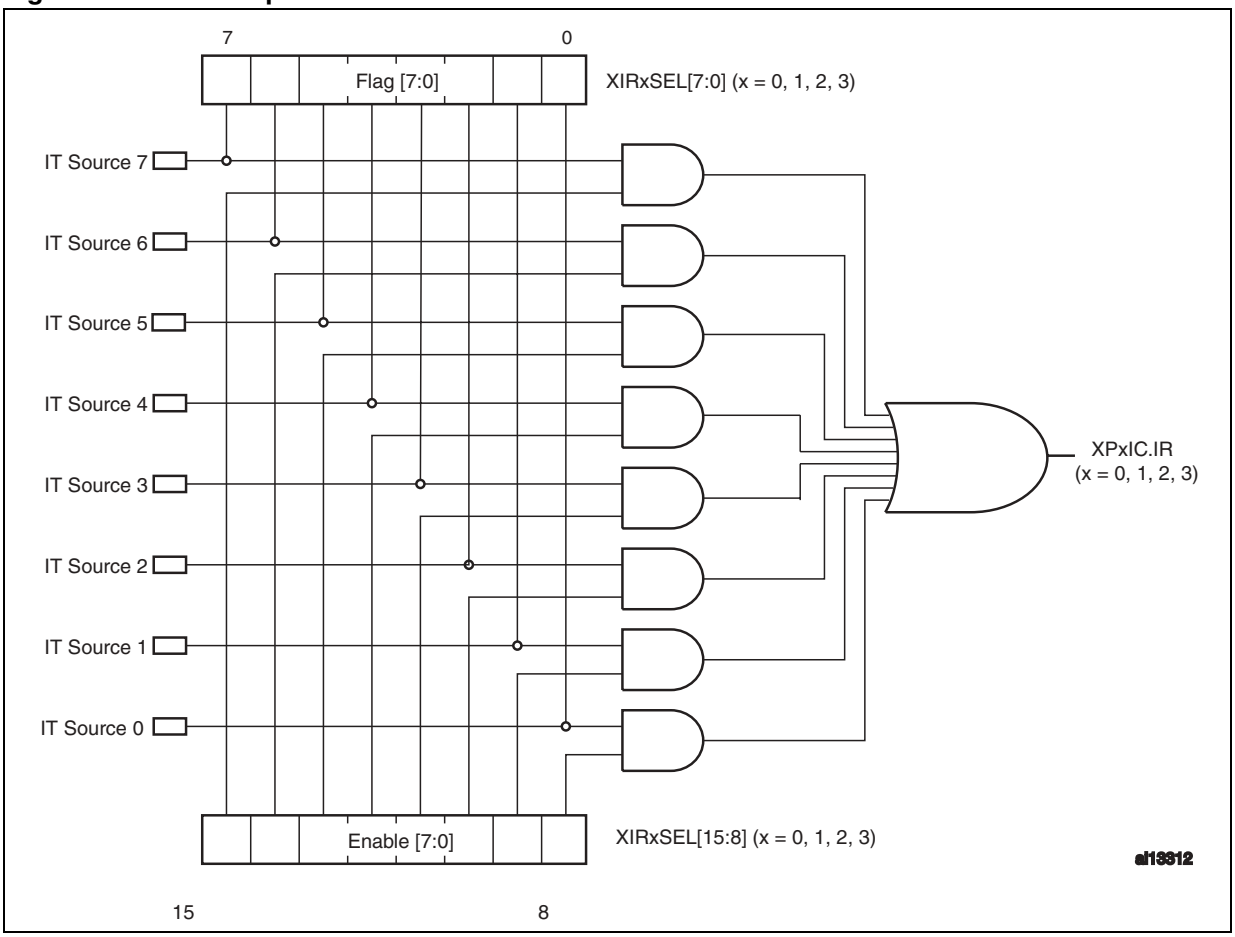
2.3 New multiplexer for X-Interrupts

The limited number of XBus interrupt lines of the present ST10 architecture imposes some constraints on the implementation of new functionalities. In particular, the additional XPeripherals XSSC, XASC, XI2C and XPWM need some resources to implement interrupt and PEC transfer. For this reason, a complex but very flexible multiplexed structure for interrupt is suggested. In *Figure 2: X-Interrupt basic structure* the principle is represented through a simple diagram, which shows the basic structure replicated for each of the four X-interrupt vectors (XP0INT, XP1INT, XP2INT and XP3INT).

It is based on a new 16-bit register XIRxSEL (x = 0,1,2,3), divided in two portions:

- Byte High (XIRxSEL[15:8]) Interrupt Enable bits
- Byte Low (XIRxSEL[7:0]) Interrupt Flag bits

Figure 2. X-Interrupt basic structure



When different sources submit an interrupt request, the enable bits (Byte High of the XIRxSEL register) define a mask which controls which sources will be associated with the unique available vector. If more than one source is enabled to issue the request, the service routine will have to take care to identify the real event to be serviced. This can easily be done by checking the flag bits (Byte Low of XIRxSEL register). Note that the flag bit can provide information about events which are not currently serviced by the interrupt controller (since masked through the enable bits), allowing an effective software management in the absence of the possibility to serve the related interrupt request. A period polling of the flag bits may be implemented inside the user application.

XMISCEN, bit 10 of XPERCON register, must be set to have access to these registers. Refer to *Section 3.1: XPERCON register on page 24* for more details.

Table 13: X-Interrupt detailed mapping gives an overview of the different settings available.

Table 13. X-Interrupt detailed mapping

	XP0INT	XP1INT	XP2INT	XP3INT
CAN1 Interrupt	X			X
CAN2 Interrupt		X		X
I2C Receive	X	X	X	

Table 13. X-Interrupt detailed mapping (continued)

	XP0INT	XP1INT	XP2INT	XP3INT
I2C Transmit	X	X	X	
I2C Error				X
SSC1 Receive	X	X	X	
SSC1 Transmit	X	X	X	
SSC1 Error				X
ASC1 Receive	X	X	X	
ASC1 Transmit	X	X	X	
ASC1 Transmit Buffer	X	X	X	
ASC1 Error				X
PLL Unlock / OWD				X
PWM1 Channel 3...0			X	X

2.3.1 Hardware impacts

None.

2.3.2 Software impacts

The XIRxSEL registers must be configured. If none of the new X-Peripherals are used, that is, only the X-Peripherals that were already present on ST10F269Zx are used, the following values must be programmed:

- XIR0SEL = 0x0100, only CAN1 interrupt is enabled and can generate an interrupt to the ST10 through XP0IC.
- XIR1SEL = 0x0100, only CAN2 interrupt is enabled and can generate an interrupt to the ST10 through XP1IC.
- XIR2SEL = 0x0, not used.
- XIR3SEL = 0x2000, only PLL unlock interrupt is enabled and will generate an interrupt to the ST10 through XP3IC.

Then, in the interrupt routines associated with the XPxIC, the respective flag in the XIRxSEL register must be cleared. Since the XIRxSEL registers are not bit addressable, a pair of registers (a pair for each XIRxSEL) is provided to allow setting and clearing the bits of XIRxSEL without risking overwriting requests coming after reading the register and before writing it. Therefore the following registers must be written to clear the flags:

- In the CAN1 interrupt routine, XIR0CLR (@ EB14h) = 0x0001.
- In the CAN2 interrupt routine, XIR1CLR (@ EB24h) = 0x0001.
- In the PLL unlock interrupt routine, XIR3CLR (@ EB44h) = 0x0020.

Additional information on the X-Interrupt multiplexer structure

Figure 1 on page 17 shows that the X-Interrupt sources are connected to the interrupt request flag of the XIRxSEL registers and to the XPxIR request flag via an AND gate with

the enable bit. This AND gate is activated by a transition on the Interrupt source line and not by the latched value in the XIRxSEL register meaning:

- A transition on the IT source line will generate an interrupt to the ST10 core if the source is enabled.
- Writing to an interrupt request flag in a XIRxSEL register will not generate an interrupt to the ST10 core.

Example: If XIR0SEL = 0x0100: CAN1 interrupt enabled on XP0IC interrupt.

To trigger by software the CAN1 interrupt routine with the XP0IC register the following code must be used:

```
XIR0SET = 0x0001;/* Set CAN1 interrupt request Flag in XIR0SEL */
XP0IC = XP0IC | 0x0080;/* Set XP0IR flag, generate an interrupt */
```

Executing only the first line will only set the flag in the XIR0SEL register but will not be seen by the AND gate and cannot set the XP0IR flag.

2.4 Additional ports input control: XPICON register

The possibility to select between TTL and CMOS-like input thresholds has been extended to the Ports 0, 1 and 5.

ST10F273Z4: XPICON (EB26) **XREG** **Reset value: --00h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										P5HIN	P5LIN	P1HIN	P1LIN	P0HIN	P0LIN
-										RW	RW	RW	RW	RW	RW

Table 14. ST10F273Z4 XPICON register

Bit	Function	Reset value
PxLIN	**Port x Low Byte Input Level Selection** 0: Pins Px.7..0 switch on standard TTL input levels. 1: Pins Px.7..0 switch on CM0OS input levels	0
PxHIN	**Port x High Byte Input Level Selection** 0: Pins Px.15..8 switch on standard TTL input levels. 1: Pins Px.15..8 switch on CM0OS input levels.	0

2.4.1 Hardware impacts

None.

2.4.2 Software impacts

None.

3 Modified registers

3.1 XPERCON register

In ST10F273Z4, new bits have been added with regard to the additional X-Peripherals.

The XPERCON register allows the X-Bus peripherals to be separately selected so they are visible to the user by means of corresponding bits. If not selected (not activated with a bit of XPERCON) **before** the XPEN bit in SYSCON is set, the corresponding address space, port pins and interrupts are not occupied by the peripheral, and thus this peripheral is not visible and not available.

ST10F269Zx: XPERCON (F024h/12h) **SFR** **Reset value: --05h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											RTC EN	XRAM 2EN	XRAM 1EN	CAN2 EN	CAN1 EN
-											RW	RW	RW	RW	RW

ST10F273Z4: XPERCON (F024h/12h) **SFR** **Reset value: -005h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					XMIS CEN	X12 CEN	XSSC EN	XAS CEN	XPW MEN	XFLA SHEN	RTC EN	XRAM 2EN	XRAM 1EN	CAN2 EN	CAN1 EN
-					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 15. XPERCON register description

Bit	Bit name	Function
0	CAN1EN	**CAN1 Enable Bit** 0: Accesses the CAN1 XPeripheral and its functions are disabled (P4.5 and P4.6 pins can be used as general purpose I/Os). 1: The CAN1 XPeripheral is enabled and can be accessed.
1	CAN2EN	**CAN2 Enable Bit** 0: Accesses the CAN2 XPeripheral and its functions are disabled (P4.4 and P4.7 pins can be used as general purpose I/Os). 1: The CAN2 XPeripheral is enabled and can be accessed.
2	XRAM1EN	**XRAM1 Enable Bit** 0: Access to the XRAM1 block is disabled, external access performed. 1: The on-chip XRAM1 is enabled and can be assessed
3	XRAM2EN	**XRAM2 Enable Bit** 0: Access to the XRAM2 block is disabled, external access performed. 1: The on-chip XRAM2 is enabled and can be assessed.
4	RTCEN	**RTC Enable Bit** 0: Access to the Real Time Clock is disabled, external access performed. 1: The Real Time Clock is enabled and can be accessed.

Table 15. XPERCON register description (continued)

Bit	Bit name	Function
5	XFLASHEN	**XFlash Enable Bit** 0: Access to the Flash Registers are disabled. The on-chip Flash cannot be programmed. 1: Access to the Flash Registers are enabled. The on-chip Flash can be programmed.
6	XPWMEN	**XPWM Enable** 0: Access to the XPWM module is disabled, external access performed. 1: The XPWM module is enabled and can be accessed.
7	XASCEN	**XASC Enable Bit** 0: Access to the XASC is disabled, external access performed. 1: The XASC is enabled and can be accessed.
8	XSSCEN	**XSSC Enable Bit** 0: Access to the XSSC is disabled, external access performed. 1: The XSSC is enabled and can be accessed.
9	X12CEN	**X12C Enable Bit** 0: Access to the X12C is disabled, external access performed. 1: The X12C is enabled and can be accessed.
10	XMISCEN	**XBUS Additional Features Enable Bit** 0: Access to the Additional Miscellaneous Features is disabled. 1: The Additional Features are enabled and can be accessed.
11:15	-	Reserved

Access to the X-Peripherals are configured through three pairs of specific X-Bus configuration registers, equivalent to the External Bus register BUSCONx and ADDRSELx. Therefore several X-Peripherals sharing the same pair leading to the point that accesses a disabled X-Peripheral are only redirected to external memory if all the other X-Peripherals sharing the same pair of registers are disabled.

This gives the following groups:

- CAN1, CAN2, XASC, XSSC, XI2C, XPWM, XRTC and XMISC: accessing to range 00'E800h-00'EFFFh are redirected to external memory only if all corresponding bits are cleared.
- XRAM1: accessing to range 00'E000h-00'E7FFh are redirected to external memory if bit XRAM1EN is cleared.
- XRAM2, XFLASH: accessing to range 09'0000h-0F'FFFFh (default value in XADRS3 register, refer to *Section 4.1: XADRS3 register on page 26*) are redirected to external memory if bits XRAM2EN and XFLASHEN are cleared.

3.1.1 Hardware impacts

None.

3.1.2 Software impacts

None, if ST10F269Zx software is not written to the reserved bit.

4 New registers

4.1 XADRS3 register

On previous ST10 devices, this register was already present but its value was mask programmed. On ST10F273Z4 this register has been made available to the user. In this way the address range of the XRAM2 memory is now user programmable.

ST10F273Z4: XADRS3 ($F01C_h$) **SFR** **Reset value: 800Bh**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RGSAD												RGSZ			
RW												RW			

The register functionality is the same as the one of ADDRSELx registers used for external address range selection with some limitations:

- The address window can only be located in the first Mbyte of addressable space, that is, in the range 00'0000h-0F'FFFFh.
- The window start address must be aligned on a Range Size boundary.

Table 16. XADRS3 register bits

Bit No.	Bit name	Function
3:0	RGSZ	**Range size selection** Defines the size of the address window.
15:4	RGSAD	**Range Start Address** Defines the bits A19..A8 of the Start Address of the address window.

Table 17. Definition of address area

Bit field RGSZ	Selected window size	Relevant bit (R) of RGSAD	Selected range start address relevant bit (R) of address (A23 - A0)
0 0 0 0	256 bytes	RRRR RRRR RRRR	0000 RRRR RRRR RRRR xxxx xxxx
0 0 0 1	512 bytes	RRRR RRRR RRRx	0000 RRRR RRRR RRRx xxxx xxxx
-	-	-	-
1 0 1 0	256 Kbytes	RRxx xxxx xxxx	0000 RRxx xxxx xxxx xxxx xxxx
1 0 1 1	512 Kbytes	Rxxx xxxx xxxx	0000 Rxxx xxxx xxxx xxxx xxxx
1 1 x x	Reserved		

4.1.1 Hardware impacts

None.

4.1.2 Software impacts

In the ST10F273Z4, this register should be programmed by the user before accessing XRAM2 so that:

- RGSZ defines a 128 Kbyte window size in order to cover the Flash registers and the XRAM2 area: RGSZ = 1001b.
- RGSAD defines bits 8 to 19 of the window start address that is the Flash registers area: RGSAD = E00h.

The desired value should be written in XADRS3 register before enabling XRAM2 in SYSCON and XPERCON registers.

Note: XADRS3 cannot be changed after executing the EINIT instruction.

4.2 XPEREMU register

This register has been added as a write-only register.

ST10F273Z4: XPEREMU (EB7Eh) **XREG** **Reset value: XXXXh**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					XMIS CEN	X12 CEN	XSS CEN	XAS CEN	XPW MEN	Res	XRT CEN	XRA M2EN	XRA M1EN	CAN 2EN	CAN 1EN
-					WO	WO	WO	WO	WO	-	WO	WO	WO	WO	WO

The bit meaning is exactly the same as in the XPERCON register.

4.2.1 Hardware impacts

None.

4.2.2 Software impacts

Once the XPEN bit of SYSCON register is set and at least one of the X-peripherals (except memories) is activated, the register XPEREMU must be written with the same content of XPERCON. This is mandatory in order to allow a correct emulation of the new set of features introduced on X-Bus for the new ST10 generation. The following instructions must be added inside the initialization routine:

- If (SYSCON.XPEN && (XPERCON & 0x07D3))
- Then {XPEREMU = XPERCON}

Of course, XPEREMU must be programmed after XPERCON and after SYSCON, in such a way the final configuration for X-Peripherals is stored in XPEREMU and used for the emulation hardware setup.

4.3 Emulation dedicated registers

A set of additional four registers are implemented for emulation purpose only. Similar to XPEREMU, they are write only registers:

XEMU0 (00'EB76h)

XEMU1 (00'EB78h)

XEMU2 (00'EB7Ah)

XEMU3 (00'EB7Ch)

These registers are used by emulators. They have no user action in ST10F273Z4.

4.3.1 Hardware impacts

None.

4.3.2 Software impacts

None. In ST10F269Zx, the address range 00'E800h to 00'EBFFh is mapped to external memory but is recommended to reserve this space for upward compatibility.

4.4 XMISC register

This register has been created to handle some additional functionalities. To have access to this register, XMISCEN bit, bit 10 of XPERCON, must be set.

ST10F273Z4: XMISC (EB46h) **XREG** **Reset value: 0000h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												VREG OFF	CAN CK2	CAN PAR	ADC MUX
-												RW	RW	RW	RW

Table 18. XMISC register description

Bit No.	Bit name	Function
0	ADCMUX	**Port1L ADC Channels Enable** 0: Analog inputs on port P5.y can be converted (default configuration). 1: Analog inputs on Port P1.z can be converted. Only 8 channels can be managed.
1	CANPAR	**CAN Parallel Mode Selection** 0: CAN2 is mapped on P4.4/P4.7, while CAN1 is mapped on P4.5/P4.6. 1: CAN1 and CAN2 are mapped in parallel on P4.5/P4.6. This is effective only if both CAN1 and CAN2 are enabled (bits CAN1EN and CAN2EN set in XPERCON register). If CAN1 is disabled, CAN2 remains on P4.4/P4.7 even if bit CANPAR is set.
2	CANCK2	**CAN Clock divided by 2 disable** 0: Clock provided to CAN modules is CPU clock divided by 2 (mandatory when f_{CPU} is higher than 40 MHz). 1: Clock provided to CAN modules is the direct CPU clock.

Table 18. XMISC register description (continued)

Bit No.	Bit name	Function
3	VREGOFF	**Main Voltage Regulator disable in Power-Down mode** 0: Default value after reset and when Power-Down is not used. 1: On-chip Main Regulator is turned off when Power-Down mode is entered.
4:15	-	Reserved

4.4.1 Hardware impacts

None.

4.4.2 Software impacts

None.

5 Electrical characteristics

Note: In the tables where the device provides signals with their respective timing characteristics, the symbol CC (Controller Characteristics) is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol SR (System Requirement) is included in the Symbol column.

5.1 DC characteristics

5.1.1 Absolute maximum ratings

They are the same.

5.1.2 Overview of the DC characteristics

The pads of ST10F273Z4 have been redesigned according to the new technology and therefore the characteristics are different. The user should verify the DC characteristics.

Table 19 below lists the parameters that might have the biggest impact.

Table 19. DC characteristics

Symbol	Parameter	ST10F269Zx limit values		ST10F273Z4 limit values		Unit
		Min	Max	Min	Max	
V_{IL}**SR**	Input low voltage (all other inputs)	-0.5	0.2 V_{DD} - 0.1	-0.3	0.8	V
V_{ILS}**SR**		-0.5	2.0, special threshold	-0.3	0.3 V_{DD}, special threshold	
V_{IL1}**SR**	Input low voltage ($\overline{\text{RSTIN}}$, $\overline{\text{EA}}$, $\overline{\text{NMI}}$, and $\overline{\text{RPD}}$)	N.A.	N.A.	-0.3	0.3 V_{DD}	V
V_{IL2}**SR**	Input low voltage (XTAL1 and XTAL3)			-0.3	0.3 V_{DD}	V
V_{IH}**SR**	Input high voltage (all except $\overline{\text{RSTIN}}$, $\overline{\text{EA}}$, $\overline{\text{NMI}}$, $\overline{\text{RPD}}$, XTAL1 and XTAL3)	0.2 V_{DD} + 0.9	V_{DD} + 0.5	2.0	V_{DD} + 0.3	V
V_{IHS}**SR**		0.8 V_{DD} - 0.2	V_{DD} + 0.5, special threshold	0.7 V_{DD}	V_{DD} + 0.3, special threshold	
HYS	Input hysteresis	NA	-	400, default	700	mV
		400, special threshold		700, special threshold	1400	
V_{HYS1}**CC**	Input hysteresis $\overline{\text{RSTIN}}$, $\overline{\text{EA}}$, $\overline{\text{NMI}}$			750	1400	mV

Table 19. DC characteristics (continued)

Symbol	Parameter	ST10F269Zx limit values		ST10F273Z4 limit values		Unit
		Min	Max	Min	Max	
V_{OL}**CC**	Output low voltage	- PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$	0.45; I_{OL} = 2.4mA	- PORT6, ALE, CLKOUT, $\overline{WR}$, $\overline{BHE}$, $\overline{RD}$, $\overline{RSTOUT}$, $\overline{RSTIN}$, READY	0.4; I_{OL} = 8mA 0.05; I_{OL} = 1mA	V
V_{OL1}**CC**	Output low voltage (all other outputs)	-	0.45; I_{OL} = 2.4mA	-	0.4; Iol = 4mA 0.05; I_{OL} = 0.5mA	V
V_{OH}**CC**	Output high voltage	0.9V_{DD}; I_{OH} = -0.5mA 2.4; I_{OH} = -2.4mA	- PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$	V_{DD} - 0.8/ I_{OH} = -8mA V_{DD} -0.08/ I_{OH} = -1mA	- PORT6, ALE, CLKOUT, $\overline{WR}$, READY, $\overline{BHE}$, $\overline{RD}$, $\overline{RSTOUT}$, $\overline{RSTIN}$	V
V_{OH1}**CC**	Output high voltage (all other outputs)	0.9$V_{DD;}$ I_{OH} = -0.25mA 2.4; I_{OH} = -1.6mA	-	V_{DD} - 0.8; I_{OH} = -4mA V_{DD} - 0.08; I_{OH} = -0.5mA	-	V
I_{OZ1}**CC**	Port5 Input leakage current	-	±0.5	-	±0.2	µA
I_{OZ2}**CC**	Input leakage current (all other inputs)	-	±1	-	±0.5	µA

5.2 AC characteristics at 40 MHz

As the technology is different for the two devices, the I/Os present some differences in AC behavior. *Table 20* and *Table 21* below list all the timing differences. Please carefully check your design for any possible impacts.

5.2.1 External memory bus timings

Note that for CPU clock frequencies above 40 MHz (when using the ST10F273Z4Q3), some numbers in the timing formulas become zero or negative. In most cases this is not acceptable or meaningful. In such cases, it is necessary to relax the speed of the bus setting properly t_A (ALE extension), t_C (Memory Cycle Time wait-states) and t_F (Memory tri-state time).

Multiplexed bus

Table 20. Multiplexed bus timings (ns)

Symbol	Parameter	ST10F269Zx		ST10F273Z4		ST10F269Zx @f_{CPU} = 40 MHz		ST10F273Z4 @f_{CPU} = 40 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t_6 CC	Address setup to ALE	TCL - 10.5 + t_A	-	TCL - 11 + t_A	-	2 + t_A	-	1.5 + t_A	-
t_{16} SR	ALE low to valid data in	-	3 TCL - 19 + t_A + t_C	-	3 TCL - 20 + t_A + t_C	18.5 + t_A + t_C	-	17.5 + t_A + t_C	-
t_{17} SR	Address/ Unlatched $\overline{CS}$ to valid data in	-	4 TCL - 28 + 2t_A + t_C	-	4 TCL - 30 + 2t_A + t_C	22 + 2t_A + t_C	-	20 + 2t_A + t_C	-
t_{39} SR	Latched $\overline{CS}$ low to Valid Data in	-	3 TCL - 19 + 2t_A + t_C	-	3 TCL - 21 + 2t_A + t_C	18.5 + 2t_A + t_C	-	16.5 + 2t_A + t_C	-
t_{44} CC	Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	-	0	-	1.5	-	0	-	1.5
t_{45} CC	Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	-	TCL	-	TCL + 1.5	-	12.5	-	14

Demultiplexed bus

Table 21. Demultiplexed bus timings

Symbol	Parameter	ST10F269Zx		ST10F273Z4		ST10F269Zx @f_{CPU} = 40 MHz		ST10F273Z4 @f_{CPU} = 40 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t_6 CC	Address setup to ALE	TCL - 10.5 + t_A	-	TCL - 11 + t_A	-	2 + t_A	-	1.5 + t_A	-
t_{88} CC	Address/ Unlatched $\overline{CS}$ setup to $\overline{RD}$, $\overline{WR}$ (with RW delay)	-	2 TCL - 8.5 + 2t_A	-	2 TCL - 12.5 + 2t_A	16.5 + 2t_A	-	12.5 + 2t_A	-
t_{81} CC	Address/ Unlatched $\overline{CS}$ setup to $\overline{RD}$, $\overline{WR}$ (no RW delay)	-	TCL - 8.5 + 2t_A	-	TCL - 12 + 2t_A	4 + 2t_A	-	0.5 + 2t_A	-
t_{16} SR	ALE low to valid data in	-	3 TCL - 19 + t_A + t_C	-	3 TCL - 20 + t_A + t_C	18.5 + t_A + t_C	-	17.5 + t_A + t_C	-
t_{17} SR	Address/ Unlatched $\overline{CS}$ to valid data in	-	4 TCL - 28 + 2t_A + t_C	-	4 TCL - 30 + 2t_A + t_C	22 + 2t_A + t_C	-	20 + 2t_A + t_C	-

Table 21. Demultiplexed bus timings (continued)

Symbol	Parameter	ST10F269Zx		ST10F273Z4		ST10F269Zx @f_{CPU} = 40 MHz		ST10F273Z4 @f_{CPU} = 40 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t_{28} **CC**	Address/ Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	0 (no t_F) -5 + t_F (t_F > 0)	-	0 + t_F	-	0 (no t_F) -5 + t_F (t_F > 0)	-	0 + t_F	-
t_{39} **SR**	Latched $\overline{CS}$ low to valid data in	-	3 TCL - 19 + $2t_A$ + t_C	-	3 TCL - 21 + $2t_A$ + t_C	18.5 + $2t_A$ + t_C	-	16.5 + $2t_A$ + t_C	-
t_{82} **CC**	Address setup to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	2 TCL - 10.5 + $2t_A$	-	2 TCL - 11 + $2t_A$	-	14.5 + $2t_A$	-	14 + $2t_A$	-

5.2.2 Hi-speed synchronous serial interface (SSC)

The maximum baudrate of the SSC in ST10F273Z4 is 8 Mbaud while it is 10 in ST10F269Zx. For CPU frequencies strictly higher than 32 MHz, the minimum value of the SSCBR register (prescaler value) must not be lower than 2.

6 Revision history

Table 22. Revision history

Date	Revision	Description of changes
06-July-2007	1	Initial release