AN2386
Application note

How to achieve the threshold voltage thermal coefficient of the MOSFET acting on design parameters

Introduction

Today, the MOSFET devices are used mainly as switches in electronic circuits. In such operational conditions, the MOSFET device works in switch on and switch off modes. However, in some applications, as in audio amplifiers or air conditioning, the MOSFET works in a linear zone. The MOSFET works in a linear zone when either it is subject to a high voltage, or a high current passes through the device. As it is well known in literature, during the linear zone operation mode the MOSFET could fail if a thermal run-away occurs. The failure conditions depend on either of the internal structure of MOSFET or of the package used. The threshold voltage thermal coefficient (TVTC) is one of the big elements that could bring the MOSFET to fail. TVTC is achieved deriving the MOSFET threshold voltage against the temperature. TVTC is a negative coefficient because of when the temperature increases the threshold voltage decreases. When TVTC increases in absolute value, the MOSFET becomes thermally instable and a failure could occur. Therefore, in order to understand if a MOSFET device can be used in an application working in linear zone in safety conditions, a device with a low TVTC value must be considered and, thus, it is important to achieve a theoretical expression for it.

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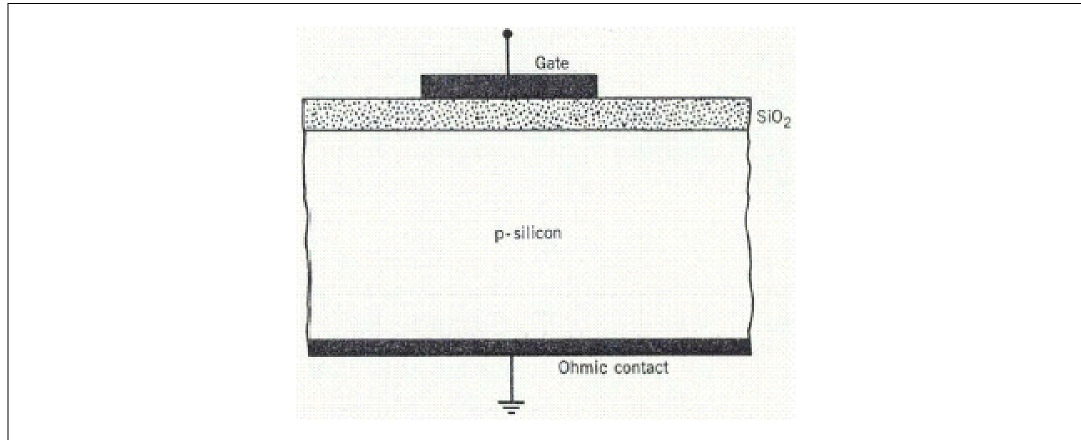
1 MOS structure

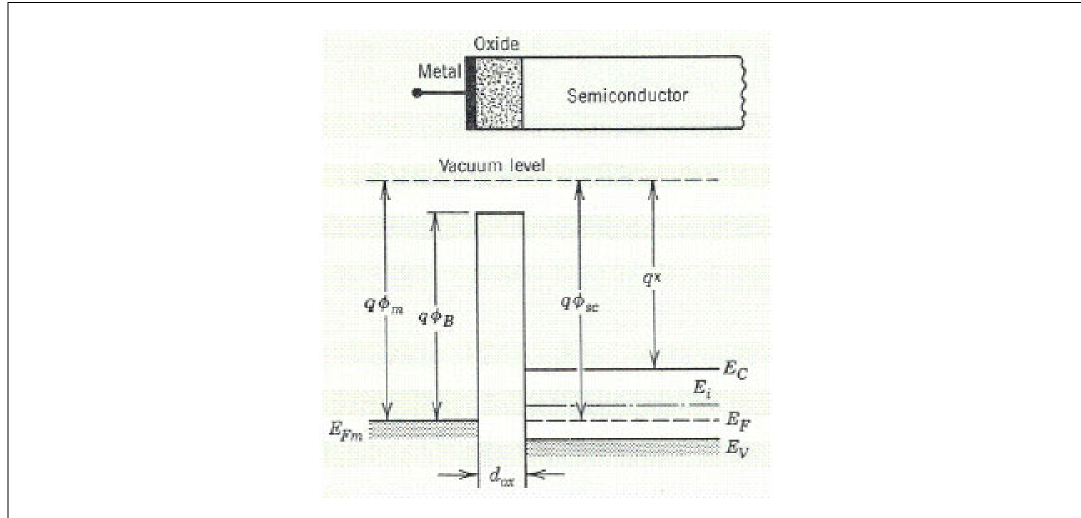
As it is well known, a MOS structure is composed by three layers: the first one is metal or heavily doped polycrystalline silicon, the second one is an insulator of SiO_2 and the third one is the semiconductor (see *Figure 1.*).

Figure 1. Cross section view of a MOS capacitor



Considering an ideal MOS system with a p-doped semiconductor, the energy band diagram can be illustrated as in *Figure 2.*

Figure 2. Energy band diagram of an ideal MOS capacitor under thermal equilibrium.

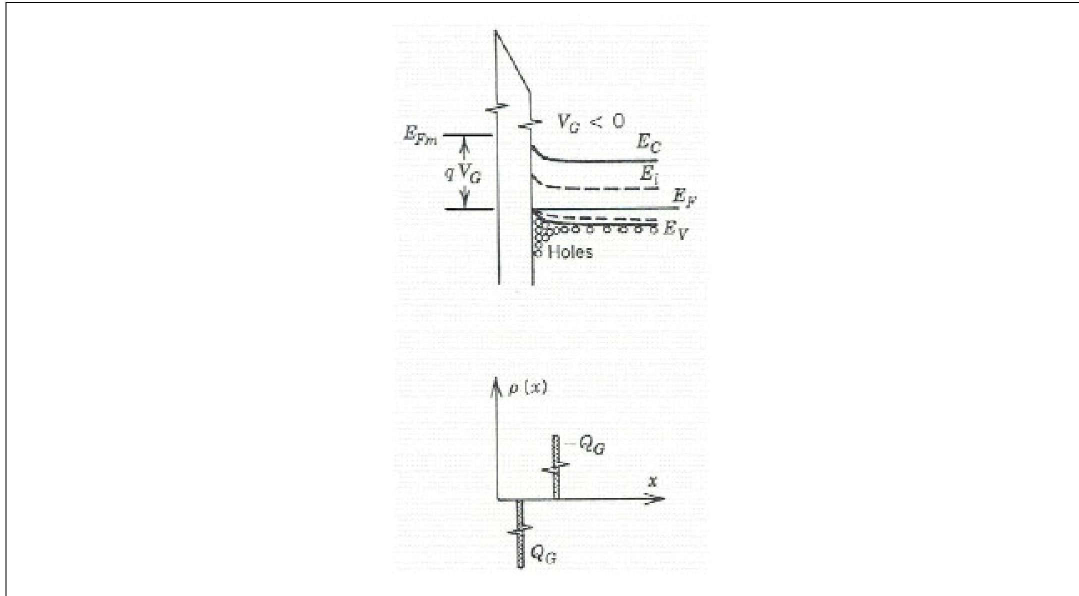


q Φ_m is the work function (energy that needs to extract an electron from the metal); q Φ_B is the energy difference between the oxide conduction band and the metal Fermi energy level (metal-to-oxide barrier energy); q Φ_{sc} is the work function of the semiconductor; q χ is the energy difference between the vacuum level and the conduction band edge.

When a negative voltage (V_g) is applied on the gate terminal respect to the semiconductor, the Fermi level of the metal raises of qV_g compared to the semiconductor side. In moving from the semiconductor to the metal, the vacuum level must bend up gradually to

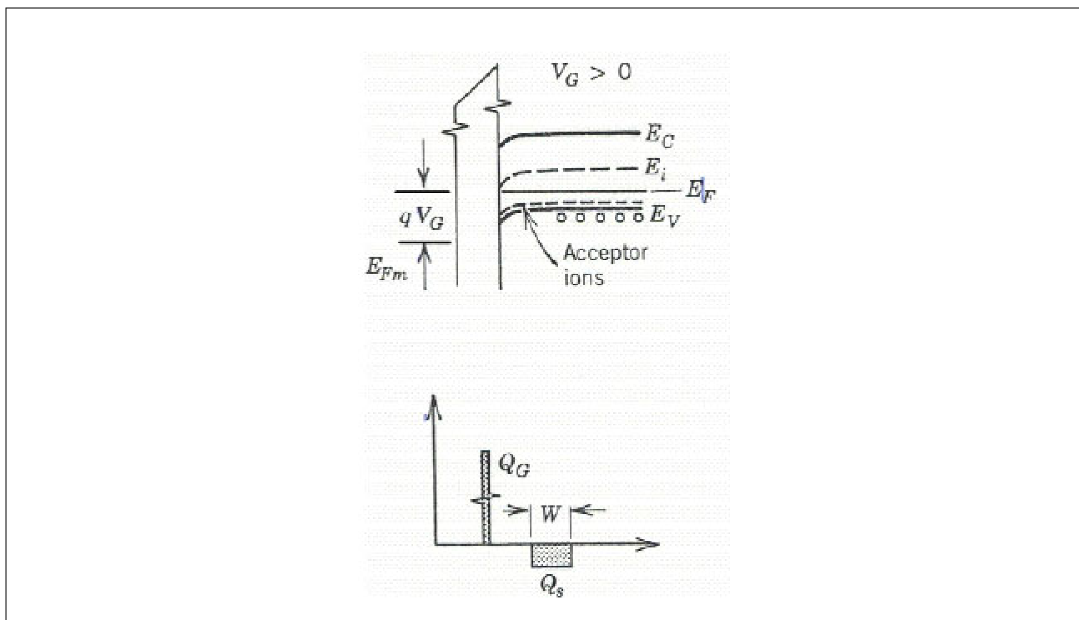
accommodate the gate voltage applied. Part of this bending occurs in the semiconductor and the rest in the oxide. The metal and the semiconductor affinity remain the same (see *Figure 3.*).

Figure 3. Energy band diagram and charge distribution in an ideal MOS capacitor in accumulation condition.



The negative charge on the gate creates an opposite charge on the semiconductor (enhanced concentration of holes near the oxide interface). When a small positive bias is applied to the gate, holes are pushed away from the oxide interface and create a depletion layer in the semiconductor, consisting on the negative charges due to the acceptor ions. The energy band diagram and the charge distribution are shown in *Figure 4.*

Figure 4. Energy band diagram and charge distribution in an ideal MOS capacitor in accumulation condition.



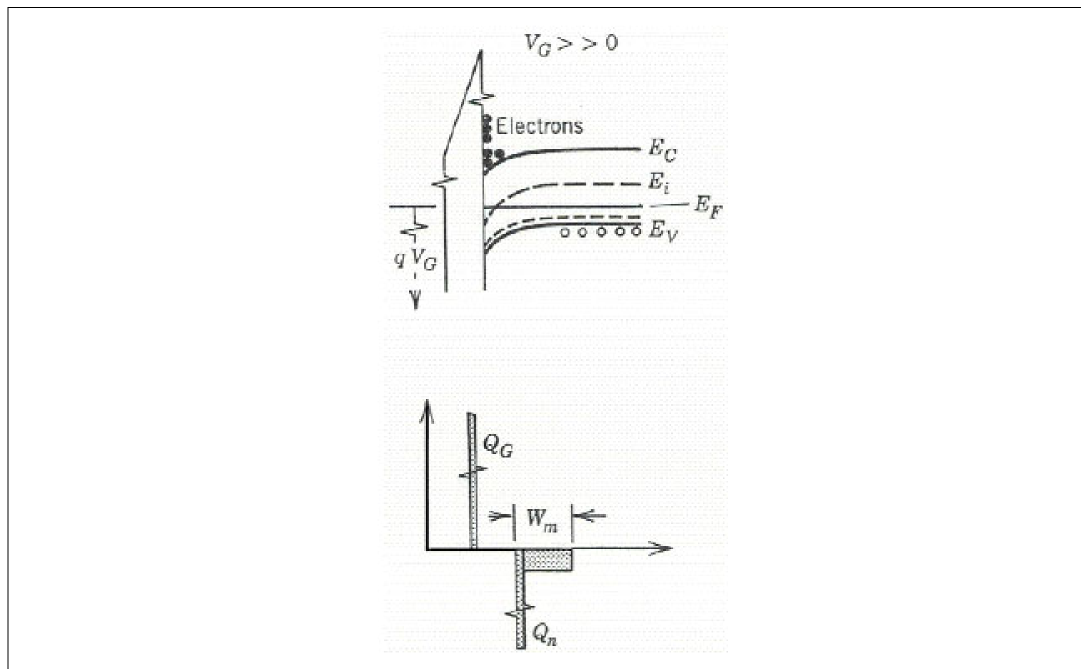
The charge Q_s in the semiconductor side near the oxide interface is equal to Q_g and it can be written as:

Equation 1

$$Q_s = -qN_aW$$

N_a is the acceptor concentration and W is the width of the surface depletion layer. Increasing the gate voltage the bands continue to bend downward until E_i (the intermediate level energy between the conduction and the valence bands) equals E_F (the Fermi energy level) at the surface. In this condition, at the interface near the oxide, the semiconductor becomes intrinsic. Increasing the gate voltage again, E_i crosses E_F and, thus, the minority carriers, in this case the electrons, are attracted to the oxide-semiconductor interface. In this new condition, the surface layer contains more electrons than holes and it becomes n-type (inversion layer) (see *Figure 5.*).

Figure 5. Energy band diagram and charge distribution in an ideal MOS capacitor in inversion condition



Now, Q_s can be written as:

Equation 2

$$Q_s = -Q_n - qN_aW$$

Q_n is the inversion layer charge.

The relationships between the band bending, the electron and hole concentrations in the interface oxide-semiconductor may be obtained assuming that the semiconductor is non degenerate and that the doping is uniform. The electron and hole concentrations on the bulk semiconductor can be written respectively as:

Equation 3

$$n_0 = n_i e^{\left(\frac{E_F - E_i}{kT}\right)} = n_i e^{-\left(q \bullet \frac{\phi_F}{kT}\right)}$$

Equation 4

$$p_0 = n_i e^{\left(\frac{E_F - E_i}{kT}\right)} = n_i e^{\left(q \bullet \frac{\phi_F}{kT}\right)}$$

n_i is the intrinsic electron concentration; Ei is the intrinsic Fermi level; EF is the Fermi level; k is the Boltzmann constant and it is equal to 1.38×10^{-23} J/K; Φ_F is the Fermi potential. Considering that the semiconductor is doped of N_a acceptor, (*Equation 4*) becomes:

Equation 5

$$N_a = n_i e^{-\left(\frac{E_F - E_i}{kT}\right)} = n_i e^{\left(q \bullet \frac{\phi_F}{kT}\right)}$$

Now, it is possible achieve Φ_F as:

Equation 6

$$\Phi_F = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right)$$

For an intrinsic semiconductor ni can be written in two different ways as:

Equation 7

$$n_i = N_c e^{-\left(\frac{E_c - E_F}{kT}\right)}$$

Equation 8

$$n_i = N_V e^{-\left(\frac{E_c - E_F}{kT}\right)}$$

Multiplying (*Equation 7*) and (*Equation 8*) it is possible obtain:

Equation 9

$$n_i^2 = N_c N_V e^{\left(\frac{E_c - E_v}{kT}\right)} = N_c N_v e^{\left[\frac{E_g(T)}{kT}\right]}$$

N_C and N_V are the effective density of states at the conduction and valence edges respectively and E_g is the energy band-gap. N_C and N_V can be achieved by the electron and hole distribution functions and they are equal to:

Equation 10

$$N_c = 2\left(\frac{2\pi m_e \bullet kT}{h^2}\right)^{\left(\frac{3}{2}\right)}$$

Equation 11

$$N_v = 2\left(\frac{2\pi m_h \bullet kT}{h^2}\right)^{\frac{3}{2}}$$

m_e* and m_h* are the electron and hole density of the states effective masses and h is the Planck constant. The energy band gap depends on the temperature and it can be written as:

Equation 12

$$E_g = E_{g0} - b_1 T$$

where b1 is equal to 4.76 x 10^{-23}J/K.

E_{g0} is equal to 1.21eV and it is the extrapolate value of the band-gap at 0°K while b_1 is the rate of energy gap shift with temperature. Now, (*Equation 9*) can be rewritten as:

Equation 13

$$n_i^2 = N_c N_V e^{\left(\frac{E_{g0} - b_1 T}{kT}\right)} = N_c N_V e^{\left(\frac{b_1}{k}\right)} e^{\left(\frac{E_{g0}}{kT}\right)}$$

Considering that for the silicon:

Equation 14

$$N_c N_V e^{\left(\frac{b_1}{k}\right)} = 3.88 \bullet 10^{16} T^{\frac{3}{2}} [cm^{-3}]$$

and that:

Equation 15

$$\frac{E_{g0}}{k} = 14047[K]$$

n_i becomes:

Equation 16

$$n_i = 3.88 \bullet 10^{16} T^{\frac{3}{2}} e^{-\left(\frac{E_{g0}}{2kT}\right)} = 3.88 \bullet 10^{-16} T^{\frac{3}{2}} e^{-\left(\frac{7023}{T}\right)} [cm^{-3}]$$

In the interface layer oxide-semiconductor, the electron and hole concentrations depend on the gate voltage and can be written as:

Equation 17

$$n_s = n_0 e^{-\left(\frac{E_{is} - E_i}{kT}\right)} = n_0 e^{\left(q \bullet \frac{\Phi_s}{kT}\right)}$$

Equation 18

$$n_s = n_0 e^{-\left(\frac{E_{is} - E_i}{kT}\right)} = n_0 e^{\left(q \bullet \frac{\Phi_s}{kT}\right)}$$

When Φ_s is equal to Φ_F the semiconductor surface becomes intrinsic. Instead, increasing Φ_s again, the layer becomes n-type. When n_s equals to p_0 a "strong inversion" occurs and the minority carriers at the surface become the same of the majority carriers in the bulk. The potential condition for the strong inversion occurs when:

Equation 19

$$\Phi_s = 2\Phi_F$$

As explained above, when V_G is applied on the MOS structure, V_{OX} (a part of V_G) will appear across the oxide and the rest on the silicon surface:

Equation 20

$$V_G = V_{OX} - \Phi_s$$

If no charges are placed inside the oxide and if the MOS structure can be considered as a simple parallel plate capacitor, its capacitance can be written as:

Equation 21

$$C_{OX} = \varepsilon_{OX} \bullet \frac{A}{t_{OX}} = -\frac{Q_s}{V_{OX}}$$

ε_{ox} is the oxide permittivity (34.5x10^{-12}F/m); t_{OX} is the oxide thickness; A is the plate area.

Thus, considering (*Equation 21*), V_{OX} can be written as:

Equation 22

$$V_{OX} = -\frac{Q_s}{C_{OX}}$$

and the gate voltage as:

Equation 23

$$V_G = -\frac{Q_s}{C_{OX}} + \Phi_s$$

Considering (*Equation 2*), neglecting Q_n, V_G can be rewritten as:

Equation 24

$$V_G = \frac{qN_aW}{C_{OX}} + \Phi_s$$

By applying the Poisson equation in the semiconductor surface, the following equation can be obtained:

Equation 25

$$\mathrm{rot}E = \frac{qN_a}{\varepsilon_s} = \nabla^2\Phi$$

rotE is the electric field rotor; $\nabla^2\Phi$ is the voltage space second order derived; and es is the silicon permittivity (105.4x10^{-12}F/m). From (*Equation 25*) the following equation can be achieved:

Equation 26

$$\Phi_2 = \frac{qN_aW^2}{2\varepsilon_s}$$

and, thus, the depletion layer width can be achieved as:

Equation 27

$$W = \sqrt{\frac{2\varepsilon_s\Phi_s}{qN_a}}$$

V_G will became:

Equation 28

$$V_G = \sqrt{\frac{2\varepsilon_s q N_a \Phi_s}{C_{OX}}} + \Phi_s$$

The gate voltage at the strong inversion condition is the threshold voltage V_{TH} of the MOS and it can be written as:

Equation 29

$$V_{TH} = \sqrt{\frac{4\varepsilon_s q N_a \Phi_F}{C_{OX}}} + 2\Phi_F$$

Up to now, the ideal MOS structure was considered. In the real MOS structure, when no voltage is applied on the gate, a difference between metal and semiconductor work function exists, as well as charges in the oxide. In this paper, the charges inside the oxide will be neglected and also the metal-semiconductor difference work function Φ_{ms} will be studied. The charges inside the oxide are related to the real process flow and they involve a small threshold voltage shift. In order to consider the effect of Φ_{ms} on the threshold voltage, the following formula must be taken into account:

Equation 30

$$V_{TH} = V_{FB} + t_{OX}\sqrt{\frac{4\varepsilon_s q N_a \Phi_F}{\varepsilon_{OX}}} + 2\Phi_F = \Phi_{ms} + \frac{Q_{OX}}{C_{OX}} + t_{OX} \bullet \frac{\sqrt{4\varepsilon_s q N_a \Phi_F}}{\varepsilon_{OX}} + 2\Phi_F$$

V_{FB} is the flat-band voltage and it is the gate voltage required to bring the semiconductor bands flat; Q_{OX} are the charges inside the oxide. Such voltage equals to Φ_{ms} when the charges inside the oxide are neglected.

For metal gate, Φ_{ms} can be written as:

Equation 31

$$\Phi_{ms} = \Phi_m - \left(\chi + \frac{E_g(T)}{2q} \pm \Phi_F\right)$$

where $E_g(T)$ is the band-gap energy versus the temperature.

Instead, for polysilicon gate (the real case usually) of n-type and the semiconductor is of p-type, Φ_{ms} can be written as:

Equation 32

$$\Phi_{ms} = -\frac{kT}{q}\ln\left(\frac{N_g \bullet N_a}{ni^2}\right)$$

N_g is the doping level of the polysilicon.

TVTC can be, thus, achieved deriving (*Equation 30*) against the temperature:

Equation 33

$$\frac{\partial V_{TH}}{\partial T} = \frac{\partial \Phi_{ms}}{\partial T} + t_{OX} \bullet \frac{\sqrt{4\varepsilon_s q N_a}}{\varepsilon_{OX}} \bullet \frac{\partial \sqrt{\Phi_F}}{\partial T} + 2 \bullet \frac{\partial \Phi_F}{\partial T}$$

and also:

Equation 34

$$\frac{\partial V_{TH}}{\partial T} = \frac{\partial \Phi_{ms}}{\partial T} + t_{OX} \bullet \frac{\sqrt{\varepsilon_s q N_a}}{\varepsilon_{OX}\sqrt{\Phi_F}} \bullet \frac{\partial \Phi_F}{\partial T} + 2 \bullet \frac{\partial \Phi_F}{\partial T}$$

At the beginning, the thermal coefficient of Φ_{ms} will be studied.

Deriving (*Equation 32*), it is possible achieve:

Equation 35

$$\frac{\partial \Phi_{ms}}{\partial T} = -\frac{k}{q}\ln\left(\frac{N_g \bullet N_a}{ni^2}\right) + \frac{2kT}{qni} \bullet \frac{\partial ni}{\partial T}$$

and, thus:

Equation 36

$$\frac{\partial \Phi_{ms}}{\partial T} = \frac{\Phi_{ms}}{T} + \frac{2kT}{qni} \bullet \frac{\partial ni}{\partial T}$$

Considering (*Equation 16*) and deriving it versus T is possible obtain:

Equation 37

$$\frac{\partial n_i}{\partial T} = \frac{3}{2} \bullet 3.88 \bullet 10^{16} T^{\frac{1}{2}} e^{\left(\frac{E_{g0}}{2KT}\right)} + 3.88 \bullet 10^{16} T^{\frac{3}{2}} e^{\left(\frac{E_{g0}}{2KT}\right)} \bullet \frac{E_{g0}}{2KT^2}$$

and also:

Equation 38

$$\frac{\partial n_i}{\partial T} = \frac{n_i}{2T} \bullet \left[3 + \frac{E_{g0}}{KT}\right]$$

Replacing (*Equation 38*) in (*Equation 36*) it is possible obtain:

Equation 39

$$\frac{\partial \Phi_{ms}}{\partial T} = \frac{\Phi_{ms}}{T} + 3\frac{K}{q} + \frac{E_{g0}}{qT}$$

Now, the thermal coefficient of the Fermi voltage is studied. In fact, deriving (*Equation 6*) it is possible achieve:

Equation 40

$$\frac{\partial \Phi_F}{\partial T} = \frac{K}{q}\ln\left(\frac{N_a}{n_i}\right) - \frac{KT}{qn_i} \bullet \frac{\partial n_i}{\partial T}$$

Replacing (*Equation 38*) in (*Equation 40*), the following equation can be achieved:

Equation 41

$$\frac{\partial \Phi_F}{\partial T} = \frac{\Phi_F}{T} - \frac{3}{2} \bullet \frac{K}{q} - \frac{E_{go}}{2qT}$$

Replacing (*Equation 41*) and (*Equation 39*) in (*Equation 34*), TVTC can be rewritten as:

Equation 42

$$\frac{\partial V_{TH}}{\partial T} = \frac{\Phi_{ms}}{T} + 2 \bullet \frac{\Phi_F}{T} + t_{OX} \bullet \frac{\sqrt{\varepsilon_s q N_a}}{\varepsilon_{OX}\sqrt{\Phi_F}} \bullet \frac{\partial \Phi_F}{\partial T}$$

If the silicon is doped of p-type (n-channel MOSFET) and the polysilicon is also doped of p-type, (*Equation 32*), Φ_{ms} becomes positive and it can be rewritten as:

Equation 43

$$\Phi_{ms} = \frac{kT}{q}\ln\left(\frac{N_g \bullet N_a}{ni^2}\right)$$

and (*Equation 39*) becomes negative:

Equation 44

$$\frac{\partial\Phi_{ms}}{\partial T} = \frac{\Phi_{ms}}{T} - 3 \bullet \frac{K}{q} - \frac{E_{go}}{qT}$$

and, thus, (*Equation 42*) becames:

Equation 45

$$\frac{\partial V_{TH}}{\partial T} = \frac{\Phi_{ms}}{T} + 2 \bullet \frac{\Phi_F}{T} + t_{OX} \bullet \frac{\sqrt{\varepsilon_s q N_a}}{\varepsilon_{OX}\sqrt{\Phi_F}} \bullet \frac{\partial\Phi_F}{\partial T} - 6 \bullet \frac{K}{q} - 2 \bullet \frac{E_{go}}{qT}$$

2 Some considerations on V_{TH} and TVTC equations and real examples

Looking at (*Equation 30*) it is possible see that the threshold voltage is the sum of three components: the metal-oxide work function (it is negative when the polysilicon is of n-type and the silicon substrate is of p-type, while, it is positive when the polysilicon is of p-type), two times the Fermi potential (it is positive for p-type silicon substrate) and the voltage drop on the oxide (it is positive for a p-type silicon substrate). TVTC (see *Equation 42*) also depends on three contributes: the metal-oxide work function divided by the temperature (it is a negative value for n-type gate doped in p-type silicon), two times the Fermi potential divided by the temperature (for a p-type silicon it is a positive value) and a third contribute function of the Fermi potential thermal coefficient and other parameters as the oxide thickness and the body concentration of impurity (it is a negative contribute because of its negative the Fermi potential thermal coefficient).

Considering low voltage power MOSFETs working in linear zone in applications like air fans, it is important have devices with standard threshold voltage (around 3V in ambient temperature) and very low TVTC in absolute value, in order to avoid the thermal instability behavior that could bring the component to fail.

The modern MOSFETs have TVTC in the negative value range (it becomes more negative when the temperature increases). Therefore, when the device works in linear zone, a power pulse is dissipated on the component, the temperature increases, the threshold voltage decreases and the drain current rises.

To avoid the thermal run-away of the device, it is important to minimize the TVTC in absolute value. The parameters that make TVTC negative, considering an n-type gate and p-type silicon, are the metal-oxide work functions divided by the temperature and the term of the Fermi potential thermal coefficient. Instead, the parameter that makes TVTC positive is the Fermi potential divided by the temperature (T). As shown in (*Equation 32*), the metal-oxide work function divided by T depends on the doping concentration of the gate, silicon and the intrinsic carrier concentration. This parameter increases in absolute value, increasing the doping concentration of the gate or substrate, while it decreases in absolute value when the temperature increases because of the intrinsic carrier concentration increases too. In order to minimize this parameter, the gate and substrate doping concentration must be lowered.

The Fermi potential divided by T depends on the doping concentration of the substrate and the intrinsic concentration of the carriers. When the doping concentration of the substrate increases, the parameter also increases its value. By increasing the temperature, the parameter decreases because the intrinsic carrier concentration increases. In order to maximize the parameter, the substrate doping concentration should be increased.

The threshold voltage thermal coefficient (see *Equation 41*) depends on the Fermi potential divided by T, minus a constant and minus a term function of the inverse of T. Its value is negative because the parameter with the minus sign is generally higher than the term, due to the Fermi potential divided by T. When the temperature increases, the parameter also increases in absolute value because the Fermi potential decreases too. Thus, in order to minimize the Fermi potential thermal coefficient, the substrate doping concentration must be increased. However, the third term of (*Equation 42*), as previously explained, also depends on the substrate doping concentration root-square. Therefore, considering the modern MOSFET technology, this term increases in absolute value when the substrate doping concentration also increases.

In the modern device, it is possible to observe that TVTC (as described in *Equation 42*) increases in absolute value when the doping concentration also increases because the first and third components are higher than the second term.

Another important parameter in order to establish TVTC is the oxide thickness. This parameter only affects the third term of *Equation 42*. When the oxide thickness decreases, the third term in (*Equation 42*) also decreases and that involves in a TVTC lowering in absolute value.

A real example of threshold voltage and TVTC compared to the theoretical model implemented in this paper is shown below. The low voltage power MOSFET takes into consideration a device of 55V of breakdown voltage and 5mOhm of on resistance (production line DEVICE1). This device has a gate doping concentration (N_g) equals to 1e+20cm^{-3}, a substrate doping concentration peak in the channel (N_a) equals to 2e+17cm-3, an oxide thickness of 470Å and a channel length of 0.35µm.

The following table summarizes the main simulated electrical parameter function of T (T range is 250-400K), then some graphs highlight the DEVICE1 measured and simulated data.

Table 1. Main electrical parameter simulated by DEVICE1

T	Ni	Φ_{ms}	$\partial F_{ms}/\partial T$	Φ_{ms}/T	Φ_F	$\partial\Phi_F/\partial T$	Φ_F/T	V_{OX}	$\partial V_{OX}/\partial T$	V_{th}	$\partial V_{th}/\partial T$
250	9.67E+13	-1.058	0.000868	-0.00423	0.462	-0.00070	0.0018	3.40	-0.0026	3.27	-0.0031
255	1.73E+14	-1.053	0.000873	-0.00413	0.458	-0.00070	0.0018	3.39	-0.0026	3.25	-0.0031
260	3.02E+14	-1.049	0.000878	-0.00403	0.455	-0.00071	0.0017	3.38	-0.0026	3.24	-0.0032
265	5.18E+14	-1.045	0.000883	-0.00394	0.451	-0.00071	0.0017	3.36	-0.0026	3.22	-0.0032
270	8.70E+14	-1.040	0.000888	-0.00385	0.448	-0.00071	0.0017	3.35	-0.0027	3.21	-0.0032
275	1.43E+15	-1.036	0.000892	-0.00377	0.444	-0.00071	0.0016	3.34	-0.0027	3.19	-0.0032
280	2.33E+15	-1.031	0.000897	-0.00368	0.441	-0.00072	0.0016	3.32	-0.0027	3.17	-0.0032
285	3.71E+15	-1.027	0.000901	-0.00360	0.437	-0.00072	0.0015	3.31	-0.0027	3.16	-0.0033
290	5.82E+15	-1.022	0.000906	-0.00352	0.433	-0.00072	0.0015	3.30	-0.0027	3.14	-0.0033
295	9.00E+15	-1.018	0.000910	-0.00345	0.430	-0.00072	0.0015	3.28	-0.0028	3.12	-0.0033
300	1.37E+16	-1.013	0.000915	-0.00338	0.426	-0.00073	0.0014	3.27	-0.0028	3.11	-0.0033
305	2.07E+16	-1.009	0.000919	-0.00331	0.423	-0.00073	0.0014	3.25	-0.0028	3.09	-0.0033
310	3.07E+16	-1.004	0.000923	-0.00324	0.419	-0.00073	0.0014	3.24	-0.0028	3.07	-0.0034
315	4.50E+16	-0.999	0.000927	-0.00317	0.415	-0.00073	0.0013	3.23	-0.0028	3.06	-0.0034
320	6.53E+16	-0.995	0.000931	-0.00311	0.412	-0.00073	0.0013	3.21	-0.0029	3.04	-0.0034
325	9.37E+16	-0.990	0.000935	-0.00305	0.408	-0.00074	0.0013	3.20	-0.0029	3.02	-0.0034
330	1.33E+17	-0.985	0.000939	-0.00299	0.404	-0.00074	0.0012	3.18	-0.0029	3.01	-0.0034
335	1.87E+17	-0.981	0.000943	-0.00293	0.401	-0.00074	0.0012	3.17	-0.0029	2.99	-0.0035
340	2.60E+17	-0.976	0.000947	-0.00287	0.397	-0.00074	0.0012	3.15	-0.0029	2.97	-0.0035
345	3.59E+17	-0.971	0.000951	-0.00281	0.393	-0.00074	0.0011	3.14	-0.0030	2.95	-0.0035
350	4.90E+17	-0.966	0.000955	-0.00276	0.389	-0.00074	0.0011	3.12	-0.0030	2.94	-0.0035

Table 1. Main electrical parameter simulated by DEVICE1

T	Ni	Φ_{ms}	$\partial F_{ms}/\partial T$	Φ_{ms}/T	Φ_F	$\partial\Phi_F/\partial T$	Φ_F/T	V_{OX}	$\partial V_{OX}/\partial T$	V_{th}	$\partial V_{th}/\partial T$
355	6.64E+17	-0.962	0.000958	-0.00271	0.386	-0.00075	0.0011	3.11	-0.0030	2.92	-0.0035
360	8.93E+17	-0.957	0.000962	-0.00266	0.382	-0.00075	0.0011	3.09	-0.0030	2.90	-0.0036
365	1.19E+18	-0.952	0.000965	-0.00261	0.378	-0.00075	0.0010	3.08	-0.0031	2.88	-0.0036
370	1.58E+18	-0.947	0.000969	-0.00256	0.375	-0.00075	0.0010	3.06	-0.0031	2.87	-0.0036
375	2.07E+18	-0.942	0.000972	-0.00251	0.371	-0.00075	0.0010	3.05	-0.0031	2.85	-0.0036
380	2.70E+18	-0.937	0.000976	-0.00247	0.367	-0.00076	0.0010	3.03	-0.0031	2.83	-0.0037
385	3.51E+18	-0.933	0.000979	-0.00242	0.363	-0.00076	0.0009	3.02	-0.0031	2.81	-0.0037
390	4.52E+18	-0.928	0.000982	-0.00238	0.359	-0.00076	0.0009	3.00	-0.0032	2.79	-0.0037
395	5.78E+18	-0.923	0.000986	-0.00234	0.356	-0.00076	0.0009	2.99	-0.0032	2.77	-0.0037
400	7.36E+18	-0.918	0.000989	-0.00229	0.352	-0.00076	0.0009	2.97	-0.0032	2.76	-0.0038

Figure 6. DEVICE1 V_{TH} - comparison between simulated and measured data

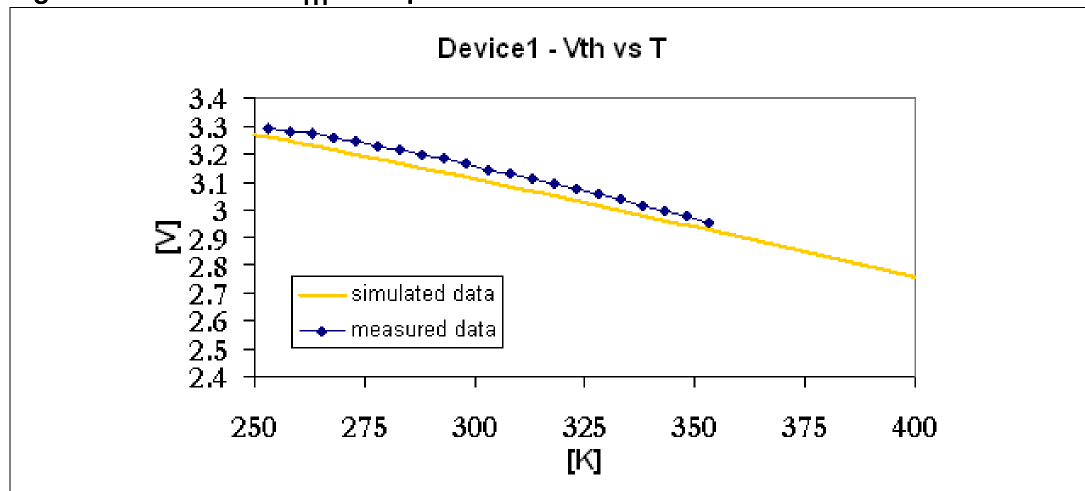
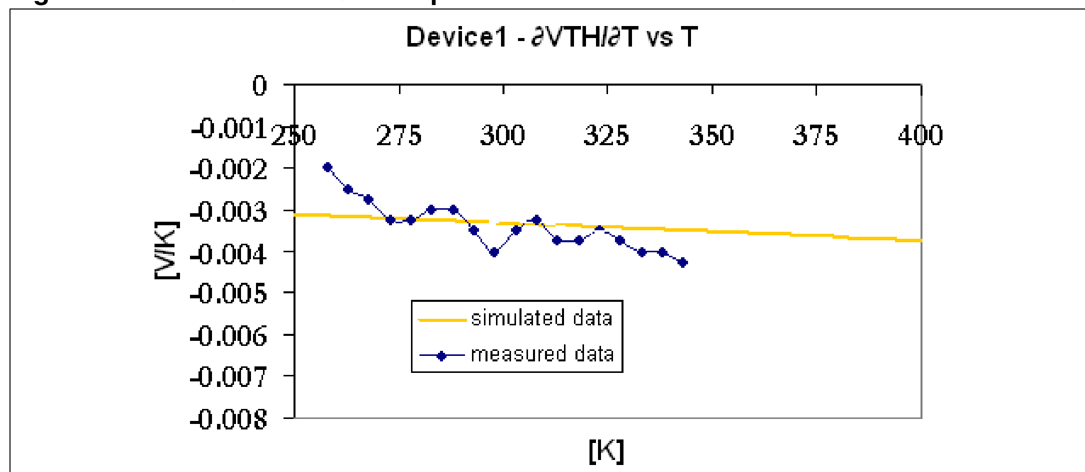
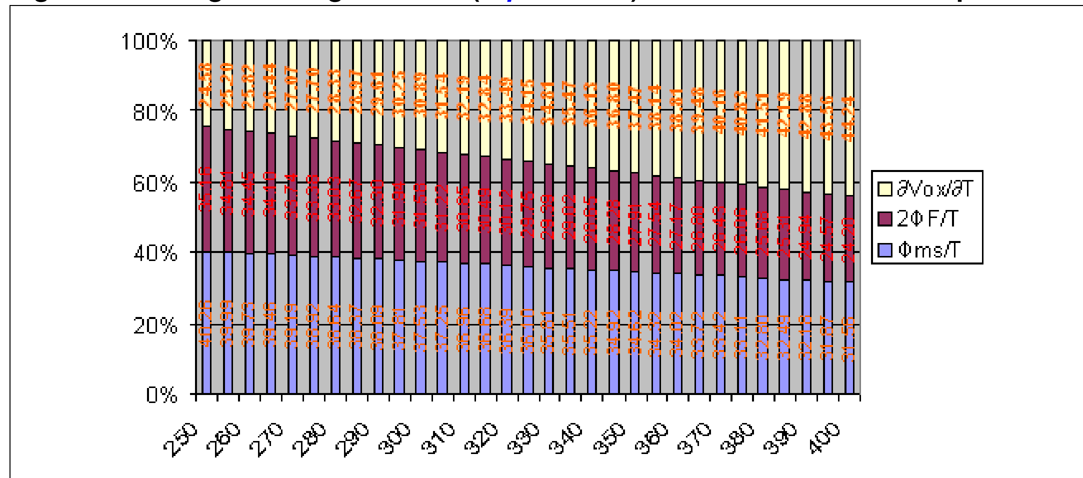


Figure 7. DEVICE1 TVTC - comparison between simulated and measured data



As shown in *Figure 6.* and *Figure 7.*, the data simulated and measured are quite close to each other. In this case, for DEVICE1, the threshold voltage is around 3.2V (standard V_{TH}) and TVTC is around 3mV/K at ambient temperature. In the next *Figure 8.* the contribution of each component of (*Equation 42*) is highlighted.

Figure 8. Weight of single term of (*Equation 42*) on TVTC at different temperatures



In the graph above it is possible see that at a low temperature, the higher weight in the TVTC formula is established by the parameters Φ_{ms}/T and $2\Phi_F/T$. The first term is negative and makes TVTC negative, while the second term in positive and makes TVTC positive. When the temperature increases, TVTC increases in absolute value because even if Φ_{ms}/T decreases, $2\Phi_F/T$ also decreases and in particular, the weight of $\partial V_{ox}/ \partial T$ increases too.

Another real example of threshold voltage and TVTC compared to the theoretical model implemented is shown below. The low voltage power MOSFET takes into consideration a device of 55V of breakdown voltage and 6.5mOhm of on resistance (production line DEVICE1). This device has a gate doping concentration (N_g) equal to 1e+20cm^{-3}, a substrate doping concentration peak in the channel (N_a) equal to 1e+17cm^{-3}, an oxide thickness of 350Å and a channel length of 0.35µm. The following tab summarizes the main simulated electrical parameter function of T (T range is 250-400K) and then a graphs highlights the DEVICE2 measured and simulated data.

Table 2. Main electrical parameter simulated by DEVICE2

T	ni	Φ_{ms}	$\partial_{ms}/\partial T$	Φ_{ms}/T	Φ_F	$\partial\Phi_F/\partial T$	Φ_F/T	V_{OX}	$\partial V_{OX}/\partial T$	V_{th}	$\partial V_{th}/\partial T$
250	9.67E+13	-1.043	0.000927	-0.00417	0.447	-0.00076	0.0018	1.76	-0.0015	1.61	-0.0021
255	1.73E+14	-1.038	0.000932	-0.00407	0.443	-0.00076	0.0017	1.75	-0.0015	1.60	-0.0021
260	3.02E+14	-1.033	0.000937	-0.00397	0.439	-0.00077	0.0017	1.74	-0.0015	1.59	-0.0021
265	5.18E+14	-1.029	0.000942	-0.00388	0.436	-0.00077	0.0016	1.74	-0.0015	1.58	-0.0021
270	8.70E+14	-1.024	0.000947	-0.00379	0.432	-0.00077	0.0016	1.73	-0.0015	1.57	-0.0021
275	1.43E+15	-1.019	0.000952	-0.00371	0.428	-0.00077	0.0016	1.72	-0.0016	1.56	-0.0022
280	2.33E+15	-1.015	0.000957	-0.00362	0.424	-0.00078	0.0015	1.71	-0.0016	1.55	-0.0022
285	3.71E+15	-1.010	0.000961	-0.00354	0.420	-0.00078	0.0015	1.71	-0.0016	1.54	-0.0022
290	5.82E+15	-1.005	0.000966	-0.00347	0.416	-0.00078	0.0014	1.70	-0.0016	1.53	-0.0022

Table 2. Main electrical parameter simulated by DEVICE2

T	ni	Φ_{ms}	$\partial_{ms}/\partial T$	Φ_{ms}/T	Φ_F	$\partial\Phi_F/\partial T$	Φ_F/T	V_{OX}	$\partial V_{OX}/\partial T$	V_{th}	$\partial V_{th}/\partial T$
295	9.00E+15	-1.000	0.000970	-0.00339	0.412	-0.00078	0.0014	1.69	-0.0016	1.51	-0.0022
300	1.37E+16	-0.995	0.000974	-0.00332	0.408	-0.00078	0.0014	1.68	-0.0016	1.50	-0.0022
305	2.07E+16	-0.990	0.000979	-0.00325	0.404	-0.00079	0.0013	1.67	-0.0016	1.49	-0.0022
310	3.07E+16	-0.985	0.000983	-0.00318	0.400	-0.00079	0.0013	1.67	-0.0016	1.48	-0.0022
315	4.50E+16	-0.980	0.000987	-0.00311	0.397	-0.00079	0.0013	1.66	-0.0017	1.47	-0.0022
320	6.53E+16	-0.976	0.000991	-0.00305	0.393	-0.00079	0.0012	1.65	-0.0017	1.46	-0.0023
325	9.37E+16	-0.971	0.000995	-0.00299	0.389	-0.00080	0.0012	1.64	-0.0017	1.45	-0.0023
330	1.33E+17	-0.966	0.000999	-0.00293	0.385	-0.00080	0.0012	1.63	-0.0017	1.44	-0.0023
335	1.87E+17	-0.961	0.001003	-0.00287	0.381	-0.00080	0.0011	1.62	-0.0017	1.42	-0.0023
340	2.60E+17	-0.956	0.001007	-0.00281	0.377	-0.00080	0.0011	1.61	-0.0017	1.41	-0.0023
345	3.59E+17	-0.951	0.001011	-0.00276	0.373	-0.00080	0.0011	1.61	-0.0017	1.40	-0.0023
350	4.90E+17	-0.945	0.001014	-0.00270	0.369	-0.00080	0.0011	1.60	-0.0017	1.39	-0.0023
355	6.64E+17	-0.940	0.001018	-0.00265	0.365	-0.00081	0.0010	1.59	-0.0018	1.38	-0.0024
360	8.93E+17	-0.935	0.001022	-0.00260	0.361	-0.00081	0.0010	1.58	-0.0018	1.37	-0.0024
365	1.19E+18	-0.930	0.001025	-0.00255	0.356	-0.00081	0.0010	1.57	-0.0018	1.35	-0.0024
370	1.58E+18	-0.925	0.001029	-0.00250	0.352	-0.00081	0.0010	1.56	-0.0018	1.34	-0.0024
375	2.07E+18	-0.920	0.001032	-0.00245	0.348	-0.00081	0.0009	1.55	-0.0018	1.33	-0.0024
380	2.70E+18	-0.915	0.001035	-0.00241	0.344	-0.00082	0.0009	1.54	-0.0018	1.32	-0.0024
385	3.51E+18	-0.910	0.001039	-0.00236	0.340	-0.00082	0.0009	1.53	-0.0018	1.31	-0.0024
390	4.52E+18	-0.904	0.001042	-0.00232	0.336	-0.00082	0.0009	1.53	-0.0019	1.29	-0.0025
395	5.78E+18	-0.899	0.001045	-0.00228	0.332	-0.00082	0.0008	1.52	-0.0019	1.28	-0.0025
400	7.36E+18	-0.894	0.001049	-0.00223	0.328	-0.00082	0.0008	1.51	-0.0019	1.27	-0.0025

Figure 9. DEVICE2 V_{TH} - comparison between simulated and measured data

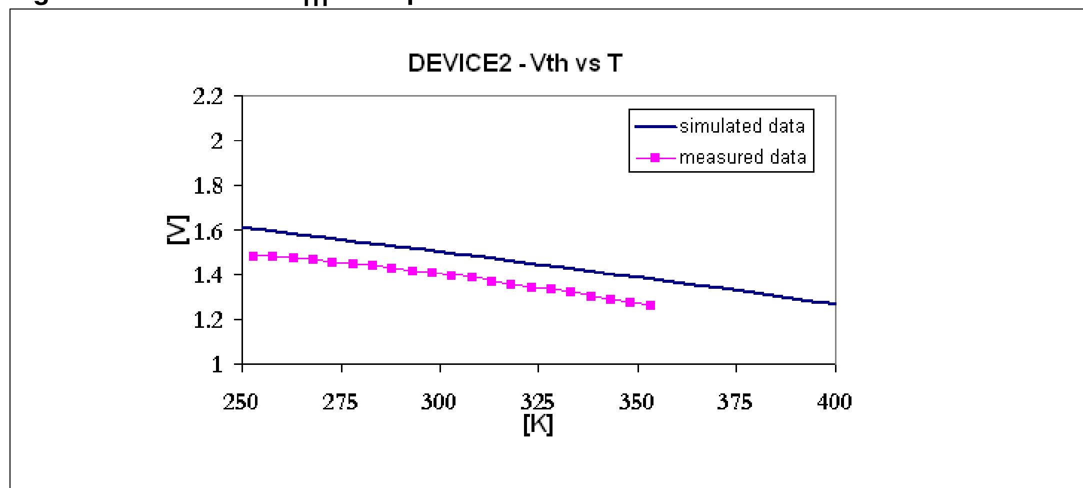
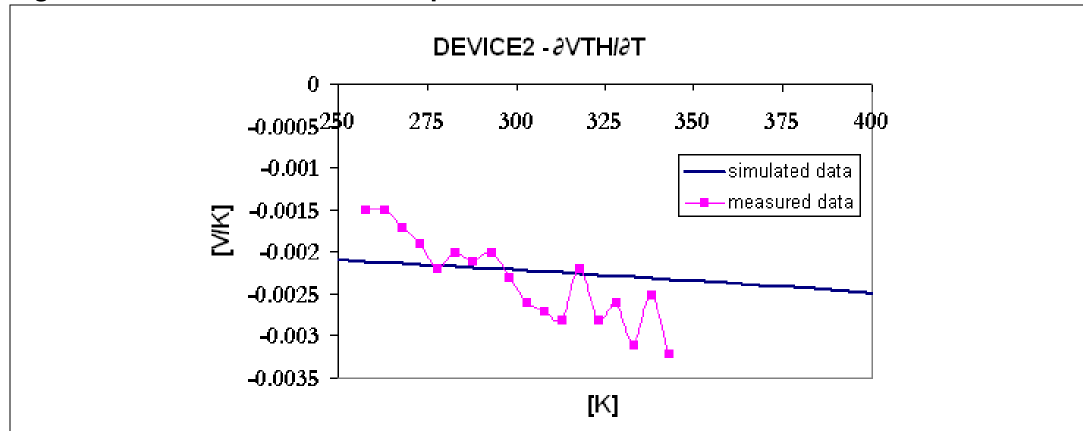


Figure 10. DEVICE2 TVTC - comparison between simulated and measured data



Also in this new case, the data simulated and measured are quite close to each other. In this case, for DEVICE2, the threshold voltage is around 1.5V and TVTC is around 2mV/K at ambient temperature.

Now it is possible to consider the DEVICE1 device and simulate the V_{TH} and TVTC thermal behavior changing N_g, N_a and t_{ox} respectively.

At the beginning, the thermal behavior increasing and decreasing the gate doping concentration is simulated (see *Figure 11.* and *Figure 12.*).

Figure 11. DEVICE1 V_{TH} simulated data - comparison between different N_g

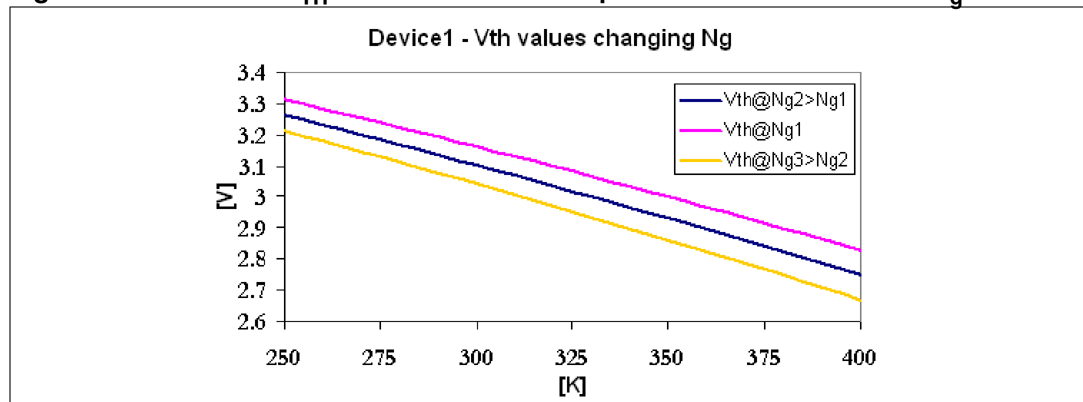
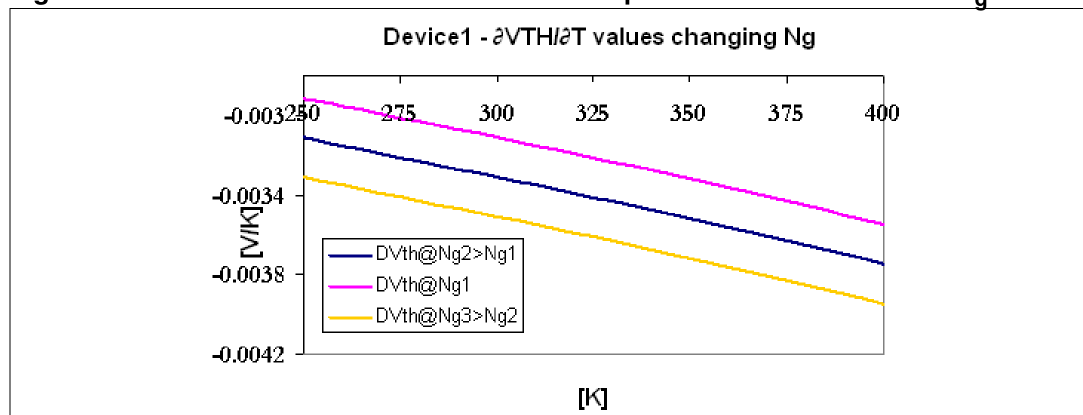


Figure 12. DEVICE1 TVTC simulated data - comparison between different N_g



When the gate concentration doping increases from 1e+20cm^{-3} to 1e+21cm^{-3} the threshold voltage decreases its value, while, TVTC increases in absolute value and vice versa, decreasing the gate concentration doping from 1e+20cm^{-3} to 1e+19cm^{-3}. Now, the thermal behavior increasing and decreasing the substrate doping concentration is simulated (see *Figure 13.* and *Figure 14.*).

Figure 13. DEVICE1 V_{TH} simulated data - comparison between different N_a

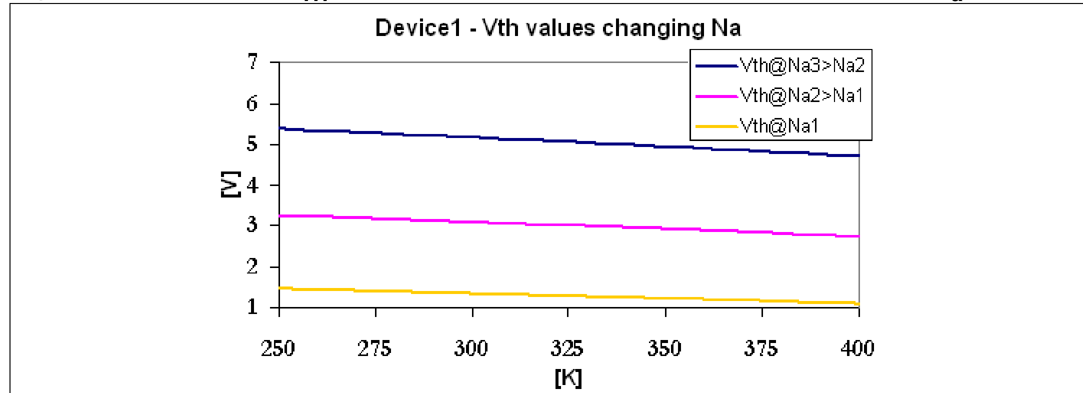
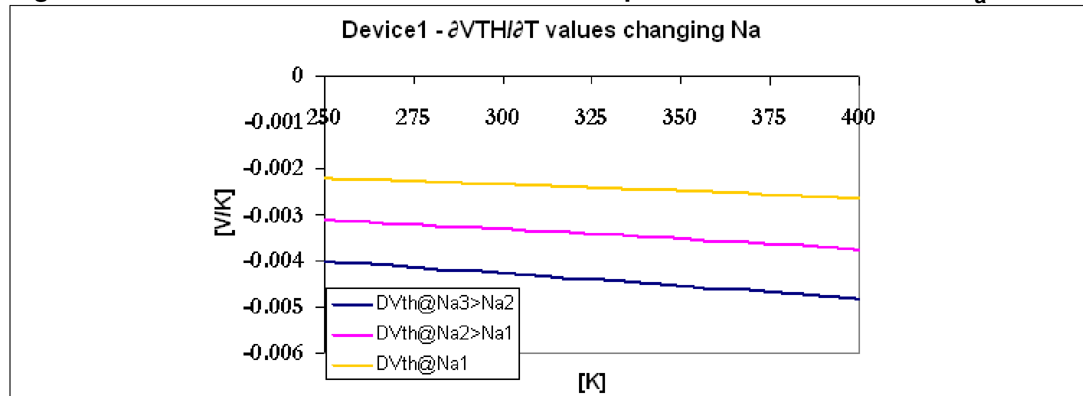


Figure 14. DEVICE1 TVTC simulated data - comparison between different N_a



When the substrate concentration doping increases from 2e+17cm^{-3} to 5e+17cm^{-3} the threshold voltage increases its value and also TVTC increases in absolute value and vice versa, decreasing the substrate concentration doping from 2e+17cm^{-3} to 5e+16cm^{-3}. Now, the case of different thickness oxide will be studied (see *Figure 15.* and *Figure 16.*).

Figure 15. DEVICE1 V_{TH} simulated data - comparison between different t_{ox}

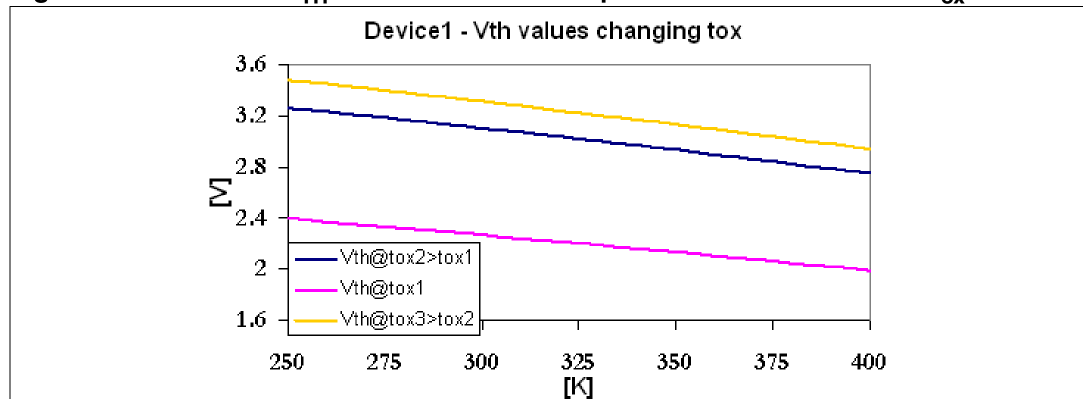
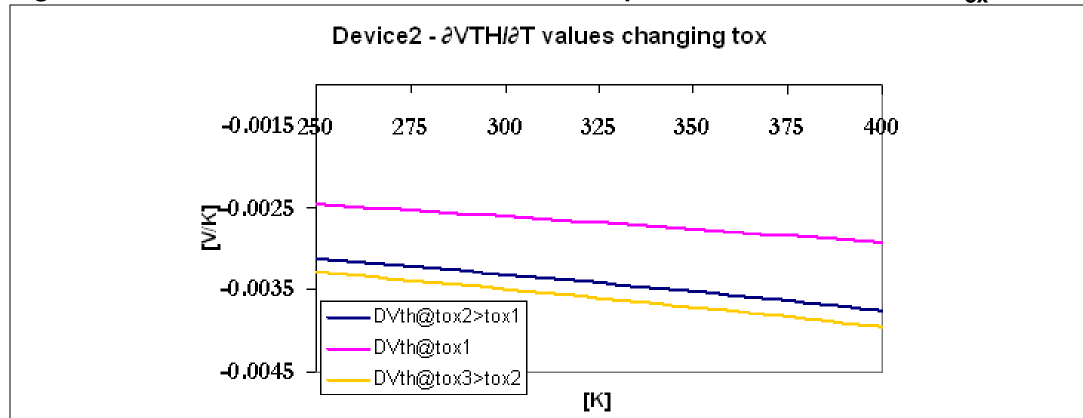


Figure 16. DEVICE1 TVTC simulated data - comparison between different t_{ox}



When the oxide thickness increases from 470Å to 500Å, the threshold voltage increases its value and also TVTC increases in absolute value and vice versa, decreases the thickness oxide from 470Å to 350Å. Now, it is possible simulate V_{TH} and TVTC supposing that the temperature is fixed to 300K and the gate doping concentration changes in the range of 1e+18-1.5e+20cm^{-3} (see *Figure 17.* and *Figure 18.*).

Figure 17. DEVICE1 V_{TH} simulated data - fixing T and acting on N_g

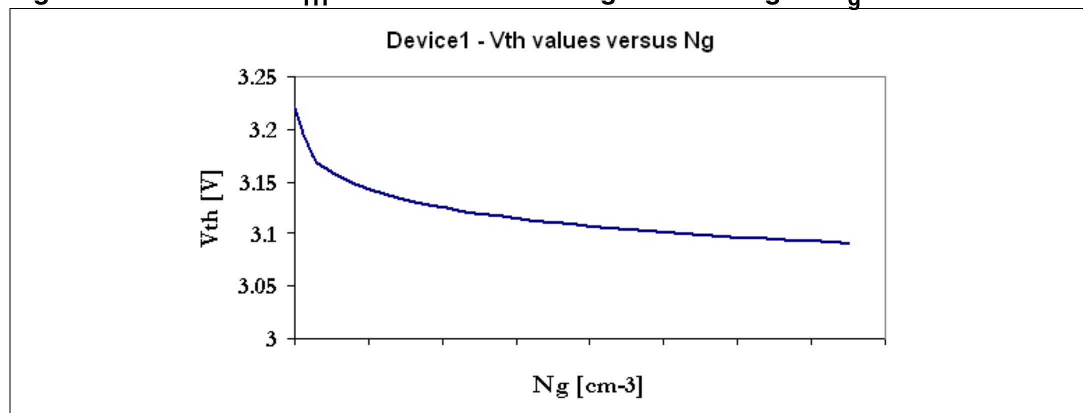
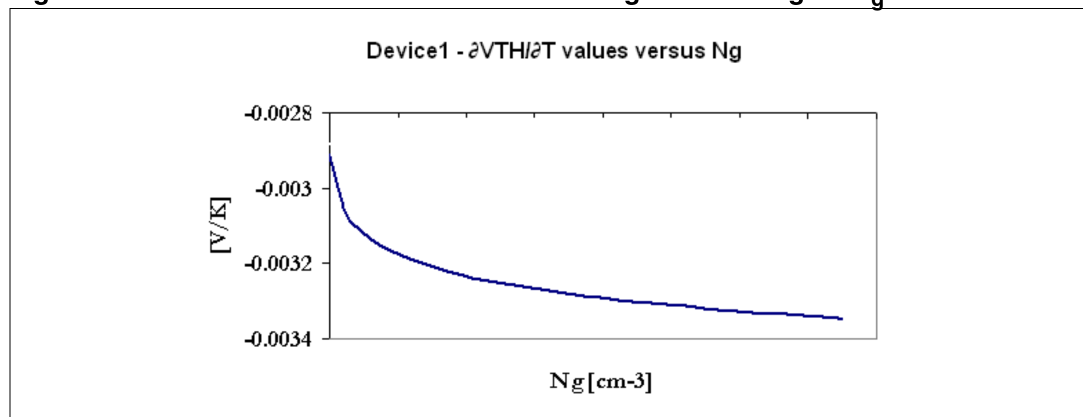


Figure 18. DEVICE1 TVTC simulated data - fixing T and acting on N_g



The graph in *Figure 19.* and *Figure 20.* show V_{TH} and TVTC trend fixing the temperature to 300K and changing N_a in the range of 1e+16-6.1e+17cm^{-3}.

Figure 19. DEVICE1 V_{TH} simulated data - fixing T and acting on N_a

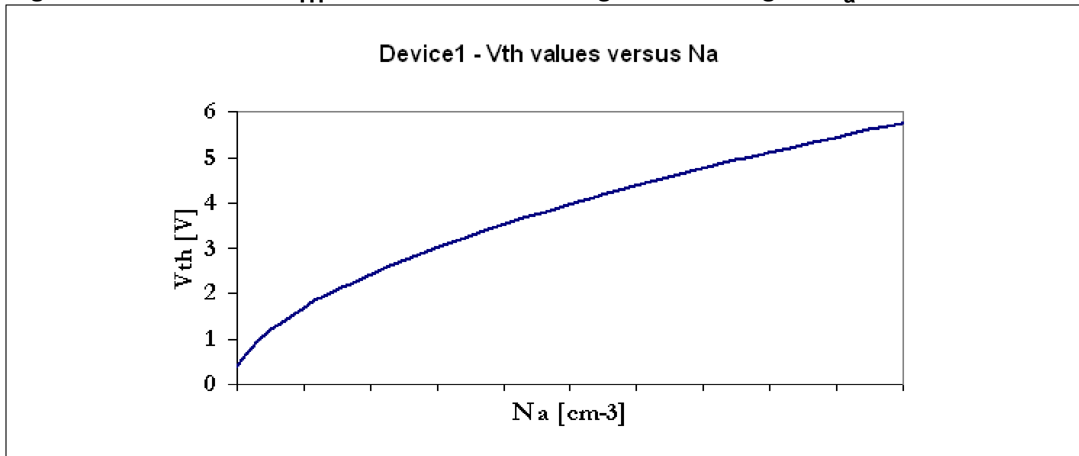
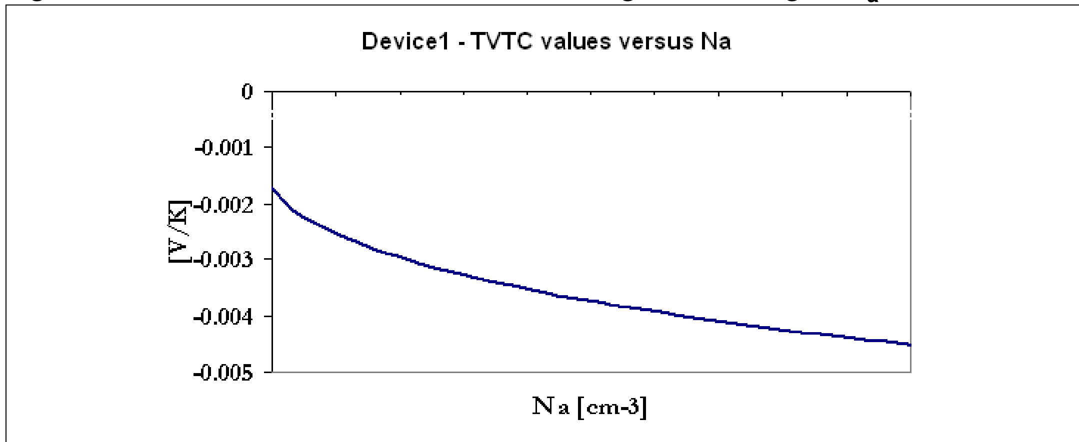


Figure 20. DEVICE1 TVTC simulated data - fixing T and acting on N_a



The graph in*Figure 21.* and *Figure 22.* shows V_{TH} and TVTC trend fixing the temperature to 300K and changing t_{ox} in the range of 300-600Å.

Figure 21. DEVICE1 V_{TH} simulated data - fixing T and acting on t_{ox}

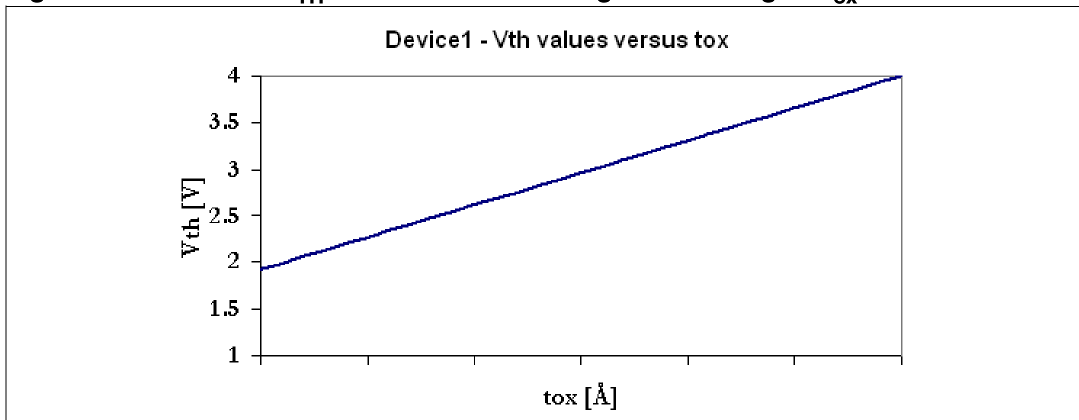
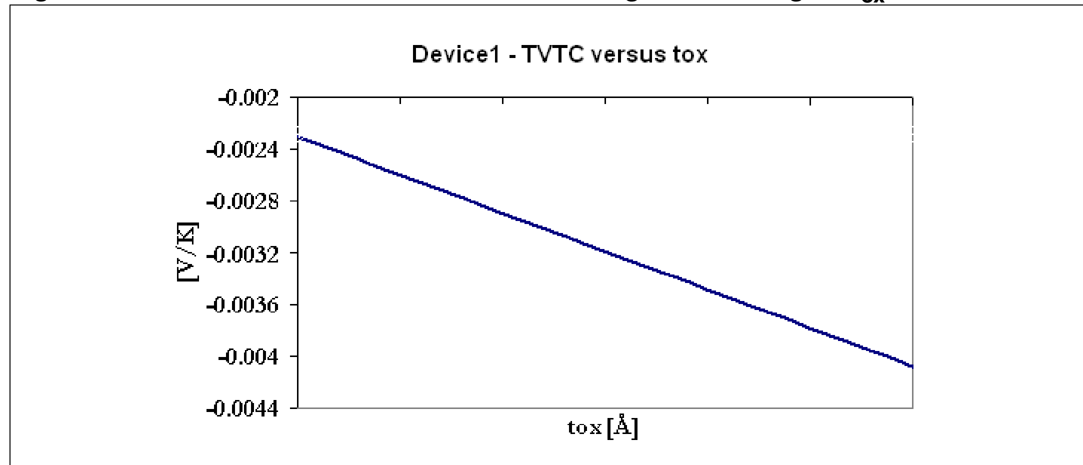


Figure 22. DEVICE1 TVTC simulated data - fixing T and acting on t_{ox}



The next graphs show the simulated data of V_{TH} and TVTC considering DEVICE1 and a hypothetical new device with standard threshold voltage and minimized TVTC. This device is obtained changing on N_a, N_g and t_{ox} together. For example, this new device has N_g is equal to 1e+18cm^{-3}, N_a is equal to 3e+17cm^{-3} and tox is equal to 350Å.

Figure 23. V_{TH} simulated data - comparison between DEVICE1 and the new device

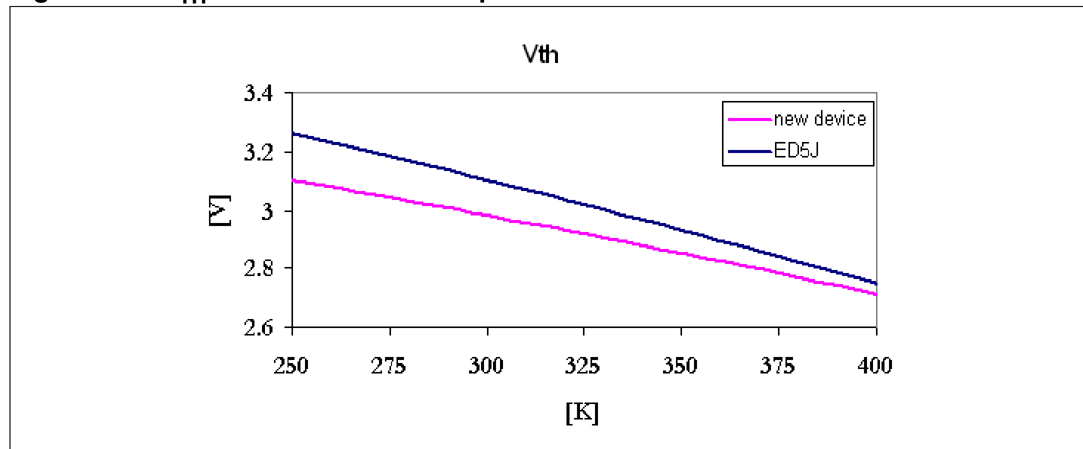
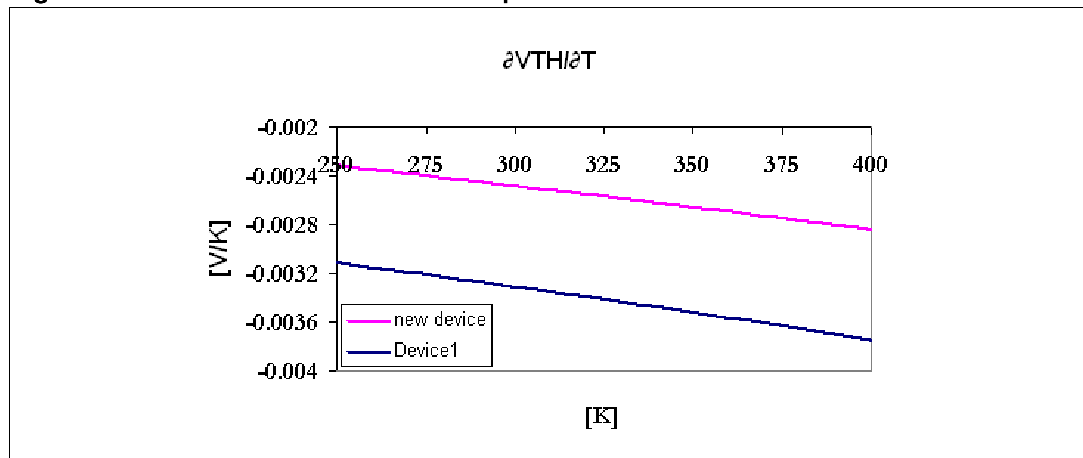


Figure 24. TVTC simulated data - comparison between DEVICE1 and the new device



It is possible see that by rearranging N_g, N_a and tox the threshold voltage remains fixed and TVTC decreases in absolute value.

Finally, the following graphs highlight the V_{TH} and TVTC trend simulates a p-type gate doped MOS with N_g equal to 1e+21cm^{-3}, N_a is equal to 3e+16cm^{-3} and t_{ox} is equal to 470Å.

Figure 25. V_{TH} simulated data considering a p-gate doped MOS

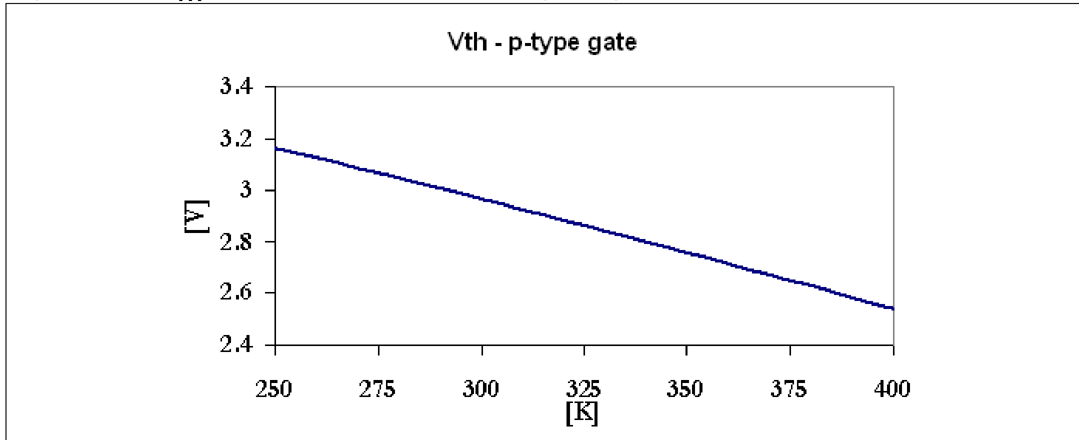
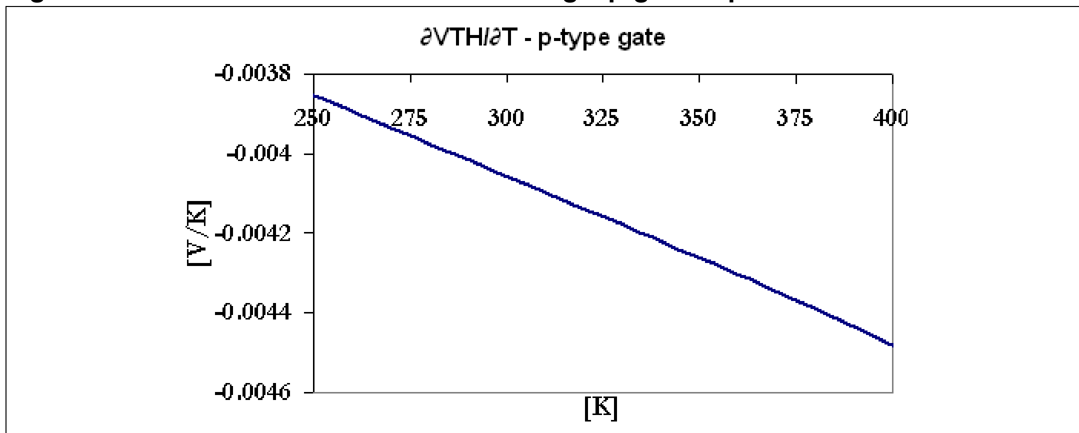


Figure 26. TVTC simulated data considering a p-gate doped MOS



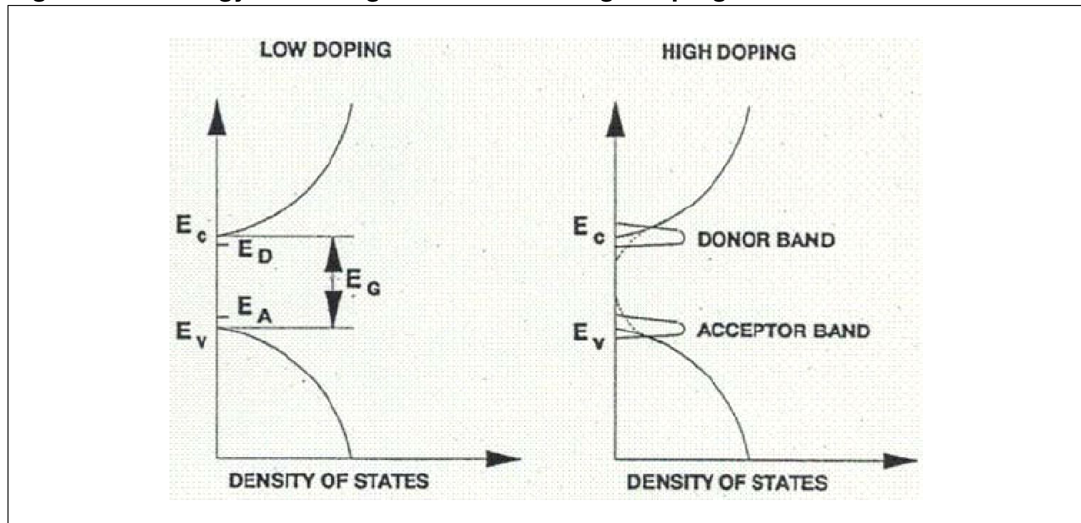
The only difference with the n-type doped gate is that increasing the gate doping concentration, TVTC decreases in absolute value instead of increasing.

3 Case of DEVICE3

The device DEVICE3 has similar characteristics of DEVICE1 in terms of tox (470Å), gate doping (1e+20cm^{-3}), silicon doping (2.4e+17cm^{-3}) and breakdown voltage 55V. The main difference between the two devices consists in the channel length (0.8µm) and the source doping thermal process activation; DEVICE3 perform a form while DEVICE1 an RTA thermal process.

The only difference on the length channels between the two devices should not have an effect on the threshold voltage and TVTC. Instead, the different source thermal process doping activation could bring a variation on the TVTC because the net charge peak concentration in the channel near the source well is higher in the silicon processed in the form compared to the RTA one. In fact, when the net charge concentration in the silicon overcomes typically 1e+17[cm^{-3}], a band-gap narrowing effect occurs (see *Figure 27.*) because new impurity band states are created inside the forbidden silicon band near the conduction and valence edges.

Figure 27. Energy band diagram at low and high doping concentration



In order to consider this effect the Slotboom-De Graaf model is used.

Equation 46

$$\Delta E_g = b_1 T \left\{ \ln\frac{N_T}{10^{17}} + \left[\left(\ln - \right)^2 + 0.5 \right]^{\frac{1}{2}} \right\}$$

ΔEg is the band-gap narrowing value; N_T (expressed in cm^{-3}) is the net charge concentration (the sum of acceptor and donor doping elements concentration).

The net charge concentration is not easy to establish so, in order to fit the real data, a net charge concentration of 3.5e+17cm^{-3} was considered for DEVICE3.

The real data on DEVICE3 using RTA process are shown in the following figures where are compared to the simulated and the data of the device using the form process.

Figure 28. DEVICE3 V_{TH} - comparison between simulated and measured data

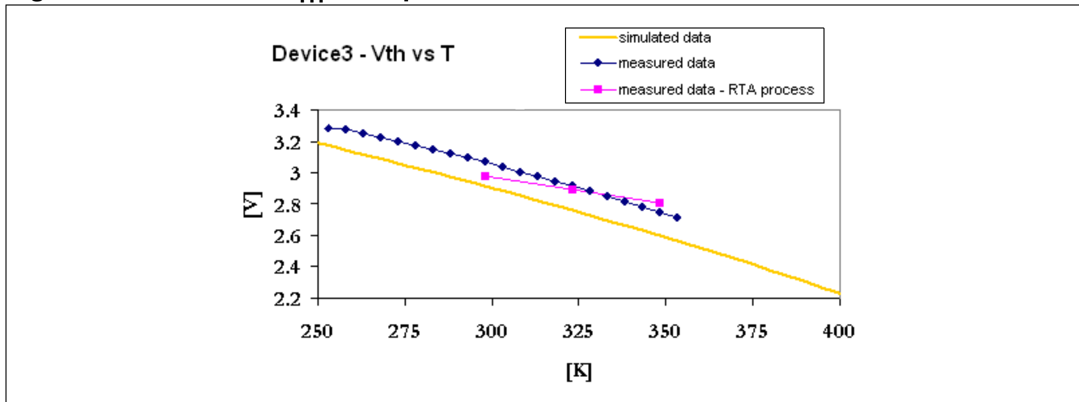
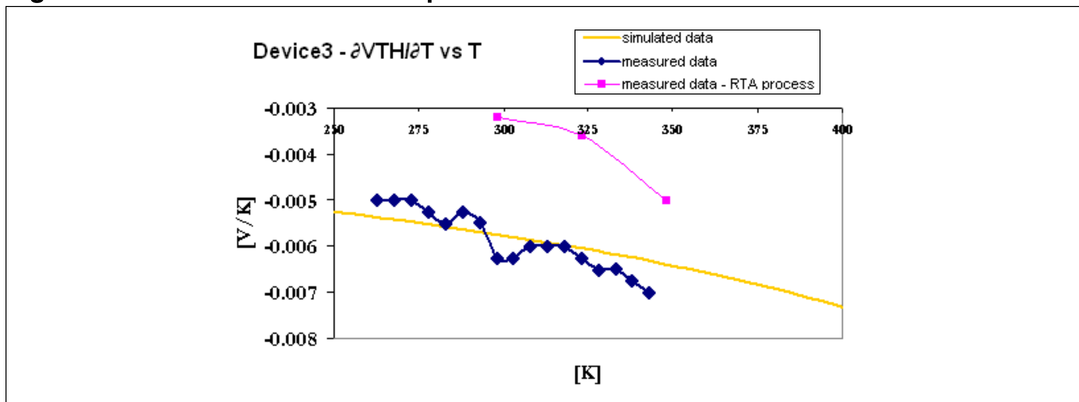


Figure 29. DEVICE3 TVTC - comparison between simulated and measured data



Also in this case, the simulated data and the measured data are close to each other.

4 Conclusions

This paper has studied the effect of the temperature on the MOSFET threshold voltage and its thermal coefficient. In particular, a mathematical model for both parameters was achieved and a comparison with real measurement was performed considering three low voltage power MOSFET devices by ST; DEVICE1, DEVICE2 and DEVICE3. The simulated and real data obtained for all the devices under test are quite close and, thus confirming the validation of the theory.

The model has highlighted that, in order to decreases in absolute value TVTC to avoid thermal run-away of the device, the thickness oxide, silicon and the gate doping concentration must be decreased. However, minimizing TVTC and obtaining a standard threshold voltage device can't be done by decreasing the three parameters together, they must be rearranged as in the example shown in *Figure 23.* and *Figure 24.* of this article. Another important result shown in this paper regards the example of the device DEVICE3. In this case, the higher total charge concentration in the channel involves a band-gap narrowing that increases in absolute value TVTC and makes the device more thermally instable.

5 References

- Introduction on semiconductor materials
  – Au. Tyagi - Ed. Wiley&Sons
- Atlas User's Manual Vol.I - February 2000
  – Silvaco International
- Mutual Compensation of Mobility and Threshold Voltage Temperature Effects with Applications in CMOS Circuit
  – Au. I.M. Filanovsky A. Allam Ed. IEEE Vol. 48 No. 7, July 2001

6 Revision history

Table 3. Revision history

Date	Revision	Changes
13-Jun-2006	1	Initial release.

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