AN2366
Application note

Guidelines for migrating ST72F324 or ST72324 (ROM) applications to ST72F324B or ST72324B (ROM)

Introduction

This application note provides information on using ST72F324B, ST72324B (ROM) microcontroller devices in applications originally designed for the ST72F324 and ST72324 (ROM) series.

Table 1.   Migration cross-reference table

From	To	Description
ST72F324, ST72324	ST72F324B, ST72324B	8K to 32K program memory, 32-pin and 42-/44-pin

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1 ST72F324 migration: feature overview

Table 2. Feature overview

Feature[1]	ST72F324	ST72324 ROM	ST72F324B	ST72324B ROM
Package	TQFP44 (10x10) / SDIP42[2]/ TQFP32 (7x7) / SDIP32			
Program memory	8K to 32K			
RAM	384 bytes to 1 Kbyte			
Operating supply	3.8V to 5.5V			
Register map	128 bytes			
I/Os	32/24 Multifunction bidirectional lines 22/17 Alternate function lines 12/10 High sink outputs			
Power saving modes	Slow / Wait / Active Halt / Halt	Slow / Wait / Active Halt / Halt	Slow / Wait / Active Halt / Halt[3]	Slow / Wait / Active Halt / Halt[3]
Nested interrupts	Yes			
MCC / RTC	Yes			
Watchdog	Yes			
16-bit timer (OC / IC / PWM)	2 Timers (3/3/2)[4]	2 Timers (3/3/2)	2 Timers (3/3/2)	2 Timers (3/3/2)
SPI	Yes	Yes	Yes	Yes
SCI	Yes	Yes	Yes	Yes
ADC	Yes	Yes	Yes[5]	Yes[5]
LVD	Yes	No	Yes	Yes[6]
Emulator	ST7MDT20J-EMU3 and ST7MTD20-DVP3 (for Flash devices only)			
Programming tools	ST7MDT20J-EPB and ST7MTD20-DVP3 (for Flash devices only)			

1. Refer to the corresponding datasheets for more information.

2. SDIP42 / SDIP32 packages are valid only for non-automotive devices.

3. Exit from Active Halt mode available with external interrupts.

4. The TAOC2HR and TAOC2LR registers are write only; reading them will return undefined values and OCF2 flag in the TACSR register cannot be used (forced to '0' by hardware).

5. Improved ADC accuracy.

6. For 8K and 16K devices, Readout Protection is not supported if LVD is enabled.

2 Feature compatibility

2.1 V_{DD} Rise time

Some timing differences exist between the products (see *Table 3*). The application must ensure that the power supply ramps up within the time window specified for the microcontroller if LVD is ON.

Table 3. V_{DD} Rise time

Symbol	Description	Device	Conditions	Min	Max
Vt_{POR}	V_{DD} Rise time	ST72324	LVD on	6µs/V	Infinite ms/V
		ST72324B (8K and 16K)			20ms/V
		ST72324B (32K)			Infinite ms/V
		ST72F324, ST72F324B			100ms/V

2.2 Asynchronous $\overline{\text{RESET}}$ pin

The V_{IL}/V_{IH} of $\overline{\text{RESET}}$ pin has been changed from $0.16V_{DD}/0.85V_{DD}$ to $0.3V_{DD}/0.7V_{DD}$ respectively (see *Table 4*).

Table 4. $\overline{\text{RESET}}$ pin characteristics

	ST72F324, ST72324		ST72F324B, ST72324B	
	Min	**Max**	**Min**	**Max**
V_{IL}	-	$0.16 \times V_{DD}$	-	$0.3 \times V_{DD}$
V_{IH}	$0.85 \times V_{DD}$	-	$0.7 \times V_{DD}$	-

2.3 Oscillator pad

The ST72324B (32K Flash and ROM devices only) features a new oscillator pad which is more tolerant of the crystal type and is not disturbed if the oscillator pins are left unconnected. When migrating to these devices, the MCU needs to be validated with your existing resonator / crystal.

3 Performance improvements

The ST72F324B devices feature many significant improvements such as:

● Reduced PLL clock jitter

● Lower power consumption

● Improved A/D converter accuracy and negative injection on robust pins

Refer to the relevant datasheets for more details.

4 Limitations summary

Table 5. Limitation comparison table[1]

Limitations	ST72F324	ST72324 ROM	ST72F324B	ST72324B ROM
Unexpected reset fetch	X	X	X	X
I/O Port A & F configuration	✔	X[2]	✔	X[2]
16-bit timer PWM mode	X	X	X	X
SCI Wrong break duration	X	X	X	X
Clearing active interrupts outside interrupt routine	X	X	X	X
External interrupt missed	X	X	X	X
TIMD set simultaneously with OC interrupt	X	X	X	X
Internal RC operation	X[3]	X	✔	✔
Active Halt wake-up by external interrupt	X[4]	X[4]	✔	✔
Negative injection current immunity on analogic pins	X[5]	X[5]	✔	✔
V_{IH}(min) / V_{IL}(max) 0.7 x V_{DD} / 0.3 x V_{DD} on reset pin	X[6]	X[6]	✔	✔
LVD/AVD operation	✔	X[7]	✔	✔[8]
Active Halt mode power consumption	X[9]	X[9]	✔	✔[10]
External clock source with PLL	✔	X[11]	✔	✔
ICC mode entry with 39 pulses	✔	✔	X[12]	✔
Safe connection of OSC1/OSC2 pins	X	X	✔[13]	✔[13]
Negative current injection on pin PB0	X	✔	✔[14]	✔

1. Please refer to known limitations section in the datasheet.
2. For 8K/16K devices only.
3. Internal RC oscillator operation is not supported if LVD is disabled.
4. Only Reset or MCC/RTC interrupt can be used to exit from the Active Halt mode.
5. Negative injection current on any of the analog input pins significantly reduces the accuracy of ADC.
6. V_{IH}(min) and V_{IL}(max) on reset pin is 0.85 x V_{DD} and 0.16 x V_{DD} respectively.
7. LVD is not guaranteed.
8. For 8K/16K devices, if Readout Protection is selected, LVD may cause the product to become stuck in the reset state.
9. Max power consumption in Active Halt mode is not guaranteed.
10. For 32K ROM devices, the power consumption in Active Halt mode is 190µA typical and 300µA maximum.
11. External clock source is not supported with PLL enabled.
12. Not supported for 8K/16K devices.
13. For 32K devices only.
14. Negative current injection is allowed only for 32K devices. For 8K/16K devices, limitation is still present.

Legend:

X - Limitation occurs.
✔ - No limitation.

5 Revision history

Table 6.   Document revision history

Date	Revision	Changes
07-Aug-2006	1	Initial release
01-Jul-2009	2	Updated *Table 2: Feature overview* and *Table 5: Limitation comparison table*.

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