AN2269
Application Note

Using the ST8024 Smartcard Interface

Introduction

This application note provides information and suggestions for the optimal use and performance of the ST8024 Smartcard Interface, including PCB layout, external component placement, and connections (see *ST8024 Application Hardware Guidelines on page 16*).

The ST8024 is a smart card interface designed to minimize microprocessor hardware and software complexity in all applications that require a smart card (e.g., Set Top Box, Electronic Payment, Pay TV, and Identification cards). It was developed in accordance with New Digital Systems (NDS) conditional access requirements, and implements all of the blocks and procedures for card activation/deactivation and checking (see *Figure 1*).

Figure 1. ST8024 Internal Block Diagram

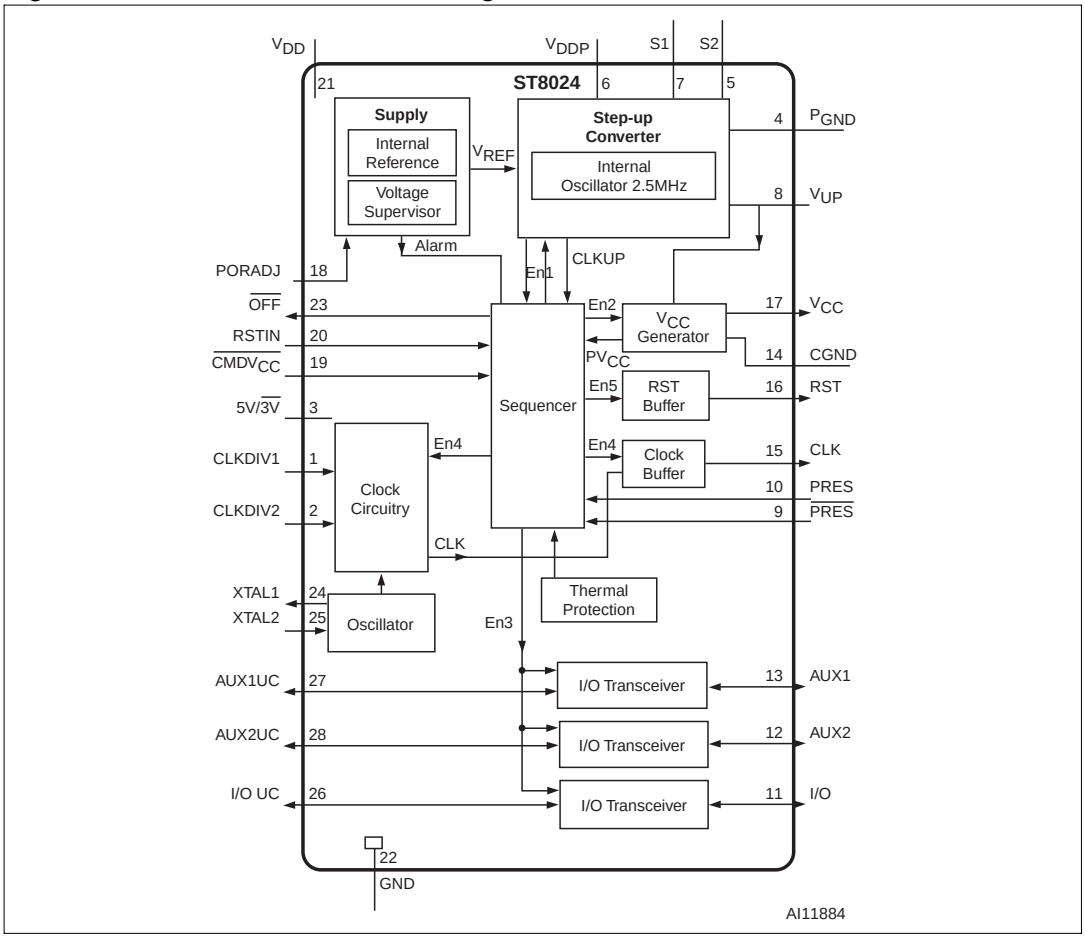


Table of Contents

List of Figures

1 Activation/Deactivation Sequence

The core of the ST8024 is the sequencer (shown in *Figure 1 on page 1*) that must coordinate the Enable signals for the activation and deactivation sequence as well as check for possible fault conditions. This because the smart card is basically a microcontroller and needs to be activated/deactivated by a correct sequence as required by the ISO/IEC7816 standard. The ST8024 activation and deactivation sequences are shown in *Figure 2* and *Figure 3 on page 5*, respectively. Please refer to the ST8024 datasheet for details.

Figure 2 shows that the PRES condition is true ($\overline{PRES}$ = low or PRES = high), and $\overline{CMDVcc}$ goes low. The activation sequence starts and the first block to be enabled is the step-up converter (V_{UP}), linked to En1 (see *Figure 1*), while the last enabled signal is the RST that allows the card software to start.

Figure 3 shows the deactivation sequence (when the $\overline{CMDVcc}$ goes high). The circuit executes an automatic deactivation sequence, finishing in the inactive state after t_{de} (deactivation time).

Figure 2. ST8024 Activation Sequence

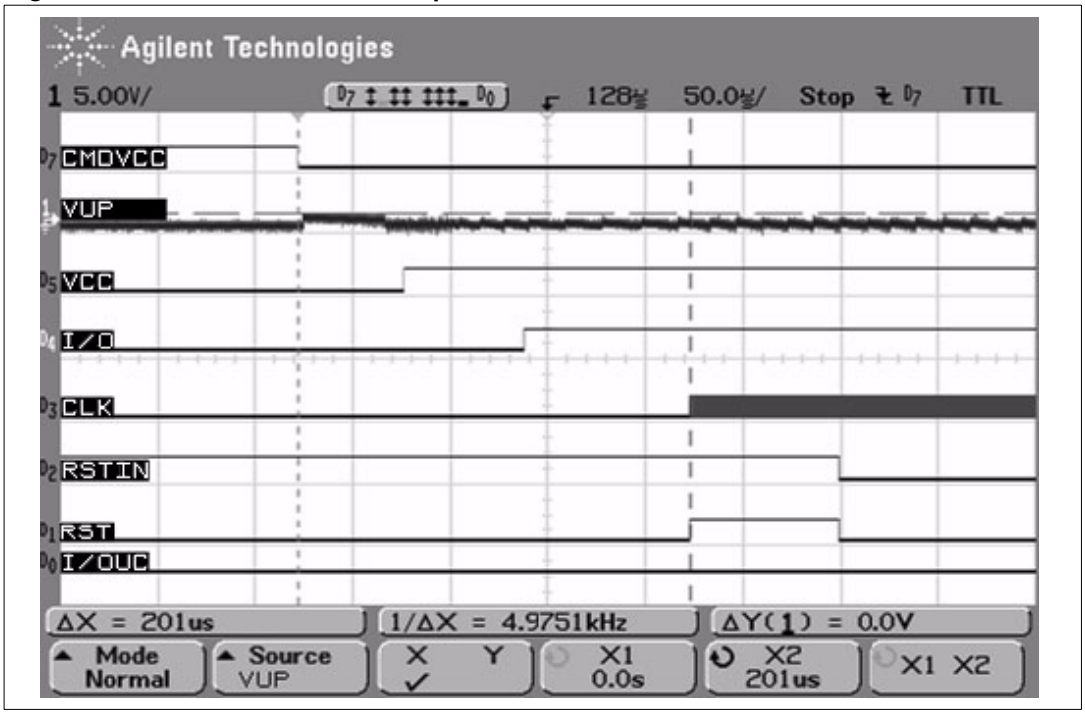
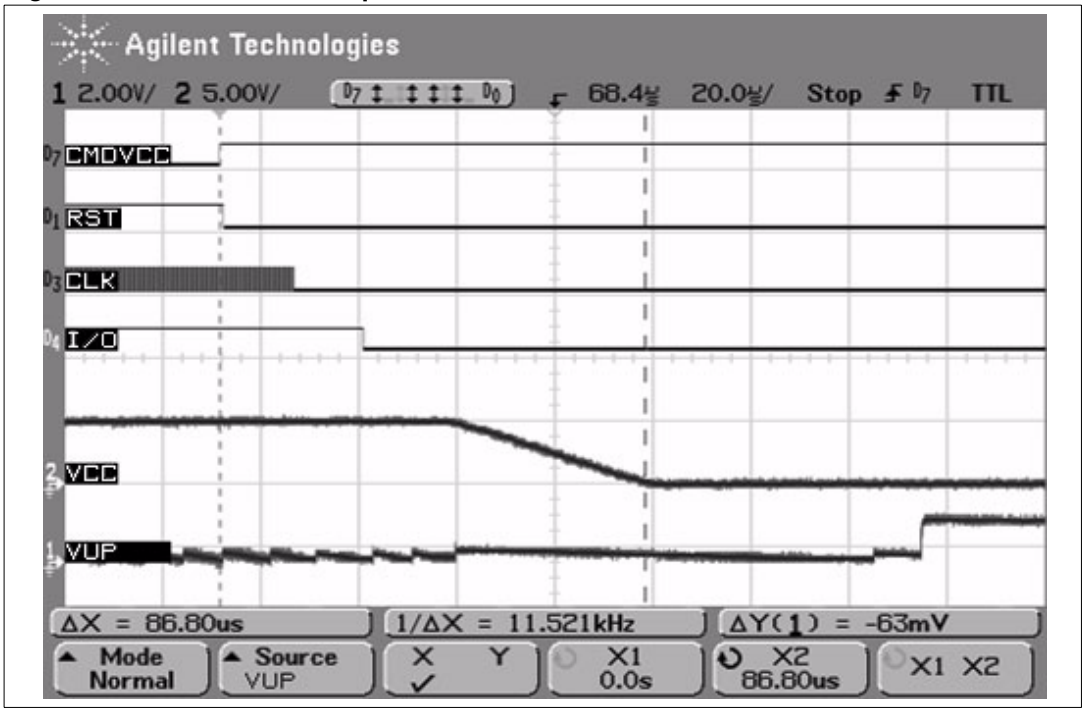


Figure 3. Deactivation Sequence



2 Card Clock

The card clock signal (CLK) is present on the CLK pin when the ST8024 is activated; it is linked with the internal En4 signal (see *Figure 1 on page 1*) and its frequency is obtained according to the settings in *Table 1*.

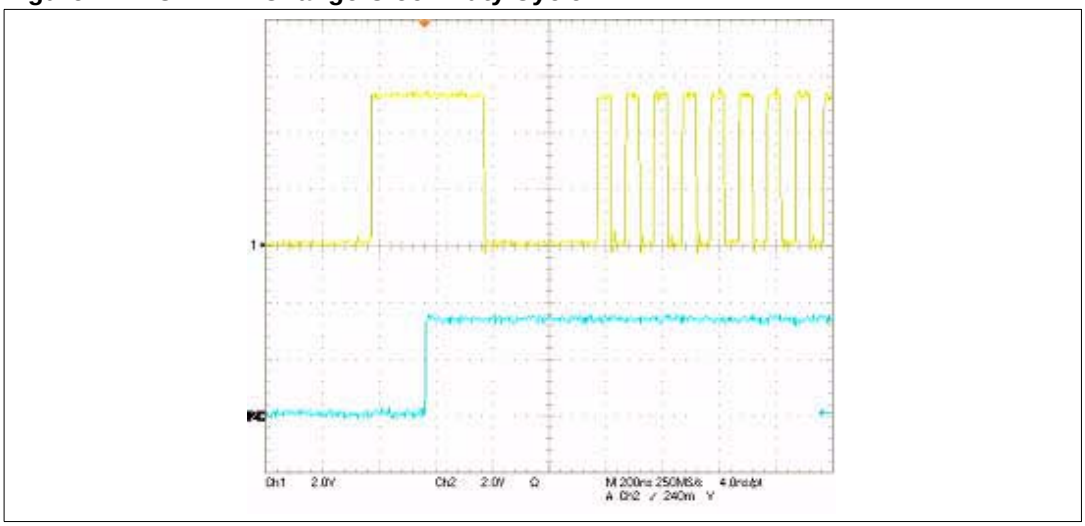
According to the ISO/IEC7816 specifications, the CLK duty cycle must be guaranteed between 45% and 55%, even when the status of CLOCKDIV1 or CLOCKDIV2 changes. *Figure 4* shows how the ST8024 ensures duty cycle accuracy by waiting for completion of a whole clock cycle before changing the frequency (CLKDIV1 change, rising edge of CH2). The output Duty Cycle is 50%±5%, even if the Clock Division changes.

The card clock signal (CLK) can be obtained by connecting a crystal (“XTAL”) between the XTAL1 and XTAL2 pins, or by an external signal applied to the XTAL1 pin. In this case the XTAL2 pin **must** be left floating. The external signal voltage level must be limited between GND and V_{DD} voltage.

Table 1. CLK Division Factor

CLKDIV1	CLKDIV2	f_{clk}
0	0	1/8 f_{Xtal}
0	1	1/4 f_{XtalL}
1	1	1/2 f_{Xtal}
1	0	f_{Xtal}

Figure 4. CLKDIV Change Clock Duty Cycle



Legend:

1. CH1 = Output CLK Waveform
2. CH2 = CLKDIV1 Pin
3. Conditions: V_{DD} = 3.3V; V_{DDP} = 5V; 5/3V = H
4. Mode: ACTIVE
5. f_{XTAL} = 10MHz; CLKDIV2 = 0V

3 Emergency Deactivation/Fault Detection

ST8024 is equipped with a fault detection circuitry which monitors the following conditions (see *Figure 1 on page 1*):

- V_{DD} undervoltage,
- Fault on card removal,
- V_{CC} Short circuit protection,
- V_{DDP} drop, and
- Over-Temperature protection.

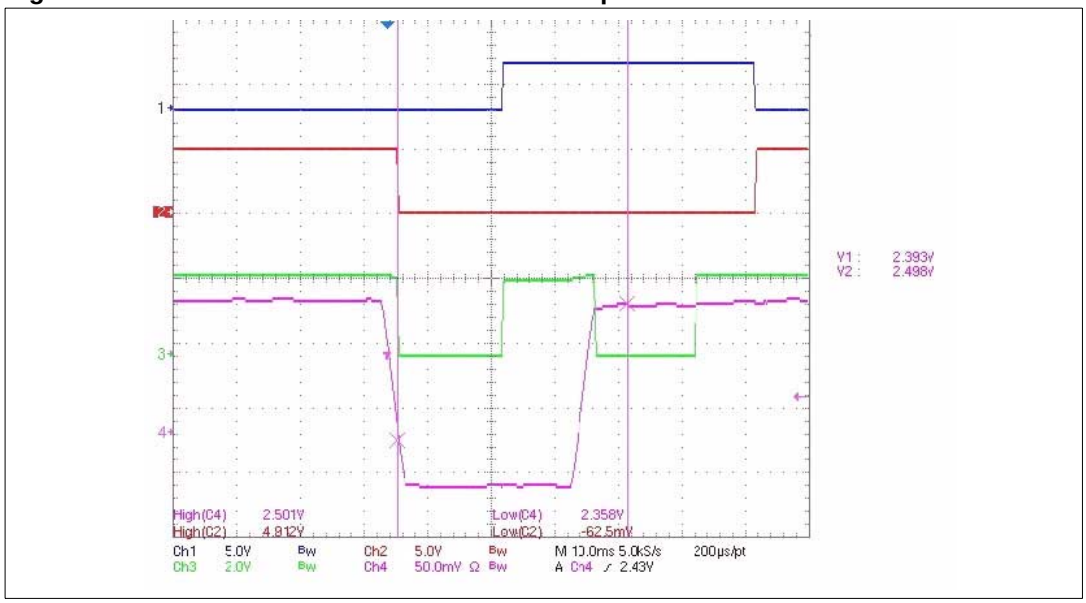
3.1 PORADJ V_{DD} Undervoltage without External Resistor Bridge

The ST8024 logic circuitry is supplied by V_{DD}. In order to avoid voltage spikes that could cause damage, or malfunction of the device and/or card, a voltage supervisor block is embedded (see *Figure 1*). This block monitors V_{DD} and when it gets lower than V_{TH2} (Falling Threshold Voltage on V_{DD}, 2.45V, typ), the supervisor immediately starts the deactivation sequence and V_{CC} goes low.

As V_{DD} goes higher than V_{TH2} + V_{HYS2}, (V_{HYS2} is the Hysteresis of threshold voltage, 100mV, typ), after a certain amount of time (t_w + $t_{debounce}$, where t_w is the internal power-on reset pulse width, 8ms typ, see *Figure 5 on page 8*), $\overline{CMDVcc}$ goes low. The activation sequence starts and V_{CC} goes high. The PORADJ pin can be left floating, but connecting it to GND to avoid noise capture is recommended.

Note: See *Fault On Card Removal on page 12* for $t_{debounce}$ feature details.

Figure 5. ST8024 Automatic Deactivation Sequence



Note: *Deactivation: $V_{TH2} \approx 2.393V$.*

Activation: As $V_{DD} \geq V_{TH2} + V_{HYS2}$ ($\approx 2.498V$) AND $\overline{CMDVcc}$ goes low, V_{CC} goes high.

Legend:

1. CH1 = $\overline{CMDVcc}$
2. CH2 = V_{CC}
3. CH3 = $\overline{OFF}$
4. CH4 = V_{DD}
5. Conditions: V_{DD} = 3.3V; V_{DDP} = 5V; 5/3V = H
6. Mode: ACTIVE
7. f_{XTAL} = 10MHz; CLKDIV2 = 0V

3.2 PORADJ V_{DD} Undervoltage with External Divider

In this case, a resistor bridge is applied to the PORADJ pin (see *Figure 6*). $V_{TH(ext)\ rise}$ and $V_{TH(ext)\ fall}$ are the External Rising Threshold Voltage and the External Falling Threshold Voltage on V_{DD}, respectively. They are the voltages on pin PORADJ that switch the device ON and OFF. By knowing these values and using the formula:

$$V_{PORADJ} = (R_2 / R_1 + R_2) \times V_{DD}$$

Where:

it is possible to set R_1 and R_2 in order to get suitable values for V_{DD} in order to turn the device ON and OFF (R_1+R_2 = 100kΩ typ).

In particular, R_1 and R_2 have to be set so that, when V_{DD} is getting low, before turning the microcontroller off, the smart card has to be switched off properly as well. The same goes for microcontroller start-up. The smart card has to be turned on after the microcontroller. *Figure 7* and *Figure 8 on page 11* show the $V_{TH(ext)\ rise}$ and $V_{TH(ext)\ fall}$ on the PORADJ pin (0.21V and 1.15V, respectively).

As long as V_{DD} gets the proper start-up value (so that $V_{TH(ext)\ rise}$ = 1.196V), $\overline{OFF}$ goes low for $t_w + t_{debounce}$ ($t_w \approx$ 16ms, in this case). During this time, the device can not be turned on by the $\overline{CMDVcc}$. To turn the device on, $\overline{CMDVcc}$ must go low at least by the end of about 16ms (while $\overline{OFF}$ is high).

Figure 6. External Resistor Bridge Applied to PORADJ

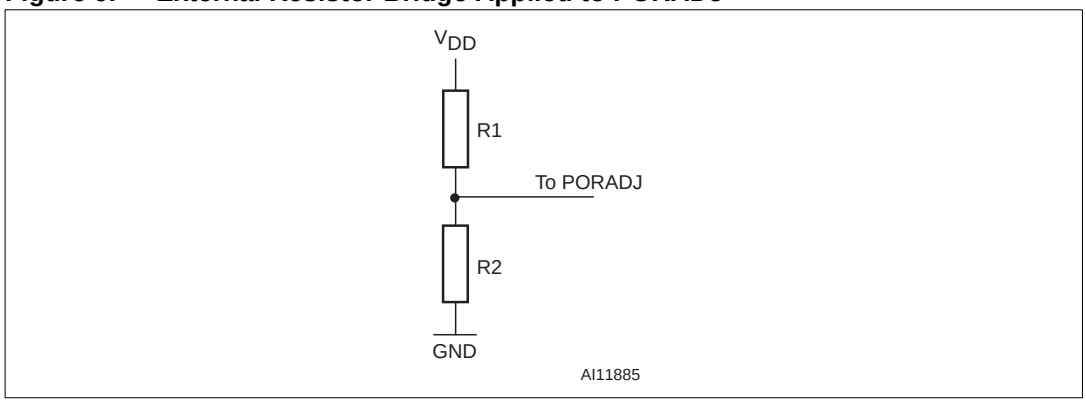
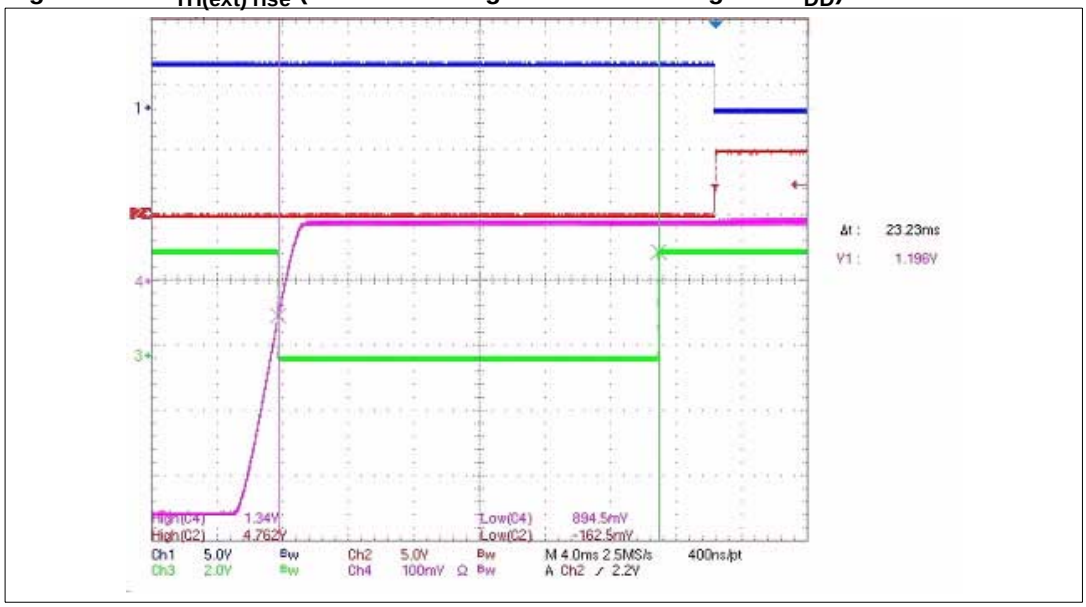


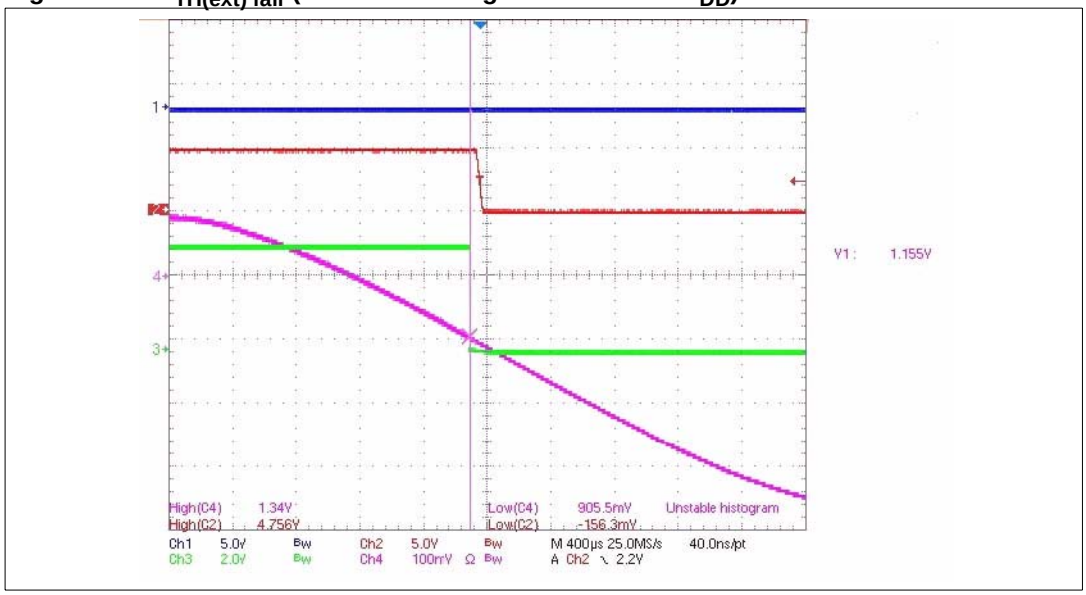
Figure 7. $V_{TH(ext)\ rise}$ (External Rising Threshold Voltage on V_{DD})



Legend:

1. CH1 = $\overline{CMDVcc}$
2. CH2 = V_{CC}
3. CH3 = $\overline{OFF}$
4. CH4 = $V_{TH(ext)\ rise}$

Figure 8. $V_{TH(ext)\ fall}$ (External Falling Threshold on V_{DD})



Note: As $V_{TH(ext)\ rise}$ = 1.155V, the device starts switching OFF and V_{CC} goes low.

Legend:

1. CH1 = $\overline{CMDVcc}$
2. CH2 = V_{CC}
3. CH3 = $\overline{OFF}$
4. CH4 = $V_{TH(ext)\ fall}$

3.3 Fault On Card Removal

If the smart card is pulled out from its socket ($\overline{PRES}$ goes high or PRES goes low), the deactivation sequence starts. The $\overline{OFF}$ pin goes low and the device switches off (see *Figure 9*). In order to avoid bouncing on the $\overline{PRES}$ (or PRES) signal at card insertion or extraction, as the card is inserted again, $\overline{OFF}$ goes high just after a period $t_{debounce}$ (≈ 8ms). If $\overline{CMDVcc}$ goes low before this time, after card insertion, the device does not turn itself on and $\overline{CMDVcc}$ must wait for $t_{debounce}$ before going low enough to switch the device on. *Figure 10 on page 12* shows the start of the activation sequence after $t_{debounce}$ is elapsed.

Figure 9. Card Extraction

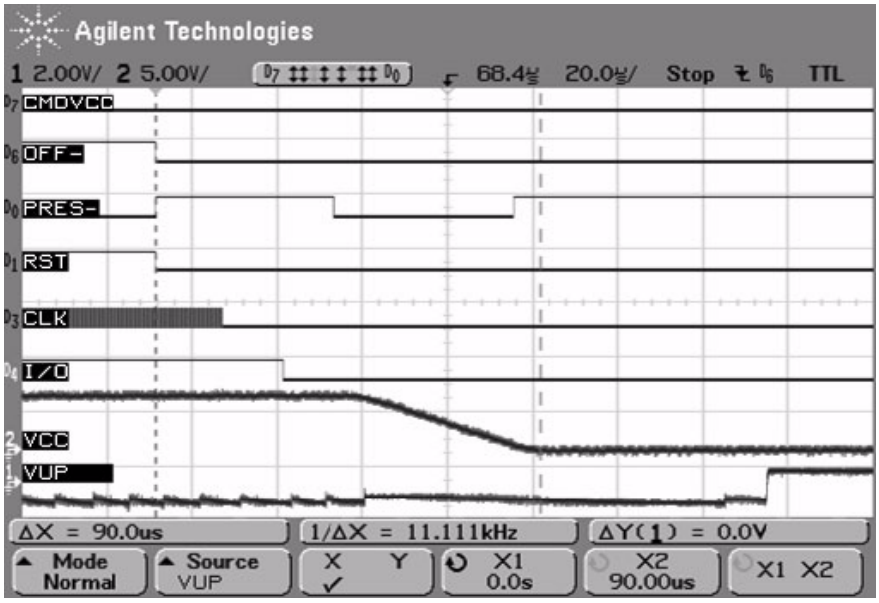
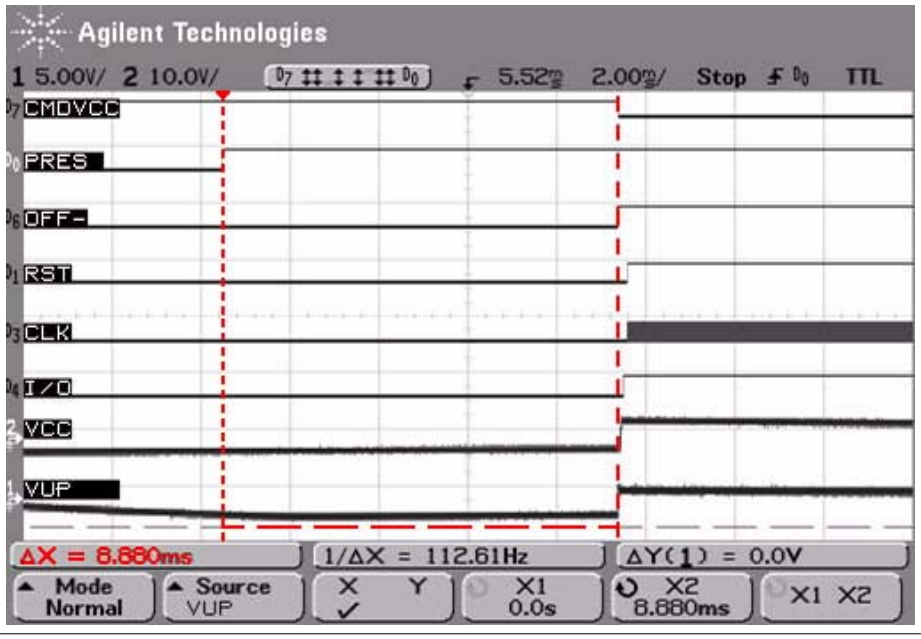


Figure 10. ST8024 Activation Sequence (after $t_{debounce}$)

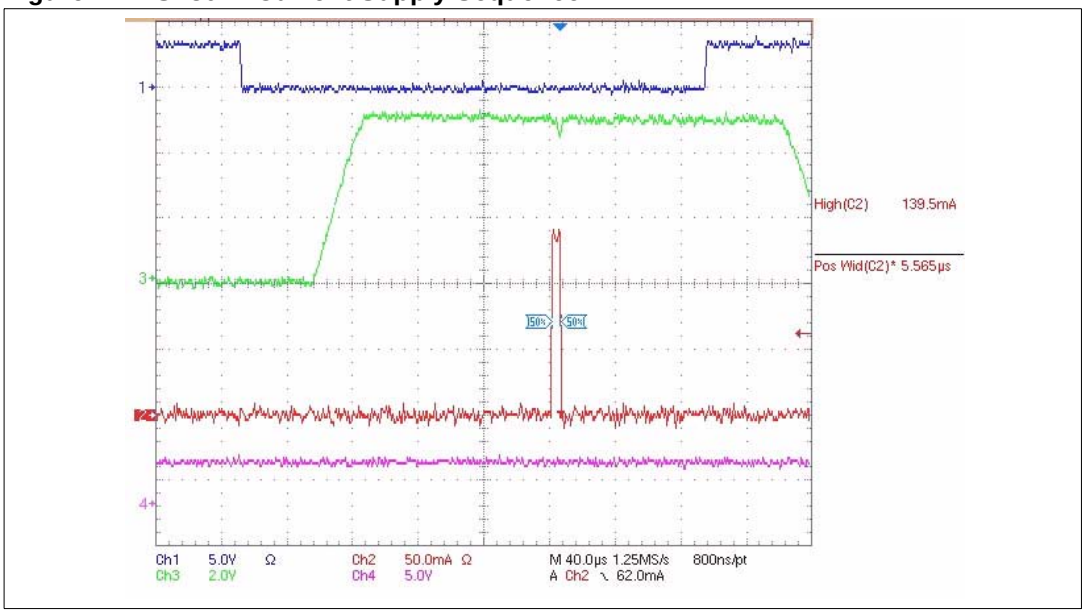


3.4 V_{CC} Short Circuit Fault Protection

The ST8024 is able to supply the card with current pulses of about 140mA for no longer than 5.5µs, typical (see *Figure 11* and *Figure 12 on page 14*).

Short circuit protection is an important interface feature that warns the sequencer block if the output current becomes higher than the short circuit current limit (≈120mA) for too much time. This characteristic allows the device to supply the card with current pulses higher than the maximum allowed, if their lengths are not too long. If the current pulses last for more than 5.5µs, the deactivation sequence starts to protect the card. The $\overline{OFF}$ pin goes low so as to warn the microcontroller about the overcurrent fault. The sequence in *Figure 12 on page 14* shows how the current pulse becomes long enough to make the short circuit protection happen.

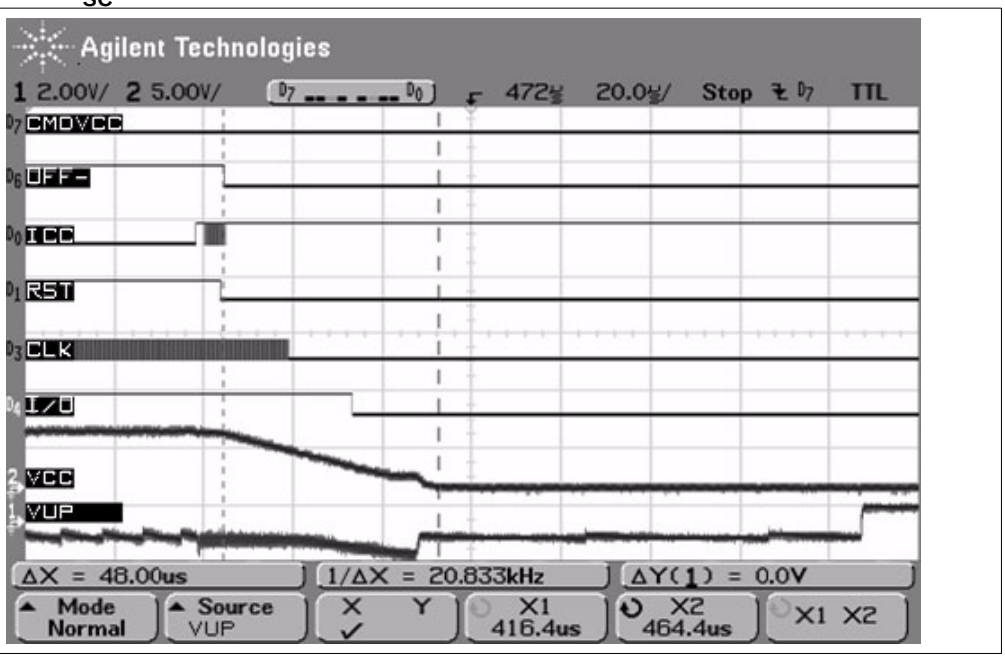
Figure 11. ST8024 Current Supply Sequence



Legend:

1. CH1 = $\overline{CMDVcc}$
2. CH2 = I_{SC} Pulse
3. CH3 = V_{CC}
4. CH4 = $\overline{OFF}$

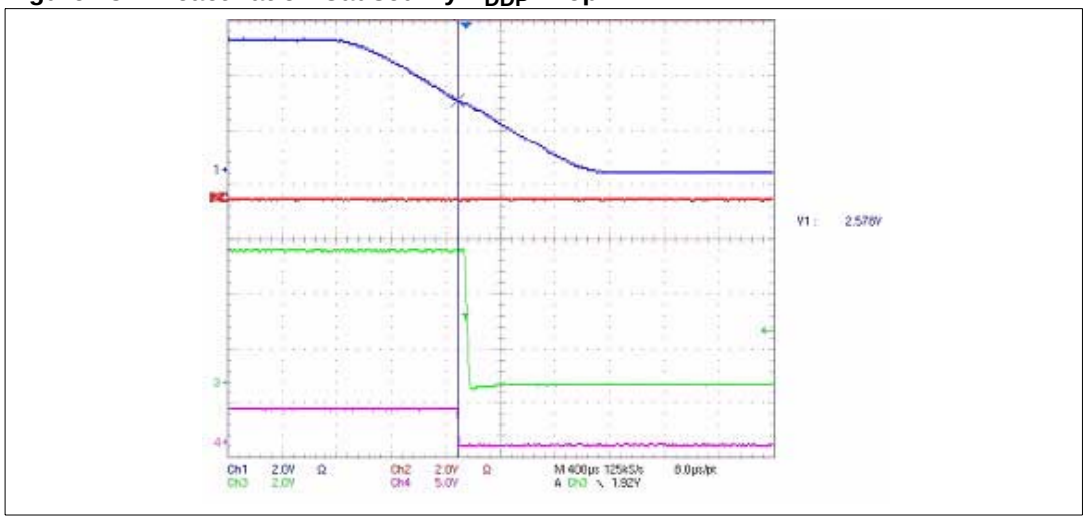
Figure 12. I_{SC} Short Circuit Protection



3.5 V_{DDP} Drop

The voltage supervisor also controls the V_{DDP} Drop. As it reaches the minimum value (≈2.578V, in this case, see *Figure 13*, the $\overline{OFF}$ pin goes low and the V_{CC} drops.

Figure 13. Deactivation Caused By V_{DDP} Drop



Legend:

1. CH1 = V_{DDP}
2. CH2 = $\overline{CMDVcc}$
3. CH3 = V_{CC}
4. CH4 = $\overline{OFF}$

3.6 Over-Temperature Fault Protection

Over-Temperature protection is another important interface feature that warns the sequencer block of fault events. If the temperature is higher than the shutdown temperature (150°C, typ), the deactivation sequence starts to protect the card. The $\overline{OFF}$ pin goes low so as to warn the microcontroller about the over-temperature fault.

4 ST8024 Application Hardware Guidelines

This section contains some optimization guidelines concerning PCB layout as well as external component placement and connections. The referenced application board in *Figure 14* and *Figure 15 on page 17* has two layers, and uses these guidelines to meet application NDS requirements.

The PCB layout provides completely separate supply and GND copper planes, which allow each plan to act as a shield for each group of noise-sensitive device pins. The PGND, and CGND and GND planes share a common point on bottom layer of the PCB (see top, *Figure 15 on page 17*).

Figure 14. ST8024 Application PCB Top Layer

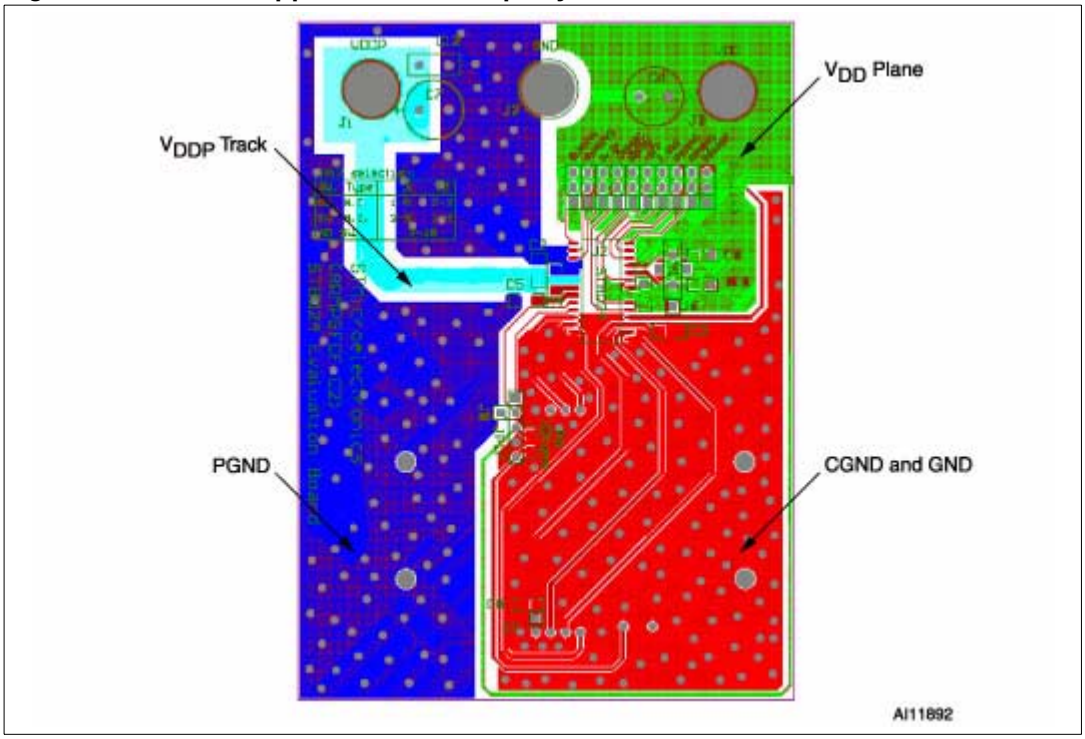
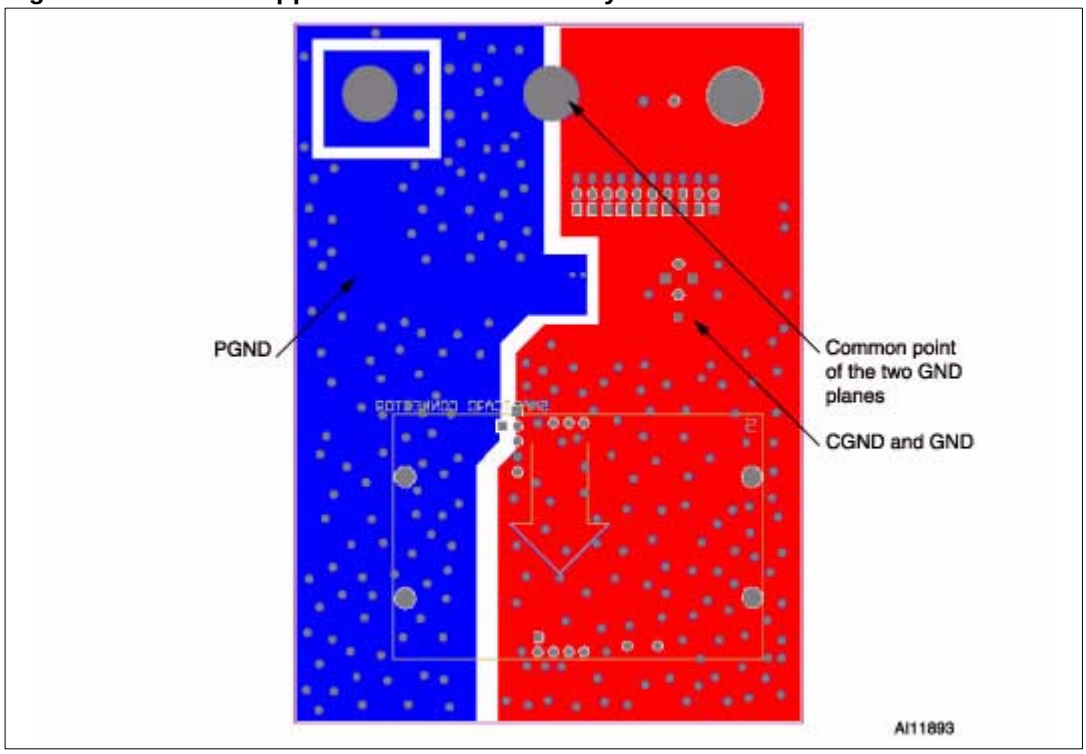


Figure 15. ST8024 Application PCB Bottom Layer



4.1 Power Supply Optimization

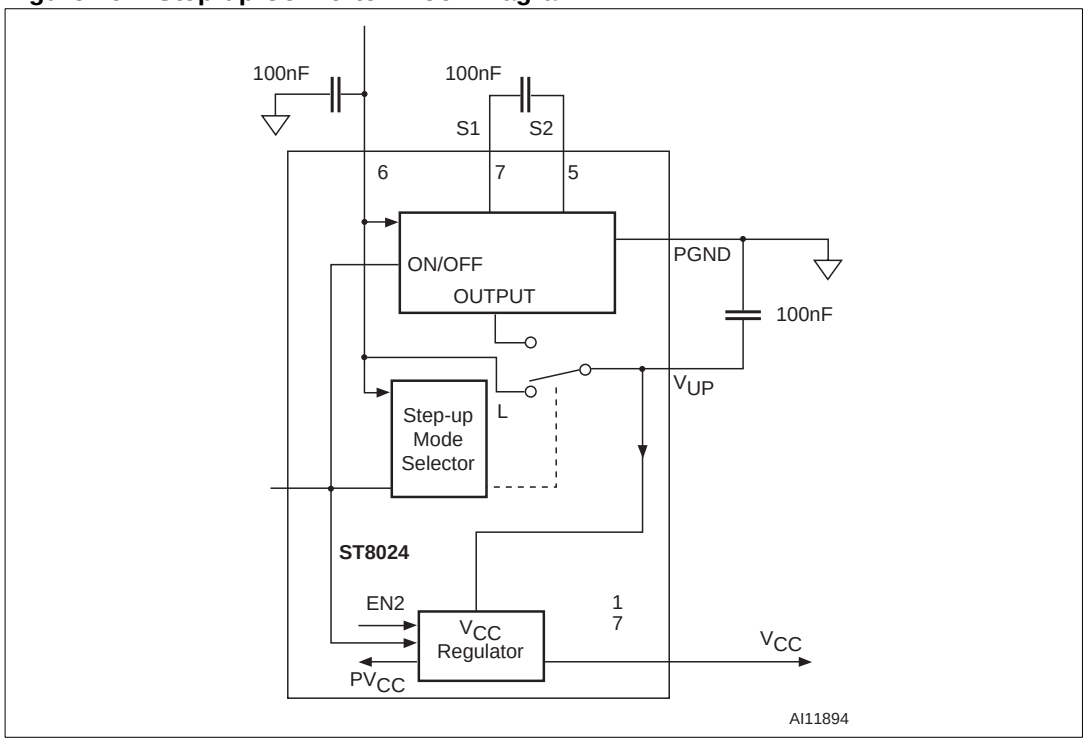
The ST8024 can drive both 3V and 5V cards by the supply voltage selector pin 5/$\overline{3V}$ (pin 3) as shown in *Figure 1 on page 1*. If the 5/$\overline{3V}$ pin is connected to GND, the V_{CC} voltage is 3V, and if the 5/3V is connected to V_{DD}, the V_{CC} voltage is 5V.

A step-up converter supplied by V_{DDP} is used for the V_{CC} voltage generation. It doubles the input voltage V_{DDP} or follows it, depending on the 5/$\overline{3V}$ and V_{DDP} values:

- 5/$\overline{3V}$=H and V_{DDP} > 5.8 V; voltage follower
- 5/$\overline{3V}$=H and V_{DDP} < 5.7 V; voltage doubler
- 5/$\overline{3V}$=L and V_{DDP} > 4.1 V; voltage follower
- 5/$\overline{3V}$=L and V_{DDP} < 4.0 V; voltage doubler

The S1 and S2 pins are used for duplicating the supply voltage V_{DDP} by using the 100nF pumping capacitor (C4). The charge pump output pin (V_{UP}) has to be connected to a 100nF storage capacitor (C5) to stabilize the voltage.

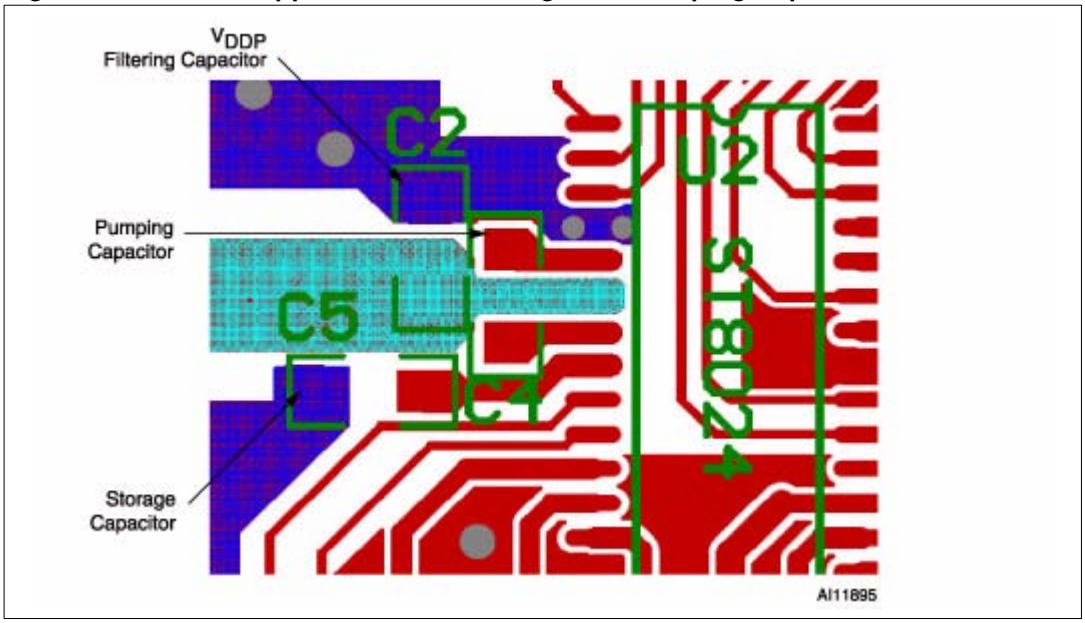
Figure 16. Step-up Converter Block Diagram



A small amount of noise is introduced into the design because of the switching circuitry. In order to reduce it and improve the efficiency of the step-up converter, the capacitors must be connected as closely as possible to the pins (see *Figure 17*). An Equivalent Series Resistance (ESR) of lower than 100mΩ at 100kHz is recommended.

The evaluation board is equipped with MURATA GRM31M7U1H104JA01B capacitors. However, other capacitors with an ESR of up to 100mΩ at 100kHz are good enough to work within the specifications. They just may be more sensitive to the layout optimization process.

Figure 17. ST8024 Application PCB Storage and Pumping Capacitors

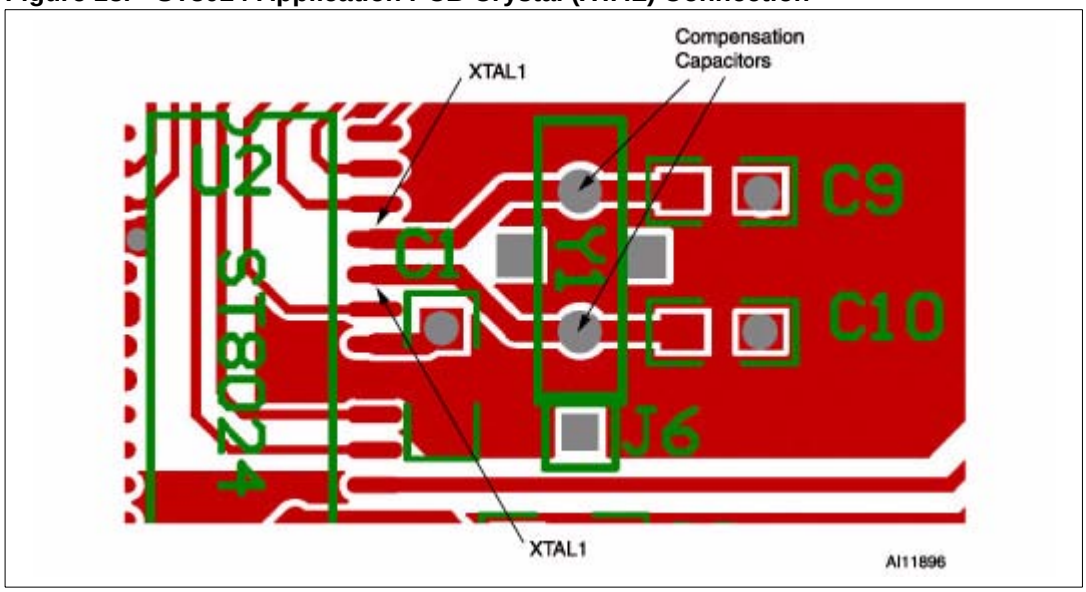


4.2 Clock Section Optimization

Recommendations for the PCB design clock area include:

- The XTAL should be connected as closely as possible to the XTAL pins to reduce signal reflections, especially for high frequency applications (see *Figure 18*).
- Two compensation capacitors (C9 and C10), each of 15pF (typ) are suggested to improve the oscillator start-up performances. Even without those additional capacitors the CLK Duty Cycle is guaranteed between 45% and 55% (according to the NDS specifications), with frequencies up to 26MHz.

Figure 18. ST8024 Application PCB Crystal (XTAL) Connection



4.3 Smart Card Connections

In typical applications, a 100nF filter capacitor (C3) is connected to the V_{CC} output towards GND/CGND, near the ST8024 pins. A second 100nF capacitor (C8) is connected between the card socket pins C1 (V_{CC}) and C5 (CGND), near the card slot (see *Figure 19*). In order to reduce noise and avoid coupling effects, the wire length between the ST8024 and card should be as short as possible.

Another recommendation is to keep the CLK track far away from the other signal tracks to limit coupling with the transceiver lines. Further decoupling is gained if the clock track is shielded by a GND/CGND plane or track on the PCB.

Keeping the PGND and GND/CGND planes as large as possible improves power supply noise rejection. With this in mind, the board design should connect these planes with a large number of vias between the top and bottom board layers (3-4 vias per cm^2).

The V_{CC} spikes are much lower than $350mV_{PP}$ even when a pulsed load of up to 80mA is applied with V_{CC} = 5V, or up to 65mA with V_{CC} = 3V, as specified by the NDS requirements. *Figure 20 on page 22* shows a typical V_{CC} output waveform where an 80mA pulsed load applied and the measured ripple is lower than $160mV_{PP}$.

Figure 19. ST8024 Application PCB Smart Card Connections

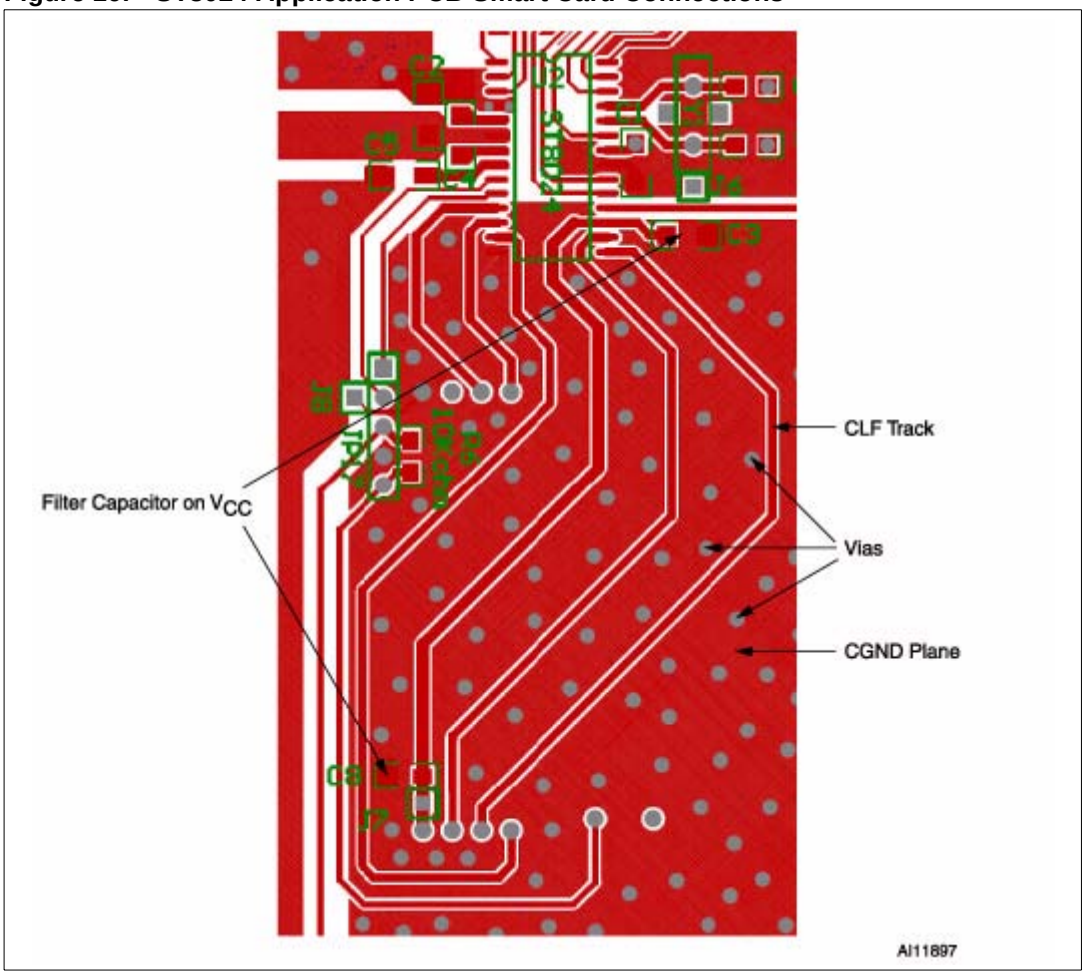
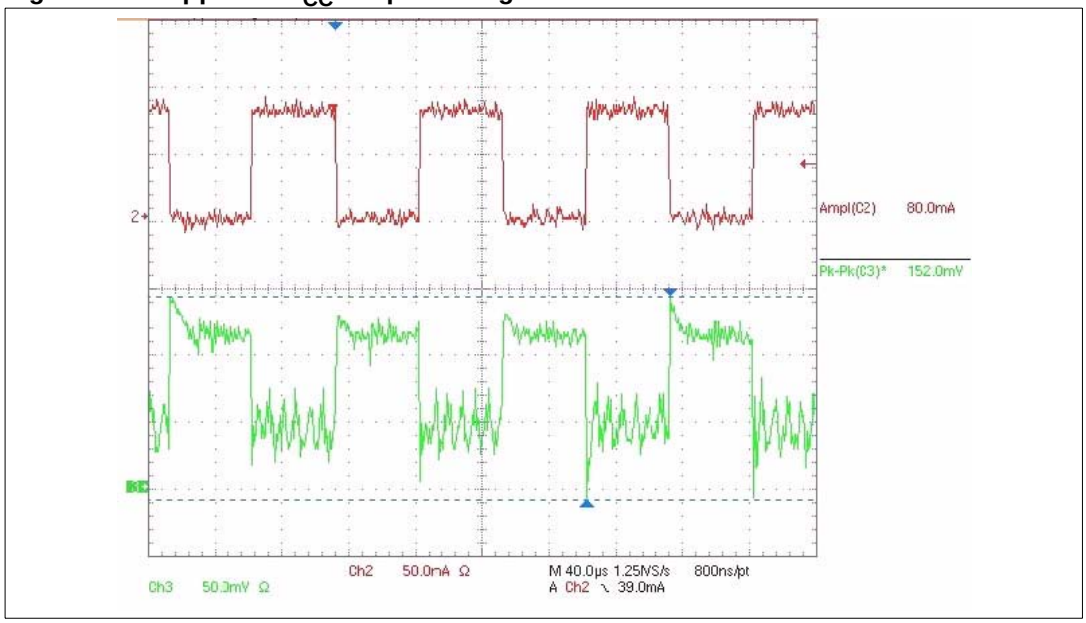


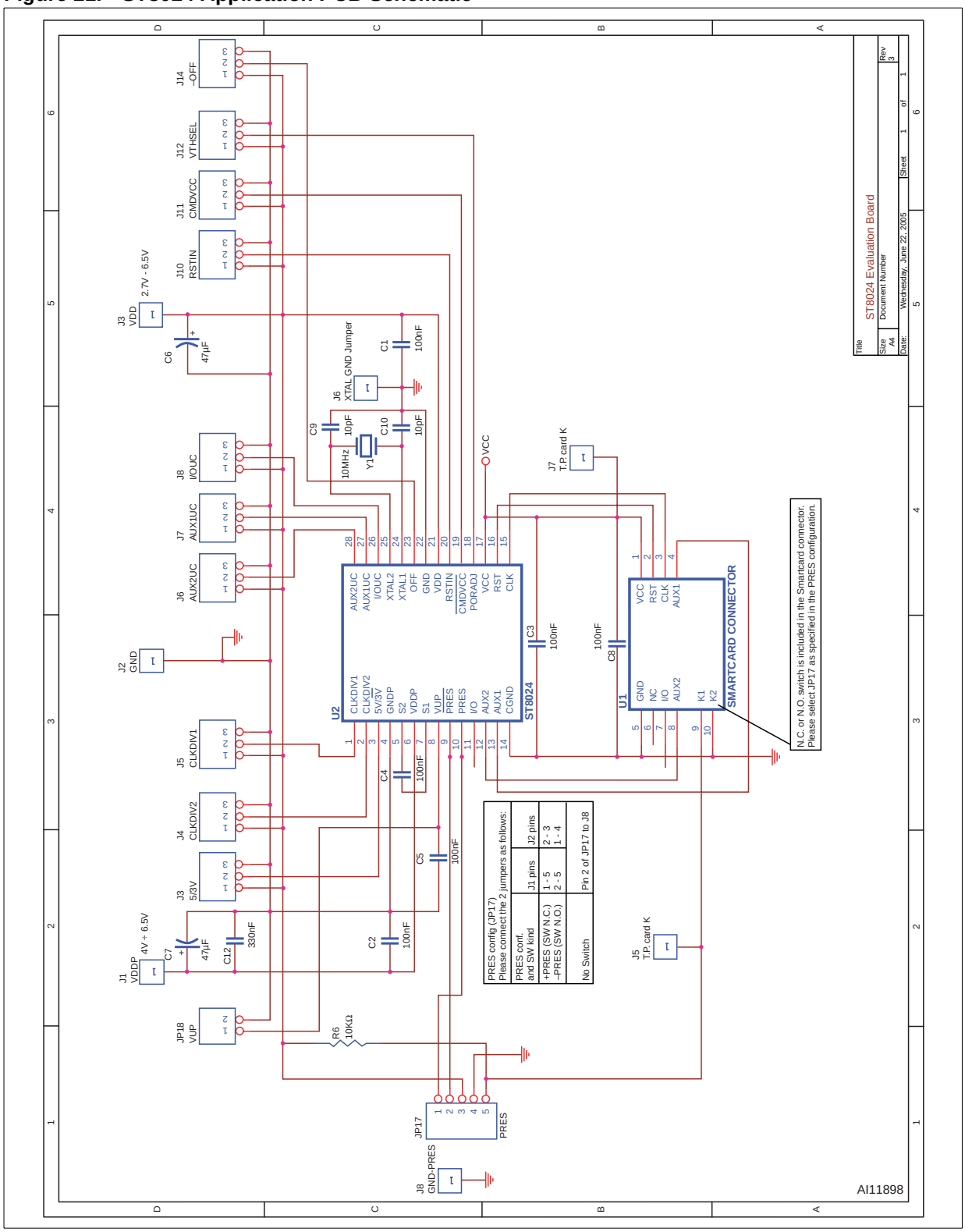
Figure 20. Ripple on V_{CC} Output Voltage



Legend:

1. V_{DD} = 3.3V
2. V_{DDP} = 5V
3. CH2 = 80mA Pulsed Current I_{CC}
4. CH4 = Ripple on V_{CC} Output Voltage
5. 5V Offset on V_{CC}

Figure 21. ST8024 Application PCB Schematic



5 Revision History

Table 2. Document Revision History

Date	Revision	Changes
10-Feb-2006	1	Initial release.