AN2260
APPLICATION NOTE

STR73x SystemMemory Boot Mode

Introduction

This application note describes the features of the SystemMemory boot mode developed for STR73x Flash microcontrollers to provide all the basic functionality to support programming of the embedded Flash. It will describe its general features, and then move on to specific features of the UART boot mode.

Contents

1 General description

The STR73x is normally woken up in SystemMemory boot Mode when the Flash is still not programmed in the manufacturing line environment. In this case the system boot is performed from SystemMemory sector in the Flash bank0. This mode allows initializing the Flash programming via a serial interface. The SystemMemory code is going to load a Flash programming code (called “loader” from now on) into internal RAM via the UART0 serial interface.

1.1 Entering SystemMemory boot mode

The STR73x enters the SystemMemory Boot Mode if the mode pins are configured with M0=0, M1=1 as the hardware reset pin (RSTIN) transitions High at the end of a hardware reset. The M1 signal is used to stretch the internal clock. M1 must be forced back to Low (0) after the RSTIN pin has stabilized. Forcing M1 Low is required in order to enable propagation of the system clock throughout the device.

As the M1 pin is forced Low the STR73x CPU begins executing the SystemMemory code which resides in the SystemMemory Sector now mapped at address 0x00000000.

Note: The normal Flash boot sector will not be available at address 0x00000000 until the SystemMemory sector is re-mapped to 0x8010C000 by clearing the SMBM bit in the Flash Control Register 0. The SystemMemory code does not perform this re-mapping operation.

Table 1. STR73x device configuration in SystemMemory Boot Mode

Feature/Peripheral	State	Comment
Instruction Set	THUMB	Save code space with 16-bit instructions
CPU Mode	Supervisor	Full access with IRQ/FIQs disabled
Input Clock	External Quartz	allow a Frequency in a range of 4 to 8MHz
CLK2	Div2 Enabled	-
PLL	Free running MX=12 DX=2	System Clock in a range of 12 to 24MHz to enable higher serial link baudrates
UART0_RX Pin	Input	UART0 receive
UART0_TX Pin	Default	Only configured for UART Boot
UART0 Registers	Default	Only configured for UART Boot

1.2 Hardware requirements

The hardware required for putting the STR73x into SystemMemory boot mode would consist of any circuitry, switch, or jumper capable of holding the M1 pin High during Reset, and then forcing M1 Low after the reset is complete. For more details refer to the application note *STR73x Hardware Getting Started (AN2156)*, Boot Management section.

To connect to the STR73x during SystemMemory boot mode, a RS232 serial interface must be directly linked to UART0 pins, for more details refer to the AN2156 document.

Note: The serial link receive interface pin (UART0_RX) must be held HIGH during the SystemMemory code initialization phase.

1.3 Loading code in SystemMemory boot mode

As previously described, the STR73x enters SystemMemory boot mode by controlling the state of the M1 pin during the Reset Sequence.

Following the serial link initialization sequence (see the following chapters) the SystemMemory code enters a loop to receive a specified number of bytes, and store them sequentially to RAM starting at address 0xA0000000. The receive byte count depends on the serial interface and is currently defined as 128 bytes for UART.

When the proper number of bytes is received, the STR73x then jumps to address 0xA0000000 and begins to execute the downloaded code.

Generally, this small piece of code (called loader or monitor) will contain another receive loop which may then continue to load code and data at a user specified location. The pre-initialized serial link may be used accomplish this without modifications.

The second level of downloaded code may contain the final user application. It may also contain another, more sophisticated, loader routine which adds a transmission protocol to enhance data integrity. The secondary loader may even change to a different download method, baud rate, system operating frequency, etc.

1.4 Exiting SystemMemory boot mode

SystemMemory boot mode must be terminated in order to execute a program in a normal USER mode. The STR73x may exit this mode by applying a hardware Reset on the RSTIN pin. At the time of the reset, the mode pins (M0 & M1) must be set at the proper levels to enter the desired user mode. Following the reset, the STR73x CPU will begin executing code from location 0x00000000 of the embedded Flash.

Table 2. Mode Pin vs Memory Mapping

M1	M0	Boot Mode	Memory Mapping	Note
0	0	User Boot mode 1	FLASH sector B0F0 mapped at 0h	All FLASH sectors accessible except SystemMemory sector
0	1	User Boot mode 2	FLASH sector B0F0 mapped at 0h	FLASH B0F1 sector and SystemMemory sector not accessible
1	0	SystemMemory	SystemMemory mapped at 0h	-
1	1	Reserved	-	-

1.5 SystemMemory code program flow

Figure 1. SystemMemory code program flow

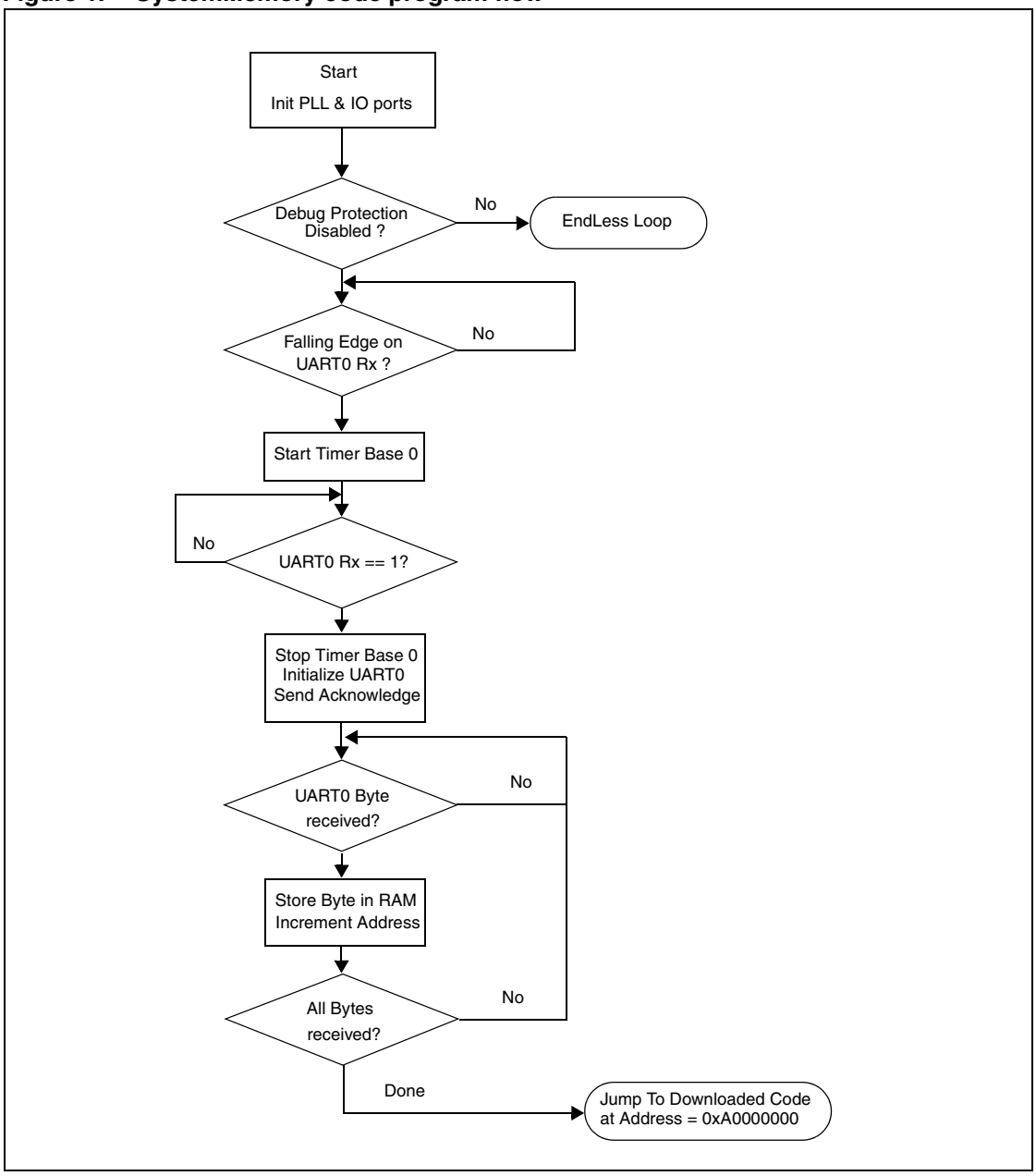


Figure 1 shows the program flow of the SystemMemory code software. A few points worth noting are:

- The boot process will not start if debug protection is active.
- The UART interface is only initialized if UART boot mode is detected.

Note: STR73x Timer Base 0 (TB0) is used to automatically detect the serial baud rate. Once initialized the UART configuration is 8-bits, No Parity, and 1 Stop bit.

2 UART SystemMemory boot mode

2.1 UART SystemMemory code sequence

After SystemMemory mode is entered and the STR73x is configured as described above, the SystemMemory code begins to scan the RXD0 line, waiting to receive a zero byte (one start bit, eight '0' data bits, and one stop bit).

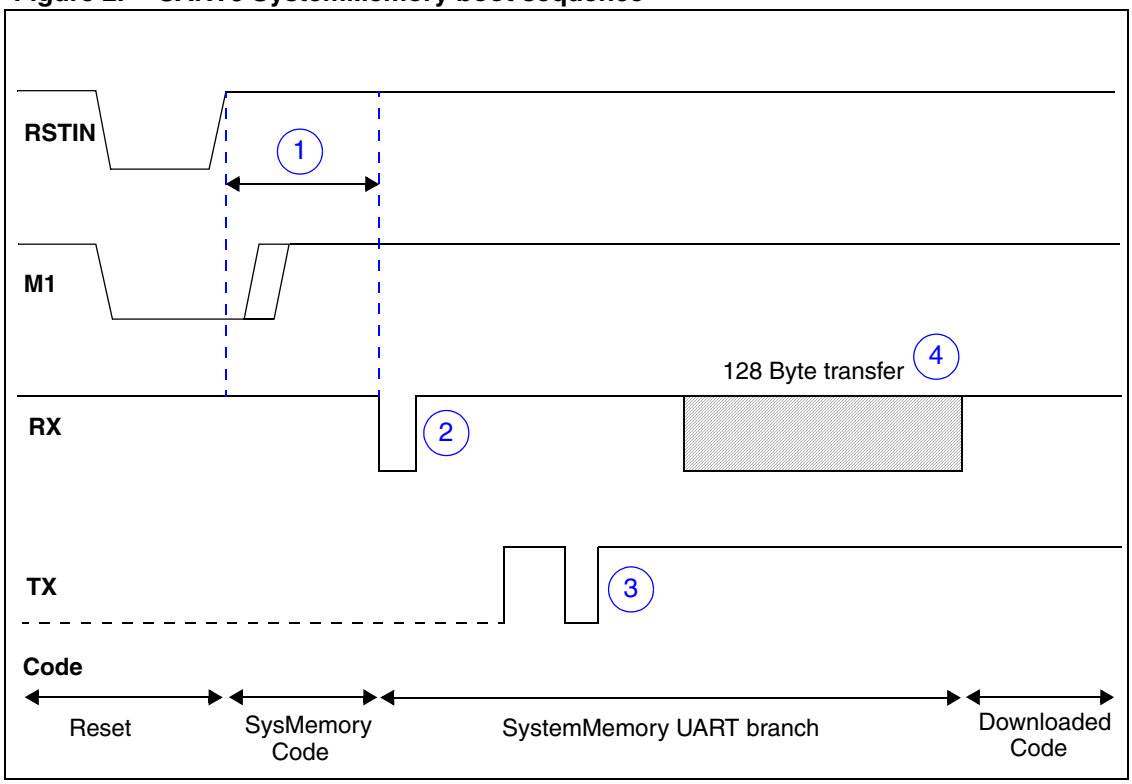
The duration of this zero byte is measured using the Timer Base 0. The count value of the timer is then used to calculate the corresponding baud rate factor with respect to the current system clock.

Next, the code initializes the serial interface accordingly, and sets up pin TXD0 to an alternate function, push-pull output. Using this calculated baud rate, an acknowledge byte is returned to the host which signals that the STR73x is ready to receive the 128 bytes of download data.

Note: The watchdog timer is disabled during SystemMemory Mode, so the boot loading sequence is not time limited.

Note: The acknowledge byte is 0x95 for the STR73x devices.

Figure 2. UART0 SystemMemory boot sequence



(1) Reset Stabilization & Code Initialization Time (> 2ms)

(2) Zero Byte Reception

(3) Acknowledge Byte Transmission

(4) 128 Byte Loader Download

2.2 Choosing the UART baud rate

The calculation of the serial baud rate for UART0, from the length of the first zero byte that is received, allows the operation of the STR73x SystemMemory boot loader within a wide range of baud rates. However, the upper and lower limits have to be kept, in order to insure proper data transfer.

STR73x Baud Rate = F_{cpu} / 16 * UART0_BAUDRATE

The STR73x uses Timer Base 0 to measure the length of the initial zero byte. The quantization uncertainty of this measurement implies the first deviation from the theoretical baud rate. The next deviation is implied by the computation of the UART0_BAUDRATE reload value from the timer contents. The formula below shows the association:

TB0_CNT / 9 = 1 Bit Time in F_{cpu} (9 Bit Times the first ZERO Byte)

UART0_BAUDRATE = TB0_CNT / 9 / 16 = TB0_CNT / 144

For a correct data transfer from the host to the STR73x, the maximum deviation between the internal initialized baud rate for UART0 and the real baud rate of the host should be below 2.5%. The deviation (f_B, in percent) between the host baud rate and STR73x baud rate can be calculated via the formula below:

f_B= abs((STR73x Baud Rate - Host Baud Rate) / STR73x Baud Rate) * 100%

f_B<= 2.5%

Note: Function (f_B) does not consider the tolerances of oscillators and other devices supporting the serial communication.

This baud rate deviation is a nonlinear function depending on the CPU clock and the baud rate of the host. The maximum of the function (f_B) increases with the host baud rate. This is due to the smaller baud rate pre-scale factors, and the implied higher quantization error.

2.2.1 Minimum baud rate

B_{Low} is the minimum baud rate determined by the maximum count capacity of Timer Base 0 when measuring the zero byte. This will be directly related to system clock frequency. Using the maximum TB0_CNT value of 65535 in the equations above we end up with a minimum Baud Rate of 1648 at F_{cpu} = 12MHz. The lowest standard Baud Rate for this case would be 2400. Baud rates below B_{Low} would cause TB0 to overflow. If this occurs, it would not be possible to properly initialize the UART0.

2.2.2 Maximum baud rate

B_{High} is the highest baud rate in which the deviation still does not exceed the limit. All baud rates between B_{Low} and B_{High} are below the deviation limit.

2.2.3 Higher baud rate deviations

A baud rate may be used as long as the actual deviation does not exceed the limit. Certain lower baud rates may violate the deviation limit, while an even higher baud rate stays very well below it. This relationship depends on the host interface.

3 Conclusion

The STR73x SystemMemory loader provides a convenient method for downloading user code into on chip RAM for a variety of applications, such as programming of the embedded Flash. The UART interface provides an easy and inexpensive, readily available serial link for desktop users.

4 Revision history

Date	Revision	Changes
31-Oct-2005	1	First revision.

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