

Guidelines for migrating ST7LITE1x applications to ST7FLITE1xB

Introduction

This application note provides information on migrating ST7FLITE1x-based applications to ST7FLITE1xB.

Table 1.Feature comparison

	ST7FLITE1x	ST7FLITE1xB					
Package	SO20 300	SO20 300"/ DIP20/ SO16 300" /DIP16					
	ST7LITE10	ST7LITE10B					
Device Name	ST7LITE15	ST7LITE15B					
	317LITE19	STILLETAB					
Program Memory	4K (No c	change)					
Operating Supply	2.4V to 5.5V	2.7V to 5.5V					
Operating Temperature	-40°C to 85°C	(No change)					
RAM (stack) - bytes	256 (128) (N	No change)					
Data EEPROM - bytes	128 (No	change)					
I/Os	15, PA7:0, PB6:0	17, PA7:0, PB6:0, PC1:0					
Interrupt	10	12					
Power saving modes	Slow, Wait, Active Halt, A	WUFH, Halt (No change)					
Clock Source	1% Internal RC, PLLx4/8, External cloc	k source, Crystal, Resonator oscillator,					
Lite Timer	Yes (no change)						
Watchdog Timer	Yes (no d	change)					
12-bit Autoreload Timer with 32 MHz input clock	Yes	Yes with two counters, one pulse mode, dead time					
SPI	Yes (no d	change)					
10-bit ADC with Op-Amp	Yes (no d	change)					
Analog Comparator	No	Yes					
Emulator	ST7MDT10-EMU	J3 (No change)					
ST7 DVP3 Series	ST7MDT10-DVI	P3(No change)					
Programming tools (EPB)	ST7MDT10-EPB	ST7MDT10-EPB (only for SO20 package)					
Programming tools (Socket Board)	ST7SB10-123/EU ST7SB10-123/US ST7SB10-123/UK (to be used along with STICK)						
ICD Tool	INDART kit (Softec) and Reva kit (Raisonance)	Reva kit (Raisonance)					

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Pinout compatibility 1

Package 1.1

ST7FLITE1x is available only in SO20 300" package. ST7FLITE1xB is available in SO20 300", DIP20, SO16 300" and DIP16 packages.

1.2 SO20 pinout

Both ST7FLITE1x and ST7FLITE1xB are pin to pin compatible. On some pins of ST7FLITE1xB new alternate functions have been added to add new peripherals/ features.

	ST7FLITE1x	ST7FLITE1xB
Pin No. 4	SS/AIN0/PB0	COMPIN+ ⁽¹⁾ /SS/AIN0/PB0
Pin No. 8	CLKIN/AIN4/PB4	Compin- ⁽²⁾ /CLKIN/AIN4/PB4
Pin No. 11	PA7	PA7/COMPOUT ⁽³⁾
Pin No. 19	OSC2	OSC2/ PC1⁽⁴⁾
Pin No. 20	OSC1/CLKIN	OSC1/CLKIN/PC0 ⁽⁵⁾

⁽¹⁾COMPIN+: Analog Comparator Input

⁽²⁾COMPIN-: Analog Comparator External Reference Input ⁽³⁾COMPOUT: Analog Comparator Output

⁽⁴⁾PC1: Port C1

⁽⁵⁾PC2: Port C2



2 Register map

In ST7FLITE1xB, some register addresses have been added, some modified to add new features and peripherals.

Note: For easy software migration, two general rules to be followed: All "reserved" byte memory areas must never be "read" or "write". All "reserved" and "unused" bits must be left unchanged when accessing the byte.

2.1 Register address

These changes are classified in two groups:

- 1. New features added: Port C, dual counters in ART Timer, one pulse mode, External Break, Dead Time generation, Force Update in ART Timer, Analog Comparator and PLL divider.
- TRANCR (Transfer Control Register) has been replaced by ATCSR2 (Timer Control Register2). Seven bits relative to the new features in ART Timer have been added in ATCSR2 register. TRAN <bit0> of TRANCR register has been replaced by TRAN1 <bit0>.

Please, refer to the datasheet for the detailed description of the new features.



	ST7F	LITE1x				ST7FLI	TE1xB
@	Block	Register Label			@	Block	Register Label
0006h	Posor	wod Aroa			0006h	Port C	PCDR
0007h	nesei	veu Alea		U	0007h	Port C	PCDDR
000Dh		ATCSR			000Dh		ATCSR
000Eh		CNTRH			000Eh		CNTRH
000Fh		CNTRL			000Fh		CNTRL
0010h		ATRH			0010h		ATRH
0011h		ATRL			0011h		ATRL
0012h		PWMCR			0012h		PWMCR
0013h		PWM0CSR			0013h		PWM0CSR
0014h		PWM1CSR			0014h		PWM1CSR
0015h		PWM2CSR			0015h		PWM2CSR
0016h		PWM3CSR			0016h		PWM3CSR
0017h	Autore-	DCR0H			0017h		DCR0H
0018h	er 2	DCR0L			0018h		DCR0L
0019h		DCR1H			0019h	Autoreload	DCR1H
001Ah		DCR1L			001Ah	Timer 2	DCR1L
001Bh		DCR2H			001Bh		DCR2H
001Ch		DCR2L			001Ch		DCR2L
001Dh		DCR3H			001Dh		DCR3H
001Eh		DCR3L			001Eh		DCR3L
001Fh		ATICRH			001Fh		ATICRH
0020h		ATICRL	0		0020h		ATICRL
0021h		TRANCR	(2)		0021h		ATCSR2
0022h		BREAKCR			0022h		BREAKCR
0023h		•		1	0023h		ATR2H
0024h	Deser	und Area			0024h		ATR2H
0025h	Reser	veu Area			0025h		DTGR
0026h				L.	0026h		BREAKEN
						•	
002Ch	Deser	und Area			002Ch	Analog	VREFCR
002Dh	nesei	veu Area		Οl	002Dh	Comparator	CMPCR
				•			
003Bh	Reser	ved Area		1	003Bh	PLL	PLLTST
						·	
004Bh		DMCR			004Bh		DMCR
004Ch		DMSR			004Ch		DMSR
004Dh	Debug	DMBK1H			004Dh	1	DMBK1H
004Eh	Module	DMBK1L			004Eh	Debug Mod- ule	DMBK1L
004Fh		DMBK2H			004Fh	210	DMBK2H
0050h		DMBK2L			0050h	1	DMBK2L
0051h	Reser	ved Area		1	0051h	1	DMCR2
				-	·		

Figure 1. Register map modifications



2.2 Register content differences

2.2.1 SICSR register

In the SICSR (System Integrity Control/Status Register) three new bits have been added (see Figure 2).

LOCK32: It is set when PLL 32 MHz reaches its operating frequency

CR[1:0]: RC Oscillator Frequency Adjustment bits: These bits, as well as CR[9:2] in the RCCR RC oscillator frequency and to obtain an accuracy of 1%. 10 bits are used for calibration of Internal RC when compared to 8 bits in ST7FLITE1x.

Figure 2. SICSR Register

0 0 0 WDG LOCKED LVDRF AVDF AVDIE		ST7FLITE1x				ST7FLITE1xB									
HF 32 HF	0 0	0	WDG RF	LOCKED	LVDRF	AVDF	AVDIE	LOCK 32	CR1	CR0	WDG RF	LOCKED	LVDRF	AVDF	AVDIE

2.2.2 PWMxCSR Register

In the PWMxCSR (PWMx Control Status Register) two new bits have been added (see Figure 3) corresponding to the One Pulse mode of the Auto reload Timer.

Figure 3. PWMxCSR Register

	ST	7FLI	TE1x						ST	7FLI	TE1x	В				
0	0	0	0	0	0	OPx	CMPFx	0	0	0	0	OP_EN	OPEDG E	OPx	CMPFx	

2.2.3 BREAKCR Register

In the BREAKCR (Break Control Register) two new bits have been added (see Figure 4) related to Break Input Select (External break pin or the output of the comparator) and Break Input Edge selection.

Figure 4. BREAKCR Register





2.2.4 TRANCR Register

The TRANCR (Transfer Control Register) has been replaced by ATCSR2 (Timer Control Register2) (see Figure 5). ATCSR2 contains bits related to the additional features of the Auto Reload Timer i.e. Dual counters, Forced update, Long Input Capture

Figure 5. TRANCR Register Changes

	ST	7FLI	TE1x	(TRA	NCR	1)			ST7FI	ITE1x	B (A1	FCSR	12)	
0	0	o	o	0	0	0	TRAN	FORCE FC	DRCE 1 ICS	OVFIE2	OVF2	ENCNT R2	TRAN2	TRAN1



3 New features in ST7FLITE1xB

3.1 Clock management

Some changes have been made in the clock management. They are as follows:

- It is possible to also run at 4MHz with RC and PLL from 2.7V to 5.5V. An additional PLLTST register is available in ST7FLITE1xB containing the PLLDIV2 bit which allows you to divide the PLL output clock by 2. Hence, x4 PLL (x4PLL from 2.7V to 3.3V and x8PLL / 2 from 3.3V to 5.5V) is effectively available for the entire operating voltage range of the device (2.7V to 5.5V).
- 2. Ceramic Oscillator has a self-controlled gain feature, an oscillator of any frequency from 1 to 16 MHz can be connected to the OSC1 and OSC2 pins. For the ST7FLITE1xB through the option bytes External Oscillator is enabled but the frequency range need not be selected. For STFLITE1x the frequency range of the oscillator should also be selected. Refer to section 7 for details.
- 3. The Internal RC of ST7LITE1x has to be calibrated by writing a 8-bit calibration value in the RCCR (RC Control Register). In contrast, the Internal RC of ST7LITE1xB must be calibrated by writing a 10-bit calibration value in the RCCR (RC Control Register) and in bits 6:5 in the SICSR (SI Control Status Register).
- 4. The predefined calibration values for ST7LITE1x: RCCR0 @ 5V and RCCR1 @ 3V are stored at locations FFDEh and FFDFh for ST7LITE1x. The predefined calibration values for ST7LITE1xB: RCCRH0 & RCCRL0 @ 5V and RCCRH1 & RCCRL1 @ 3.3V are stored at locations DEE0h, DEE1h, DEE2h and DEE3h.
- 5. The predefined calibration value for ST7LITE1x: RCCR1 @ 3V is used for obtaining an Internal RC frequency of 700KHz. The value for ST7LITE1xB, RCCRH1 & RCCRL1 @ 3.3V is used for obtaining an internal RC frequency of 1MHz.

3.2 12-bit autoreload timer

The 12-bit Auto-Reload Timer has been modified to provide more features like Dual counters, Long Input Capture, Internal Break Control, Dead Time generation, One Pulse mode and Forced Update. All the other features of the timer do not change.

3.2.1 Dual counters

Apart from Single Timer mode, Dual Timer mode is available with two 12-bit upcounters and two 12-bit autoreload registers.

3.2.2 Break function

Some additions in this feature are

- Break function can be activated through an Internal Comparator output
- Break active level can be programmed instead of just low level in ST7FLITE1x
- When the break function is active, the break pattern is forced on the PWMx outputs if OEx is set whereas in ST7FLITE1x the active break pattern is forced on the PWMx outputs irrespective of whether OEx bit is set or reset.

3.2.3 Dead time generation

A programmable dead time can be inserted between PWM0 and PWM1. This is required for half-bridge driving where PWM signals must not be overlapped.

3.2.4 Long input capture

In addition to the normal Input Capture mode, Long Input Capture is available in ST7FLITE1xB. Using this mode, pulses that last more than 8us can be measured with an accuracy of 4us. This configuration allows you to cascade the Lite Timer and the 12-bit AT3 Timer to get a 20-bit Input Capture value.

3.2.5 One pulse mode

One pulse mode can be used to control PWM2/3 signal with External LTIC pin. This mode is only available in dual timer mode.

3.2.6 Forced update

In order not to wait for CNTRx overflow to load the value into the active DCRx registers, a programmable CNTRx overflow is provided. For both counters, a separate bit is provided which when set makes the counters start with the overflow value i.e. FFFh. After overflow, the counters start counting from their respective auto reload registers.

3.3 Analog comparator

ST7FLITE1B has an analog comparator and an internal voltage reference. The voltage reference can be external or internal, selectable under program control. The comparator input pins, COMPIN+ and COMPIN- are also connected to A/D Converter.

3.3.1 On-chip analog comparator

The analog comparator compares the voltage at the two inputs COMPIN+ and COMPIN- which are connected to VP and VN at the input of the comparator. When the analog input at COMPIN+ is less than analog input at COMPIN-, the output of the comparator is 0. When the analog input at COMPIN+ is greater than analog input at COMPIN- the output of the comparator is 1.

3.3.2 Programmable internal voltage reference

The voltage reference module can be configured to connect the comparator pin to one of the following sources:

- **Fixed internal voltage bandgap:** The voltage reference module can generate a fixed voltage reference of 1.2V on the VN input.
- **Programmable internal reference voltage:** The internal voltage reference module can provide 16 distinct internally generated voltage levels from 0.2V to 3.2V each at a step 0.2V on the comparator pin VN.
- External voltage reference: If you want to have a reference voltage other than the one generated by the internal voltage reference module, you can connect the COMPIN- to an external voltage source.



4 Electrical characteristics

There are several differences in the electrical parameters between the ST7LITE1x and ST7LITE1xB. The principal differences are shown in the tables below. Please refer to the respective datasheets for the complete specifications.

Symbol	Parameter	Conditions	ST7Lite1x	ST7FLite1xB	Unit
		High Threshold	4.25	4.15	V
V _{IT+(LVD)}	Reset release	Medium Threshold	3.60	3.55	V
		Low Threshold	2.90	2.85	V
		High Threshold	4.05	3.95	V
V _{IT-(LVD)}	Reset generation threshold (Vpp fall)	Medium Threshold	3.40	3.35	V
		Low Threshold	2.7	2.7	V
V _{hys}	LVD Voltage thresh- old hysteresis		200	200	mV
Vt _{POR}	V _{DD} rise time rate		0.02 - 20	0.02 - 100	ms/V

 Table 2.
 Operating conditions with Low Voltage Detector (LVD) - typical values

Table 3. Auxiliary Voltage Detector (AVD) - typical values

Symbol	Parameter	Conditions	ST7Lite1x	ST7FLite1xB	Unit
	1=> 0 AVDF flag tog-	High Threshold	4.70	4.40	V
V _{IT+(AVD)}	gle threshold (V _{DD}	Medium Threshold	4.10	3.85	V
	rise)	Low Threshold	3.40	3.15	V
	0=1 0 AVDF flag tog-	High Threshold	4.60	4.15	V
V _{IT-(AVD)}	gle threshold (V _{DD}	Medium Threshold	3.90	4.0	V
	fall)	Low Threshold	3.20	3.35	V
V _{hys}	LVD Voltage thresh- old hysteresis		200	200	mV

Table 4. Internal RC oscillator and PLL

Symbol	Paramatar	:	ST7Lite1>	[s	Unit		
Symbol	Farameter	Min	Тур	Max	Min	Тур	Мах	Onit
V _{DD(RC)}	Internal RC Oscillator operat- ing voltage	2.4		5.5	2.7		5.5	
V _{DD(x4PLL)}	x4 PLL operating voltage	2.4		3.3	2.7		3.3	V
V _{DD(x8PLL)}	x8 PLL operating voltage	3.3		5.5	3.3		5.5	
t _{STARTUP}	PLL startup time		60			60		f _{PLL} cy- cles

Note: Refer to 3.1 for more details.



Symbol	Parameter	Conditions	ST7Lite1x	ST7FLite1xB	Unit
	Supply current in RUN mode	f _{CPU} = 8MHz	7.50	5.7	mA
	Supply current in WAIT mode	f _{CPU} = 8MHz	3.70	2.2	mA
I _{DD}	Supply current in SLOW mode	f _{CPU} = 8MHz	1.60	0.7	mA
	Supply current in SLOW-WAIT mode	f _{CPU} = 8MHz	1.60	0.5	mA
	Supply current in HALT mode	-40°C°‹TA°‹+85°C	1.0	1.0	μΑ
I _{DD}	Supply current in AWUFH mode	TA= +25°C	20	20	μA

Table 5. Supply current - typical values @ $V_{DD} = 5.5V$



5 Device ordering information

The complete order code of ST7LITE1x is ST7FLITE1xF1M6.

The complete order code of ST7LITE1xB is ST7FLIT1xB(F/Y)1(M/B)6.

Please note that the The 'E' in "LITE" is suppressed in the ST7LITE1xB order code for length reasons.



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