AN1948
APPLICATION NOTE

DVD Combo Power Supply with VIPer53

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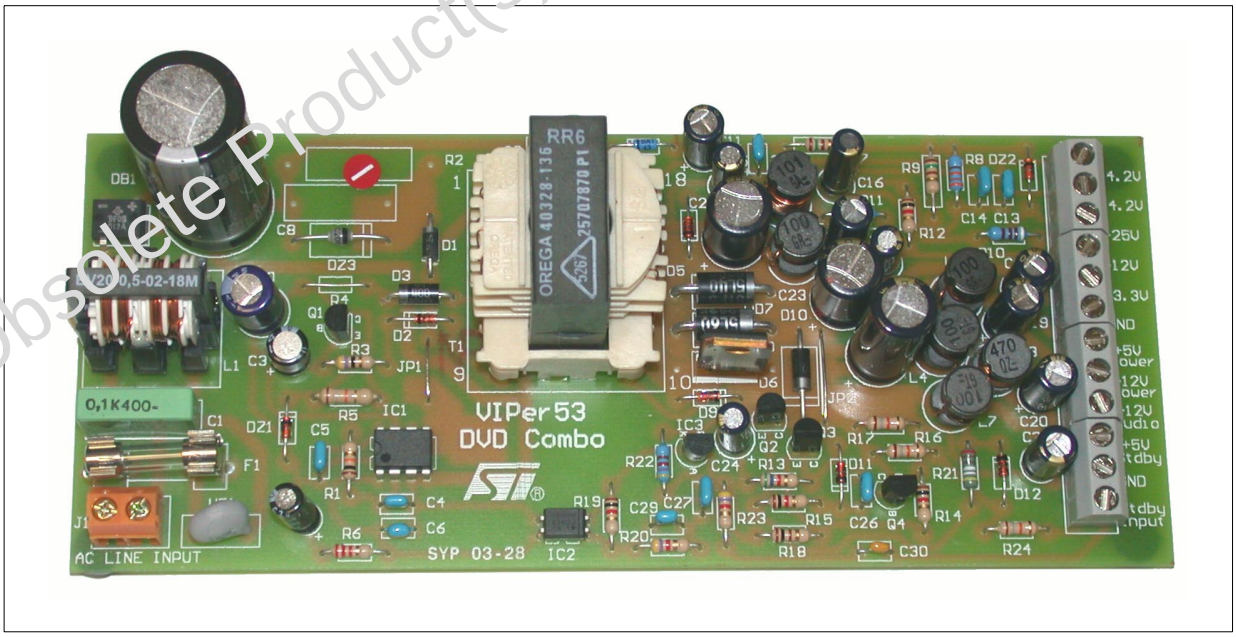
Despite the strong growth of the DVD readers, the VCR ones are still present on the market. A lot of equipment now includes both types of media in the same case. This paper proposes a typical solution to efficiently supply such applications and other equipment where logic, DC motor drive and LCD display are to be implemented together in the 35W power range and suite any input voltage standard (85Vac to 265Vac).

Key features for this application are high efficiency, low standby consumption and cost effective solutions to fit the high volume consumer market needs.

The specification can be summarized as shown in the following table:

	Voltage +/-5%	Maximum Current	Output Power	MaximumPower	Board Size L x W x H
Output 1	**3.3V**	1.5A	4.95W	Normal Operation: **35W max output power** Stand-by Operation: **750mW max input power** With 40mA on the 5VStandby output	170x 70 x 40 (mm)
Output 2	5V Stand-by	100mA	500mW		
Output 3	5V Power	1.5A	7.5W		
Output 4	12V Power	1.5A	18W		
Output 5	12V Audio	200mA	2.4W		
Output 6	-12V Power	15mA	180mW		
Output 7	-25V	25mA	625mW		
Output 8	4.2V Display	50mA	210mW		



1. VIPer53 DESCRIPTION

VIPer53, the first multichip device of the VIPer family has been chosen to fulfill the requirements. It features very low Rdson of 1Ω allowing to deliver up to 35W in wide range in a standard DIP-8 package without a heatsink, answering the need for higher efficiency and reduced space thanks to a lower power dissipation.

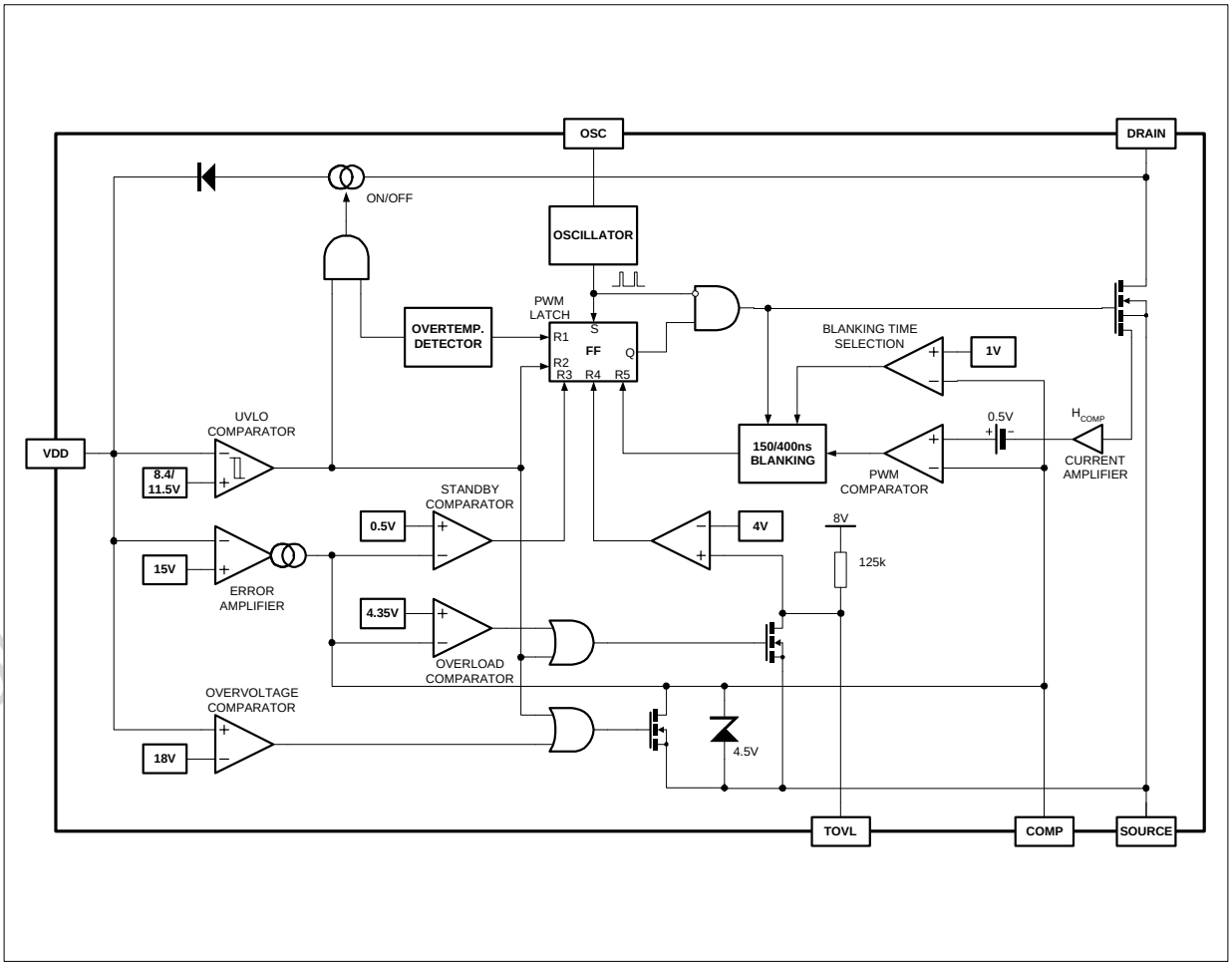
1.1 General features

The block diagram is given in figure 1. An adjustable oscillator drives a current controlled PWM at a fixed switching frequency. The peak drain current is set for each cycle by the voltage present on the COMP pin. The useful range of the COMP pin extends from 0.5V to 4.5V, with a corresponding drain current range from 0A to 2A.

This COMP pin can be either used as an input when working in secondary feedback configuration, or as an output when the internal error amplifier connected on the VDD pin operates in primary feedback to regulate the VDD voltage to 15V.

The VDD undervoltage comparator drives a high voltage startup current source, which is switched off during the normal operation of the device. This feature together with the burst mode capability allows to reach very low level of input power in standby mode, when the converter is lightly loaded.

Figure 1: VIPer53 block diagram



1.2 Overload protection

A threshold of 4.35V typical has been implemented on the COMP pin. This overload threshold is 150mV below the clamping voltage of 4.5V which corresponds to the current limitation of the device. In case of a COMP voltage exceeding the overload threshold, the pull up resistor on the TOVL pin is released and the external capacitor connected on this pin begins to charge. When a value of 4V typical is reached, the device stops switching and remains in this state until the VDD voltage reaches VDDoff, or resumes normal operation if the COMP voltage returns to a value below the overload threshold. The drain current that the device is able to deliver without triggering the overload threshold is called "current capability", specified as IDmax in the datasheet. This value must be used to correctly size the converter versus its maximum output power.

When an overload occurs on secondary side of the converter, the output power is first limited by the current limitation of the device. If this overload lasts for more than a time constant defined by a capacitor connected on the TOVL pin, the device is reset, and a new restarting sequence is initiated by turning on the startup current source. The capacitors on the VDD pin and on the TOVL pin will be defined together in order to insure a correct startup and a low restart duty cycle in overload or short circuit operation. Here are the typical corresponding formulas:

$$C_{OVL} > 12.5 \cdot 10^{-6} \cdot tss$$

$$C_{VDD} > 8 \cdot 10^{-4} \cdot \left(\frac{1}{D_{RST}} - 1\right) \cdot \frac{C_{OVL} \cdot I_{DDch2}}{V_{DDhyst}}$$

$$C_{VDD} > \frac{I_{DD1} \cdot tss}{V_{DDhyst}}$$

Where tss and DRST are respectively the time needed for the output voltages to pass from 0V to their nominal values at startup, and the restart duty cycle in overload or short circuit condition. A typical value of 10% is generally set for this last parameter, as it insures that the output diodes and the transformer don't overheat. The other parameters can be found in the datasheet of the device.

As the VDD capacitor has to respect two conditions, the maximum value will be retained to define its value.

1.3 Stand-by operation

On the opposite load configuration, the converter is lightly loaded and the COMP voltage decreases until it reaches the shutdown threshold typically at 0.5V. At this point, the switching is disabled and no more energy is passed on secondary side. So, the output voltage decreases and the regulation loop rises again above the shutdown threshold, thus resuming the normal switching operation. A burst mode with pulse skipping takes place, as long as the output power is below the one corresponding to the minimum turn on of the device. As the COMP voltage works around 0.5V, the peak drain current is very low (it is actually defined by the minimum turn on time of the device, and by the primary inductance of the transformer) and no audible noise is generated.

In addition, the minimum turn on time depends on the COMP voltage. Below 1V (VCOMPbl), the blanking time increases to 400ns, whereas it is 150ns for higher voltages. The minimum turn on times resulting from these values are respectively 600ns and 350ns, when taking into account the internal propagation time. This feature brings the following benefits:

- this brutal change induces an hysteresis between normal operation and burst mode which is reached sooner when the output power is decreased.
- a short value in normal operation insures a good drain current control in case of short circuit on secondary side.
- long value in standby operation reinforces the burst mode by skipping more switching cycles, thus decreasing switching losses.

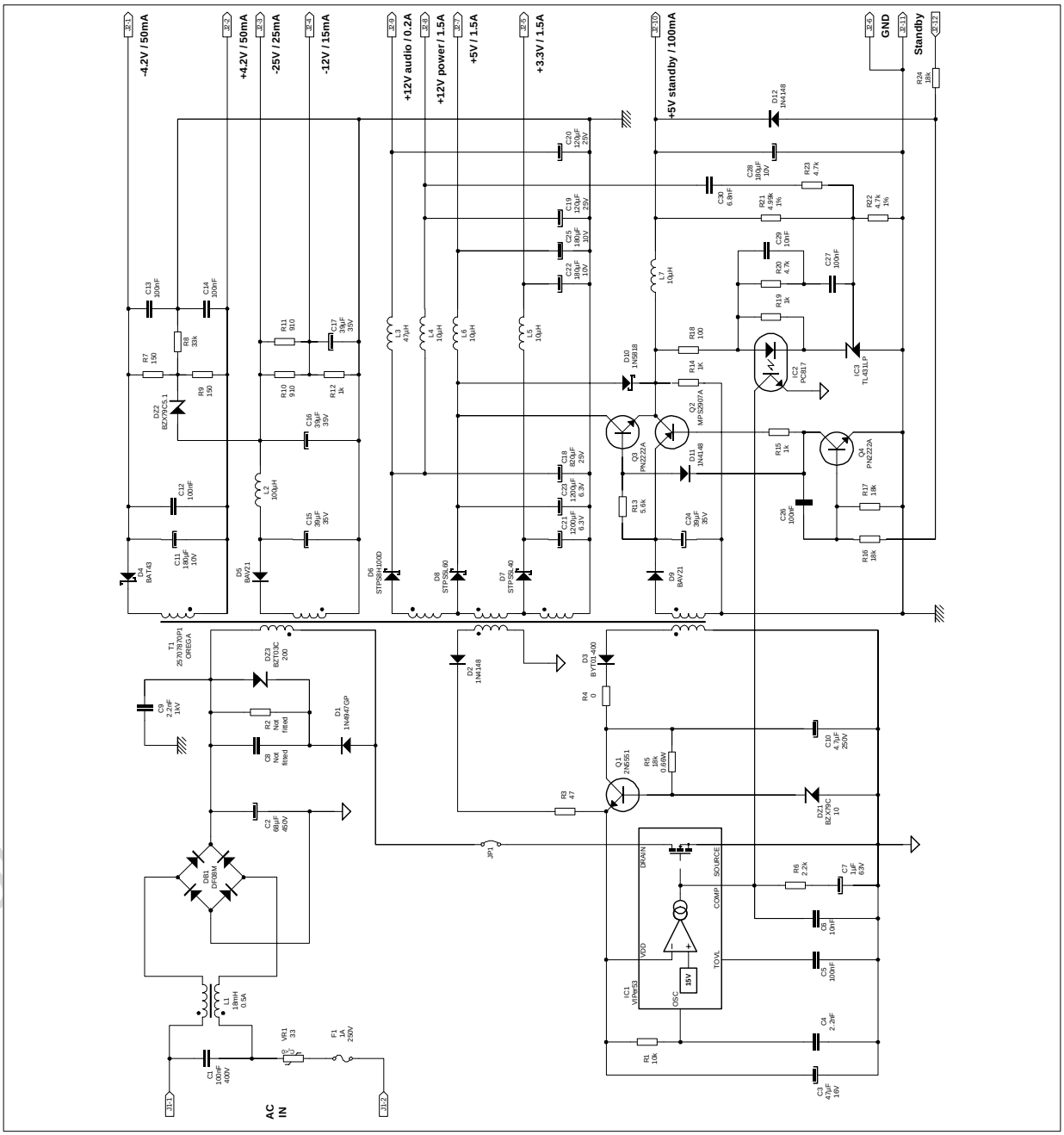
More details regarding the standby operation can be found in the datasheet.

2.0 DVD COMBO POWER SUPPLY

2.1 Schematics

The power topology is an off line flyback working at a fixed switching frequency of 70kHz. The board offers two operating modes. The normal one delivers 8 different output voltages and the standby one only provides a 5V output. This is achieved by a smart standby management feature, based on a specific transformer design which allows to dropout most of the output voltages, providing a low power consumption in standby mode. The overall schematics is presented in figure 2.

Figure 2: schematics



2.1.1 Normal operation mode

In this mode, the Standby input is driven low, Q4 and Q2 are blocked and Q3 conductis. All the output voltages are delivered to the loads and both 5V and 5VStandby outputs are provided.

The transformer turn ratio leads to a voltage of about 30V across C24. This voltage is blocked by Q2, and the 5VStandby output is derived from the main 5V output through Q3. In the case where no load is connected on the 5VStandby output, R14 allows to absorb the Q3 base current delivered by R13.

The same applies at primary side for the auxiliary supply of IC1. In normal operation, the VDD pin energy is delivered by the standard auxiliary winding though D2. The corresponding voltage is higher than the one developed by the zener diode DZ1 on the base of Q1, and this transistor is blocked. In the mean time, the second auxiliary winding delivers five times more voltage than the one needed in standby mode (see section 2.1.2), and values as high as 130V can be observed across C10. As a consequence, C10, D3 and Q1 are high voltage type, and R5 may dissipate up to 1W.

2.1.2 Stand-by mode

All the output voltages are dropped down, except the 5VStandby one which is typically used to supply an infrared receiver and its decoding circuit, and also to maintain the Standby input in the high state, which makes Q4 and Q2 conducting, and disables Q3 thanks to D11.

As Q2 is conducting, the 5VStandby output is supplied through D9 and the corresponding winding of the main transformer. This winding therefore reduces its voltage by a ratio of about 5, because the regulation loop still maintains the value of 5V on this output. Since all the outputs are coupled together on the same transformer core, they are all divided by a ratio of about 5. This is sufficient to insure a reduced consumption mode, as the loads are now supplied with a much lower voltage.

D11 is needed in this mode to efficiently turn off Q3. Otherwise, its base remains high as it is supplied by R13 connected to a voltage of about 5V, and some reverse current flows from the 5VStandby output to the main 5V one.

On primary side, the standard auxiliary winding doesn't provide a sufficient voltage, and Q1 acts as a serial regulator with the voltage delivered by the second auxiliary winding, maintaining the VDD pin of IC1 at higher level than the disabling threshold VDDoff. R14 on the 5VStandby output provides a minimum consumption in this mode to insure a suitable voltage for Q1.

The transition between the normal mode and the standby mode has been slowed down by C26. This is mandatory to avoid any under- or overvoltage on the outputs during this event. See also the following section.

2.1.3 Regulation

The regulation sets the DC operating point from the 5VStandby output through R21 and R22. Note that it would be difficult to implement a split regulation, as the other outputs operate with a different value when in standby mode.

Some AC signals are also introduced into the regulation loop to insure stability. The conventional path is done through R18 connected to the 5VStandby output, but another AC component has been added thanks to C30 and R23 connected on the 12V power output. This is needed to prevent any instability in situations where the 5VStandby output is lightly loaded versus the 12V one. In order to transmit this signal, a resistance R20 has also been added in series with the conventional capacitive feedback C27 at the level of IC3.

The bandwidth of this regulation loop has been set at a few kHz in order to insure a good dynamic response when submitted to load variations, or during the transitions between the normal mode and the standby mode.

C29 on secondary side and C6 on primary side cancel any switching noise which may produce subharmonic operation.

2.1.4 Drain voltage clamping

The board comes with a zener (DZ3) clamp type on the drain of the VIPer53 device. Provision is made to also use an R-C type clamping network to replace this zener. The corresponding components R2 and C8 are to be populated according to the bill of material. See par. 2.3.1.

2.1.5 Short circuit protection

This paragraph only deals with the main outputs (i.e. all the 5V, 12V and 3.3V outputs). The following section deals with the plasma ones.

When in normal mode, all these outputs are protected against a permanent short circuit. When the short circuit is applied on the 5VStandby, the short circuit current flows into D10 which bypasses Q3, thus avoiding its destruction. The protection is done through the overload feature of the VIPer53 device, which leads to hiccup mode when the COMP voltage remains high for a too long time. This time is adjusted by the capacitor on the TOVL pin, and is needed at startup for authorizing a temporary overload during the charge of the output capacitors.

In standby mode, only the 5VStandby output is protected thanks to D12 which forces the standby signal in the low state, and the converter returns to the normal mode where Q2 is off. This is mandatory to avoid the destruction of Q2 and D9 in this condition. The other outputs are not protected against a permanent short circuit, because the converter can still regulate correctly the 5VStandby output even if one of the others is short circuited. This is due to the high turn ratio existing between the 5VStandby winding and the other ones, and to the low consumption on this output. Nevertheless, the user will adopt one of the following options:

- these outputs can withstand a short circuit for a few seconds. If this time is too long, the corresponding rectifying diode may blow up, and the converter will enter into hiccup mode because of the short circuit presented by the blown diode on secondary side of the transformer.
- additional diodes similar to D12 can be implemented on the other outputs to force the converter to the normal mode, where it can withstand permanent short circuit on the main outputs.

2.1.6 Plasma display outputs

A whole set of outputs are dedicated to the driving of a plasma display in front of the equipment: Negative 25V and 12V outputs, together with a symmetrical +/-4.2V centered 5V higher than the -25V output voltage.

Please note that these outputs are not protected against short circuits or overloads. For instance, the short circuit of the 4.2V outputs to ground leads to the destruction of R7 or R9. Also, the rectifying diodes chosen for these outputs don't withstand a permanent short circuit.

Figure 3: startup in normal mode

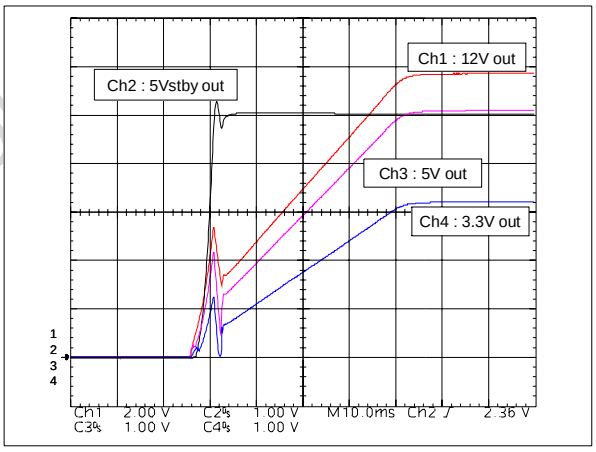
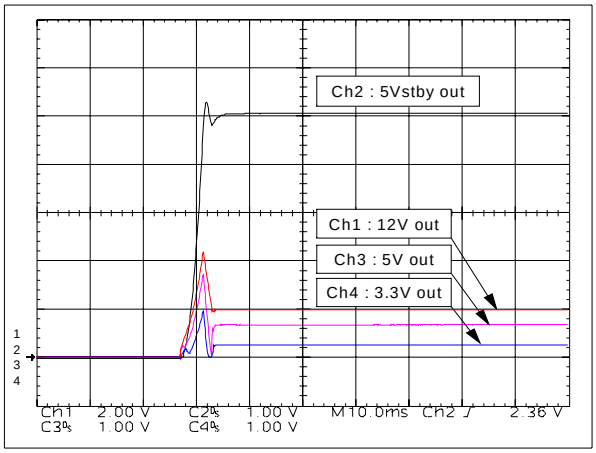


Figure 4: startup in standby mode



2.2 Results

Unless otherwise specified, all the tests are made at 300VDC input voltage and full load.

2.2.1 Startup

When starting, C26 is discharged, and the converter operates in standby mode. So, the 5VStandby voltage appears first, and the other outputs rise slowly, just like a transition from a standby mode to the normal one. Of course, if the Standby signal is asserted high (active level), the converter remains in this mode and only the 5VStandby output is delivered. This is illustrated in figures 3 and 4.

The input voltage doesn't impact on the dynamic behavior of the converter. The rising slope of the output voltage at startup is mainly governed by the charge of C26 with the current defined by the base to emitter voltage of Q4 together with R16 and R17.

2.2.2 Switch off

Figure 5 presents the output voltages at switch off of the converter. All the voltages drop down at the same time, because the converter doesn't deliver any more energy. So, the slopes are individually driven by the output capacitors and the output current.

Figure 5: switch off

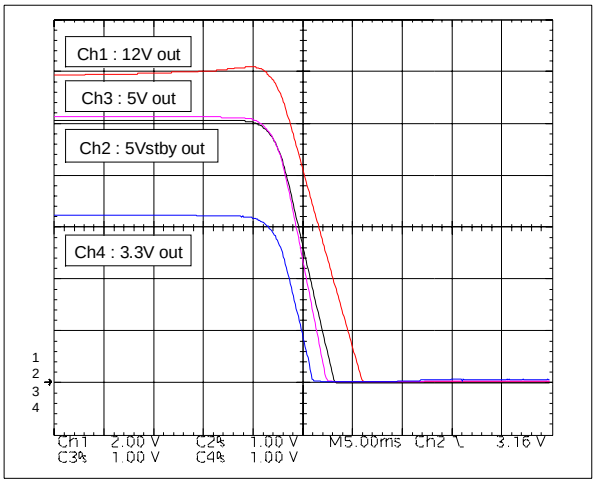


Figure 6: normal to stand-by mode transition

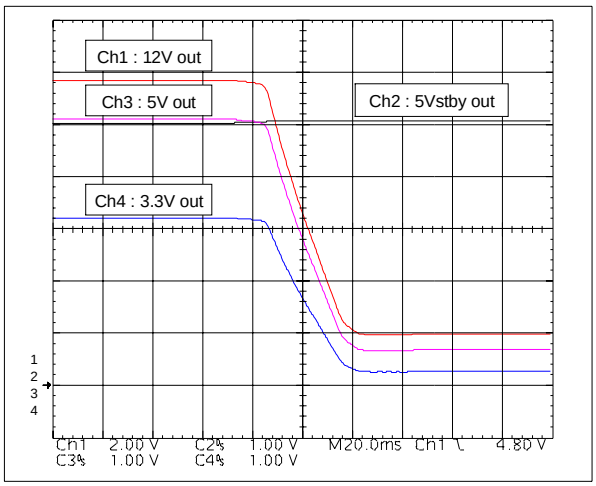


Figure 7: stand-by to normal mode transition

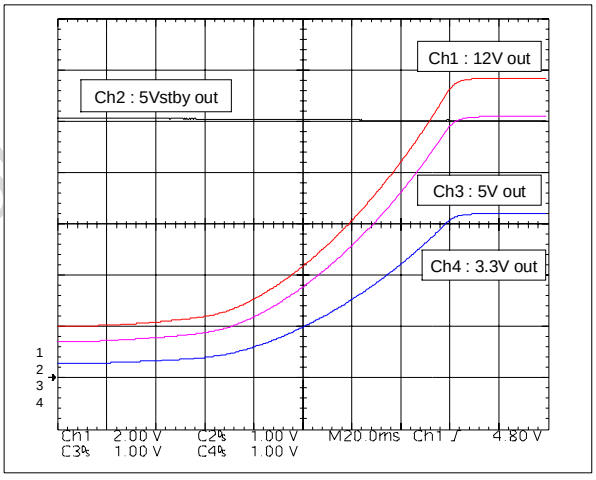
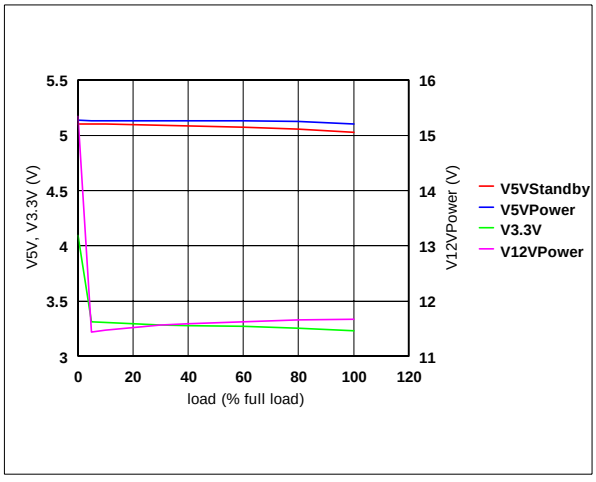


Figure 8: load regulation



2.2.3 Transitions between normal and stand-by modes

The standby input is quickly driven from low state to high state, and inversely. The corresponding evolution of the output voltages are shown in figures 6 and 7. Note the very low disturbance on the 5VStandby output.

2.2.4 Load and cross regulation in normal mode

For these tests, the 12V audio output has always been let open. As it is connected almost in parallel with the 12V power output (only an L-C filter), it is assumed to follow the same voltage variation than this output, and its current is summed to the power one.

Also, load variation are only made on the main power outputs, that is to say the 5Vstandby, the 5V power, the 3.3V and the 12V power ones. The -25Vand +/-4.2V secondary outputs are either not loaded (load regulation test) or fully loaded (cross regulation test).

The load regulation is checked by changing the loads on all the outputs simultaneously. This test is also used for measuring the efficiency of the converter over a large range of output power. Figure 8 shows the corresponding results for the four main outputs and figure9 the ones for the two secondary ones.

When not loaded, the converter operates correctly, except for the 12V and 3.3V outputs which do not have any load. So, the corresponding voltages rise up respectively to 15.3V and 4.1V. If this is not acceptable, the user has to foresee an adequate minimum load or a clamper.

Figure 9: cross regulation for secondary outputs

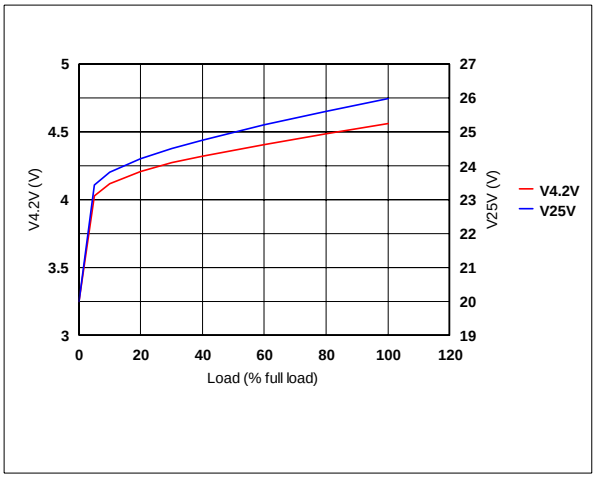
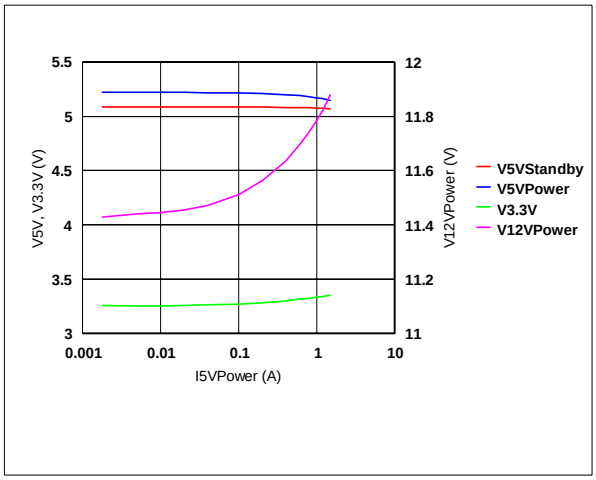


Figure 10: 5VPower cross regulation



As the load on the secondary outputs is zero during this test, figure 9 shows the cross regulation between the main outputs and the secondary ones. Note that the secondary output voltages don't change significantly versus their own load current, because these currents are low values, and these outputs are already significantly loaded on the board itself. So, no load regulation is presented for the secondary outputs.

The cross regulation between the main outputs has been measured. For this purpose, all the output are loaded at intermediate level (half the maximum rated load), except one output which varies between zero and maximum load. This test is repeated for the four main outputs and is presented in figures 10 to 13. The result is also used for computing the relative efficiency for each main output.

Figure 11: 5VStandby cross regulation

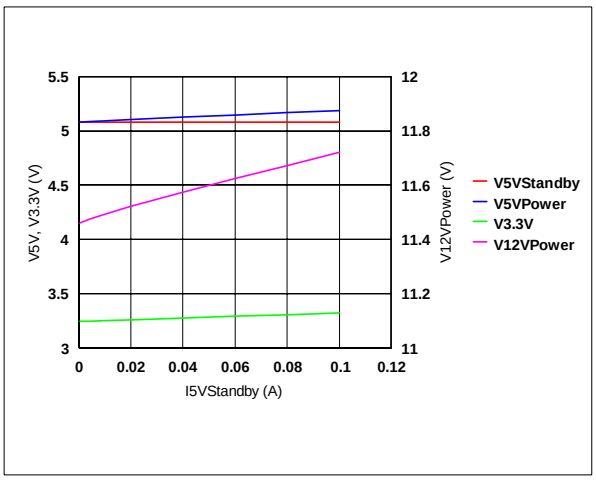


Figure 12: 3.3V cross regulation

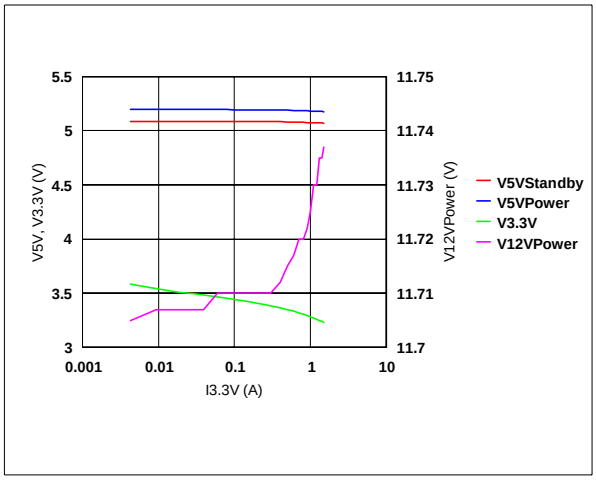


Figure 13: 12VPower cross regulation

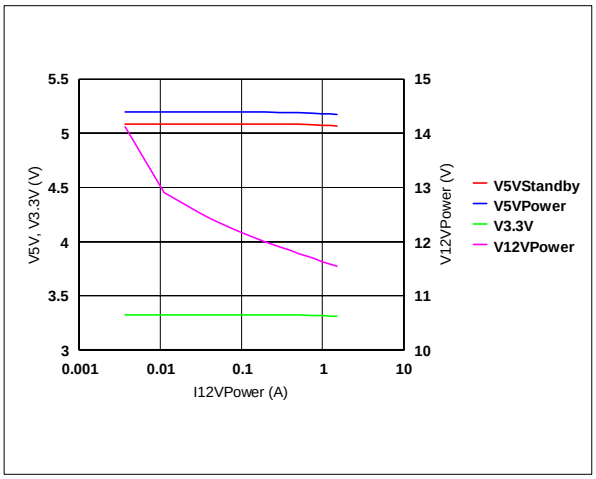
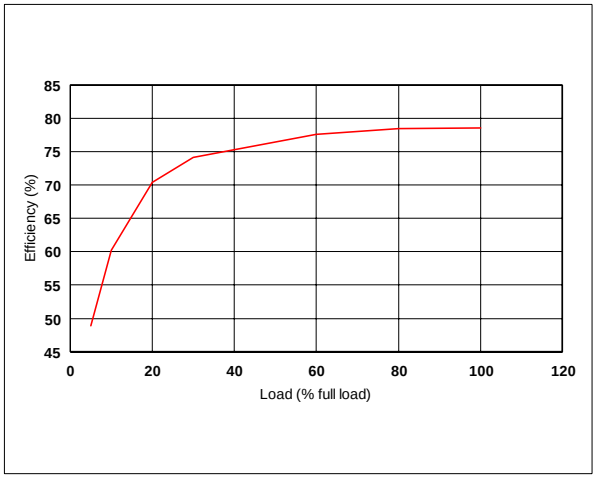


Figure 14: Global efficiency



2.2.5 Efficiency in normal mode

The global efficiency is measured by varying all the outputs load simultaneously, except for the secondary ones (-25V and +/-4.2V) which are not loaded in order to get the lowest values. Figure 14 presents the result.

Each cross regulation measurement is used for computing the relative efficiency Er on the corresponding output by using the following formula:

$$E_R = \frac{P_{outmax} - P_{outmin}}{P_{inmax} - P_{inmin}}$$

The results are shown in the following table:

	3.3V	5VStandby	5VPower	12VPower
Er	77%	73%	80%	85%

The lower the output voltage, the lower the relative efficiency because of the fixed voltage drop in the output rectifying diodes. The relative efficiency for the 5VStandby output is low when compared to the other ones, because of two reasons:

1) it is derived from the 5VPower output, with a voltage drop in Q2 of about 100mV which leads to a loss of 2% in efficiency.
2) when the output current on the 5VStandby increases, its output voltage remains fixed by the regulation loop, and all the other outputs increase by 2%. So, the onboard dummy loads for the secondary outputs (R7 to R12) increase by 5% (related to the 500mW of full load on the 5VStandby output), and the relative efficiency is decreased by this figure.

Overall, the total efficiency is decrease by 7%, which corresponds to the difference between the 5VPower and the 5VStandby outputs.

The efficiency has also been measured at full load and for an input voltage varying between 120Vdc and 400Vdc. The results are shown in figure 15.

Figure 15: efficiency Vs. input voltage

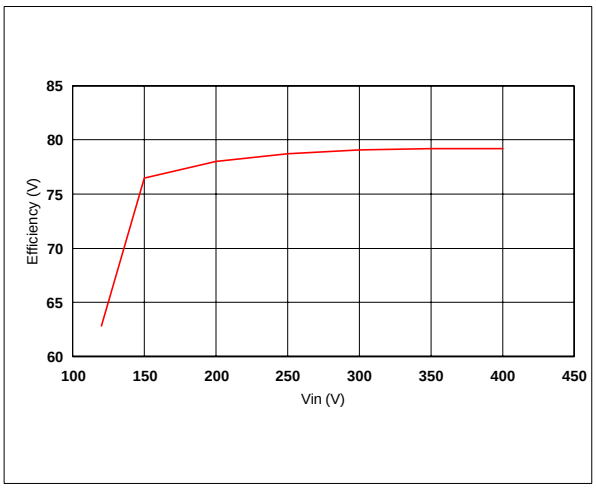
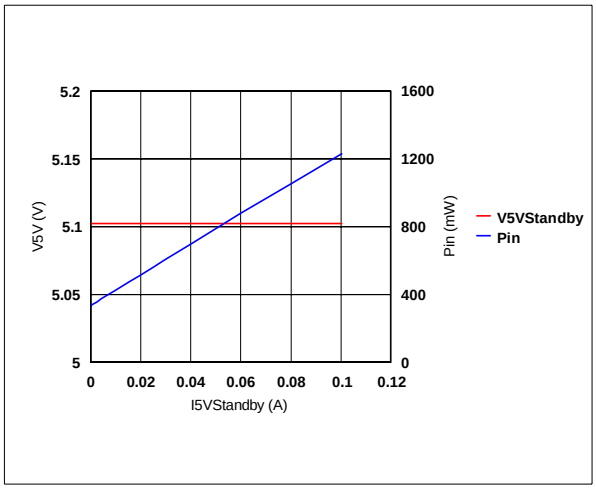


Figure 16: load regulation and input power in standby mode



2.2.6 Load regulation and input power in standby mode

As there is only one active output in standby mode, there is no cross regulation measurement. Instead, the input power is measured to check its compliance versus specific energy saving standards like Energy Star or Blue Angel. Both output voltage value and input power are shown in figure 16.

All the other outputs are not loaded. The user will pay attention to its real load, which may consume some power in this condition: Even if the voltages are reduced by a ratio of five or more, they are still able to deliver the rated current!

At 300Vdc input voltage, the converter always works in burst mode in standby condition. This mode is characterized by the fact that the device skips some switching cycles, as shown in figure 17. The magnification in figure 18 presents a conduction time of 700ns, which corresponds to the long blanking time of the VIPer53 device, as the COMP voltage operates around the shutdown value (0.5V typical), well below the blanking value threshold (1V typical). Also note the reduced reflected value versus the normal full load switching cycle in figure19.

Figure 17: burst mode in standby condition

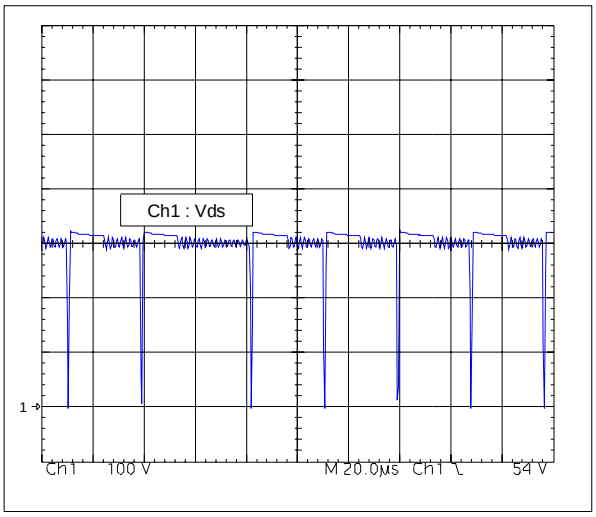
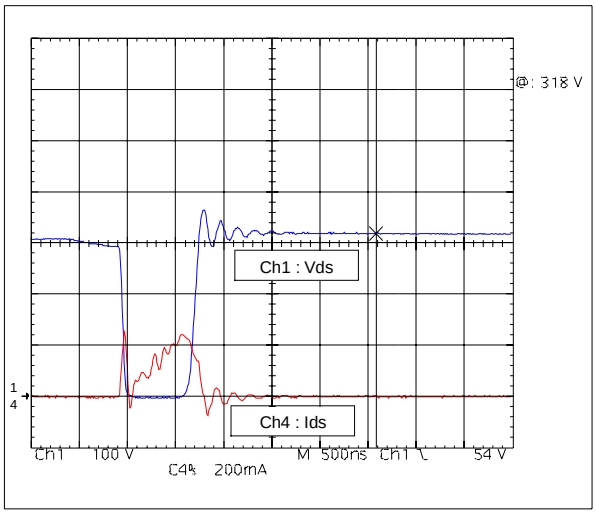


Figure 18: Magnification of a switching cycle in standby condition



2.2.7 Line regulation

The output voltage has been measured at full load for an input voltage varying between 120Vdc and 400Vdc for both power (figure 20) and secondary (figure 21) outputs.

Figure 19: normal full load switching cycle

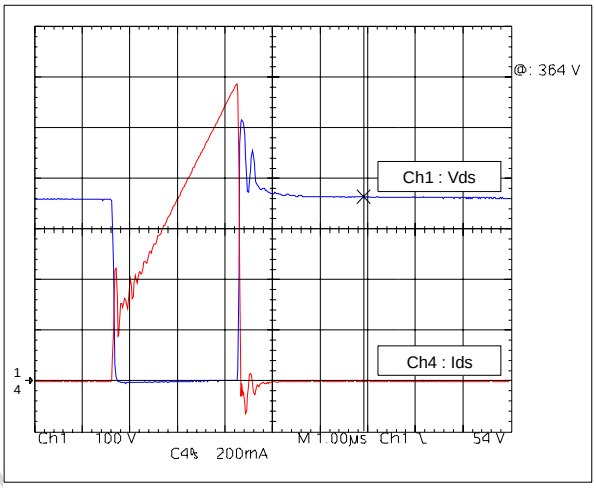
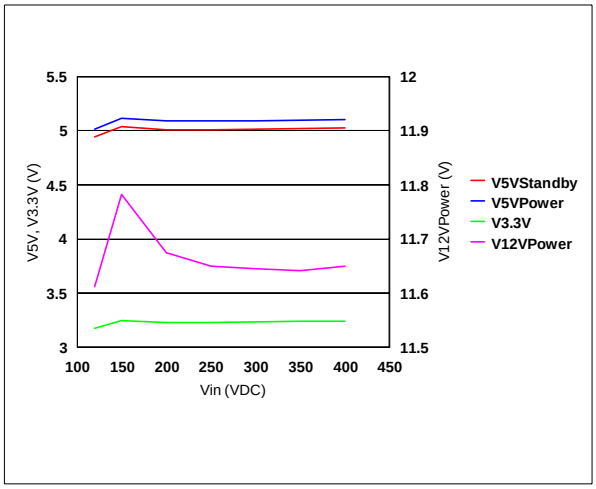


Figure 20: Line regulation for the main outputs



2.2.8 Dynamic load variation

Each main output has been submitted to fast load variation between 10% and 100% of their rated full load. All the others are loaded with a fixed current corresponding to half load. Results are presented in figures 22 to 25.

Figure 21: line regulation for secondary outputs

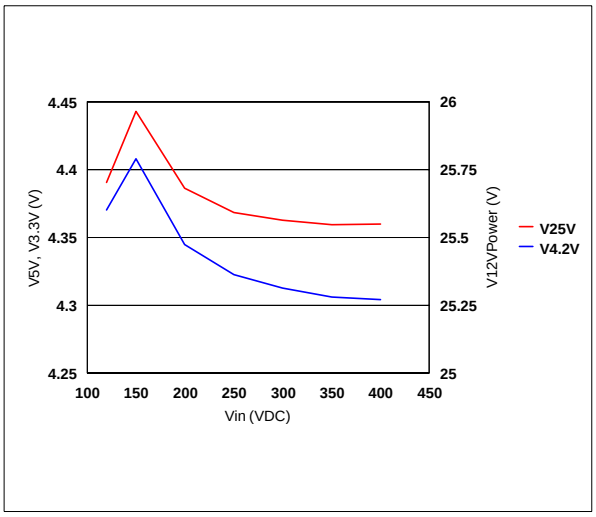


Figure 22: 5VPower dynamic load regulation

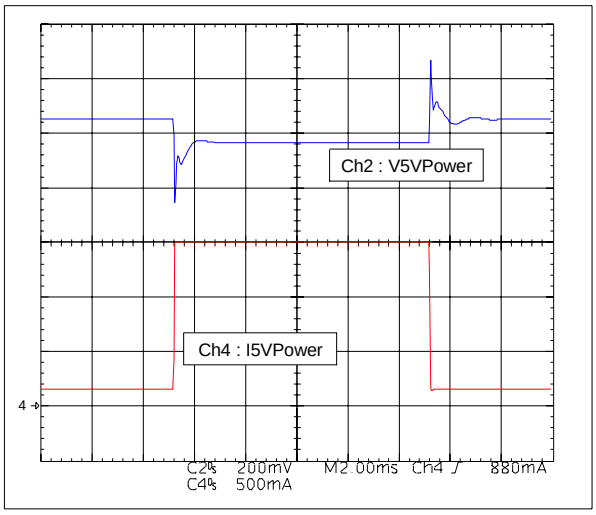


Figure 23: 5VStandby dynamic load regulation

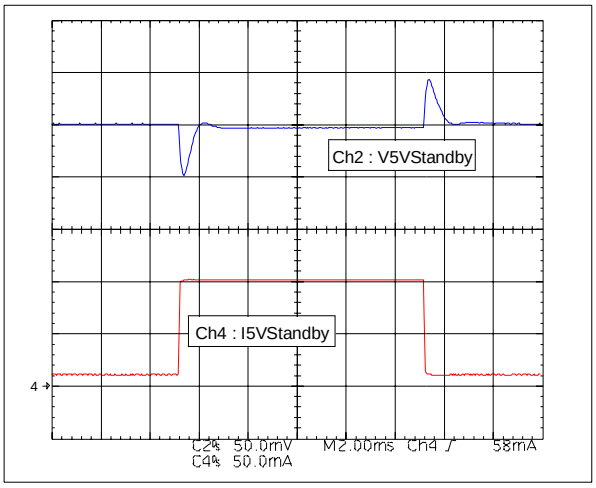
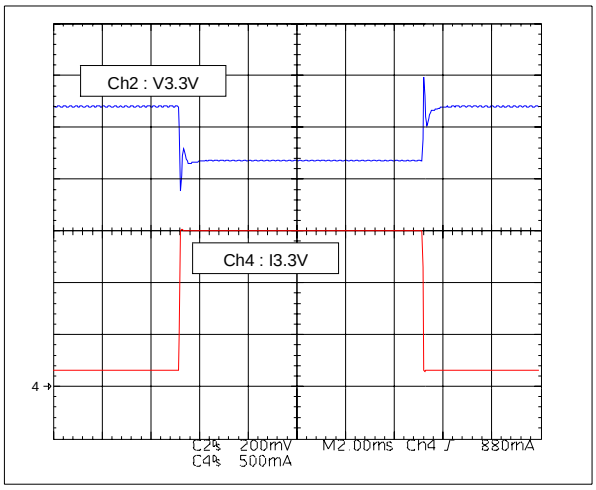


Figure 24: 3.3V dynamic load regulation



2.2.9 Stability

An example of stability measurement is presented in figure 26 at full load. The phase margin is about 50° with a gain margin of about 10dB.

Figure 25: 12V dynamic load regulation

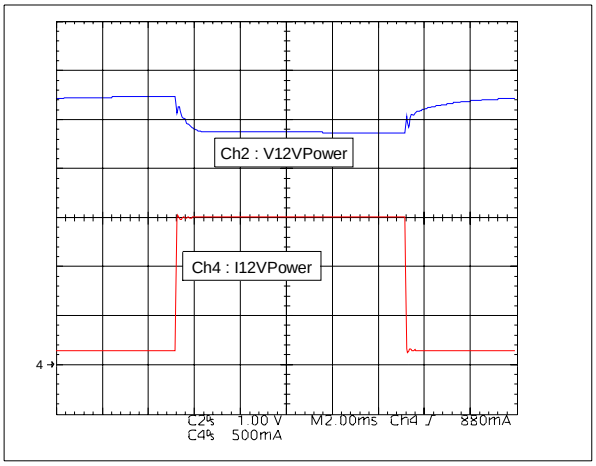
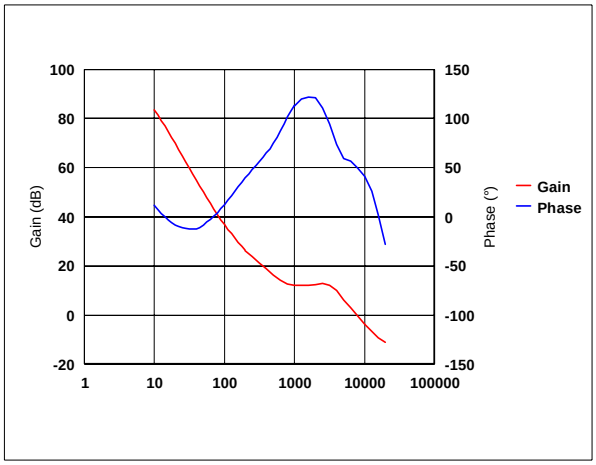


Figure 26: gain and phase plot at full load



2.2.10 Short circuit operation

Refer to paragraph2.1.4 and 2.1.5 for the effectiveness of the short circuit protections.

A short circuit has been made on the 12VPower output in the normal mode. The converter protects itself by entering an endless restarting sequence, driven by the VIPer53 VDD voltage collapsing down to the VDDoff threshold periodically.

Note that the VDD voltage doesn't decrease sufficiently during the switching operation, and that the overload feature of the device is the real protection. This is visible in figure27, where the TOVL voltage rises up as soon as the COMP pin is stuck to its maximum value of about 4.5V. When it reaches the overload threshold (about 4V), the converter halts switching, and the VDD voltage decreases a little bit and remains at 9.6V for 30ms. This is due to the additional auxiliary winding and associated components which discharge the energy stored in C10, and act as a serial regulator. Then, the VDD voltage definitely decreases until it triggers the reset voltage VDDoff (8.4V typical), and the device activates its internal high voltage startup current source to recharge the VDD capacitor C3.

The full restarting cycle can be observed in figure28. The restarting duty cycle defined as the ratio of the active phase where the VIPer53 device switches, over the total restarting cycle, is kept to about 8%. This low value prevents any overheating of the output diode and of the transformer. The short circuit can be indefinitely applied without any stress for the converter.

Figure 27: short circuit protection

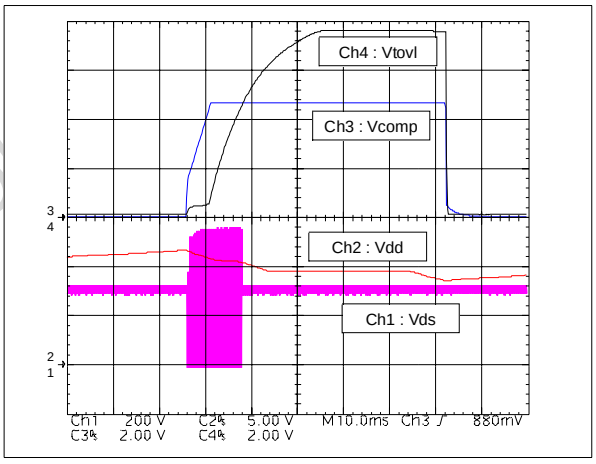
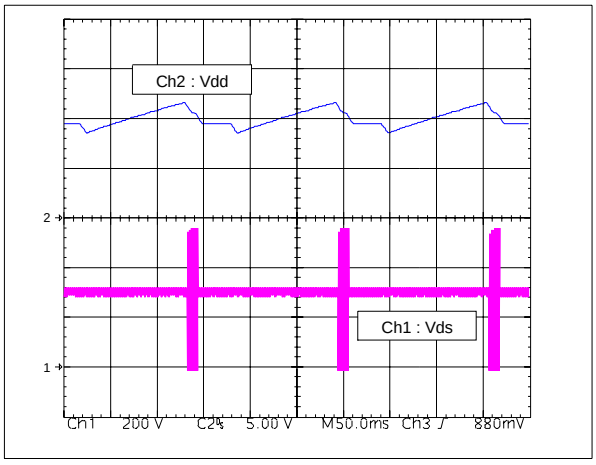


Figure 28: Restarting cycles



2.3 Board description

2.3.1 Bill of material

Q.ty	Reference	Description	Note
1	D1	1N4947GP Diode	
3	D2, D11, D12	1N4148 Diode	
1	D3	**STMicroelectronics BYT01-400 Diode**	
1	D4	**STMicroelectronics BAT43 Schottky Diode**	
2	D5, D9	BAV21 Schottky Diode	
1	D6	**STMicroelectronics STPS8H100D Schottky Diode**	
1	D7	**STMicroelectronics STPS5L40 Schottky Diode**	
1	D8	**STMicroelectronics STPS5L60 Schottky Diode**	
1	D10	**STMicroelectronics 1N5818 Schottky Diode**	
1	DZ1	BZX79C10 Zener Diode	
1	DZ2	BZX79C5.1 Zener Diode	
1	DZ3	BZT03C200 Zener Diode	
1	DB1	DF08M Diode bridge	
1	Q1	2N5551 transistor	
1	Q2	**STMicroelectronics PN2907A** transistor	
2	Q3, Q4	**STMicroelectronics PN2222A** transistor	
1	IC1	**STMicroelectronics VIPer53 SMPS controller**	
1	IC2	PC817 Optocoupler	
1	IC3	**STMicroelectronics TL431ILP Voltage reference**	
1	C1	100nF 20% 400V Ceramic capacitor	
1	C2	68µF 20% 450V Electrolitic capacitor	
1	C3	47µF 20% 16V Electrolitic capacitor	
1	C4	2.2nF 10% 100V Ceramic capacitor	
6	C5, C12, C13, C14, C26, C27	100nF 10% 100V Ceramic capacitor	
2	C6, C29	10nF 10% 100V Ceramic capacitor	
1	C7	1µF 20% 63V Electrolitic capacitor	
0	C8	6.8nF 10% 400V Ceramic capacitor	Option - not fitted
1	C9	2.2nF 10% 1KV Ceramic capacitor	
1	C10	4.7µF 20% 250V Electrolitic capacitor	
4	C11, C22, C25, C28	180µF 20% 10V Electrolitic capacitor	
4	C15, C16, C17, C24	39µF 20% 35V Electrolitic capacitor	
1	C18	820µF 20% 25V Electrolitic capacitor	
2	C19, C20	120µF 20% 25V Electrolitic capacitor	
2	C21, C23	1200µF 20% 6.3V Electrolitic capacitor	
1	C30	6.8nF 10% 100V Ceramic capacitor	
1	R1	10KΩ 1/4W 5% Resistor	
0	R2	22KΩ 3W 5% Resistor	Option - not mounted
1	R3	47Ω 1/4W 5% Resistor	
1	R4	0 Resistor	
1	R5	18KΩ 1/2W 5% Resistor	
1	R6	2.2KΩ 1/4W 5% Resistor	
2	R7, R9	150Ω 1/4W 5% Resistor	
1	R8	33KΩ 1/4W 5% Resistor	
2	R10, R11	910Ω 1/4W 5% Resistor	

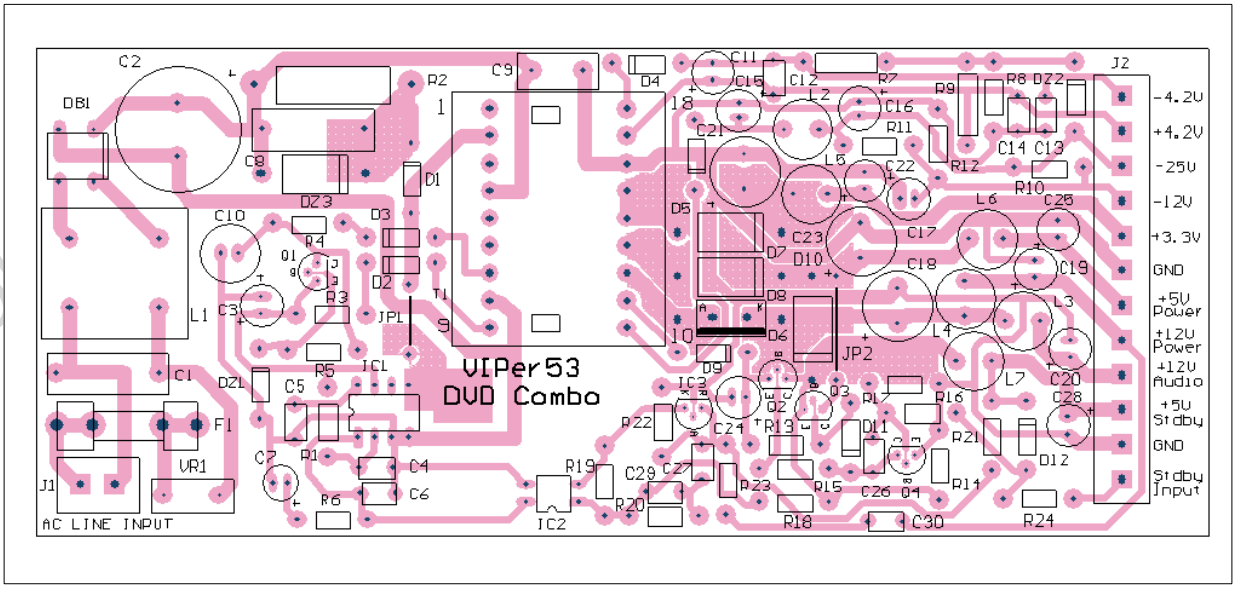
Bill Of Material (Continued)

Q.ty	Reference	Description	Note
4	R12, R14, R15, R19	1KΩ 1/4W 5% Resistor	
1	R13	5.6KΩ 1/4W 5% Resistor	
3	R16, R17, R24	18KΩ 1/4W 5% Resistor	
1	R18	100Ω 1/4W 5% Resistor	
2	R20, R23	4.7KΩ 1/4W 5% Resistor	
1	R21	4.99KΩ 1/4W 1% Resistor	
1	R22	4.7KΩ 1/4W 1% Resistor	
1	L1	18mH 0.5A Common mode filter	
1	L2	100µH 10% 0.75A Inductor	
1	L3	47µH 10% 1.4A Inductor	
4	L4, L5, L6, L7	10µH 20% 4.3A Inductor	
1	T1	Thomson Multimedia - Orega 25707870P1 Transformer	
1	F1	250V 1V Fuse	
2	F1	Fuse clip	
0	No Ref.	18ºC/W Dissipator	Option - not fitted
1	J1	2 Points connector	
4	J2	3 Points connector	
4	No Ref.	Adhesive base	1 per board angle

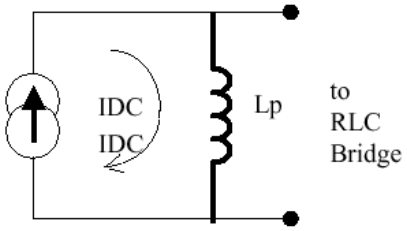
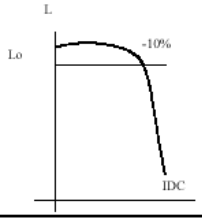
2.3.2 Board layout

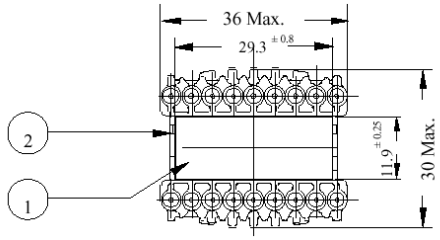
Conventional cares have been observed when designing this board:

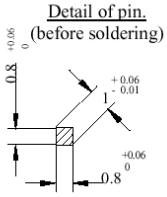
- the ground pin of IC1 (VIPer53 device) is a star point for two connections: The first one is dedicated to the power ground line issued from C2 and the transformer T1, and the second one is reserved for all low signal components associated with this circuit. This rule should be respected in order to avoid any spurious noise to be injected on the signal pins.
- a sufficient copper area is foreseen at the level of the drain pin of IC1 and for all main secondary rectifying diodes (D6 to D8) in order to provide a heatsink capability for these devices.

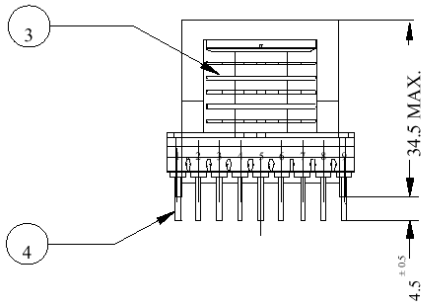


2.3.3 Transformer specification

	ITEMS	CONDITIONS	SPECIFICATIONS
1	Primary inductance	Measuring points : 2 and 4 Measuring frequency 1 kHz Applied voltage : 250 mV	Lp = 808 µH ± 12 %
2	Leakage inductance	Measuring points 2 and 4 Measuring frequency 10 kHz (all secondaries shorted)	See typical value
3	DC superimposed current	 **Lp : primary inductance**	L = Lo x 0.9 for I sat = 1.8 A at 100°C 
4	Max. primary power		45 w
5	Operating voltage		90v-270v
6	Operating frequency		70 Khz fixed
7	Controller circuit		Viper53
8	Regulation Mode		Secondary (5V)







Number of turns:	
Primary	67 turns
Auxiliary	66 turns
Add. auxiliary	66 turns
3.3V	4 turns
5VPower	6 turns
12V	13 turns
- 25V	27 turns
- 4.2V / 4.2V	5 turns
5VStandby	28 turns