AN1787
Application note

Conversion Guide, uPSD3200 to uPSD3400 series

1 Introduction

The uPSD family currently consists of three series, uPSD3200, uPSD3300, and uPSD3400. All three series are available in the same kind of packages (52-pin and 80-pin TQFP), but there are a few differences in pin definitions. This document describes the differences and suggests methods to easily migrate designs from the uPSD3200 series to uPSD3400. You can implement simple techniques on your printed circuit board to accept either a uPSD3200 or a uPSD3400 during manufacturing. Please see Application Note AN1724 for similar information regarding migrating designs from the uPSD3200 series to the uPSD3300 series, and see AN1773 for migrating from uPSD3300 to uPSD3400 designs.

Pin differences will be presented two categories:

- Mandatory pin function changes for all applications, and
- Conditional pin function changes depending on the application.

There are also differences in SFRs and interrupt vectors, which may impact firmware depending on the application. These differences are identified to help you migrate your firmware.

For simplicity, the uPSD3200 series will be referred in this document as 3200, and the uPSD3400 series will be referred to as 3400.

Contents

1.1 Summary of differences

1.1.1 MCU Core Voltage

The 3400 MCU core requires a 3.3V supply, even when used in a 5V system. This means two separate supplies (5V V_{DD} and 3.3V V_{CC}) are required in a 5V system, but just one supply (3.3V V_{CC}) is required for a 3.3V system. In contrast, 3200 devices use only a single V_{CC} supply, which is 5V V_{CC} for 5V devices, or 3.3V V_{CC} for 3.3V devices.

1.1.2 MCU Core

The 3200 MCU requires 12 clocks per instruction but the 3400 uses just 4 clocks. The 3400 does not have an optional 12-clock operation mode. No modifications are needed to 3200 firmware for standard 8032 functions unless timing was established with software loops. Modifications ARE required for firmware controlling some peripherals when migrating to 3400.

1.1.3 PWM

The five 8-bit PWM channels of the 3200 are implemented with the Programmable Counter Array (PCA) in the 3400, which has six 16-bit timer/counter modules. There are new SFRs, and some PWM pin number assignments have changed on the 3400.

1.1.4 ADC

The four 8-bit ADC channels of the 3200 are implemented using four of the eight 10-bit ADC channels on the 3400. There are new SFRs, but there are no ADC input pin number changes. The ADC reference voltage (V_{REF}) input pin is not available on 52-pin 3400 devices and V_{REF} is shared internally with the 3.3V V_{CC} core supply. 80-pin 3400 devices do have an ADC V_{REF} pin, and its maximum input voltage is V_{CC} (3.3V). The maximum input voltage on any 3400 ADC input or reference is V_{CC} (3.3V) even in a 5V system.

1.1.5 LVD

Both 5V and 3.3V 3400 devices have Low-Voltage Detect (LVD) trip point set for the 3.3V V_{CC} supply level (2.5V). This must be considered when designing 5V systems.

1.1.6 Watchdog

The watchdog timer is enabled after reset on 3200 devices, but it is disabled after reset on 3400 devices.

1.1.7 I/O characteristics

The 3.3V 3400 devices have 5V tolerant I/O on ports 3, and 4, but ports A,B,C, and D are not 5V tolerant. The 3.3V 3200 devices do not have any 5V tolerant I/O ports.

1.1.8 USB

The 3200 supports low-speed USB 1.1 (1.5Mbps), the 3400 supports full-speed USB 2.0 (12Mbps). The 3400 has all new SFRs for the USB channel. Some USB bus pin numbers have changed between the 3200 and 3400.

1.1.9 UART and I^2C

Minor changes to SFR definitions.

1.1.10 DDC

No DDC interface is on the 3400.

1.2 Summary of new uPSD3400 functions

Listed below are new functions on the 3400 that were not available on the 3300:

1.2.1 USB

The 3400 supports USB 2.0 Full-Speed (12Mbps) and includes the USB physical interface. There are a total of 5 pair of endpoints (each pair consists of In and Out). One endpoint pair is for USB Control transfer types, the remaining four endpoint pairs can be used for any combination of USB Interrupt or USB Bulk transfer types. Each individual endpoint has a 64-byte FIFO (10 FIFOs total) to maintain USB data throughput.

1.2.2 MCU Core

The 8032 MCU core of the 3400 operates on 4-clocks per instruction, with a maximum clock rate of 40MHz, yielding 10 MIPS (Million Instructions Per Second) maximum performance for single-byte instructions. The 3400 MCU core has a 16-bit internal path from memory to enhance performance, meaning that double-byte instructions are fetched in a single MCU cycle, which pushes average performance close to the peak performance. No firmware changes are required to take advantage of this enhancement. In summary, 3400 has 10 MIPS peak performance, but you can expect about 9 MIPS average performance, compared to 3.3 MIPS peak and 3.0 MIPS average performance from the 3200.

1.2.3 MCU core timing

The 3400 Turbo MCU core has a six-deep instruction prefetch queue and a four-way branching address cache to increase performance. Code in smaller localities operate very fast. No special firmware is required to take advantage of the prefetch queue or branching cache. Be aware that firmware timing loops will not be accurate because of the non-deterministic nature of pipeline and cache architecture. Please use one of the many hardware timer modules to create timing functions, not firmware loops.

1.2.4 MCU core data pointers

The 3400 Turbo MCU core includes dual data pointers to speed data transfers of XDATA. The pointers can auto-increment and auto-decrement, providing rapid data movement from source to destination locations. The 3200 has one only data pointer.

1.2.5 SPI

An SPI bus master interface is provided on the 3400.

1.2.6 ADC

Eight 10-bit ADC inputs are provided, compared to only four 8-bit ADC inputs on the 3200.

1.2.7 IrDA

The 2nd UART channel supports IrDA protocol, which be connected directly to an IR transceiver.

1.2.8 PCA

The Programmable Counter Array unit has six 16-bit timer/counter (TC) modules that can be used for PWM, Capture/Compare, Timers, or Counters. Three of the six TC modules can operate from one time base, and the other three TC modules can operate from another time base if desired. These six TC modules are in addition to the standard three 16-bit timer units inside the 8032 MCU core, bringing a total of nine 16-bit timer/counters. The 3200 provides only the three standard 16-bit 8032 timers.

1.2.9 JTAG debug

The JTAG port now functions as a debug port in addition to In-System Programming (ISP). This eliminates the need for conventional hardware In-Circuit Emulation (ICE) tools.

1.2.10 Debug

The 3400 has a dedicated debug input/output pin. As an output, it can signal that a specified debug event has occurred, as an input it can trigger a debug event to begin (e.g., breakpoint or trace)

1.2.11 MCU clock

3.3V 3400 devices can be clocked up to 40MHz, unlike 3.3V 3200 with 24MHz maximum.

1.2.12 MCU clock division

The 8032 MCU clock can be divided internally for lower power operation. The MCU may change the clock divider ratio on-the-fly using SFRs. This affects the MCU only, not peripheral clocks.

1.2.13 Cross-Bar I/O

Peripheral functions on Port 1 are also available on Port 4 (cross-bar switch), providing more flexibility. There is no need to sacrifice one peripheral function when two functions are available on a single pin, just use the other port.

1.2.14 High Current I/O

Eight I/O pins on Port 4 are each capable of sinking or sourcing 10mA for both, 3.3V and 5.0V 3400. In contrast, 3.3V 3200 pins are capable of sinking 4mA each, while the 5V 3200 can sink 8mA each.

1.2.15 5V-tolerant I/O

The following pins are 5V tolerant on 3.3V, 52-pin 3400 devices: P1.1 through P1.7, P3.1 through P3.7, P4.1 through P4.7, and RESET_IN_.

On 3.3V, 80-pin 3400 devices, the following pins are also 5V tolerant: MCU_AD0 through MCU_AD7, RD_, WR_, and _PSEN. In contrast, 3.3V 3200 devices had no 5V tolerant I/O pins.

Note: PSD functions have NOT changed from the 3200 to 3400. These functions include PLD, memory mapping, memory management (code space vs. data space, and paging), Flash memories, SRAM memory, and PSD I/O. The wider 16-bit internal data path on the 3400 (compared to 8-bit path on 3200) is transparent to the user.

Please note the SRAM on the 3400 can not be configured to reside in code space.

2 Pin definitions

Figure 1 and *Figure 2* show pin assignments of the 3200 and 3400 devices in both 52-pin and 80-pin TQFP packages. Please see the 3200 and 3400 data sheets for detailed pin function descriptions and physical dimensions of packages. Pins requiring mandatory changes during migration are darkened in the figures, this assumes that USB will be used in both the 3200 and 3400 applications.

Note: 5V 3200 devices support USB while the 3.3V 3200 devices do NOT support USB.

Figure 1. uPSD3200 52-pin TQFP pin definition

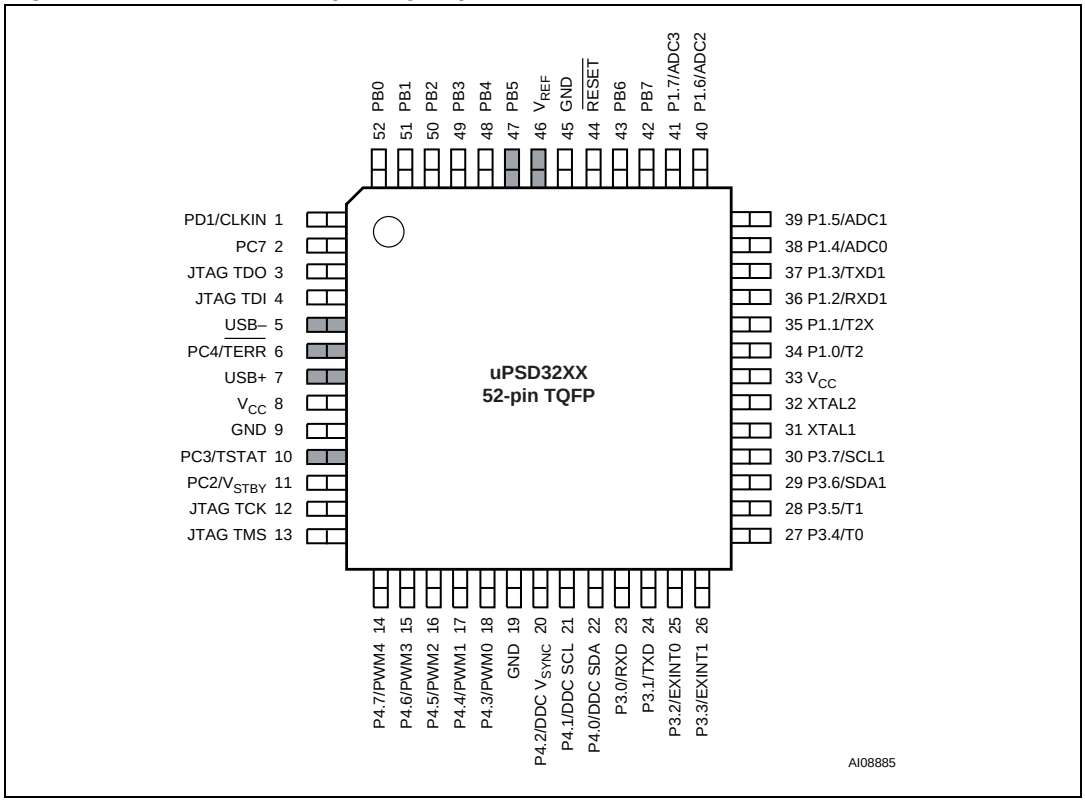
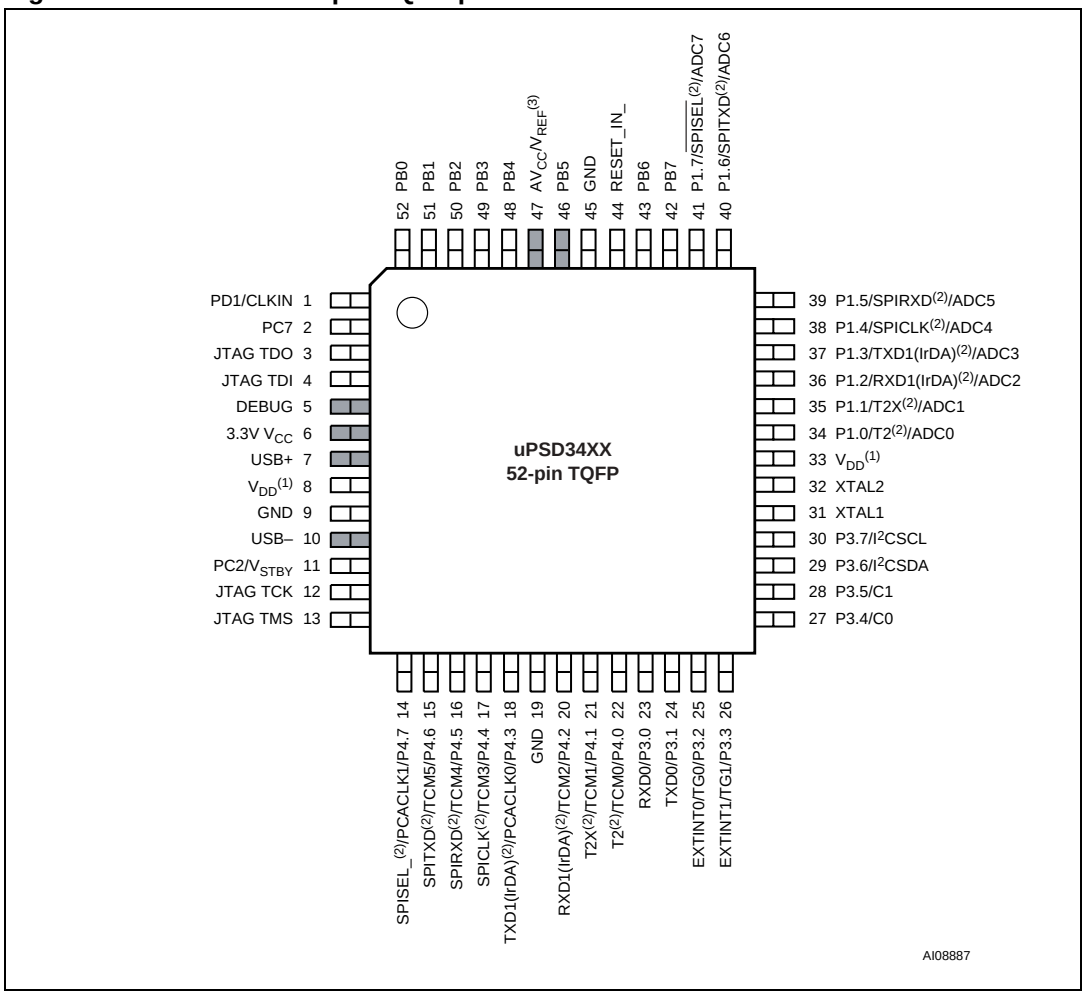


Figure 2. uPSD3400 52-pin TQFP pin definition



1. For 5V applications, V_{DD} must be connected to 5.0V source. For 3.3V applications, V_{DD} must be connected to a 3.3V source.
2. These signals can be used on one of two different ports (Port 1 or Port 4) for flexibility. Default is Port 1.
3. V_{REF} and 3.3V AV_{CC} are shared. ADC channels must use 3.3V as V_{REF} for 52-pin package.

Figure 3. uPSD3200 80-pin TQFP pin definition

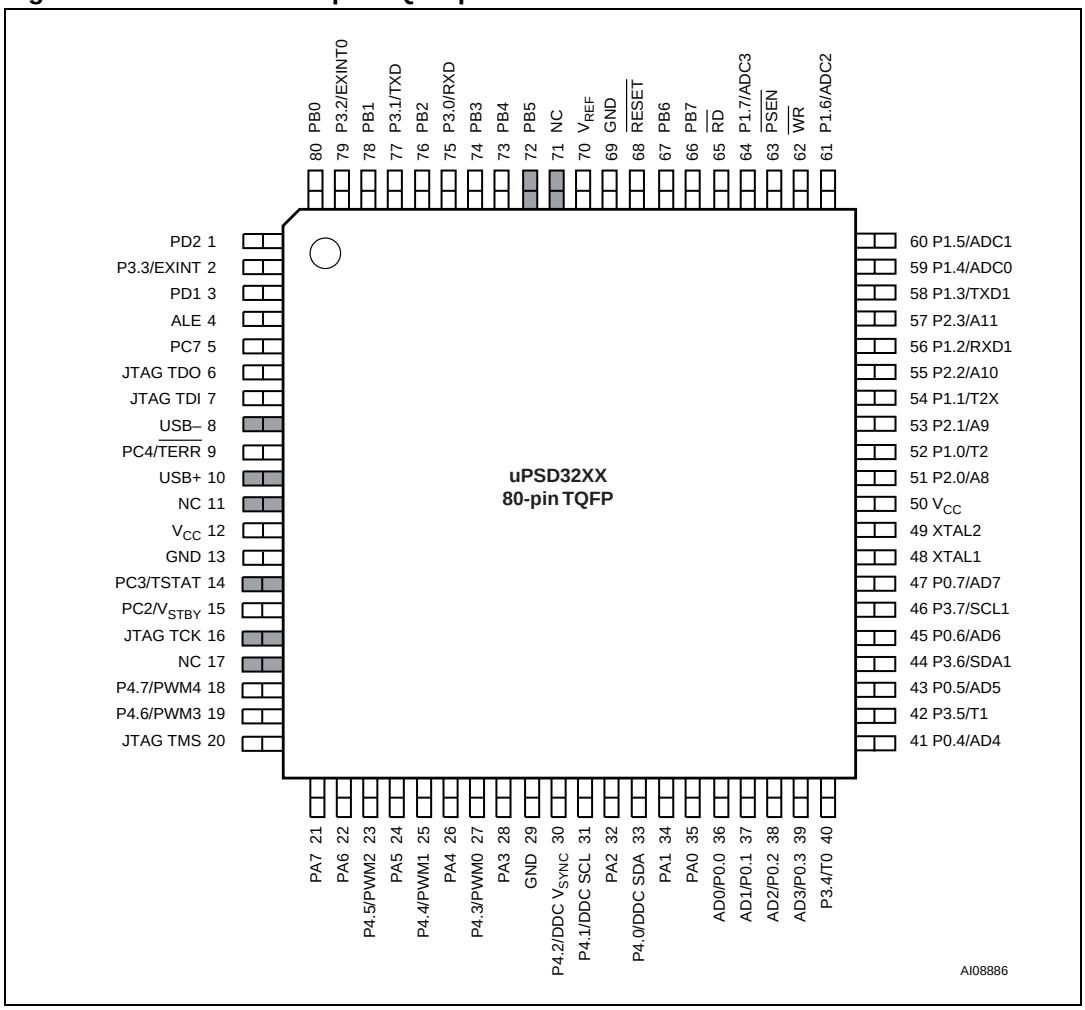
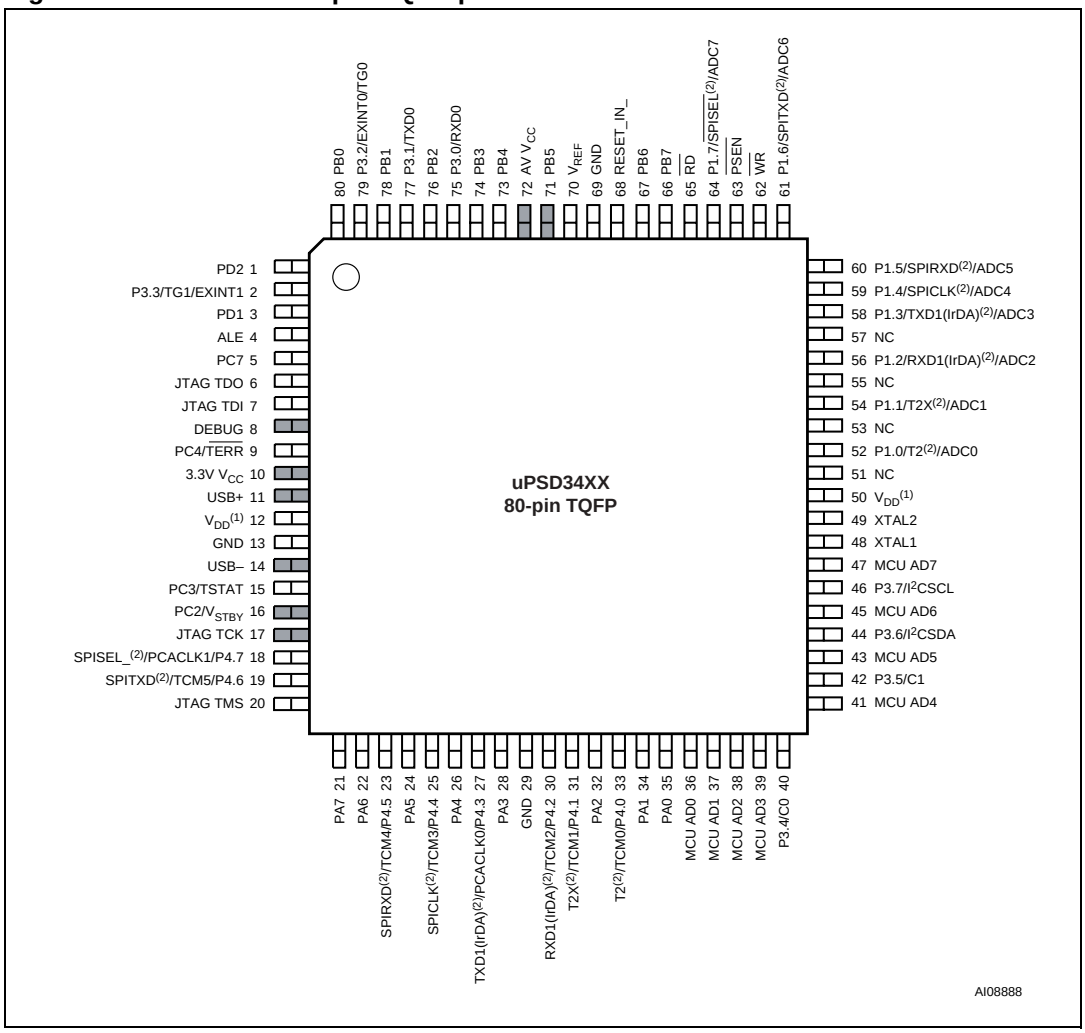


Figure 4. uPSD3400 80-pin TQFP pin definition



1. For 5V applications, V_{DD} must be connected to 5.0V source. For 3.3V applications, V_{DD} must be connected to a 3.3V source.
2. These signals can be used on one of two different ports (Port 1 or Port 4) for flexibility. Default is Port 1.

3 Mandatory pin changes

There are some pin changes (see *Table 1* and *Table 2*) that are absolutely required when migrating from the 3200. These changes are a result of the additional voltage source required by the 3400 MCU core and the reassignment of USB pins, which are highlighted as dark colored pins in *Figure 1* though *Figure 4*. It is assumed that USB was used in the 3200 and will be used in the 3400 design.

Note: 5V 3200 devices support USB while the 3.3V 3200 devices do NOT support USB.

3.1 52-pin Devices

Refer to *Figure 1* and *Figure 2*.

- **Pin 5**

  Pin 5 (USB–) on the 3200 must be pulled up to V_{CC}, regardless of whether USB is used or not. The pull-up resistor value for 3.3V 3200 devices is 2KΩ; the pull-up value for 5V 3200 devices is 7.5KΩ.

  Pin 5 on the 3400 device functions as a Debug input/output, and does not need a pull-up to V_{CC}.

- **Pins 6 and 10**

  The functions of pin 6 (PC4/$\overline{\text{TERR}}$) and pin 10 (PC3/TSTAT) on 3200 devices have been eliminated on the 52-pin 3400 devices to accommodate some pin function reassignments. These two signals on the 3200 were used as general purpose I/O or as optional JTAG ISP pins that reduce programming time.

  Pin 6 on the 3400 is V_{CC} and must always be connected to a 3.3V V_{CC} supply.

  Pin 10 on the 3400 is USB– and is connected to the USB bus for 3400 applications (with no pull-up resistor).

- **Pin 7**

  Pin 7 on both the 3200 and the 3400 is the USB+ signal and has not changed. However, the 3200 supports low-speed USB, while the 3400 supports full-speed USB. Low-speed USB requires a pull-up resistor on the USB– signal whereas the full-speed USB requires a pull-up resistor on the USB+ signal for identification purposes. Since 3400 is full-speed, a pull-up resistor (1.5KΩ) to 3.3V_{CC} is required. This pull-up resistor should be in place on 3400 designs even if USB is not used.

- **Pins 46 and 47**

  The functions of pins 46 and 47 have been swapped. Pin 47 on the 3400 must always be connected to AV_{CC}/V_{REF}.

  The ADC V_{REF} (voltage reference) input was on pin 46 for the 3200, but is now on pin 47 for the 3400.

- **V_{CC} and V_{DD}**

  In a 3.3V system using a 3.3V 3400 device, pins 6, 8, 33, 47 must be connected to a 3.3V V_{CC} source.

  In a 5V system, using a 5V 3400 device, pins 6 and 47 should be connected to a 3.3V V_{CC} source, and pins 8 and 33 should be connected to a 5.0V V_{DD} source.

- **Pin 47** is dedicated to A/D Converter on the 3400 devices

Table 1. 52-pin device changes

	Pin 5	Pin 6	Pin 7	Pin 10	Pin 46	Pin 47
3200	USB– (pull-up)	PC4/$\overline{TERR}$	USB+	PC3/TSTAT	ADC V_{REF}	PB5
3400	DEBUG	3.3V V_{CC}	USB+ (pull-up)	–	PB5	AV_{CC}/V_{REF}

3.2 80-pin devices

Refer to *Figure 3* and *Figure 4*. *Table 2* summarizes the mandatory pin changes for 80-pin devices.

- **Pins 8**

  Pin 8 (USB–) on the 3200 must be pulled up to V_{CC}, regardless of whether USB is used or not. The pull-up resistor value for 3.3V 3200 devices is 2KΩ, the pull-up value for 5V 3200 devices is 7.5KΩ.

  Pin 8 on 3400 devices functions as a Debug input/output, and does not need a pull up to V_{CC}.

- **Pin 10**

  Pin 10 is the USB+ signal on 3200 devices, but on 3400 it must always be connected to 3.3V V_{CC}.

- **Pin 11**

  Pin 11 on 3200 is not used, but on 3400 devices it is the USB+ signal and must be pulled up to 3.3V V_{CC} (with 1.5KΩ) for USB identification purposes.

- **Pin 14**

  Pin 14 on 3200 is PC3/TSTAT which can be a general purpose I/O signal or an optional JTAG ISP signal used to reduce programming time. If this signal was used in the 3200 design, you can connect it to pin 15 on the 3400 (not a mandatory signal).

  Pin 14 on the 3400 is the USB– signal and is connected to USB bus (with no pull-up resistor).

- **Pins 16 and 17**

  Pin 16 on the 3200 is JTAG CLK used for ISP. Pin 16 on the 3400 is PC2/V_{STBY} used for general purpose I/O or for the battery input for SRAM backup. You will need to reroute JTAG CLK to pin 17 on the 3400. JTAG CLK is a mandatory signal.

  If PC2/V_{STBY} was used in the 3200 design, you can connect it to pin 16 on the 3400. PC2/V_{STBY} is not a mandatory signal.

- **Pins 71 and 72**

  The functions of pins 71 and 72 have been swapped. Pin 72 on the 3400 must always be connected to AV_{CC}/V_{REF}.

- **V_{CC} and V_{DD}**

  In a 3.3V system using a 3.3V 3400 device, pins 10, 12, 50 must connect to 3.3V V_{CC} source.

  In a 5V system, using a 5V 3400 device, pin 10 should be connected to a 3.3V V_{CC} source, and pins 12 and 50 should be connected to a 5.0V V_{DD} source.

- **Pin 72** is dedicated to A/D Converter on 3400 devices.

- **Pin 51, 53, 55 and 57** are No Connect on 3400 devices. Address A8-A11 can be brought out on PLD pins.

Table 2. 80-pin device changes

	Pin 8	Pin 10	Pin 11	Pin 14	Pin 16	Pin 17	Pin 51, 53, 55, 57	Pin 71	Pin 72
3200	USB– (pull-up)	USB+	No Connect	PC3/ TSTAT	JTAG TCK	No Connect	A8-A11	No Connect	PB5
3400	DEBUG	3.3V V_{CC}	USB+ (pull-up)	USB–	PC2/V_{STBY}	JTAG TCK	No Connect	PB5	AV_{CC}

4 PC layout suggestions

You can plan your printed circuit board layout in anticipation of migrating from the 3200 to the 3400 by using simple and low cost techniques. One method involves the use of zero-ohm resistors (either surface mount or thru-hole) and multiple circuit traces on the printed circuit board. The idea is to install or not install these zero-ohm resistors at the time of board manufacture, depending on which uPSD is installed.

For example, *Figure 5* shows how you can use this method to handle the swapped functions of pins 46 and 47 on the 52-pin uPSD. In this example, resistors are installed at some locations, and no resistors are installed at other locations as specified in *Table 3*.

A similar method can be used for an 80-pin device, using pins 71 and 72 instead of pins 46 and 47, respectively.

Figure 5. PC layout example for pin swapping

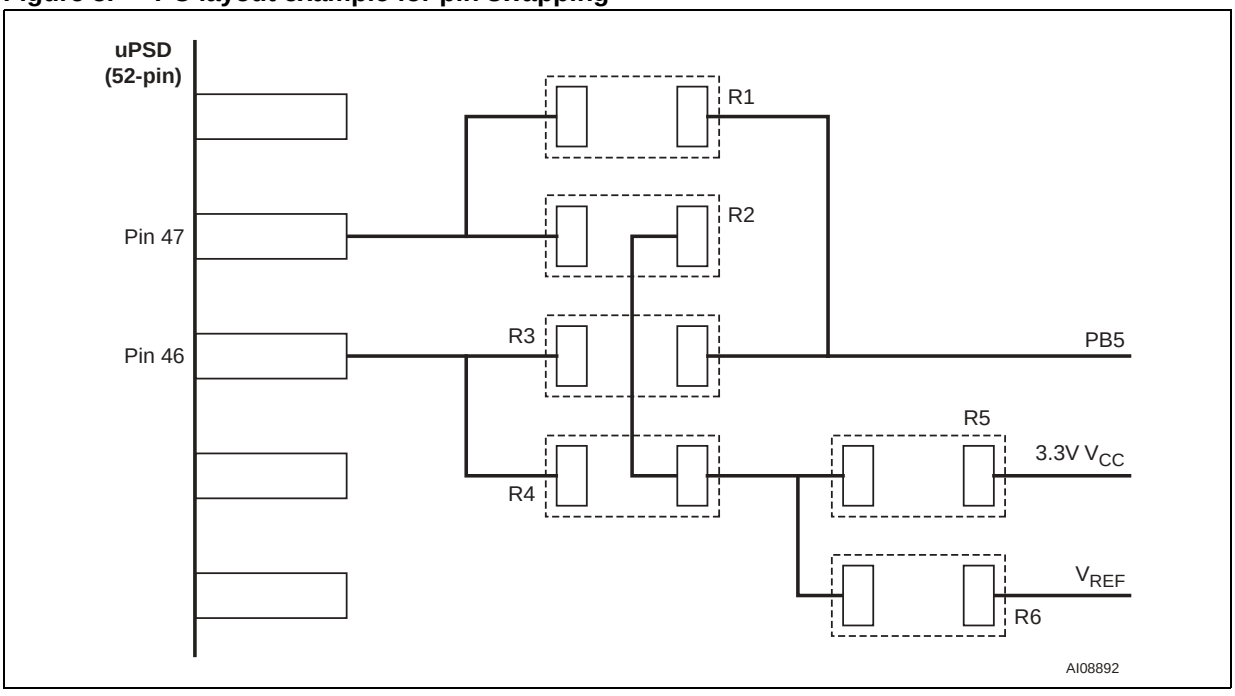


Table 3. 52-pin uPSD (0Ω) resistor installation example

	R1	R2	R3	R4	R5	R6
3200	0Ω	Blank	Blank	0Ω	Blank	0Ω
3400	Blank	0Ω	0Ω	Blank	0Ω	Blank

Figure 6 illustrates one way to handle the differing functions of Pins 5 through 10 on the 52-pin uPSD. For this example, resistors are installed at some locations, and no resistors are installed at other locations as specified in *Table 4*.

Note: The Debug signal is only for laboratory use and typically will be routed to a test point on the circuit board.

Figure 6. PC Layout Example for 52-pin Devices

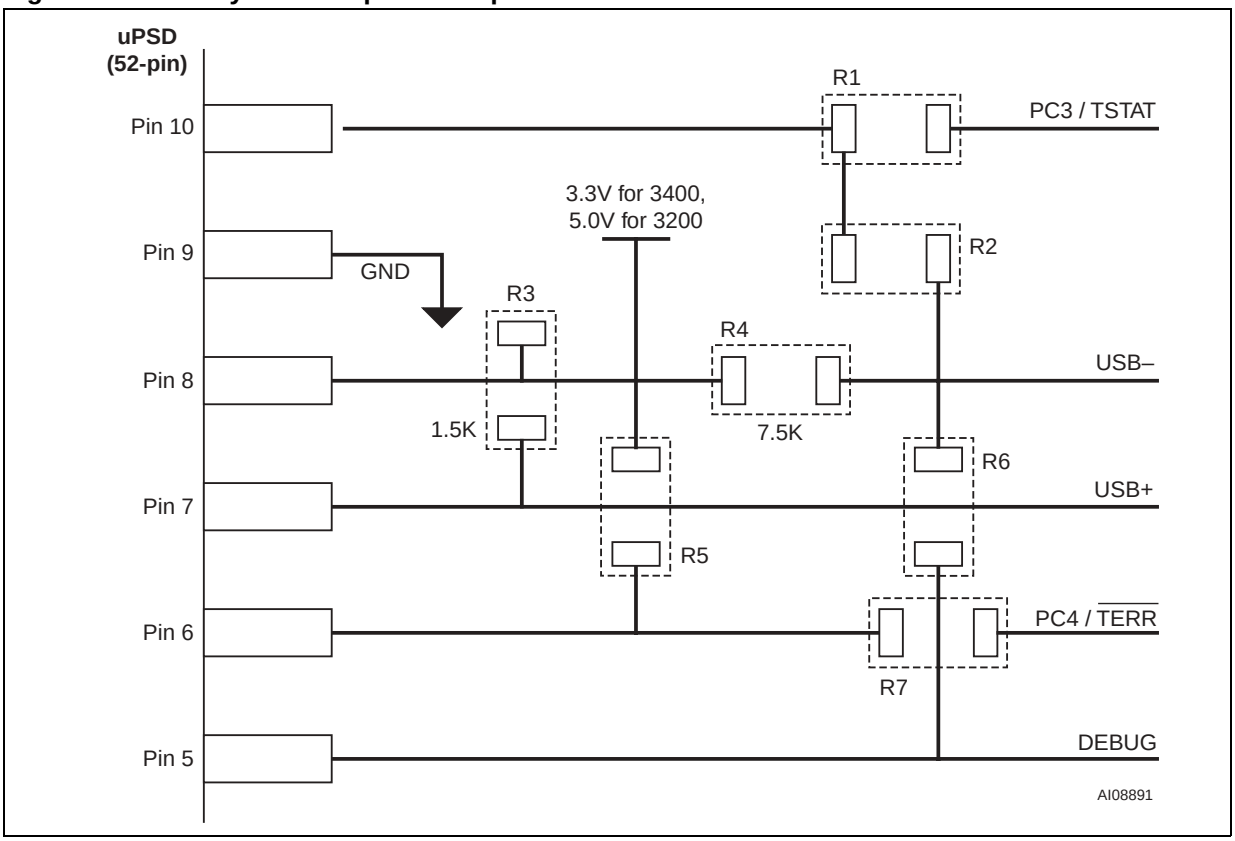


Table 4. 52-pin uPSD Resistor Installation Example (for Pins 5 through 10)

	R1	R2	R3	R4	R5	R6	R7
3200	0Ω	Blank	0Ω	7.5KΩ	Blank	0Ω	0Ω
3400	Blank	0Ω	1.5KΩ	Blank	0Ω	Blank	Blank

Figure 7 illustrates one way to handle the differing functions of pins 5 through 17 on the 80-pin uPSD. For this example, resistors are installed at some locations, and no resistors are installed at other locations as specified in the following *Table 5*.

Note: The Debug signal is only for laboratory use and typically will be routed to a test point on the circuit board.

Figure 7. PC layout example for 80-pin devices

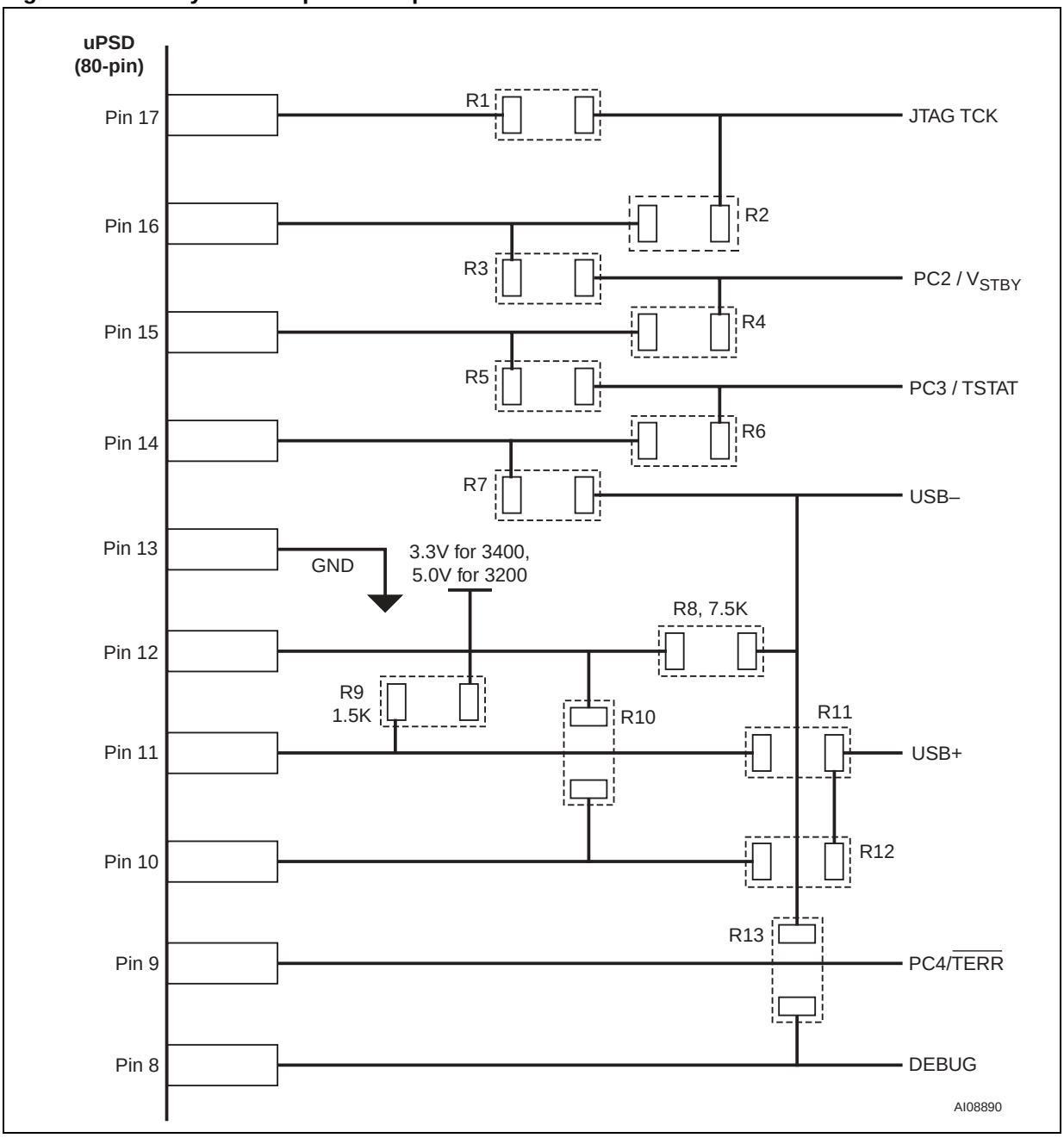


Table 5. 80-pin uPSD resistor installation example (for pins 5 through 17)

	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13
3200	Blank	0Ω	Blank	7.5 KΩ	Blank	0Ω	Blank	0Ω	Blank	Blank	Blank	0Ω	0Ω
3400	0Ω	Blank	0Ω	Blank	0Ω	Blank	0Ω	Blank	1.5 KΩ	0Ω	0Ω	Blank	Blank

5 Conditional pin changes

There are some pin changes that may or may not apply to your design, depending on your application. These changes must be considered when migrating to the 3400 and you have used the PWM or ADC peripherals of the 3200. There is also a conditional change regarding the use of the Low-Voltage Detect (LVD) feature in 5V 3400 devices.

5.1 PWM

There are five PWM outputs on the 3200, and six PWM outputs on the 3400. If you have used any of PWM outputs PWM1, PWM2, or PWM3, on the 3200 then there are no pin changes when migrating to the 3400. However, if you have used PWM outputs PWM0 or PWM4 on the 3200, then you will have to connect to different pins on the 3400.

The Programmable Counter Array (PCA) on the 3400 has six Timer/Counter I/O pins, labeled TCM0 through TCM5, that can be used for PWM outputs, and the PCA also has two clock input pins labeled PCACLK0 and PCACLK1. These eight PCA pins are all on Port 4. It is the two PCA clock input pins of the 3400 that conflict with the PWM0 and PMW4 pin assignments of the 3200.

5.2 52-pin devices

Refer to *Figure 1* and *Figure 2*.

If you are using up to three of the five PWM outputs on the 3200, do not use outputs PMW0 or PWM4. Instead, use outputs PWM1, PWM2, or PWM3 and there will be no pin conflicts when migrating to the 3400.

If you are using four or more PWM outputs on the 3200, then PWM0 on pin 18, or PWM4 on pin 14, they will have to be moved to one of the following pins on the 3400: pins 15, 16, 17, 20, 21, or 22.

5.3 80-pin devices

Refer to *Figure 3* and *Figure 4*.

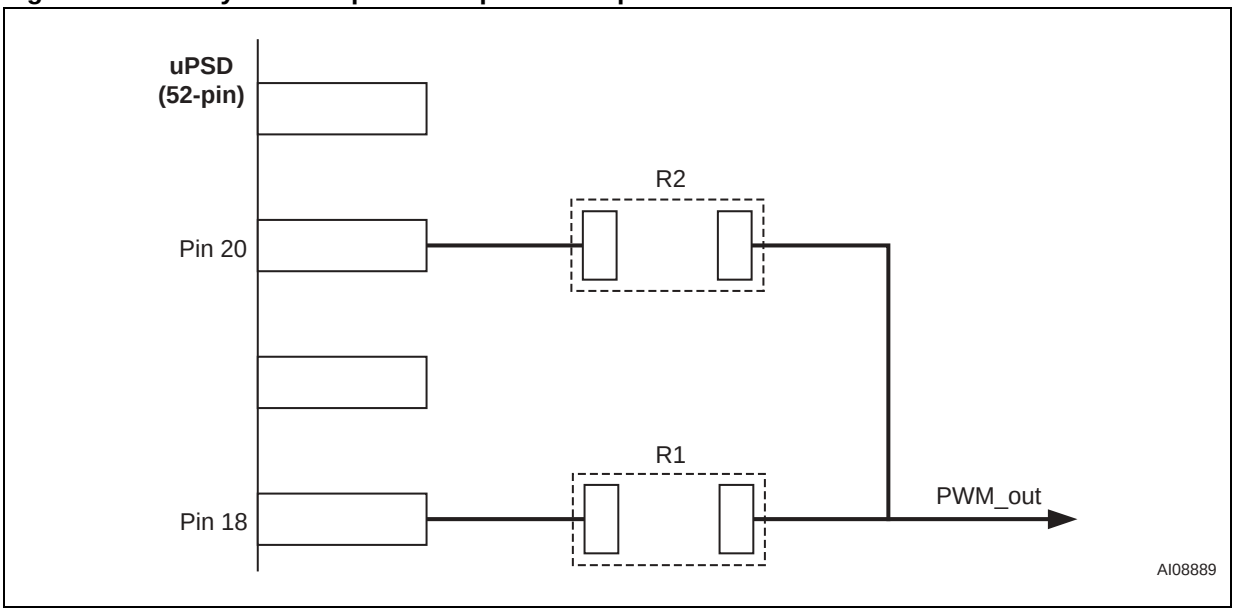
If you are using up to three of the five PWM outputs on the 3200, do not use outputs PMW0 or PWM4. instead, use outputs PWM1, PWM2, or PWM3 and there will be no pin conflicts when migrating to the 3400.

If you are using four or more PWM outputs on the 3200, then PWM0 on pin 27, or PWM4 on pin 18, they will have to be moved to one of the following pins on the 3400: pins 19, 23, 25, 30, 31, or 33.

5.4 PC Layout Suggestion for PWM

Figure 8 is an example of how to move PWM output PWM0 on a 3200 device to the PCA output TCM2 on a 3400 device (52-pin). When a 3200 is installed, R1 is populated with a zero-ohm resistor and R2 is blank. When a 3400 is installed, only R2 is populated. A similar method can be used for an 80-pin device using pins 27 and 30 instead of pins 18 and 20, respectively.

Figure 8. PC layout example to swap PWM outputs



5.5 ADC, reassigned ADC channel numbers

The 3200 has four ADC inputs (8-bit resolution), and the 3400 has eight ADC inputs (10-bit resolution). The physical ADC input pin numbers have not been changed, but the logical ADC channel numbers change when migrating from 3200 to 3400. This means no changes to the PC board are required, but MCU firmware must change to account for different channel numbers. Firmware changes must occur anyway because there are SFR changes, identified in the next section. *Table 6* refers to 52-pin uPSD devices and *Table 7* refers to 80-pin uPSD devices.

Table 6. Reassigned ADC Channel Numbers, 52-pin uPSD

Pin Number on 52-pin TQFP	3200 Device	3400 Device
38	ADC Channel 0	ADC Channel 4
39	ADC Channel 1	ADC Channel 5
40	ADC Channel 2	ADC Channel 6
41	ADC Channel 3	ADC Channel 7

Table 7. Reassigned ADC Channel Number, 80-pin uPSD

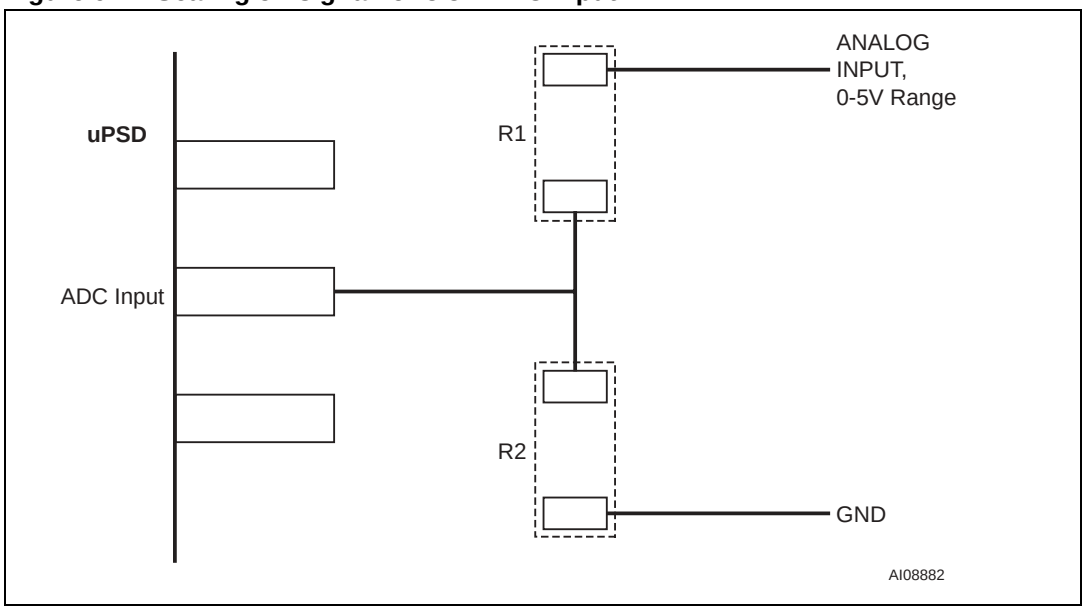
Pin Number on 80-pin TQFP	3200 Device	3400 Device
59	ADC Channel 0	ADC Channel 4
60	ADC Channel 1	ADC Channel 5
61	ADC Channel 2	ADC Channel 6
64	ADC Channel 3	ADC Channel 7

5.6 ADC voltage scaling

For all 3400 devices, both 3.3V and 5V, the maximum input voltage level on any of the eight ADC inputs is the MCU core voltage, V_{CC} (3.6V maximum). This means that if 5V signals are to be sampled in a 5V 3400 system, they must be scaled down to 3.3V V_{CC}. In contrast, for 5V 3200 devices, if 5V signals are sampled, they do not have to be scaled down because the maximum ADC input voltage is 5V Vcc (5.5V max).

Figure 9 illustrates one way to scale a 0-5V analog signal down to 0-3.3V when a 3400 device is used. For example, if a 3400 device is installed, resistor R1 is populated with a 332KΩ resistor, and R2 is populated with a 665KΩ resistor. Precision 1% resistors are recommended. Alternately, if a 3200 is installed, R1 is populated with a zero-ohm resistor and R2 is left blank because no scaling is needed.

Figure 9. Scaling 5V signal for 3.3V ADC Input

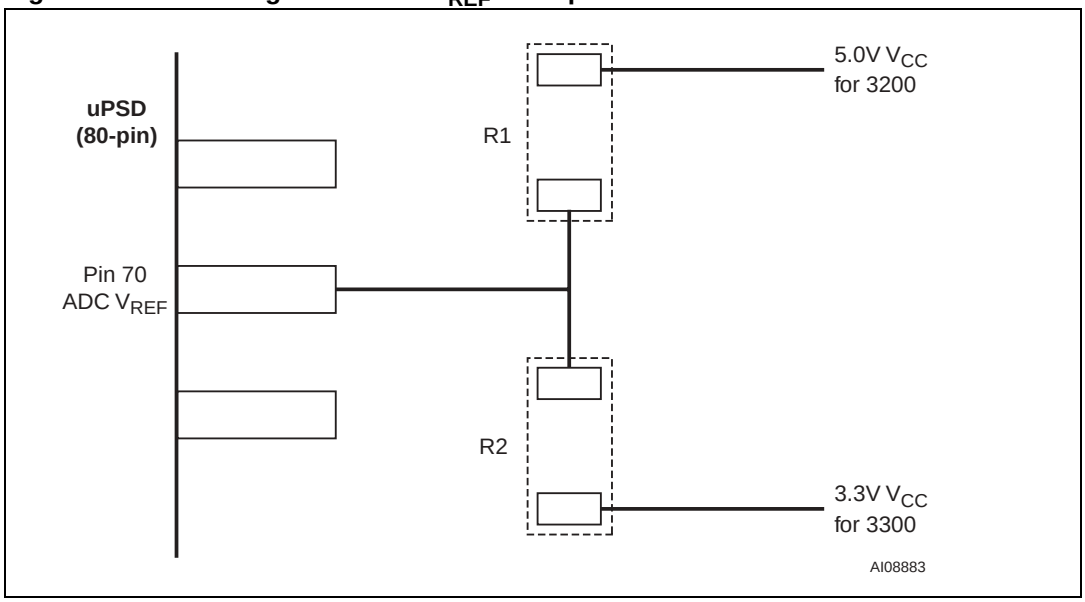


5.7 ADC reference voltage

The maximum ADC Reference Voltage (V_{REF}) allowed on the 3400 is the MCU core voltage, V_{CC} (3.6V max), for both 3.3V and 5V 3400 devices. In contrast, for 5V 3200 devices the maximum ADC reference voltage is 5V V_{CC} (5.5V max). *Figure 10* shows one method to switch the source for V_{REF} during manufacturing if needed. If a 5V 3200 is installed, R1 populated with a zero-ohm resistor and R2 is blank. If a 5V 3400 is installed, only R2 gets

the zero-ohm resistor. This ONLY applies to 80-pin uPSD devices because 52-pin 3400 devices do not have a V_{REF} input as discussed in the MANDATORY PIN CHANGE section and in *Figure 5*.

Figure 10. Switching sources of V_{REF} in 80-pin uPSD devices



5.8 LVD

The Low Voltage Detect (LVD) circuitry on all 3400 devices (both 3.3V and 5V) will generate an internal reset signal whenever the MCU 3.3V V_{CC} voltage level dips below 2.5V. This is fine for 3.3V systems using a 3.3V 3400 device. However, for 5V systems using a 5V 3400 device, it is recommended to use an external LVD circuit to drive the RESET_IN_ pin if it is desired to monitor the 5.0V V_{DD} system supply in addition to the 3.3V V_{CC} supply. Regarding the 3200, there is no problem with 5V devices because the LVD circuitry has an internal trip point at 4.0V.

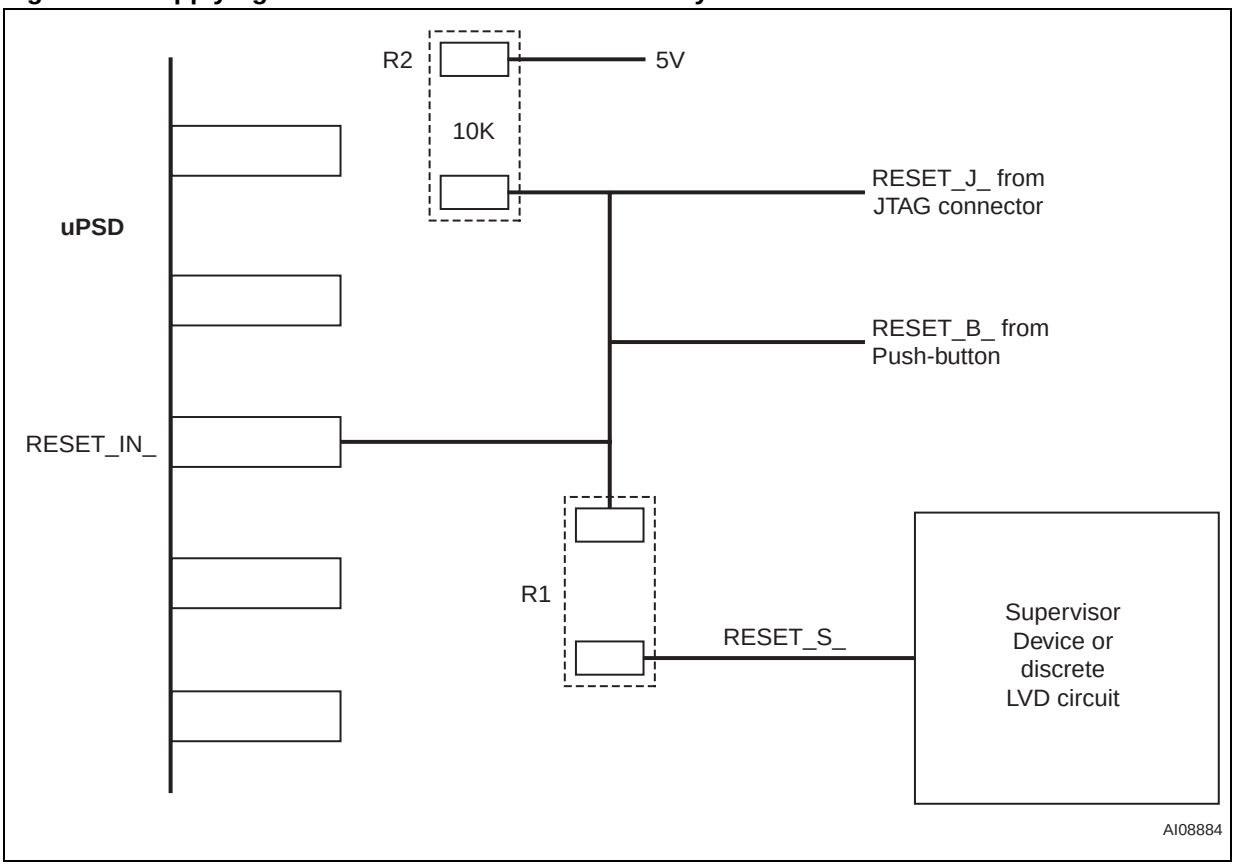
RESET_IN_ is an active-low, open-drain, 5V tolerant input. RESET_IN_ is located at pin 44 on 52-pin devices, or pin 68 on 80-pin devices.

Figure 11 illustrates a scheme that may be used when migrating from a 5V 3200 device to a 5V 3400 device. In this example, R1 is populated with a zero-ohm resistor only when a 3400 is installed, but R1 is left blank when a 3200 is used (supervisor device is optional when 3200 is used). R2 is always populated with a 10K resistor. Since the pin RESET_IN_ is open-drain, it may be driven by multiple open-drain sources.

Suggestion: If a real-time clock (RTC) is needed in the system, choose an RTC that also has an LVD reset output so you can use it as shown in *Figure 11*. There are many types of these devices available from ST at www.st.com/nvram.

Note: An external LVD circuit is not needed for 3.3V 3400 devices in a 3.3V system.

Figure 11. Applying External LVD Circuit to 3400 5V System



6 Special function register (SFR) differences

The are a number of SFRs in the 3200 that have changed compared to the 3400. There are also a number of new SFRs in the 3400 to control new peripherals and features. None of the standard 8032 SFRs have changed (those defined in standard Intel 8032 architecture).

Please see the full 3400 data sheet for a detailed description of new and changed SFRs. Below is a summary of the differences for those SFRs that have changed function or location (the SFRs with black background in *Table 8*). Please adjust your firmware for these changes.

- 87: PCON

  New POR Bit to determine source of last reset.
- 91: P3SF1

  Used to be P1SF1. P1SF1, but it now has new meaning since it is linked to P4SF1 (please see the full 3400 data sheet).
- 96: ADAT1

  Now different because 3400 has a 10-bit ADC, not an 8-bit ADC.
- 97: ACON

  New bits to control ADC interrupt.

  New bit to access eight ADC channels instead of four channels.
- A7/A8: ICA/IA

  New Interrupt Enable bits for Debug, ADC, SPI, and PCA.
- B7/B8: IPA/IP

  New Interrupt priority bits for Debug, ADC, SPI, and PCA.
- D8/D9: SCON1/SBUF1

  2nd UART control and data buffer. Same function as 3200, but new SFR address location in 3400.
- DC: S1CON

  STO and STA Bits do not have to be cleared by software as they did in 3200. The 3400 has hardware (silicon) to assist, which improves I^2C performance and reduces software overhead.
- DD: S1STA

  More efficient use of INTR and ACK_REP_ Bits for I^2C.
- MANY USB SFRS

  There are 19 new SFRs related to the Full-Speed USB interface, all of which start with the letter “U” and the CCON1 SFR.

Table 8 shows all the 3400 SFRs. Those with a black background and white letters indicate 3400 SFRs that have changed from the 3200 definition. Those with a gray background and black letters are new SFRs in the 3400.

Table 8. SFRs in the 3400

SFR Addr	SFR Register Name								SFR Addr
F8		CCON0	CCON1(1)	CCON2	CCON3				FF
F0	B	UCON(1)	USIZE(1)	UBASEH(1)	UBASEL(1)	USCI(1)	USCV(1)		F7
E8	UIF0(1)	UIF1(1)	UIF2(1)	UIF3(1)	UCTL(1)	USTA(1)		USEL(1)	EF
E0	ACC		UADDR(1)	UPAIR(1)	UIE0(1)	UIE1((1)	UIE2(1)	UIE3(1)	E7
D8	SCON1(2)	SBUF1(2)		S1SETUP	S1CON(2)	S1STA(2)	S1DAT	S1ADR	DF
D0	PSW		SPICLKD	SPISTAT	SPITDR	SPIRDR	SPICON0	SPICON1	D7
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2	IRDACON	DSTAT	CF
C0	P4	CAP COML3	CAP COMH3	CAP COML4	CAP COMH4	CAP COML5	CAP COMH5	PWMF1	C7
B8	IP(2)		PCACL1	PCACH1	PCACON1	TCM MODE3	TCM MODE4	TCM MODE5	BF
B0	P3	CAP COMH1	CAP COML2	CAP COMH2	PWMF0			IPA(2)	B7
A8	IE(2)	TCM MODE0	TCM MODE1	TCM MODE2	CAP COML0	CAP COMH0	WDTKEY	CAP COML1	AF
A0	P2		PCACL0	PCACH0	PCACON0	PCASTA	WDRST	IEA(2)	A7
98	SCON0	SBUF0				BUSCON	DIR	DVR	9F
90	P1	P3SFS(2)	P4SFS0	P4SFS1	ADCPS	ADAT0	ADAT1(2)	ACON(2)	97
88	TCON	TMOD	TL0	TL1	TH0	TH1	P1SFS0	P1SFS1	8F
80	P0	SP	DPL	DPH		DPTC	DPTM	PCON(2)	87

1. New SFRs in uPSD3400
2. SFRs changed in uPSD3400

7 Interrupt vector differences

There are new interrupt vectors for the 3400, and some interrupt priority levels have changed. See *Table 9* for comparison of interrupt vectors of 3200 and 3400 and their relative priorities. Please adjust your firmware accordingly.

Table 9. interrupt vector tables and priority

Interrupt Source	3400 Priority	3400 Vector Address (hex)	3200 Priority	3200 Vector Address (hex)
JTAG Debug	0 (high)	0063	N/A	N/A
External INT0	1	0003	0	0003
Timer 0	2	000B	2	000B
External INT1	3	0013	4	0013
Timer 1	4	001B	6	001B
UART0	5	0023	8	0023
Timer 2 + EXF2	6	002B	9	002B
SPI	7	0053	N/A	N/A
USB	8	0033	7	0033
I^2C	9	0043	3	0043
ADC	10	003B	N/A	N/A
PCA	11	005B	N/A	N/A
UART1	12 (low)	004B	1	004B
DDC	N/A	N/A	5	003B

8 Conclusion

The suggestions for methods to easily migrate designs from the uPSD3200 series to uPSD3400 allow the user to implement firmware and software settings, as well as simple techniques on the printed circuit board to accept either a uPSD3200 or a uPSD3400 during manufacturing.

For current information on ST Flash uPSD products, please consult our pages on the world wide web:

www.st.com/micropsd

For application support:

apps.psd@st.com (please include your name, company, location, telephone number, and fax number)

9 Revision history

Table 10. Document revision history

Date	Revision	Changes
26-Apr-2004	1	First Issue
14 -May-2007	2	Document reformatted. Updated page 4, 6, 8,10, 11 and 12.

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