AN1696
APPLICATION NOTE

L6615, LOAD SHARE CONTROLLER FOR N+1 REDUNDANT, HOT-SWAPPABLE APPLICATION

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Power supply systems are often designed by paralleling converters in order to improve performance or reliability. To ensure uniform distribution of stresses, the total load current should be equally shared among the converters.

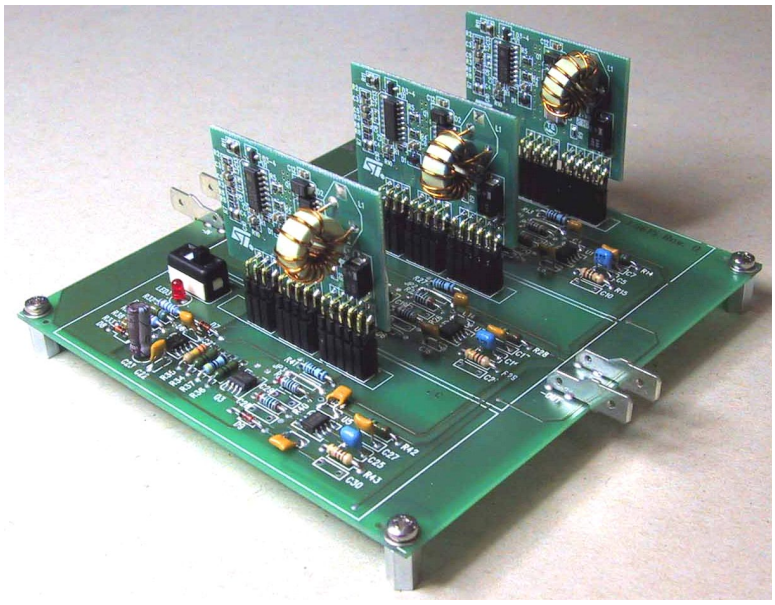
This application note describes a redundant system (a demo board is available) composed by three paralleled DC-DC converter modules (synchronous buck topology, managed by ST L6910) whose output currents are shared through the new ST current sharing controller (L6615).

In this application it is shown the innovative use of a MOSFET as both OR-ing element (replacing OR-ing diode) and sensing element ($R_{ds(ON)}$).

Introduction

Load sharing is a technique commonly used when powering loads requiring low voltage and high current; for this reason a modular power system is built where two (or more) power supplies or DC-DC converters are paralleled and supply the load.

Sharing the output currents is useful to equalize the thermal stress of the different modules providing an advantage in terms of electronic components reliability (mean time between failure roughly doubles every 10°C decrease in operating temperature).



In this application, load sharing control is entrusted to ST's L6615 [1] that features automatic master-slave current sharing control [2] [3]: the supply that delivers the highest current (sensed by means of an external resistor) acts as the master and drives a common reference (share bus) to a voltage proportional to its output current; the feedback voltage of the others paralleled power supplies (slaves) is then trimmed by an "adjustment" network so that they can support their amount of load current. The slave supplies work as current-controlled current sources.

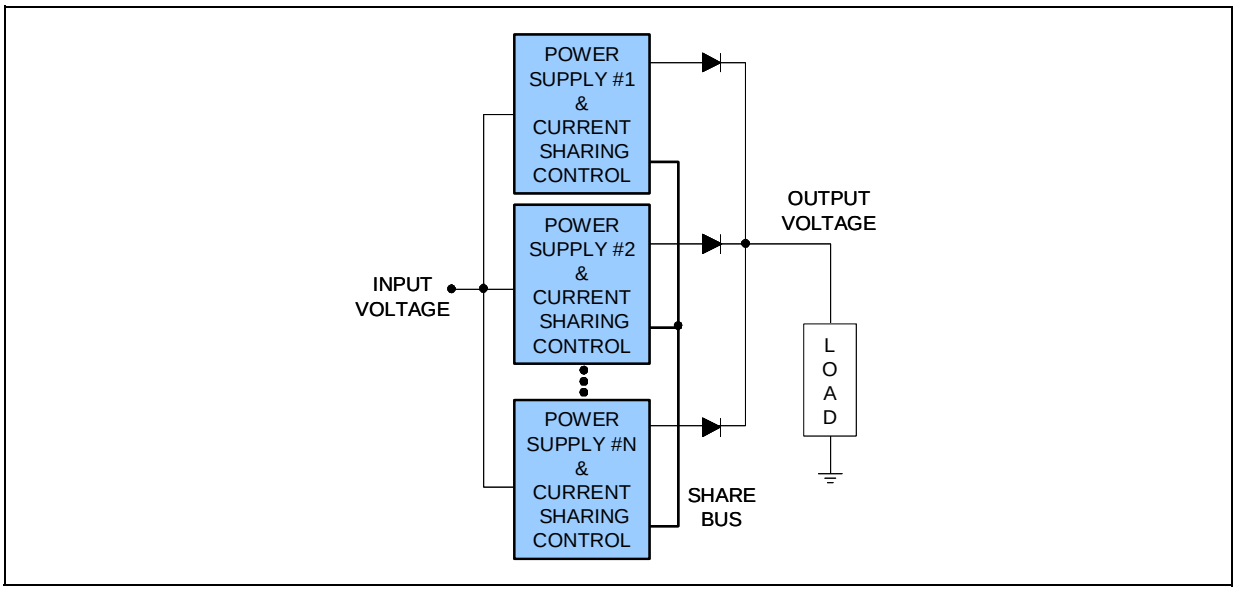
Moreover a paralleled supply architecture allows achieving redundancy (a system of paralleled power supplies, each delivering a current lower than its nominal capability); the failure of one of the modules can be tolerated until the capability of the remaining power supplies is enough to provide the required load current. In this way an interruptible power supply will be designed, reducing the failure rate of the output bus.

In hot-swappable applications, whenever a section fails, it has to be removed and replaced without turning off the system and causing significant perturbation to both input and output system buses.

At insertion, each section exhibits a certain amount of discharged capacitance between the input terminals: if no inrush current limiting protection is implemented, this will cause a large negative drop on the input bus voltage (the analysis of this issue is beyond the purpose of this document).

The same problem occurs on the output side whenever the load is already supplied by other running sections: the discharged output capacitors of the inserted section are a very low impedance that can generate a negative drop on the load bus. This could trigger the UV/OC protection or cause a false value if a logic circuit reads the power supply output voltage at its input.

Figure 1. System architecture



This is way an isolating element is introduced on each of the lines connecting the power output of each section with the load; often an OR-ing diode is used for this purpose but the latest trend is to use an OR-ing FET to save some points in efficiency.

This, combined with the capability of ST's L6615 load share controller to perform high side sensing, allows the use of the $R_{DS(ON)}$ of this FET as a sensing element as well.

System Description

The system (fig. 2) is composed of:

– three identical sections (daughter boards) able to perform DC-DC conversion starting from $+5V_{DC}$; each of them is designed to deliver 3.3V/5A to the load. They must be inserted in the motherboard;
– a motherboard whose input terminals will be connected to a **$+5V_{DC}$ external source** and output terminals to the load. This board can accommodate up to three DC-DC converters.

On the motherboard there is the circuitry necessary to perform current sharing (L6615) and to isolate a failed section from the load; it is designed to be adaptable to all power supplies (whose rating are compatible with L6615 absolute maximum ratings) having remote sense pins; in fact only changing few components it can be rearranged for new specs.

It is so possible to build a system to supply a **10A load at +3.3V in 2+1 redundant configuration.** That is, whenever three sections are running, each of them supplies 3.33A, a value lower than its nominal capability.

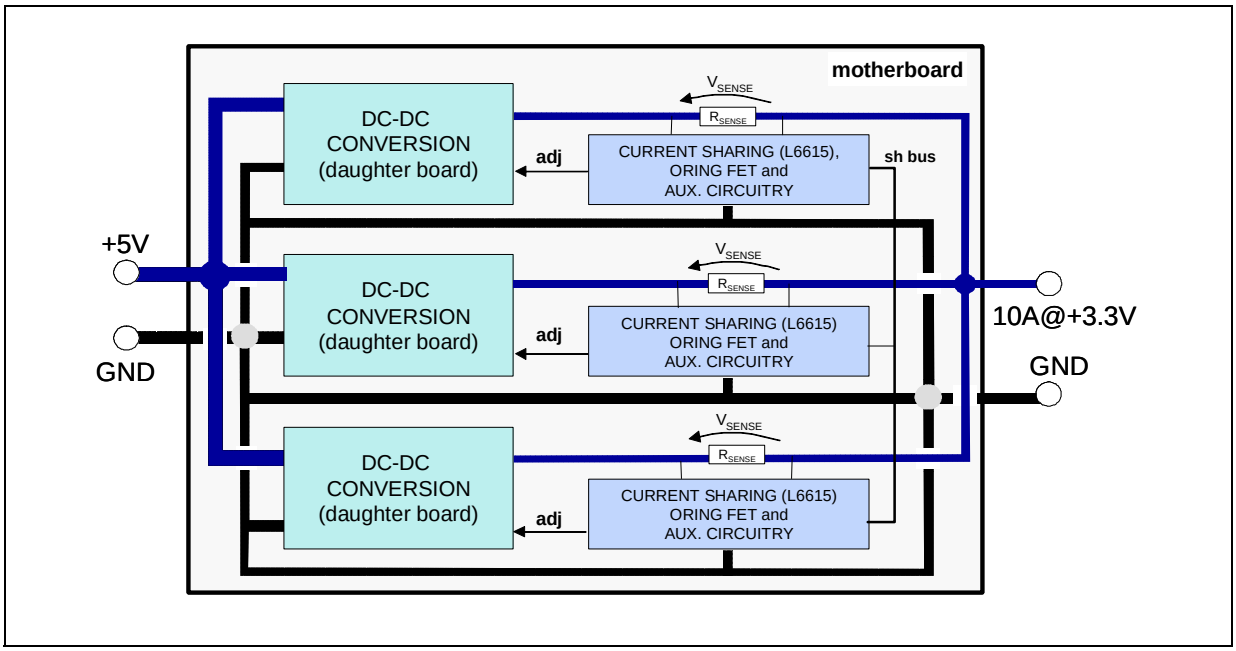
If one of them is switched off, the system is however able to supply the load and each section will carry 5A.

The DC-DC conversion management is entrusted to the L6910 [4].

It is possible to verify that disabling one section (through the relevant switch on the motherboard) does not cause either overvoltage on the output or overcurrent in other sections.

At the same way, enabling one section (with other two already running) does not cause output voltage negative drop or even short to ground and current sharing is established.

Figure 2. System overview



1.0 DAUGHTER BOARD

The L6910 controller drives a synchronous step-down stage at 200KHz; the internal reference is used for the regulation. The external power mosfet's are included in one SO8 package to save space and increase power density.

Fig. 3 shows the schematic of each daughter board and in table 1 the part list is indicated (for the description of this section see [4]).

Figure 3. Daughter board schematic

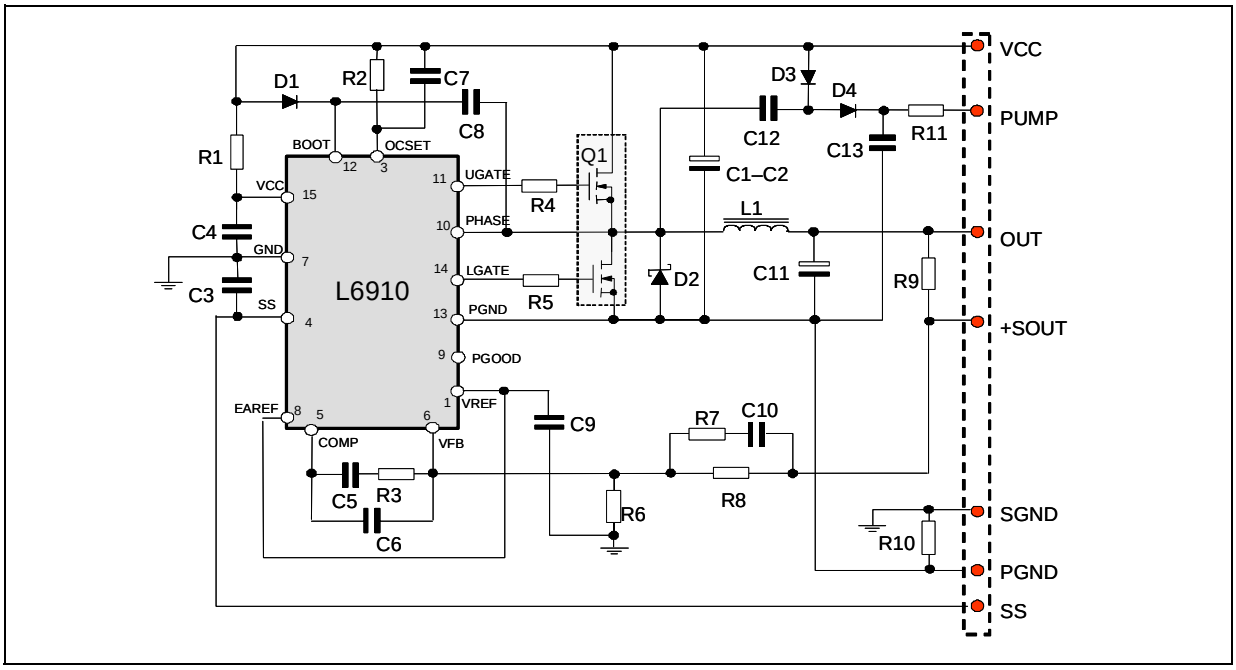


Table 1. Part list board L6910

RESISTORS

R1, R9, R10	10	SMD 0805	R7	1K2	SMD 0805
R2	1K5	SMD 0805	R8	10K	SMD 0805
R3	2K7	SMD 0805, 1%	R9	82	SMD 0805
R4, R5	2.2	SMD 0805	R10	39	SMD 0805
R6	3K75	SMD 0805, 1%	R11	680	SMD 0805

CAPACITORS

C1, C2	10µF	(TOKIN) C34Y5U1E106ZTE12	C7, C12	1nF	SMD0805, Ceramic
C3, C4, C8, C13	100nF	SMD0805, Ceramic	C9, C10	10nF	SMD0805, Ceramic
C5	47nF	SMD0805, Ceramic	C11	330 µF – 6.3V	(POSCAP) 6TPB330M
C6	N.C.	SMD0805, Ceramic			

INDUCTOR

L1	10µH	T50-52B Core 12T			

IC's

U1	L6910	(ST) SO16 NARROW	Q1	STS8DNF3LL	(ST) SO8

DIODES

D1, D3, D4	1N4148	SOT23	D2	STP130A	SMA

Besides the standard components necessary to perform DC-DC conversion, a charge pump (D3, D4, C12, C13, R11) has been added to provide a voltage high enough to bring the gate of the OR-ing FET (on the motherboard) at least one threshold above V_{OUT} (V_{GATE}>3.3V+$V_{GS(TH)}$); moreover, increasing V_{GS} voltage allows working with a lower $R_{DS(ON)}$ and reducing mosfet conduction losses.

This pump, running whenever PWM activity is present, pushes the gate of the OR-ing fet up to a voltage equal to:

$$V_{GATE(MAX)} = 2 \cdot V_{IN} - 2 \cdot V_F \qquad (1)$$

(where V_F is the forward drop of the diodes) supplying a current equal to:

$$I_{CH} = V_{IN} \cdot C_{12} \cdot f_{SW} \qquad (2)$$

From the daughter board, besides input/output voltages and ground, other signals exit toward the motherboard:

– SOFT-START: the soft-start voltage is brought out and connected to a switch (that can short soft-start to ground) allowing enable/disable of the relevant section;

– +SOUT and SGND are the sense terminals for positive and negative load terminals; they are connected to the relative power traces through two small resistors to avoid that any kind of open connection (or the sense pins left open) could cause a lost of control.

2.0 MOTHERBOARD

The motherboard accommodates all the auxiliary circuitry necessary to load sharing, to manage start-up and to enable/disable each of the three daughter boards; a LED indicates the disabled section.

Terminals are available to connect input DC voltage and load and three series of connectors allow inserting the daughter boards.

In fig. 4 the structure of one section of the motherboard is showed: replying this structure other two times the entire board is obtained; table 2 reports the part list.

Figure 4. Motherboard schematic

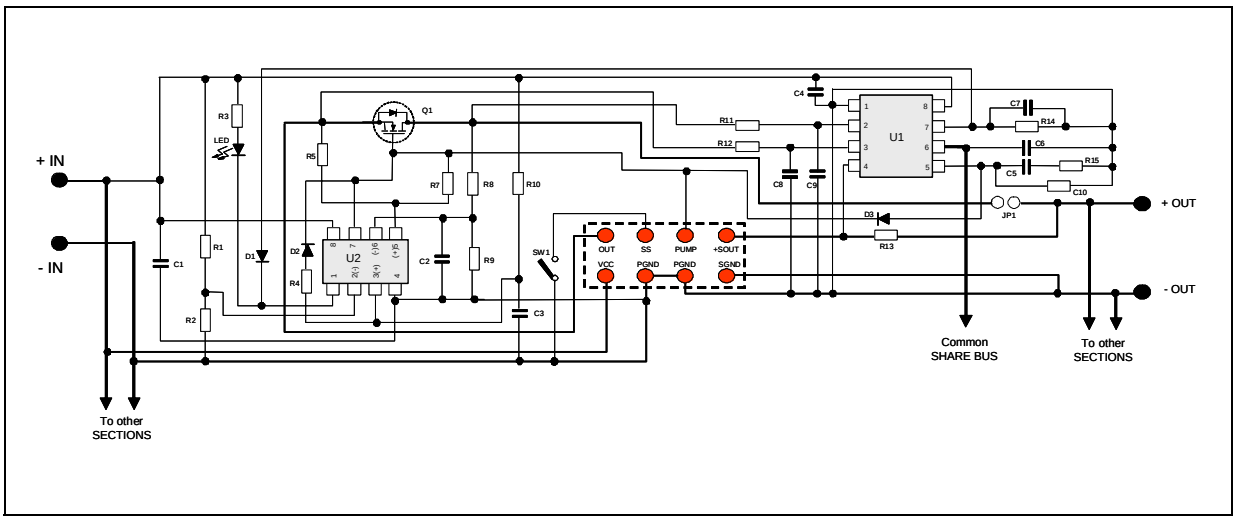


Table 2. Part list board L6615

RESISTORS

R1, R10	6K8	R5, R8	1K	R13	82
R2	20K	R7	330K	R14	7K5
R3	2K	R9	47K	R15	100
R4	3K3	R11, R12	200		

CAPACITORS

C1, C2, C4	100nF	C5	1µF	C8, C9, C10	open
C3	4.7µF	C6, C7	10nF		

IC's

U1	L6615D	(ST) SO8	U2	LM293	SO8
Q1	STS8DNF3LL	(ST) SO8			

DIODES

D1, D2, D3	1N4148	SOT23			

To measure the current carried by each section, it is possible to open the jumper JP1 (see schematic) and to place a ring for inserting a current probe.

2.1 OR-ing FET and current sensing

High side current sensing is implemented by reading the voltage drop across the $R_{DS(ON)}$ of Q1 (during normal operation the FET is maintained on by the charge pump); the voltage at L6615 CGA pin of the section #N is proportional to its output current, in particular [1]:

$$V_{CGA}(\#N) = I_{OUT}(\#N) \cdot R_{DS(ON)} \cdot \frac{R_{14}}{R_{12}} \quad (1)$$

The first parameter to consider when selecting the OR-ing FET is its $R_{DS(ON)}$ because, for a given output current, it defines both the power dissipation and the drop useful for current sharing. Increasing $R_{DS(ON)}$ leads to a wide sense signal available but also means higher power dissipation.

In the motherboard Q1 is a STS8DNF3LL [5] having (for each MOS):

$R_{DS(ON)}$ =	0.017 (nom.)	@ ID=4A, VGS=10V, TCASE=25°C
	0.020Ω (max.)	

STS8DNF3LL contains two internal MOSFETs that are paralleled leading to halve the $R_{DS(ON)}$.

The design must be done considering worst case conditions to avoid share bus saturation: only two sections running and maximum value for $R_{DS(ON)}$. Considering also the temperature variation, we have:

$$R_{DS(ON)|@Tmax} = 0.015\Omega$$

then the maximum drop will be 75mV and (1) leads to $V_{CGA(MAX)} = V_{SH(MAX)}$ of about 2.8V.

It can be useful to calculate the losses associated to the OR-ing FET and compare them with the losses in case

of OR-ing diode (as a reference we consider the low drop Schottky diode STPS10L25D [6]).

Considering T_{max} and I_D = 5A, we have:

– OR-ing FET (STS8DNF3LL) $P_{DISS} = I^2_D \cdot R_{DS(ON)} = 0.375W$

– OR-ing DIODE (STPS10L25D) $P_{DISS} = 0.22 \cdot I_{D(AVG)} + 0.013 \cdot I^2_{D(RMS)} = 1.425W$

Obviously in the case of the diode, also the sense resistor is needed: assuming the same 75mV drop, the total dissipation will be 1.8W. We can estimate 1.4W saving, leading to about 8.5% efficiency rise.

2.2 Current sharing control

For each section one L6615 controller is associated with the few external components necessary to its operation.

Load sharing is achieved through a single wire connection (share bus) between all the paralleled modules, whose voltage is proportional to the highest output current amongst all the active sections. In particular, being unity the (internal) gain between CGA and SH pins, on the share bus there will be the highest of the values given by (1).

In case of very noisy application, two capacitors (C8 and C9) allow filtering the L6615 current sense pins (#2 and #3).

The L6615 error amplifier is of transconductance type so a compensation network is required connected between L6615 pin #5 and ground; in this case an RC series network (C5-R15) determines a bandwidth of about 1KHz for the sharing loop.

The L6615 ADJ pin (pin#4) is connected to the daughter board: a current proportional to the output currents unbalance is sunk from the feedback path of the relevant section.

The value of adjustment resistor (R13, between positive output terminal and ADJ pin) must be chosen in accordance with both the maximum current sink capability of pin ADJ and the output voltage tolerance.

If we consider V_{OUT} = +3.3V with a tolerance of ±5%, the maximum spread between the master output voltage and the slave one could be 330mV: this is the drop that the L6615 must be able to correct imposing a current to flow through the adjustment resistor.

Its resistance value must be lower than the feedback divider (R6 and R8) to have no impact on the value of regulated voltage.

The design of this resistor is a very simple process: it is enough to choose for the maximum adjustment current a value lower than the maximum specified for L6615 (8mA, worst case) and verify that this does not cause the saturation of the L6615 internal BJT (see fig. 5) under steady state condition.

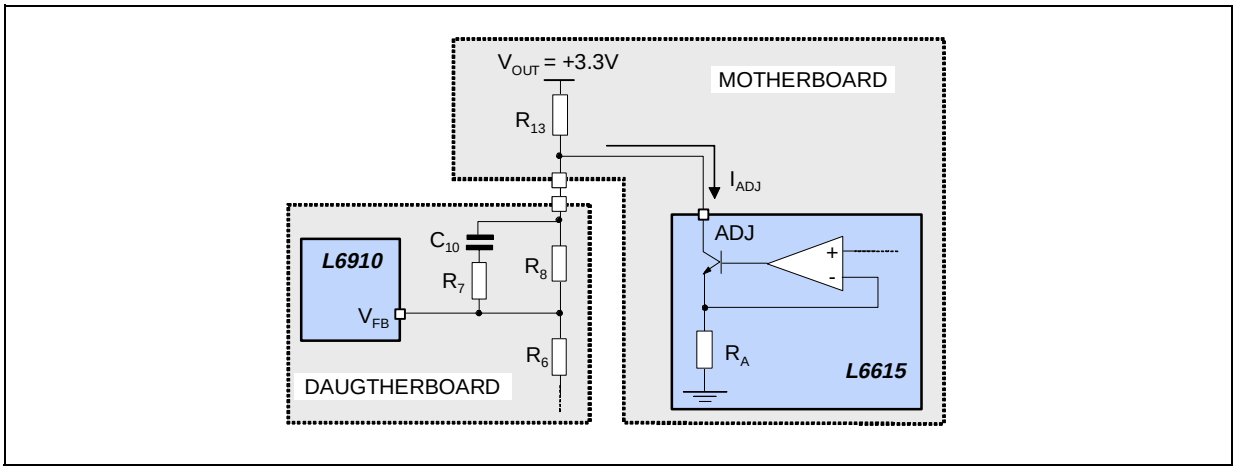
In this case:

adj. current: $I_{ADJ(max)} = 8mA$

min adj. resistor: $R_{ADJ(min)} = \frac{\Delta V_{OUT(MAX)}}{I_{ADJ}} = \frac{330mA}{8mA} = 41.25\Omega$

In fact this resistance value is obtained considering the parallel of R13 (motherboard) and R9 (daughter board), each of them equal to 82Ω.

Figure 5. Adjustment network



2.3 Gate driver of OR-ing FET

The OR-ing FET gate is driven by the output of a comparator (one section of an LM293, standard double comparator) sensing the voltage upstream (source) and downstream (drain) the OR-ing FET (see fig. 6). This turns-off the transistor whenever a current tries flowing from the load towards the output stage of a daughter board.

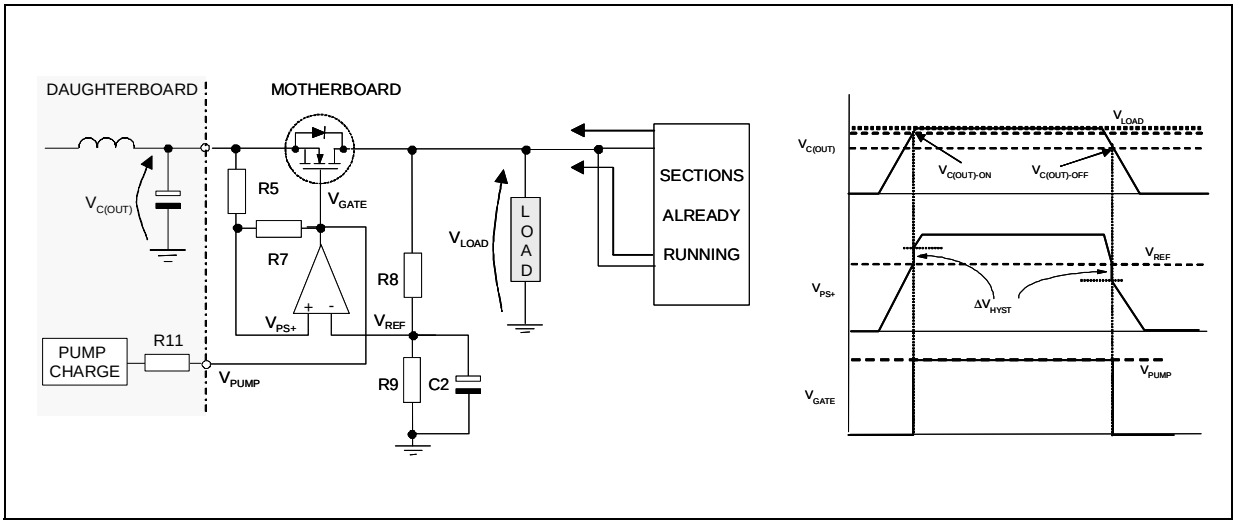
Whenever one section is enabled with the two others already running (hot plug), its output capacitor is completely discharged: to avoid a negative drop on the load voltage, the gate of the FET is kept low until $V_{C(OUT)}$ reaches a value very close to V_{LOAD} (this can be set defining the ratio between R5 and R7). The PWM starts charging output capacitor ($V_{C(OUT)}$ increases) and, only when:

$$V_{C(OUT)-ON} = V_{REF} \cdot \left(1 + \frac{R5}{R7}\right) = V_{LOAD} \cdot \left(\frac{R8}{R8 + R9}\right) \cdot \left(1 \cdot \frac{R5}{R7}\right)$$

the FET is turned on.

Moreover the load must be isolated from a failed section; for example in case of a short circuit on the low side power MOS of one section, then a current will tend to flow in reverse direction through the corresponding OR-ing FET.

Figure 6. OR-ing FET management



For a short time (before overcurrent/undervoltage protections are triggered), the unbroken sections are able to deliver such high current maintaining the load voltage in the right range.

This in turn causes $V_{C(OUT)}$ to be lower than V_{LOAD} and the OR-ing FET will be turned off whenever $V_{C(OUT)} = V_{C(OUT)-OFF}$.

It is possible to obtain the value of the current necessary to push $V_{C(OUT)}$ at $V_{C(OUT)-OFF}$:

$$I_{REV} = \frac{1}{R_{DS(ON)}} \cdot \left(V_{LOAD} \cdot \left(1 - \left(\frac{R9}{R8 + R9} \right) \cdot \left(1 + \frac{R5}{R7} \right) \right) + V_{PUMP} \cdot \frac{R5}{R7} \right)$$

3.0 DEMO-BOARD BEHAVIOUR

The aim of this demo-board is mainly to show the operation of current sharing section, drawing the attention also to the management of the OR-ing FET. For this reason no protection have been introduced to prevent in-rush current: it is not possible to actually insert or remove a daughter board during normal operating, nevertheless it is recommended to simulate a fault by enabling/disabling one section through the switch SW1 (it shorts to GND the soft-start pin).

Once all the daughter board are inserted (with the switches on the "ON" position), the system is ready to be powered-up.

Measuring the three output currents and varying the load continuously, it is possible to see the load share accuracy (fig. 7); obviously, at light load, the accuracy is not so high because is higher the weight of both the mismatches between relevant components and the noise is higher. At full load (10A) the maximum error is lower than 2.5%.

Fig. 8 shows the behaviour of the system whenever a fault condition appears on section 1 when the three sections are operating supplying a total load of 10A (each of them carries about 3.3A); in particular it is simulated a short of the low side FET of the synchronous rectifier section 1.

If no OR-ing element were implemented, this could cause a short circuit condition on the other two sections (UV and/or overcurrent protection could be activated): here the gate driver circuit opens the OR-ing FET preventing current flow from the load to the output of section 1 and the output voltage experiences only a very small drop. The currents of section 2 and 3 grow up to 5A.

Figure 7. Load share accuracy

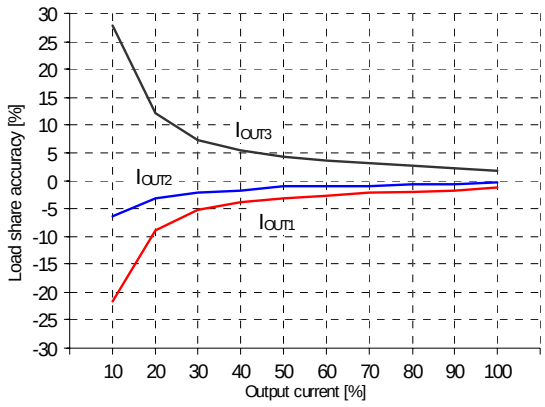
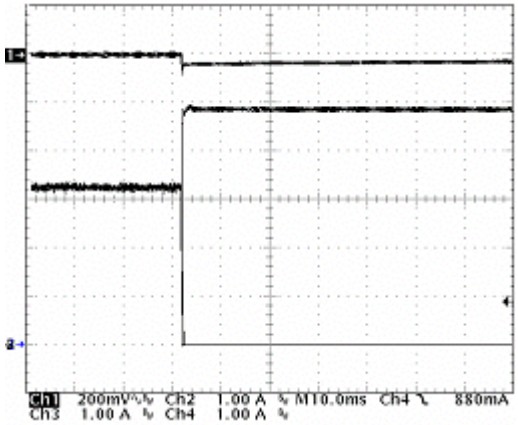


Figure 8. Fault on one section



REFERENCES

[1] "L6615 High/low side load share controller" (Datasheet)

[2] V. J. Thouttevelil, C. G. Verghese, "Analysis and control Design of Paralleled DC/DC Converters with Current Sharing", IEEE Transaction on Power Electronics, Vol. 13, N. 4, July 1998, pp. 635-644.

[3] J. Rajagopalan, K. Xing, Y. Guo, F.C. Lee, B. Manners, "Modeling and Dynamic Analysis of Paralleled DC-DC Converters with Master-Slave Current-Sharing control", IEEE Applied Power Electronics Conf. Rec. 1996, pp 678-684.

[4] "L6910 - Adjustable step down controller with synchronous rectification" (Datasheet)

[5] "STS8DNF3LL, DUAL N-CHANNEL 30V - 0.017 OHM - 8A SO-8 LOW GATE CHARGE STRIPFET II POWER MOSFET" (Datasheet)

[6] "STPS10L25D, LOW DROP POWER SCHOTTKY RECTIFIER" (Datasheet)

APPENDIX

LAYOUT

Figure 9. Daughter board layout and connectors configuration

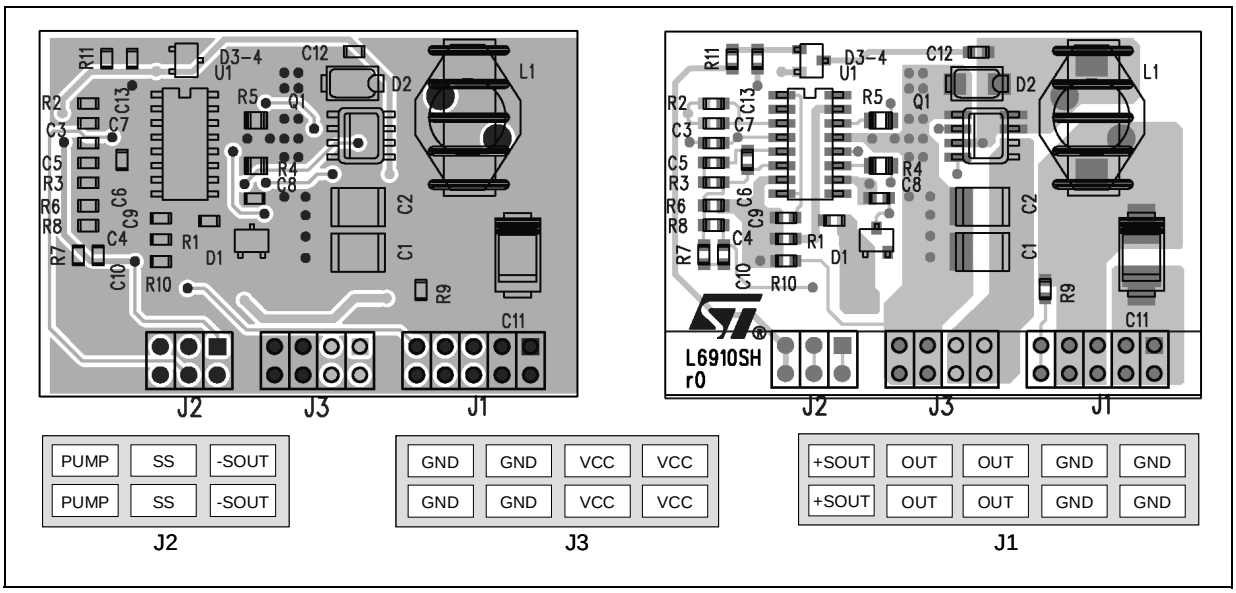


Figure 10. Motherboard layout