AN L5991-BASED CONVERTER WITH TEMPORARY EXTRA POWER CAPABILITY

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In some applications the SMPS, normally supposed to deliver a certain amount of power, from time to time undergoes load peaks that can be even two or more times as much. Such peaks are often too long to be properly handled by oversizing the output capacitors, but short if compared to the thermal time constants of the power components. Typical examples of such loads are motors and audio systems.

In this case, designing the SMPS for the peak power demand from the load would lead to a poorly used and more expensive system. It is more cost-effective to design for the maximum continuous power and allow the peak power to pass. However, if for any reason the load demands such peak power level for a long time, some of the power components, not sized for withstanding this, will definitely fail unless the system is stopped somehow.

In this application note a design example of such a system, based on the ST's advanced PWM controller L5991, is carried out.

Introduction

Purpose of this note is to provide a few brief design guidelines on the switch-mode power supply whose electrical specification is summarized in the following table.

Table 1. Design Electrical Specification

Symbol	Parameter	Value	Unit
V_{in}	Input Voltage Range	88 to 264	V_{ACrms}
f_L	Mains Frequency	50/60	Hz
P_{outx}	Maximum Continuous Output Power	45	W
P_{outpk}	Peak Output Power (t $\leq$ 0.5 s) (*)	75	W
V_{out}	Regulated Output Voltage (@ P_{out} =0 $\div$ P_{outpk}, V_{in} = 88$\div$264 V_{AC})	18V $\pm$ 2%	V
ΔV_{out}	Output Voltage Ripple (@P_{out} = P_{outx}, V_{in} =88$\div$264 V_{AC})	2	%
F_{osc}	Normal Operation Switching Frequency	70	kHz
F_{SB}	Light Load Switching Frequency	18	kHz
η	Target Efficiency (@P_{out} = P_{outx}, V_{in} =88$\div$264 V_{AC})	80	%
	Maximum Input Power (@P_{out} = 0.5 W, V_{in} =88$\div$264 V_{AC})	$\leq$ 2	W
	Maximum Input Power (Open load, V_{in} =88$\div$264 V_{AC})	$\leq$ 1	W
Notes: (*) If P_{out} is such that P_{outx} < P_{out} $\leq$ P_{outpk} the converter shall be shutdown (latch mode) within 1$\div$2 s; a load exceeding P_{outpk} shall cause converter's shutdown (latch mode) within 10$\div$100 ms.			

The special requirement for this converter is the ability to cope with a peak power demand from the load that exceeds the maximum continuous power by over 66% for a limited time ($\leq$ 0.5 s), still maintaining output voltage regulation, and to automatically shut down in case this overload lasts more than a specified time. Furthermore,

in case of anomalous power demand from the load (exceeding the peak power, e.g. due to a short circuit), converter's shutdown must occur within 10 ÷100 ms.

A power peak lasting 0.5 s is too long to be handled with just a reinforced output capacitor bank: as a matter of fact, after few ms the converter's control loop has already reacted to maintain the output voltage regulated. Thus a power demand lasting 0.5 s can be considered as a steady-state operating condition from the electrical point of view. On the other hand the thermal time constants of the power components are such that the heat generated during a power peak of even a couple of seconds will not cause an excessive temperature rise: their thermal *impedance* is to be invoked rather than their thermal *resistance*.

From these considerations, it turns out that the converter can be thermally designed just considering the maximum continuous output power P_{outx} (and the related RMS currents) that it has to deliver and not the peak power demand P_{outpk}. There are, however some points that one should consider for the electrical design:

1) the overcurrent limiting circuit must allow P_{outpk} to pass, hence its setpoint needs to be greater than the corresponding peak primary current Ip_{pklim} and, possibly, much greater than the peak primary current related to P_{outx};

2) the transformer and/or inductor must not saturate with this higher peak current;

3) there is a tradeoff between the input bulk capacitor size (which determines the minimum input DC voltage) and the value of Ip_{pklim}: a low capacitance leads to a high input voltage ripple, then to a lower minimum input DC voltage and to a higher Ip_{pklim}. Also the maximum duty cycle of the converter must account for the resulting minimum DC input voltage.

4) As envisaged by the spec in table 1, designing the converter for a given power but allowing a much higher level calls for a means to make the system work safely during abnormal operating conditions.

Except for the special requirement discussed so far, the specification is identical to that of the converter considered in [1], which will be then used as the starting point for the present design. In this context, only the modifications needed for fully complying with the spec of table 1 will be discussed. For reader's convenience figure 1 reproduces the electrical schematic of the original converter.

Additional circuitry will be needed for discriminating a peak power demand from a normal load condition and detecting a short circuit as well as realizing the required double time-out.

Figure 1. 45W, wide-range mains AC-DC adapter: electrical schematic (original design)
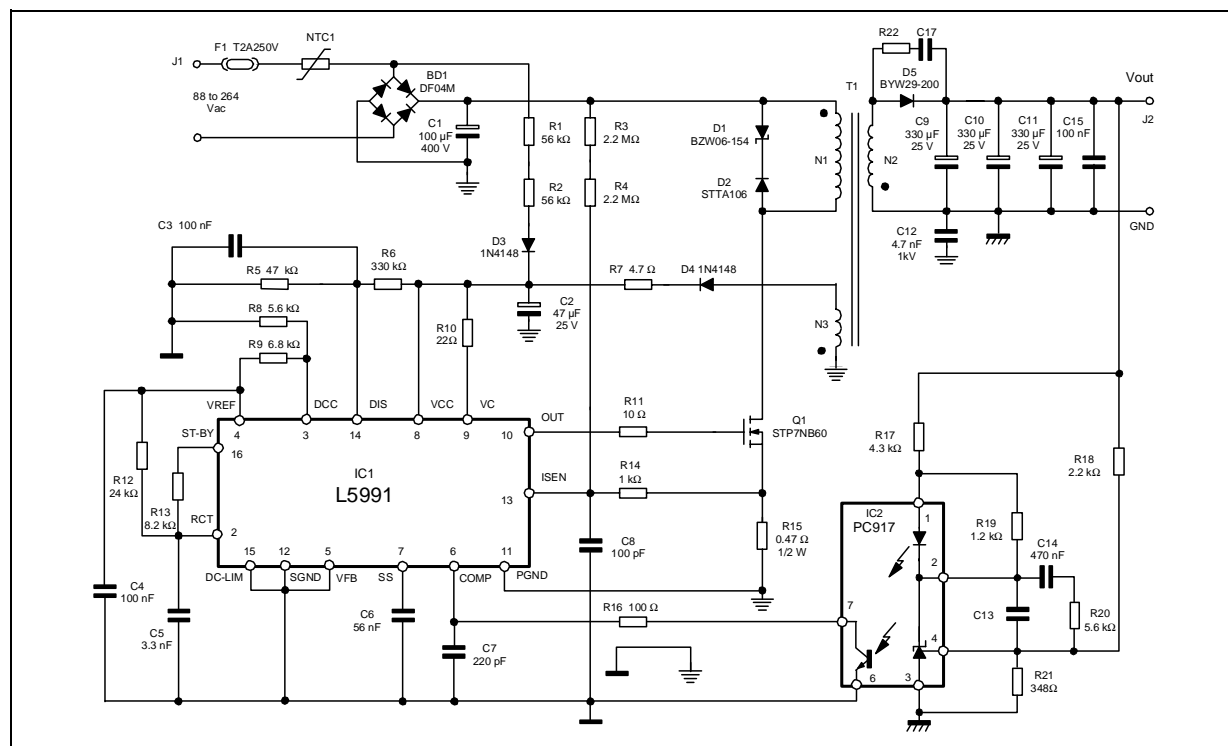
Adaptations and modifications of the original design

With reference to the schematic of figure 1, here follows a step-by-step discussion on the modifications needed for fulfilling the spec of table 1.

Input Capacitor. Looking at the evaluation results presented in [1], it is reasonable to assume that with 75 W load the input power will be around 90 W. Estimating about 5 W power loss before the transformer, the power managed by the transformer will be 85 W. With the worst-case spread (-20 %) of C1, that is with C1=80 μF, the valley voltage across C1 is expected to be around 54 V. Under these conditions the maximum peak primary current will be around 3.24A, exceeding the saturation current of the transformer (2.84A).

Moreover, the maximum duty cycle (@ Vin = 54V) will be around 59%: since the system is working in CCM, slope compensation will be needed to avoid unconditional instability of the current loop and the resulting sub-harmonic oscillations.

To avoid remaking the transformer and adding the slope compensation circuit, an attempt can be done using a larger C1. Assuming there is no change in power levels, with 150 μF capacitance (120 μF, worst case), the valley voltage across C1 will be 78 V, the maximum peak primary current 2.88 A and the maximum duty cycle 50%. Although necessary, this step is not enough to guarantee that the transformer will not saturate and then the system is still very close to the instability limit. The transformer needs then to be modified anyway (see the following points).

Sense resistor. The sense resistor R15 needs reducing, to allow a peak primary current of 2.88 A. The maximum value should be 0.92 V / 2.88 A = 0.319Ω. This will be achieved by paralleling a 1Ω resistor (1%, metallic film) to the existing 0.47Ω. The worst-case peak current, will be 1.08 V / 0.319Ω = 3.39 A.

Transformer. The changes to the transformer aim at meeting two specific requirements: 1) not to saturate with 3.39A primary current; 2) to reduce the maximum duty cycle below 50%, to avoid the use of a slope compensation circuit. Design constraint is the core size, which must be unchanged. The increase of total losses should be as low as possible.

Starting from point 2), to maintain the same maximum duty cycle as in the original design, the turn ratio should be reduced proportionally to the reduction of the valley voltage across C1. Formerly, with 45 W load, the worst-case valley voltage was 83 V and now is 78 V, then the new turn ratio is (50/12)·(78/83) = 3.916.

Table 2. Modified transformer specification

Core	Philips EFD30x15x9, 3C85 Material or equivalent				
Bobbin	Horizontal mounting, 12 pins				
Air gap	≈1.4 mm for an inductance 2-6 of 360 μH				
Leakage inductance	< 10 μH				
Windings Spec & Build	Winding	Wire	S-F	Turns	Notes
	Pri1	AWG27	2-4	30	
	Sec (a)	AWG25	11-7	16	Bifilar with Sec (b)
	Sec (b)	AWG25	12-8	16	Bifilar with Sec (a)
	Pri2	AWG27	4-6	30	
	Aux	AWG32	3-1	14	Evenly spaced
	Note: sec (a) and sec (b) are paralleled on the PCB				

To make sure that the core will not saturate with 3.39A, keeping the same inductance value, the number of turns of the primary winding should be raised from 50 to 66 and the air gap from 0.7 to 1.5 mm. To reduce the copper, it is acceptable to reduce the primary inductance by 10%: in this way the primary winding turn number will be 60 and the air gap 1.4 mm.

The secondary turn number will be 60/3.916=15.321, rounded off to 16. Keeping the same wire diameters, the primary resistance will be increased by a factor 60/50, that is 20%, and the secondary resistance by 33% and so will be the respective conduction losses (the RMS currents change very little). However, the flux swing is

reduced by 18%, which means that the core losses will be reduced by about 38%. The estimated total loss increase is only 0.1 W, hence the hot-spot temperature increase (as compared to the original design) should be under 3 °C. It is then not necessary to change the wire size.

The specification of the modified transformer is summarized in Table 2.

Table 3. List of modifications to the original design

Part	Original value	New Value	Note
C1	100 µF	150 µF	
R15	0.47 Ω	0.319 Ω = (0.47 Ω // 1 Ω)	Same power rating
T1	See [1]	See table 2	
R2, R3	2.2 MΩ	1.6 MΩ	Same power rating

Input voltage compensation. R3 and R4 compensate for the internal propagation delay of the PWM block to achieve an actual overcurrent setpoint independent of the input voltage. Their value is directly proportional to the sense resistor R15 and inversely to the primary inductance. Since both parameters are changed R3 and R4 needs adjustment. The new value for each of them will be 2.2 MΩ ·(0.319/0.47)·(400/360)=1.6 MΩ.

Table 3 summarizes all of the modifications described in this paragraph.

Circuit for delayed shutdown upon overpower/short circuit

The objective of the circuit of figure 2 is to provide a double programmable delay before shutting down the L5991 following on either an overload (a longer delay) or a short circuit (a shorter delay).

Figure 2. Circuit for delayed shutdown upon overpower/short circuit: electrical schematic
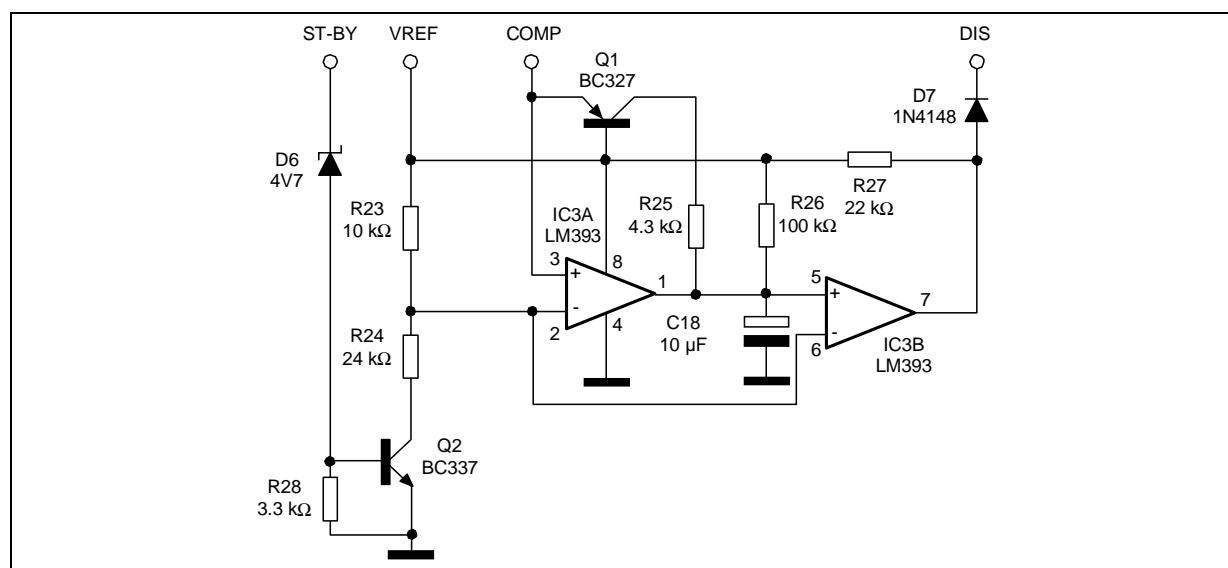
R23 and R24 define a voltage threshold, which the output of the E/A (COMP) will be compared to. If the L5991 is running at normal frequency, that is, the pin ST-BY is internally connected to the 5V reference VREF, Q2 is ON and the voltage at pin 2 of the LM393 is:

$$V2 = VREF \cdot \frac{R24}{R23 + R24} \quad (1)$$

If the L5991 is running at low frequency (because of a light load) the pin ST-BY is floating and, being connected to the oscillator through a resistor [2], oscillates between 1 and 3 V, well below the threshold of the zener D6. Q2 is then OFF and V2 equals VREF, hence the voltage at pin COMP, V(COMP), cannot exceed V2 as long as

the converter is in regulation ($P_{out} \leq P_{outpk}$). This is to avoid any interference with the Standby function: with a light load and the L5991 running at the lower frequency, V(COMP) might be greater then the value of V2 defined by (1), thus triggering the delayed shutdown function erroneously.

Assuming Q2 is ON, when V(COMP) > V2 the output of IC3A (which is open-collector) goes high and C18 is charged through R26. The time needed for C18 to be charged at V2 is:

$$Td_1 = R26 \cdot C18 \cdot \ln\left(\frac{VREF}{VREF - V2}\right)$$

When this voltage is reached, the output of IC3B goes high and the voltage at pin DIS of the L5991 is pulled above 2.5V, thus causing a latched shutdown of the PWM controller and of the converter too. The converter will stay idle as long as it is supplied by the input power source. To be able to restart the system, the power source must be removed. The diode D7 is used because the pin DIS is already biased (by a resistor divider to set up OVP protection) so as to decouple the two circuits.

Note that if the condition V(COMP) > V2 disappears (i.e. P_{out} falls below P_{outx}) before Td1 has elapsed, the output of IC3A goes back low thus discharging C18 and stopping this slow shutdown countdown.

In case of short circuit COMP will saturate high and tend to go over 6 V. In that case not only the output of IC3B will go high but also Q1 will be turned on (V(COMP) will be clamped at about 5.6V), thus C18 will be charged through R25 and R26. This circuit is analogous to that shown in [3]. The delay will be approximately:

$$Td_2 \approx R25 \cdot C18 \cdot \ln\left(\frac{VREF}{VREF - V2}\right),$$

since R25 is selected << R26, so that Td_2 << Td_1.

Note, if V(COMP) goes back to the regulation region (i.e. P_{out} falls below P_{outpk}) before Td_2 has elapsed, the charge of C18 through R25 will be stopped; the slow charge through R26 can be stopped too or still go on, depending on whether V(COMP) has fallen below V2 (P_{out} < P_{outx}) or not.

One more comment: COMP is saturated high and Q1 turned on (initiating the fast shutdown countdown) every time the converter is started up, during the ramp-up of the output voltage from zero to the regulated value. Obviously, Td_2 needs to be greater than this time (usually, 5÷20 ms) or the converter will never start.

With the part values shown in fig. 2, the results are the following:

$$V2 = 5 \cdot \frac{24}{10 + 24} = 3.53 \, V$$

$$Td_1 = 100 \cdot 10^3 \cdot 10 \cdot 10^{-6} \cdot \ln\left(\frac{5}{5 - 3.53}\right) = 1 \cdot \ln(3.4) = 1.22 \, s$$

$$Td_2 = 4.3 \cdot 10^3 \cdot 10 \cdot 10^{-6} \cdot \ln\left(\frac{5}{5 - 3.53}\right) = 4.3 \cdot 10^{-2} \cdot \ln(3.4) = 52 \, ms$$

Refer to the appendix of [4] for formulae useful for relating the voltage level on pin COMP to the power level in a flyback converter, to be able to design the circuit under different conditions.

Figure 3 shows how the circuit of figure 2 is inserted into the modified 45W demo board (the changes are highlighted by the shaded regions) and the oscilloscope pictures of figure 4 illustrate the experimental results in case of both overload and short circuit.

If converter's latched shutdown is not desired, but the user wants the system to automatically recover normal operation when the overload/short is removed, yet maintaining a low power throughput during the fault, it is very easy to modify the circuit of figure 2 to achieve this: R27 will be reduced at 2.2 kΩ and the diode D7 connected to the ISEN pin of the L5991, so as to invoke its "Hiccup" OCP [2]. The resulting schematic is illustrated in figure 5, its insertion into the 45W AC-DC adapter is obvious.

Figure 3. Electrical schematic of the modified 45W AC-DC adapter inclusive of the circuit of figure 2
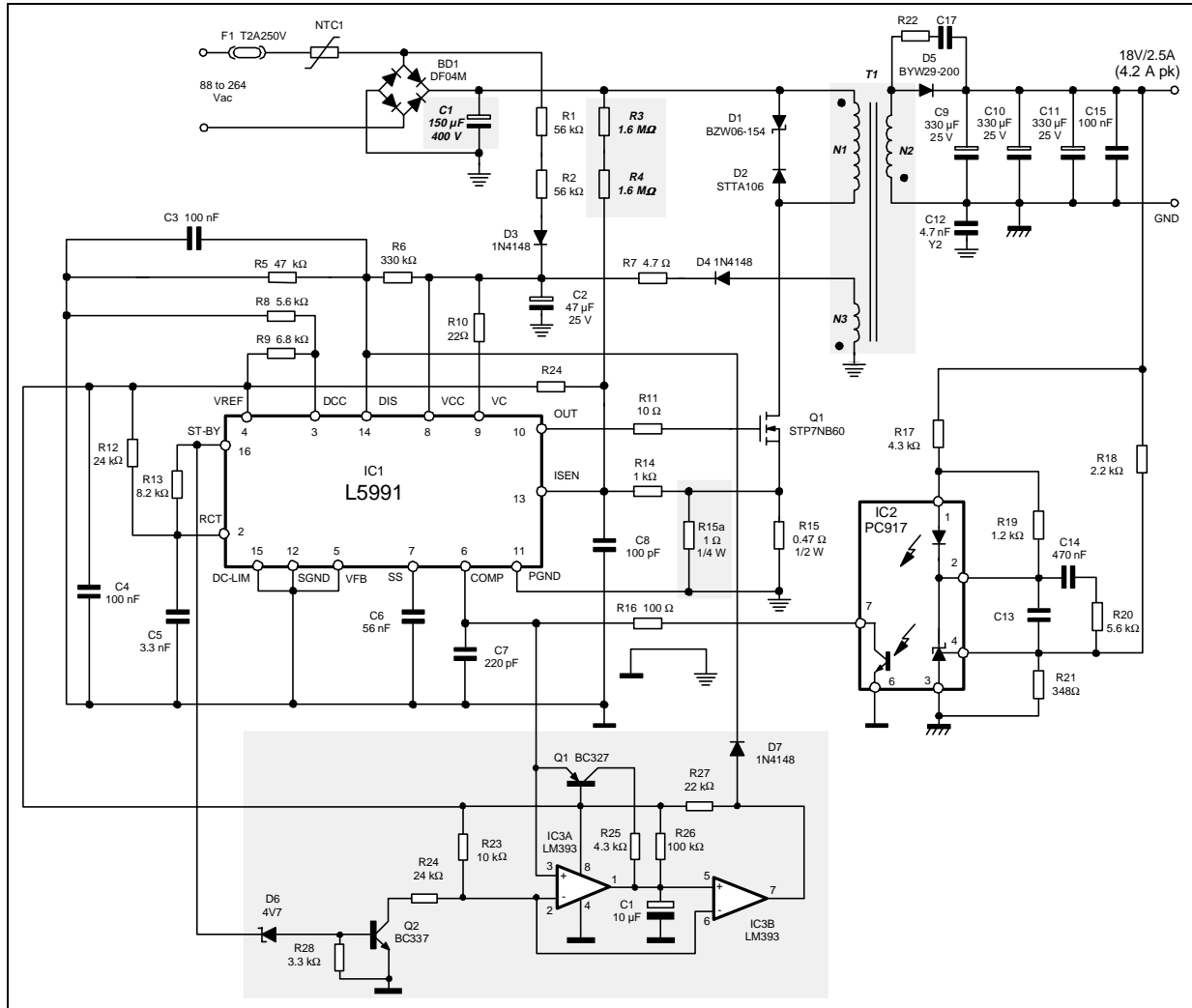

Figure 4. Timings of the circuit in figure 2: a) overload (Iout = 4 A); b) short circuit
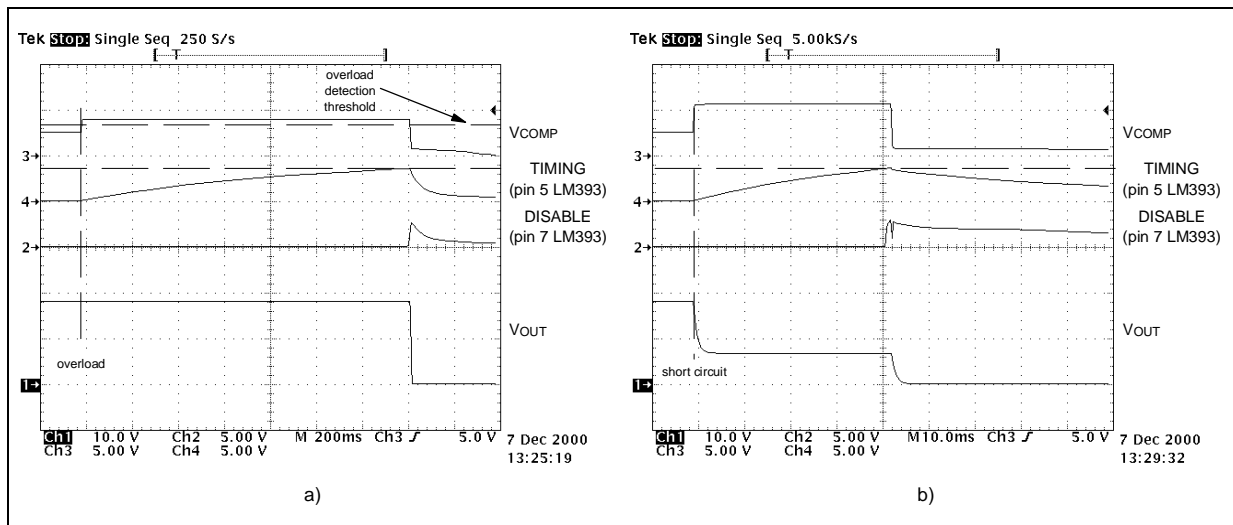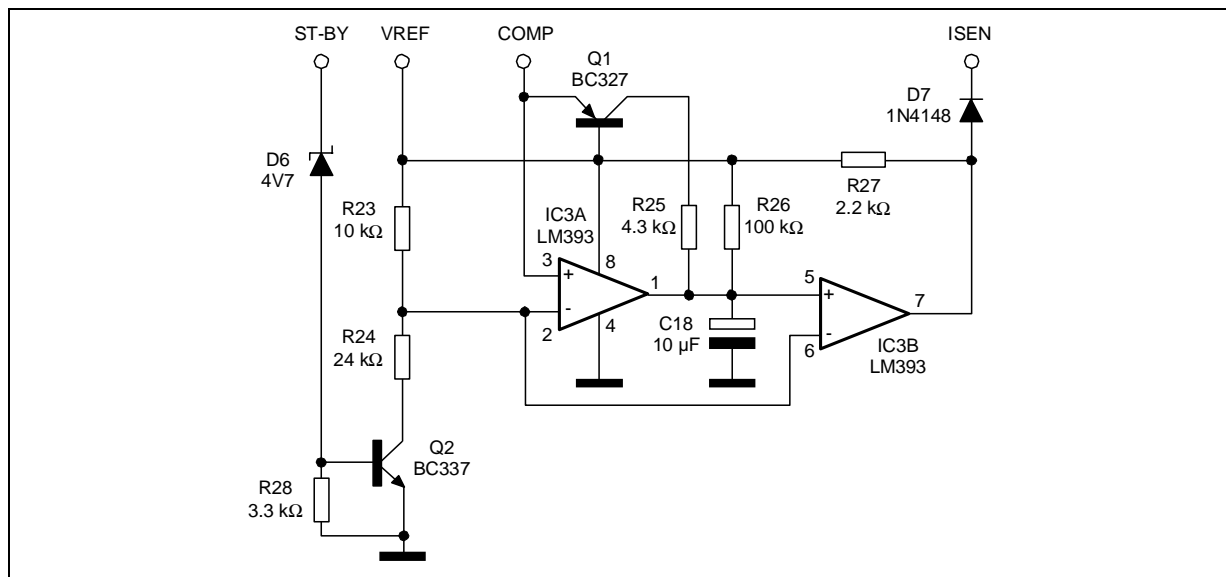
Figure 5. Circuit of figure 2 modified for autorecovery mode operation

In case of activation, the converter will be stopped and restarted after a delay set by the SS capacitor of the L5991 (C6). If this delay is long enough, the Vcc capacitor (C2) may be discharged below the UVLO threshold of the L5991, giving origin to even longer delays.

REFERENCES

[1] "45 W AC-DC Adapter with Standby Function" (AN1134)

[2] "L5991 Primary Controller with Standby" Datasheet

[3] "How to Handle Short Circuit Conditions with ST's Advanced PWM Controllers" (AN1215)

[4] "Minimize Power Losses of Lightly Loaded Flyback Converters with the L5991 PWM Controller" (AN1049)